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A 40 nW CMOS-Based Temperature Sensor with Calibration Free Inaccuracy within ±0.6 °C

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Abstract: In this study, a temperature equivalent voltage signal was obtained by subtracting output voltages received from two individual temperature sensors. These sensors work in the subthreshold region and generate the output voltage signals that are proportional and complementary to the temperature. Over the temperature range of −40 °C to +85 °C without using any calibration method, absolute temperature inaccuracy less than ±0.6 °C was attained from the measurement of five prototypes of the proposed temperature sensor. The implementation was done in a standard 0.18 µm CMOS technology with a total area of 0.0018 mm^2. The total power consumption is 40 nW for a supply voltage of 1.2 V measured at room temperature.

Keywords: PTAT; CTAT; temperature sensor; CMOS; ultra low power; calibration free

1. Introduction

The growing regime of Internet of Things (IoT) requires devices with low-power and low-cost for the consumer electronics. A wireless sensor node (WSN) is first in the long line of devices since it is the backbone of any IoT-based application [1]. One of the demanding specifications in the design of wireless sensor node is ultra low-power consumption. This is necessary due to the presence of power-hungry transceiver module [2,3]. These sensor nodes are deployed in various applications such as medical, infrastructure and environmental monitoring, where the most common sensing modality is temperature.

In the literature, various low power temperature sensing modules that are either suitable or have been used in WSN are available. These temperature sensing modules sense the temperature either by using BJT (Bipolar Junction transistor)-based or by using MOSFET (Metal Oxide Semiconductor Field-effect transistor)-based circuit arrangements. The BJT-based temperature sensors are widely accepted due to their accurate temperature sensing ability that can be below ±1 °C [4–7]. For all MOSFET-based implementations, a temperature accuracy less than ±2 °C has been achieved [8–11].

One of the common post-processing methods for either BJT-based or MOSFET-based temperature sensor designs is the calibration, which is required to assure that the measurements are accurate and within the specifications [12–14]. In the aforementioned literature, either the single-point or the two-point calibration method is used to adjust the attribute of the temperature sensor. In addition to these conventional calibration approaches, researchers have also proposed methods such as self-calibration [15,16] and/or auto-calibration [17–19], to further reduce the complexity of the post fabrication calibration process.

Since the temperature sensor is a highly demanding element, to reduce the production time as well as the maintenance cost, elimination of the calibration process would be advantageous. Especially in the

case of practical implementations such as room, automobile or refrigeration temperature monitoring, moderate temperature accuracy in the range of ±1 °C is adequate for controlling and supervision [20]. Some of the solutions to design the calibration-free temperature sensors that are useful for these purposes have been proposed in [21,22].

This work proposes a temperature sensor topology that is an all-MOSFET-based implementation to save Si area, has V_{th}-based temperature sensing for fast response time, consumes power in nano-watts, is free from calibration to save post-processing and has an acceptable temperature accuracy suitable for various general-purpose applications. The block diagram is presented in Figure 1 where a MOSFET-based temperature sensor module has been formed by using two complementary temperature sensors. These sensors generate the output voltage signals that are Proportional-To-Absolute-Temperature (PTAT) and Complementary-To-Absolute-Temperature (CTAT), respectively. These voltage signals are then measured externally and a net PTAT output voltage signal is obtained by subtracting the CTAT-voltage signal from the PTAT-voltage signal. The arrangement is capable of measuring the temperature accurately within the range of ±0.6 °C without using any calibration process. This accuracy has been achieved for the temperature range of −40 °C to +85 °C [23] where the on-chip thermal cores consume power of 40 nW when operating at the supply voltage of 1.2 V.

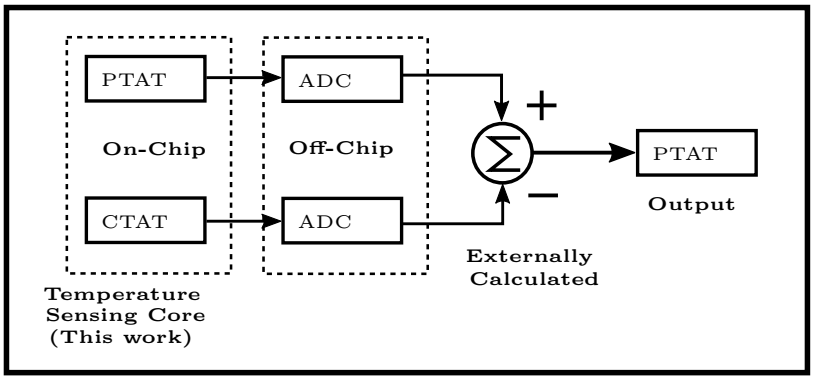


Figure 1. Conceptual block diagram of proposed temperature circuit.

This paper is organized in four sections. Section 2 introduces the design implementation of the proposed temperature sensor cores. Experimental results from the prototype temperature sensors fabricated using 0.18 µm standard CMOS process are presented in Section 3. The concluding remarks are presented in Section 4.

2. Design Implementaton

The circuit diagram of proposed temperature sensing module is shown in Figure 2 that consists of three sub-blocks, namely resistor-less beta multiplier circuit, CTAT sensor and PTAT sensor. The resistor-less beta multiplier circuit provides reference current to the PTAT and CTAT temperature sensor cores. These cores utilize this current to generate thermal equivalent voltage signals, which are proportional and complementary to the temperature, respectively. The brief description and the first order theoretical modeling of the sub-blocks are in the following subsections.

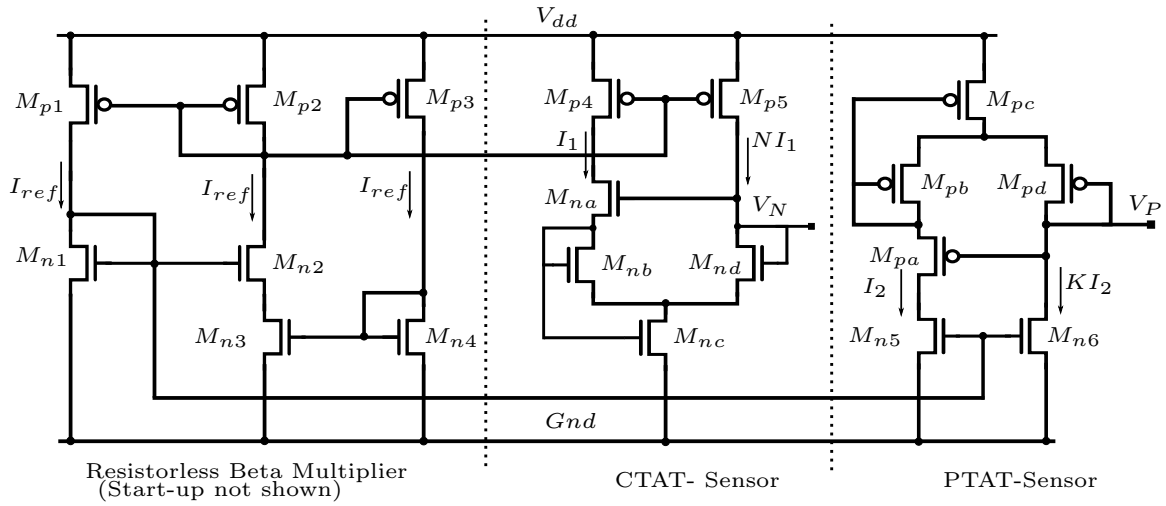


Figure 2. Circuit diagram of proposed temperature sensing module.

2.1. Resistor-Less Beta Multiplier Circuit

The classical resistor-less beta multiplier (RBM) circuit [24] has been selected to obtain the reference current for the temperature sensing core due to its implementation simplicity. In the circuit (see Figure 2), the NMOSFETs (N-type Metal Oxide Semiconductor Field Effect Transistor) M_{n1} and M_{n2} operate in the subthreshold region. The NMOSFET M_{n3} is deployed as a MOS resistor and the gate controlling voltage to keep it in strong inversion, deep-triode region has been obtained from diode-connected NMOSFET M_{n4}. Thus, the equations of a linear and the saturation currents flowing in NMOSFET M_{n3} and M_{n4} are:

$$I_{ref} = \mu_n C_{OXn} S_{n3} (V_{gs3} - V_{thn}) V_{ds3} \tag{1}$$

$$I_{ref} = \frac{\mu_n C_{OXn} S_{n4}}{2} \left(V_{gs4} - V_{thn}\right)^2 \tag{2}$$

where I_{ref} is the reference current which is flowing equally in all the branches of the RBM circuit; μ_n, C_{OX} and V_{thn} are the mobility parameter, the gate-oxide capacitance and the threshold voltage of the NMOSFET, respectively; V_{ds3} and V_{gs4} are, respectively, the drain-source and gate-source voltages of M_{n3}; and V_{gs4} is the gate-source voltage of M_{n4}. Finally, S_3 and S_4 are the aspect ratio (W/L) of M_{n3} and M_{n4}, respectively. It can be observed in Figure 2 that $V_{gs3} = V_{gs4}$, hence solving Equations (1) and (2) results in:

$$I_{ref} = 2 \frac{S_{n3}^2}{S_{n4}} \mu_n C_{OXn} V_{ds3}^2 \tag{3}$$

Applying Kirchoff's Voltage Law (KVL) in the voltage loop formed by M_{n1}, M_{n2} and M_{n3} results in:

$$V_{gs1} = V_{gs2} + V_{ds3} \tag{4}$$

The NMOSFETs M_{n1} and M_{n2} are in subthreshold saturation region [25] therefore V_{gs1} and V_{gs2} can be derived as:

$$V_{gs1} = V_{thn} + \eta V_T \ln \left(\frac{I_{ref}}{I_{DO} S_{n1}} \right) \tag{5}$$

$$V_{gs2} = V_{thn} + \eta V_T \ln\left(\frac{I_{ref}}{I_{DO} S_{n2}}\right) \tag{6}$$

where I_{DO} is the saturation diode saturation current, η is the subthreshold slope-factor and V_T is the thermal voltage. Using Equations (5) and (6) in Equation (4), and substituting the resultant into Equation (3) gives the expression of I_{ref} as follows:

$$I_{ref} = 2\frac{S_{n3}^2}{S_{n4}} \mu_n C_{OXn} \eta^2 V_T^2 \ln^2\left(\frac{S_{n2}}{S_{n1}}\right) \tag{7}$$

It can be seen from Equation (7) that I_{ref} is supply independent and its magnitude is a function of device geometries. The temperature behavior of I_{ref} is a function of the temperature behavior of parameters μ, V_T and η. Referring to the work published in [26], the mobility parameter μ decreases with increasing temperature while the thermal voltage V_T and the subthreshold slope η, increases with increasing temperature [25,27]. Thus, it can be concluded that the dominance of the terms η and V_T in (7) will will introduce the PTAT temperature dependence in it.

The post layout simulation results of the current reference circuit at typical corner obtained for the temperature ranging from -40 °C to $+85$ °C in the steps of 12.5 °C are shown in Figure 3 where the PTAT dependence of I_{ref} can be seen though the plot is not exactly linear by nature but increases with increasing temperature. By applying the 2-point calibration at -40 °C and $+85$ °C, it can be estimated that the current exhibit the PTAT behavior with the temperature coefficient of 1885 ppm/°C.

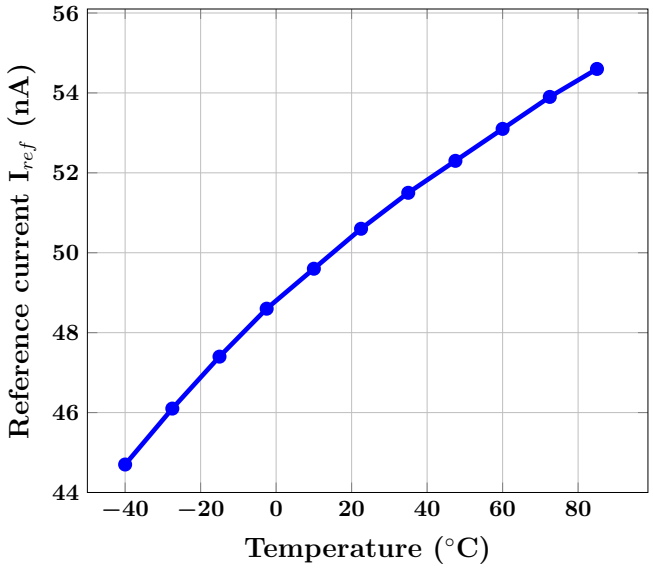


Figure 3. Post layout simulation result of reference current obtained from RBM circuit.

2.2. Temperature Sensing Core

The temperature sensing core is formed by the two temperature sensors which are labeled as CTAT sensor and PTAT sensor in Figure 2. As the name indicates, CTAT sensor generates a voltage that decreases with increasing temperature. On the contrary, PTAT sensor generates a voltage that increases with increasing temperature.

The CTAT sensor is formed by using NMOSFETs M_{na} to M_{nd} and PMOSFETs (P-type Metal Oxide Semiconductor Field Effect Transistor) M_{p4} and M_{p5} have been used to mirror reference current in the core. Similarly, the PTAT sensor is constructed by using PMOSFETs M_{pa} to M_{pd}, and uses M_{n5} and M_{n6} as the current mirror. It can be seen in Figure 2 that each sensor consists of two branches, where currents I_1,NI_1 (CTAT sensor) and I_2,KI_2 (PTAT sensor) have been utilized, respectively. The magnitude (I_1 and I_2) and their mirroring ratios (N, K) were determined by framing an optimization problem that

was solved using the Matlab® software where the difference of the output PTAT and CTAT voltages of the sensors will result into the minimum absolute temperature error, was selected as the optimization constraint. The data used in the analysis was the parametric circuit simulation results that were obtained with the Spectre© simulator in the Cadence environment®.

Let us consider the CTAT sensor, in which NMOSFETs M_{na} to M_{nd} are set to operate in the subthreshold region. Applying KVL in the voltage loops formed by NMOSFETs M_{na} to M_{nd} results in:

$$V_N = V_{gsd} + V_{dsc} \tag{8}$$

$$V_{gsc} = V_{sga} + V_{dsd} + V_{dsc} \tag{9}$$

$$V_{dsd} + V_{sdb} + V_{sga} = 0 \tag{10}$$

$$V_{gsa} = V_{gsd} - V_{dsb} \tag{11}$$

The equation for subthreshold drain-current (I_{sub}) is given by [25]:

$$I_{sub} = \frac{2\eta\mu C_{OX} V_T^2 W}{L} \exp\left(\frac{V_{gs} - Vthn}{\eta V_T}\right)\left[1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right] \tag{12}$$

For the diode-connected transistor working in saturation region ($V_{ds} > 4V_T$ or ≈100 mV), Equation (12) is rewritten as follows:

$$I_{sub} = \frac{2\eta\mu C_{OX} V_T^2 W}{L} \exp\left(\frac{V_{gs} - Vthn}{\eta V_T}\right) \tag{13}$$

In the circuit, M_{nd} and M_{nb} are diode-connected and the currents of NI_1 and I_1, respectively, are flowing through them. Hence, using Equation (13) in Equation (11) results in:

$$V_{gsa} = \eta V_T \ln\left(\frac{NS_{nb}}{S_{nd}}\right) \tag{14}$$

where, S_{nb}, S_{nd} are the aspect ratio of M_{nb} and M_{nd}, respectively. Subtracting Equation (9) from Equation (8) results in:

$$V_N = V_{gsc} + V_{gsa} \tag{15}$$

As the operating supply voltage is 1.2 V, the drain-source voltage V_{dsc} of the NMOSFET M_{nc} is greater than 100 mV, thus it is working in the subthreshold-saturation region with a total current value of $(N+1)I_1$. Hence, using Equations (13) and (14) in Equation (15) results in:

$$V_N = \underbrace{V_{thn}}_{a} + \underbrace{\eta V_T \ln\left[\frac{N(N+1)S_{nb}I_1}{2\eta\mu_n C_{OXn} V_T^2 S_{nc} S_{nd}}\right]}_{b} \tag{16}$$

It can be observed from Equation (16) that the output voltage V_N is a sum of two parts (Parts (a) and (b)), whose constituents have a well define thermal behavior. The threshold voltage, i.e., Part (a), will exhibit CTAT behavior [26]. The temperature behavior of Part (b) is governed by the combined thermal behavior of the thermal voltage V_T (0.085 mV/°C) [25], the subthreshold slope parameter η [27], the mobility factor μ [26] and I_1 which is mirrored from I_{ref} (see Figure 2). The thermal behavior of Part (b) can be predicted from the schematic-level simulation results, as shown in Figure 4.

Here, the thermal slope of V_{thn} is -0.63 mV/°C while the thermal slope of V_N is -2.1 mV/°C. This, high magnitude of negative thermal slope of V_N is feasible only when Part (b) exhibit the CTAT temperature dependence. Overall, Equation (16) will exhibit CTAT behavior which can be verified from the schematic level simulation results shown in Figure 4.

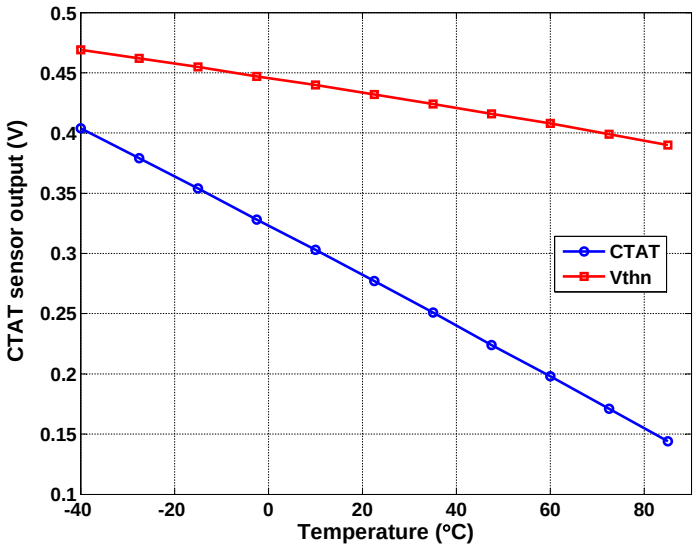


Figure 4. Simulation result of CTAT output V_N and threshold voltage V_{thn} with temperature. Thermal slopes of V_{thn} and V_N are -0.63 mV/°C and -2.1 mV/°C, respectively.

Similarly, by following the aforementioned steps, the output voltage from the PTAT sensor can be derived as:

$$V_P = \underbrace{V_{DD}}_{a1} - \left[\underbrace{V_{thp}}_{b1} + \underbrace{\eta V_T \ln \left[\frac{K(K+1)S_{pb}I_2}{2\eta\mu_p C_{OXp} V_T^2 S_{pc} S_{pd}} \right]}_{c1} \right] \tag{17}$$

In Equation (17), Term (a1) is the supply voltage, which is a constant and also independent of the temperature, while Terms (b1) and (c1) exhibit the CTAT behavior, as explained above. Thus, when the sum of the Terms (b1) and (c1) is subtracted from the constant term, it results in o the PTAT behavior. However, it causes the PTAT sensor to be highly supply dependent. The schematic level simulation results are shown in Figure 5 where the maximum deviation in output of the CTAT sensor is 4 mV for the change in supply voltage from 0.8 to 2 V. This deviation can further be reduced by changing the circuit design strategy, e.g. using folded cascode biasing. Thus, it is possible to comment that CTAT is supply independent (see Equation (16)) while the output of PTAT sensor is supply dependent (see Equation (17)). The proposed architectures are capable of working from 0.8 to 2 V. In the present implementation, the sensors are operating at supply voltage of 1.2 V, which is one of the system level specifications where the sensor has been deployed.

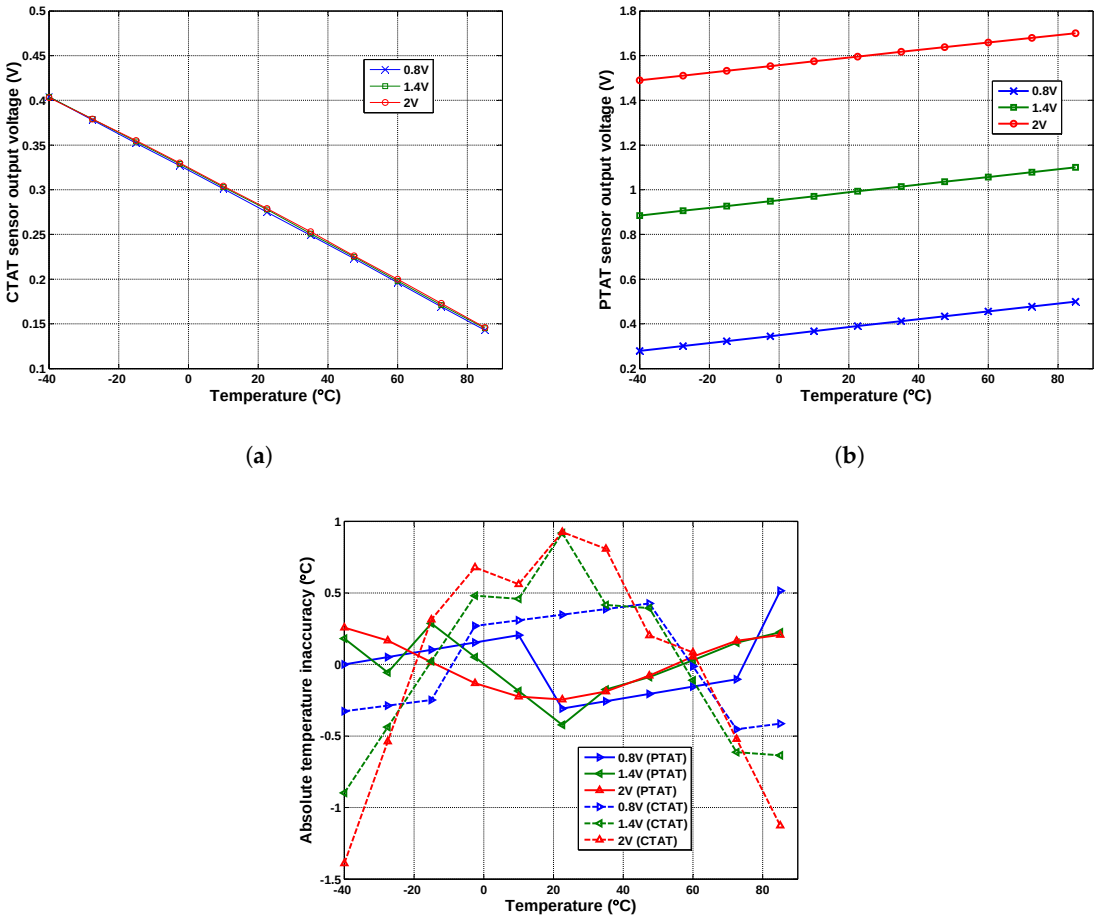


Figure 5. Schematic-level simulation results showing supply dependence of output voltage obtained from: (**a**) CTAT sensor and (**b**) PTAT sensor; and (**c**) their absolute temperature error.

The simulated absolute temperature inaccuracy results at different supply voltage values for both of the sensors are also shown (Figure 5c) where the calculated supply-sensitivity [28] at room temperature of CTAT and PTAT sensors are 0.48 °C/V and 0.15 °C/V, respectively. It should be noted that ideally magnitudes of the supply sensitivity parameter are equal for both sensors; this inequality in the magnitudes is due to the design consideration.

2.3. Differential Sensing

The different sensing is obtained by subtracting Equation (16) from Equation (17), and results in:

$$V_{diff} = V_{dd} - \left(V_{thp} + V_{thn}\right) - \eta V_T \ln\left(\frac{KN(K+1)(N+1)S_{nb}S_{pb}I_1I_2}{4C_{OXn}C_{OXp}\eta^2V_T^4\mu_n\mu_pS_{nc}S_{pc}S_{nd}S_{pd}}\right) \quad (18)$$

It can be seen in Figure 2 that the currents I_1 and I_2, which are flowing in the cores, have been derived from the reference current generator, where

$$I_1 = \alpha I_{ref}$$
$$I_2 = \beta I_{ref} \quad (19)$$

and i α and β are the scaling factors. Substituting Equation (7) into Equation (19) and then into Equation (18) results in:

$$V_{diff} = V_{dd} - \left(V_{thp} + V_{thn}\right) - \eta V_T \ln\left[\alpha\beta NK(N+1)(K+1)\left(\frac{\mu_n C_{OXn}}{\mu_p C_{OXp}}\right) \ldots \ldots \left(\frac{\eta^2 S_{nb} S_{pb} S_{n3}^4}{S_{pc} S_{pd} S_{nc} S_{nd} S_{n4}^2}\right) \ln^4\left(\frac{S_{n2}}{S_{n1}}\right)\right] \quad (20)$$

2.4. Post Layout Simulation Results

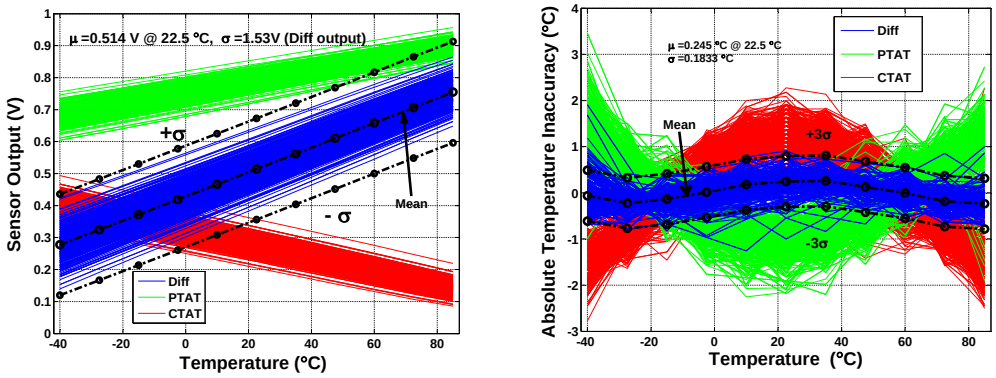
The parameters present in Equation (20) can be divided into two parts: first, the technology dependent parameters, which are $\eta, C_{OX}, V_{thp}, V_{thn}, \mu_n, \mu_p$, and, second, the circuit level design parameters, which are the aspect ratio of transistors and scaling factors. During the design development of the cores, the dataset corresponding to the temperature-dependent characteristics of V_{diff} for the temperature range of -40 °C to $+85$ °C in the steps of 12.5 °C were obtained by varying the circuit-level design parameters by using Spectre simulator in the Cadence environment. Later, Matlab® was used offline to find those circuit-level parameters for which the difference between the thermal characteristics curve and the best fitted line was minimal..

Mathematically it can be represented as:

$$f(T) = V_{diff}(T) - V_{ideal}(T) \longrightarrow 0 \quad (21)$$

where $f(T)$ is the difference of the best-fit line V_{ideal} corresponding to V_{diff} over the selected temperature range.

It is important to note that these cores can be designed individually; however, in the proposed implementation, they were designed simultaneously to follow the convergence condition in Equation (21). The post layout Monte Carlo simulation results (500 runs) of the fabrication-ready circuit are shown in Figure 6. For these simulations, the technology spread and devices mismatch at the supply voltage of 1.2 V were considered. The presence of a large spread in the sensor output voltage plots is primarily due to the dominant threshold voltage V_{th} (see Equations (16) and (17)) [29]. However, it can be seen in Figure 6b that, irrespective of wide process spread, the calculated temperature inaccuracy is within the limit of ± 1 °C for around 98% of the total Monte Carlo runs of the proposed temperature sensor.



(**a**) (**b**)

Figure 6. Post layout Monte Carlo simulation results of: (**a**) sensor outputs; and (**b**) absolute temperature error.

3. Measurement Results

The proposed temperature sensor was fabricated in a standard 0.18 µm CMOS technology and the implemented area including current reference circuit is 0.013 mm^2 (see Figure 7). The measurements were performed on five prototypes at the supply voltage of 1.2 V. The temperature chamber VTM7004® was used to perform the temperature characterization. The controlling program was implemented in the LabVIEW® to perform thermal characterization in the range of −40 °C to +85 °C in the programmed temperature step of 12.5 °C. A calibrated precision Pt-100 thermometer (±0.015 °C) was placed close to the prototype to obtain the true ambient temperature. The detailed block diagram of the measurement setup is shown in Figure 8.

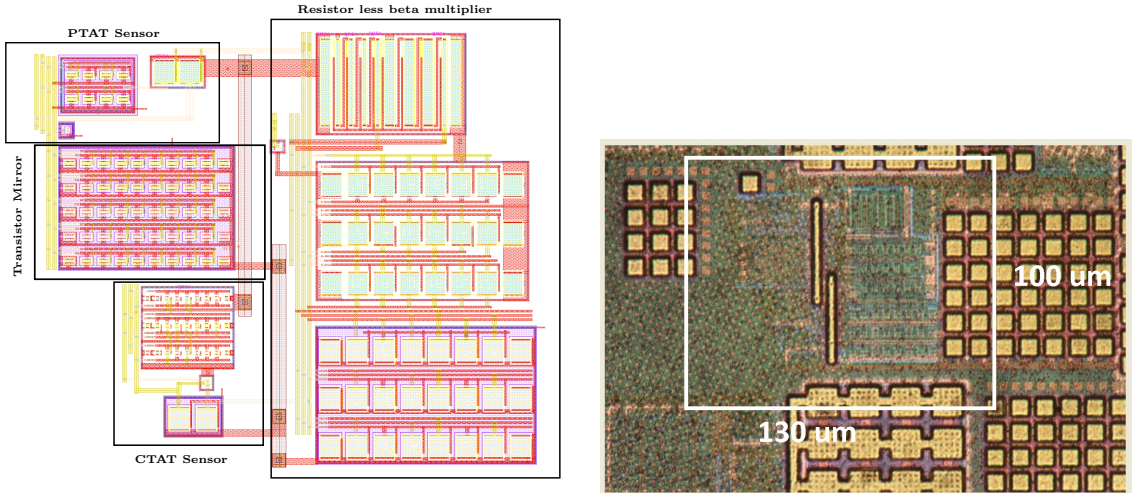


Figure 7. (**a**) Layout; and (**b**) Micrograph of the proposed temperature sensor

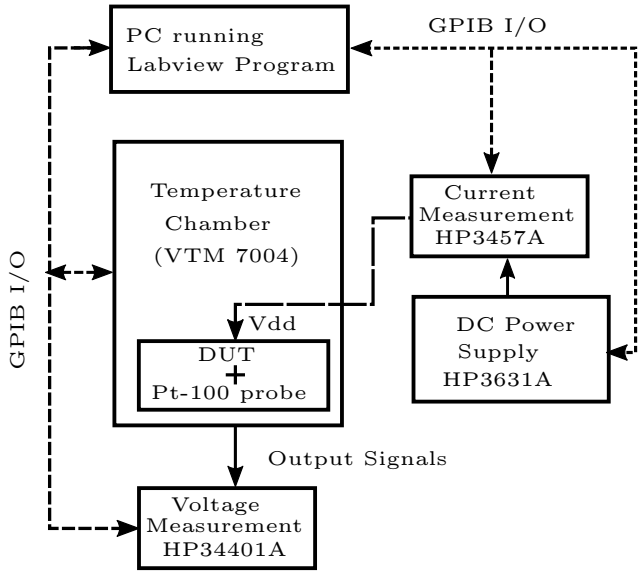


Figure 8. Block diagram of measurement setup.

The differential output voltages measured from the five prototypes are shown in Figure 9. The performance of the output voltage signals was off-line evaluated by using MATLAB® in terms of the absolute temperature error (TE), which is the difference between the temperature equivalent of the measured voltage data and the temperature obtained from the least square best fit line. This line was obtained from the measured data points using the MATLAB program. The measured absolute temperature error obtained for the five prototypes is shown in Figure 10. It can be seen from the plots that the absolute temperature error is within ±0.6 °C. The performance comparison of the proposed architecture with the state-of-the-art temperature sensors available in the literature is presented in Table 1. It can be observed in the table that temperature accuracy without any calibration offered by the proposed temperature sensing module is smaller than or comparable to most of the-state-of-art published literature.

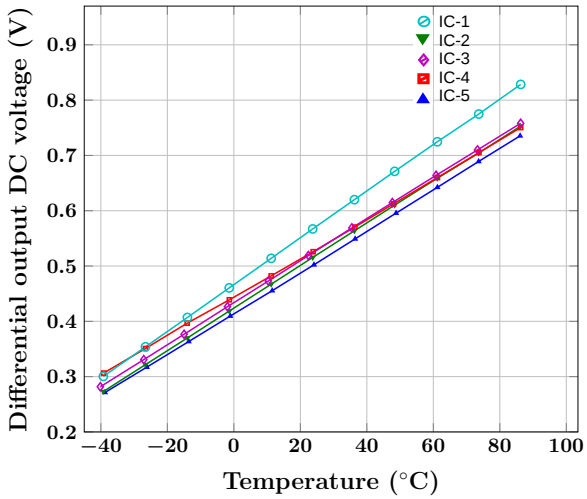


Figure 9. Differential voltage obtained from temperature sensing cores.

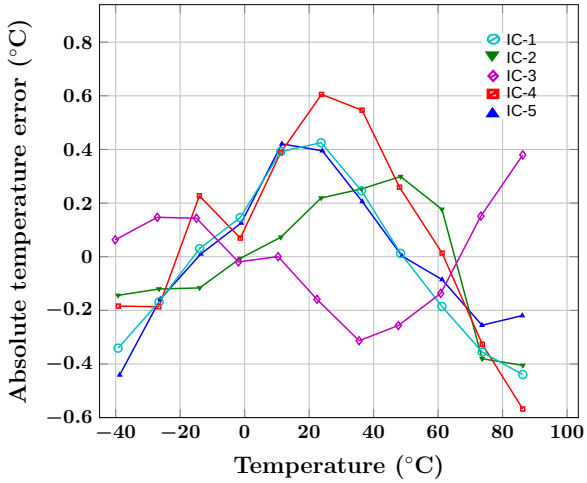


Figure 10. Measured absolute temperature error of differential output.

Table 1. Performance comparison with the-state-of-the-art temperature sensors available in literature.

Parameter	This Work	[10]	[30]	[31]	[32]	[33]	[34]	[35]	[36]
Process (nm)	180	350	180	500	180	65	180	180	180
Area (mm^2)	0.013	0.01	-	0.26	0.2	-	0.09	0.05	0.089
Temperature									
Range (°C)	−40 to 85	20 to 100	−55 to 125	−55 to 125	27 to 47	0 to 60	0 to 100	0 to 100	−20 to 80
Inaccuracy (°C)	±0.6	±1.97	±0.6	±2.5	±1	−5.1 to +3.4	+1.3 to −1.4	−1.6 to +3	±0.99
Sensing	Vol.	Freq.	Vol.	Vol.	Freq.	Delay	Vol.	Current	Freq.
Supply voltage (V)	1.2	-	0.7–1.8	1(Min.)	-	1	1.2	1	1.6
Power dissipation (W)	40n	1.05n to 65.5n @ 5samples/s	36 †µ @1V	17 µW	900n	150 µ	65n	200n to 310n	480n
Calibration	No	No	No	No	Auto	Auto	2-point	2-point	2-point

† high due to relative sensor architecture; Vol, Voltage; Freq, Frequency.

4. Conclusions

This paper explains the temperature sensor arrangement formed by using two temperature sensors with complementary thermal characteristics. The temperature equivalent voltage is a difference of voltage generated by CTAT and PTAT sensor cores, respectively. As a result, it becomes possible to measure the temperature with inaccuracy of ±0.6 °C, without use of any existing calibration methods. The only limitation of this module is high supply voltage dependence because of the PTAT sensor core. However, this limitation can be overcome by using a voltage regulator but it will increase total power consumption. In the present case, the cores all together consume 40 nW of power from the supply voltage of 1.2 V. The low power consumption and ability to measure temperature within permissible limits without use of any calibration make the proposed temperature sensing module suitable for various temperature measuring applications that are controlled by IoT in the extended industrial temperature range.

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Conflicts of Interest: The authors declare no conflict of interest.

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