

Article

High-CMRR Low-Noise Fully Integrated Front-End for EEG Acquisition Systems

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Abstract: We present in this paper a fully integrated low-noise high common-mode rejection ratio (CMRR) logarithmic programmable gain amplifier (LPGA) and chopped LPGA circuits for EEG acquisition systems. The proposed LPGA is based on a rail-to-rail true logarithmic amplifier (TLA) stage. The high CMRR achieved in this work is a result of cascading three amplification stages to construct the LPGA in addition to the lower common-mode gain of the proposed logarithmic amplification topology. In addition, the $1/f$ noise and the inherent DC offset voltage of the input transistors are reduced using a chopper stabilization technique. The CMOS 180 nm standard technology is used to implement the circuits. Experimental results for the integrated LPGA show a CMRR of 140 dB, a differential gain of 37 dB, an input-referred noise of $0.754 \mu\text{V}_{\text{rms}}$, a $189 \mu\text{W}$ power consumption from 1.8 V power supply and occupies an active area of 0.4 mm^2 .

Keywords: EEG acquisition system; front-end amplifier; high CMRR; $1/f$ noise; logarithmic programmable gain amplifier; chopper stabilization technique

1. Introduction

The electroencephalogram (EEG) experimental and clinical monitoring technique is used for long-term monitoring of the brain's electrical activity. EEG is a non-invasive and painless diagnostic test, which allows measuring the electrical activity of the brain by simply placing several electrodes on the head (scalp) around the brain. The potential differences measured from sets of two electrodes are converted into waveforms. These signals are used to evaluate the brain disorders in epileptic patients representing our interest. Recently, there was an increasing demand of miniaturized biopotential acquisition systems. These systems are lightweight, portable, do not hinder patient's mobility, and are comfortable to the patient during the monitoring. The EEG signals are difficult to be measured due to their extremely weak amplitude, in the range of $1\text{--}160 \mu\text{V}_{\text{pp}}$, and their limited band to a very low-frequency range from 0.1 to 100 Hz. Therefore, the EEG acquisition systems are susceptible to ambient noise (50/60 Hz common-mode interference signal coupled to human body from the mains), amplifier flicker noise ($1/f$), and DC offset, as well as to problems of electrode DC offset generated at the skin-electrode interface and between electrodes. This can lead to the saturation and reduction of the CMRR of the readout front-end that defines the quality of the extracted signal [1]. To extract a high-quality EEG signal under the above-mentioned conditions, low-power, low-noise, and high-CMRR and PSRR readout front-end are needed. In the remaining parts of the paper, we introduce the state-of-the-art on the front-ends dedicated to EEG signal acquisition. The proposed EEG acquisition channel is presented in Section 3, followed by a detailed explanation of the design

and implementation of the LPGA. Section 4 shows the measurement results of the LPGA prototype integrated in 180 nm CMOS process. Conclusions and future work are given in Section 5.

2. Background and Previous Work

The amplifier in [2] consists of a low-noise closed loop amplifier (LNA) including a chopper stabilization module and a GM-C servo-loop to cancel offset current. Resistances and capacitances components are used off-chip. However, these off-chip components and the transistor of the servo-loop increase the overall noise of the instrumentation amplifier. Furthermore, the amplifier provides low CMRR (60 dB) even at higher input-impedance and low-voltages operation. This is because of performing the input modulation at the op-amp virtual ground node. Additionally, mismatch in the input capacitors can convert common-mode input signals to differential-mode noise. Low-noise, low-offset, and large-output voltage swing amplifier design is introduced in [3]. It consists of AC coupled chopper folded-cascode amplifier combined with an input-impedance boosting loop and two offset trimming loops based on auxiliary current DACs for input offset and residual offset cancelation. A back-end common-mode feedback (CMFB) circuit is designed to improve the CMRR of the active electrode system. However, the CMRR of the CMFB circuit is limited by the electrode-tissue contact impedance mismatch. In addition, the use of these many active circuits (to solve offsets, ripple, input impedance problems and CMRR enhancement) reduces the SNR and increases the integration area. Recently, AC-coupled non-inverting chopped two-stage IA followed by a transconductance amplifier (TA) is reported [4]. The input pair of the IA consists of NMOS and PMOS differential pairs connected in parallel, which reduces the thermal noise of the input-referred voltage-density and doubles the input transconductance of the core amplifier without consuming extra bias current. Besides, the above design provides voltage gain, high input-impedance, low noise, and the ability to reject large electrode offset. However, the main drawback of the presented IA topology is the lack of CMFB circuit, which gives in the common-mode output variation of the TA. This results in a high-output distortion, low CMRR and PSRR, and high offset voltage. Moreover, the use of two amplifiers increases the IA noise. To adequately amplify the low EEG signals with a dynamic range of 80 dB and compress the largest ones created during the epileptic crises, we present in this paper a low-noise and high-CMRR rail-to-rail logarithmic programmable gain amplifier (LPGA) as well as a chopped LPGA (CLPGA) dedicated to EEG acquisition channels/systems.

3. The Proposed System

Figure 1 shows the architecture of EEG acquisition system, where the proposed fully integrated CLPGA is used as pre-amplification stage [5]. A high-pass filter is employed to cut off all received signals with frequencies lower than 0.1 Hz. In addition, a high resolution (up to 14 bits) delta-sigma modulator is used to digitize the amplified signal. This high-resolution modulator maximizes the number of available quantization steps, while reducing quantization noise error and increasing signal-to-noise ratio ($\text{SNR} \geq 100$ dB). In addition, the proposed design involves a gain-programming logic to fit the EEG signal into ADC's input dynamic range. The $1/f$ noise is reduced in the proposed CLPGA by using large size PMOS and NMOS input pair transistors and applying a chopper stabilization (CS) technique [6,7]. Chopper 1, which is based on CMOS switches, is used to transpose the EEG signal to 1 kHz chopper frequency to up-modulate the $1/f$ noise to a higher frequency further away from the signal band [8]. Chopper 2 acts as demodulator to place back the amplified EEG signal on its original band. Figure 2a shows the circuit implementation for Choppers 1 and 2, where dummy transistors have been added to reduce the generated spikes from the chopping process (due to charge injection from the used switches). In addition, a chopper spike filter shown in Figure 2b has been used to cancel these spike voltages. Our work in this paper focuses only on the design, implementation, and experimentally validation of the LPGA circuit.

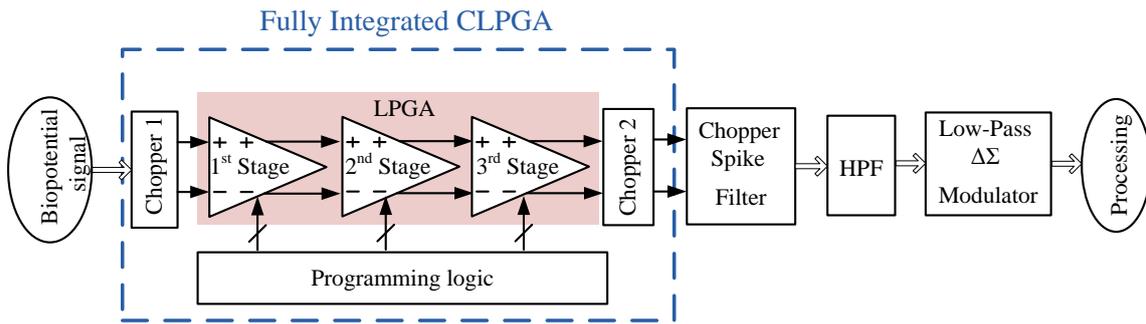


Figure 1. Block diagram of the EEG acquisition system with the proposed CLPGA.

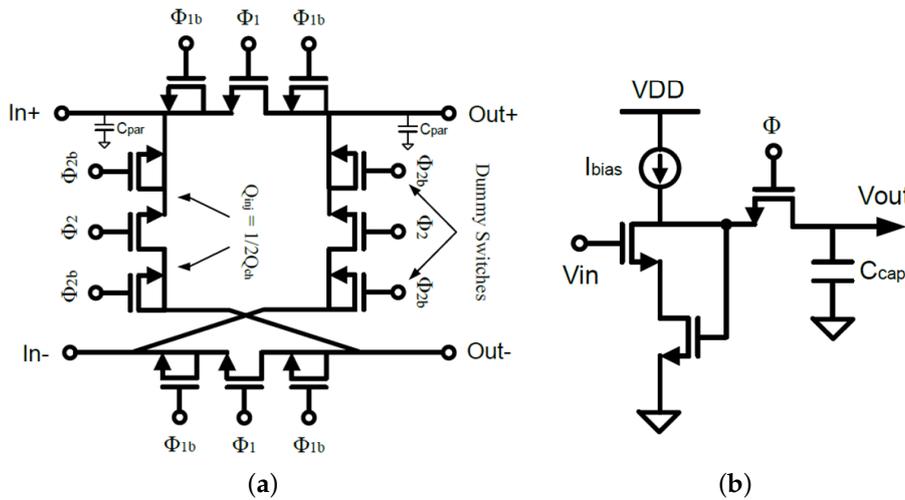


Figure 2. Circuit implementation of: (a) Choppers 1 and 2; and (b) chopper spike filter.

3.1. LPGA

Figure 3 shows the block diagram of the proposed rail-to-rail LPGA. It is based on a differential topology of true logarithmic amplifier (TLA), where the phase shift or group delay does not vary with the input signal level. The LPGA consists of three cascading rail-to-rail dual-gain stages. To achieve high CMRR, low noise, and low offset in a wide-input common-mode range, each stage is composed of chopper-stabilized parallel N and P type modules, where their differential outputs are added together to perform logarithmic function. Depending on the input common-mode range, only one chopper-stabilized module is active at any time. The N type module is active when the input common-mode voltage is from 0 V to VDD. P type module is active when the input common-mode voltage is from VSS to 0 V. The gain of each stage consists of two parallel amplifications: limiting gain amplifier (LGA) and unity gain amplifier (UGA). LGA treats the signals that have the amplitude lower than a threshold input voltage (V_{iL}) and limits the output voltage (V_{oL}) when the amplitude of the input signal is higher than or equal to V_{iL} by the following equations:

$$V_{out} = AV_{in}, \quad V_{in} < V_{iL} \tag{1}$$

$$V_{out} = V_{oL}, \quad V_{in} \geq V_{iL} \tag{2}$$

where A , V_{iL} , and V_{oL} are the gain of the LGA, the input limiting voltage, and the output limiting voltage, respectively. Usually, for the UGA, $V_{out} = V_{in}$. Thus, the output voltage of one dual-gain stage is given by:

$$V_{out} = (A + 1)V_{in}, \quad V_{in} < V_{iL} \tag{3}$$

$$V_{out} = V_{in} + V_{oL}, \quad V_{in} \geq V_{iL} \tag{4}$$

where $A + 1$ is the linear part of a dual-gain stage. Consequently, the linear gain of the cascaded three stages is equal to $(A + 1)^3$. The output voltage characteristic consists of a series of straight lines with breaking points indicating each limiting amplifier stage. Assuming n cascaded dual-gain stages are used and knowing that the limitation comes from the m th stage towards the $(m - 1)$ th stage of the TLA, the output of the m th stage (V_{om}) of the TLA is given by:

$$V_{om} = V_{oL} \left[1 + \frac{1}{A} \right] \tag{5}$$

The expected signal passed through $n - m$ limiting stages, Equation (5) applied for each stage, gives the following:

$$\begin{aligned} V_{out} &= (n - m)V_{oL} + \left(1 + \frac{1}{A} \right) V_{oL} \\ &= V_{oL} [n + 1/A - (m - 1)] \end{aligned} \tag{6}$$

The input of the m -th stage ($V_{in,m}$) at the beginning of the limitation is amplified by $m - 1$ stages and given by:

$$V_{in,m} = \frac{V_{oL}}{A} = V_{in} [(A + 1)]^{m-1} \tag{7}$$

$$m - 1 = \log_{(A+1)} \left(\frac{V_{oL}}{AV_{in}} \right) \tag{8}$$

Substituting Equation (6) into Equation (4), we find

$$V_{out} = V_{oL} \left[n + 1/A + \log_{(A+1)} \left(\frac{AV_{in}}{V_{oL}} \right) \right] \tag{9}$$

Equation (9) demonstrates that the output signals follow the suited logarithmic variation. Given that the linear gain and the precision of the LGA are determined by all involved stages, 14.67 dB gain by one stage is required. Therefore, three stages are needed to obtain a 44 dB gain by the TLA. Each dual-gain stage is based on a differential circuit used to reject the input noise coming from the previous stages. Figure 4 shows the circuit implementation of the differential rail-to-rail topology for one dual-gain stage. Both LGA and UGA circuits share M3 and M4 transistors, which are used to produce the gain limitation or blockage of differential pairs composed of M1 and M2. The UGA stage, defined by M7 and M8 transistors, is working in the triode region as resistances. The ratio of bias currents I_n and I_{ntotal} , I_p , and I_{ptotal} depends on the number of stages cascaded in order to get the desired dynamic range. The identical transistors M3 and M4 determine the limiting gain $(2A)$, which dominates the total gain of one dual-gain stage $2(A + 1)$. The sizes of these transistors are chosen to be large to get the adequate gain for each stage. M1 and M2 constitute the input differential pair of the LGA, while M3 and M4 represent the active load, and M5 and M6 form the input differential pair of the low transconductance UGA. Output currents of both LGA and UGA are added together; I_{k1} is the LGA bias current and I_{k2} is the UGA bias current. The LGA and UGA gains are linear and the transistors of their input differential pairs work in the saturation region when the amplitude of input signal is very low. However, when the amplitude of the input signal is large, one transistor of the differential pair will be off and the bias current will be drained through the other transistor. The output of LGA will be limited by the drain-source saturation voltage of transistors M3 and M4. At breaking point:

$$V_{in+} = \sqrt{\frac{2I_{k1}}{K_1}} + |V_t| = \sqrt{\frac{2I_{k3}}{K_9}} + |V_t|, \tag{10}$$

$$V_{in-} = |V_t|$$

$$V_{in} = V_{in+} - V_{in-} = \sqrt{\frac{2I_{k1}}{K_1}} = \sqrt{\frac{2I_{k3}}{K_9}} \tag{11}$$

where K_i corresponds to the transconductance's constant of transistor M_i and V_t is the threshold voltage. Therefore, V_{IL} can be set by designing I_{k1} and I_{k3} through the aspect ratio of M_3, M_4, M_{11} , and M_{12}

Rail-to-rail output stage (Buffer B), which is realized by class-AB configuration, is connected at the output of the last stage of the LPGA to achieve low-output distortion and therefore getting the maximum SNR at the output [9]

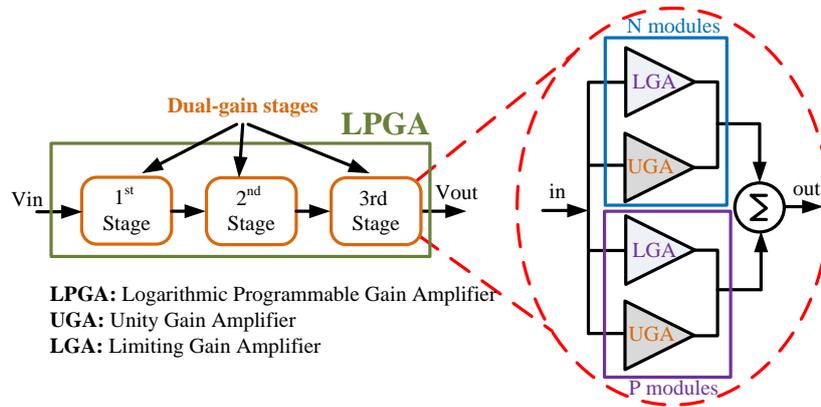


Figure 3. Block diagram of the proposed rail-to-rail LPGA.

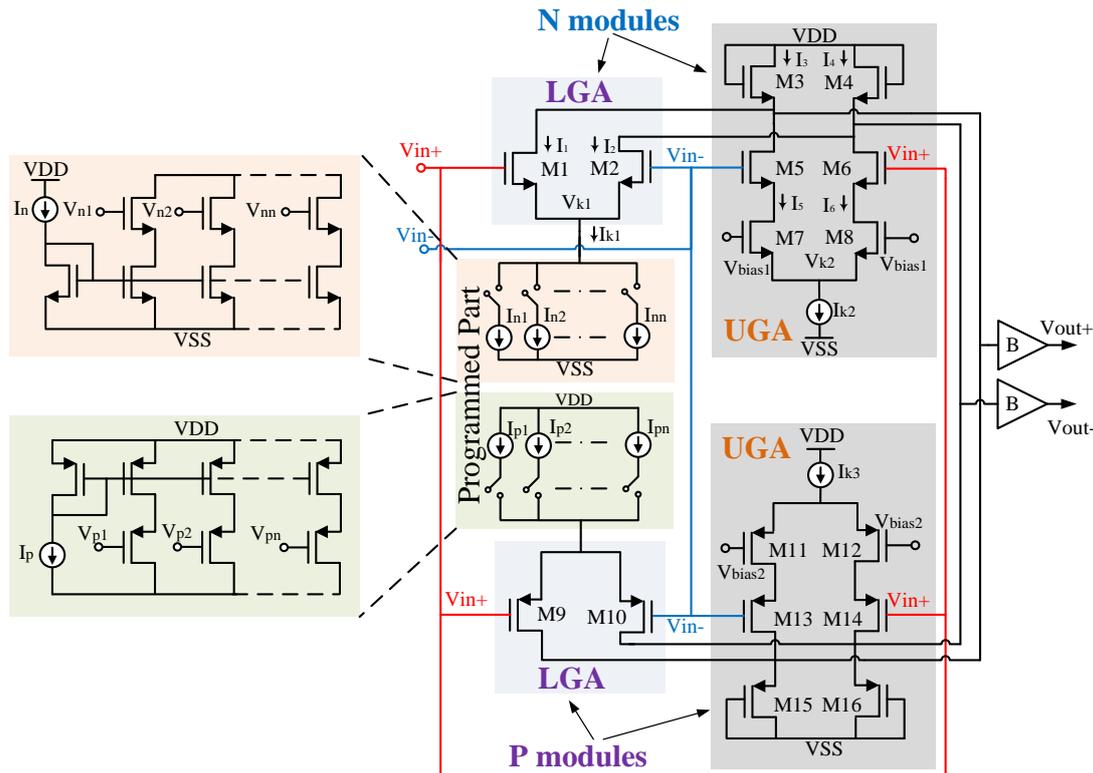


Figure 4. Circuit schematic of one dual-gain stage.

3.1.1. CMRR

The CMRR is the important critical parameter of the amplifier to be enhanced to reject the mains interference. Usually, to improve the CMRR of the EEG channel, a driven right leg (RLD) circuit is used to feed a common-mode signal to the patient body to cancel the interference [10]. This method effectively reduces the common-mode gain and increases the CMRR. However, this kind of loop is difficult to stabilize due to the uncontrollable electrode-tissue impedance of the dry electrodes.

To solve this problem, a digital RLD circuit has been presented in [11] to provide a high common-mode signal reduction at power line frequency. However, this circuit requires additional modules such as notch filter, digital signal processing and digital-to-analog converter, and hence greater power dissipation. Another technique to improve CMRR is the use of common-mode feedback [3], i.e., to feed the common-mode signal back to the input of each preamplifier. However, the feedback loop requires a summing amplifier and large compensation-capacitors for common-mode extraction and stability. This results in large silicon area. In this work, the presented LPGA is formed by cascading three amplification stages, where the CMRR (dB) of the overall LPGA can be expressed by [12]:

$$(CMRR_{LPGA})_{dB} = (CMRR_{1st})_{dB} + (CMRR_{2nd})_{dB} + (CMRR_{3rd})_{dB} \tag{12}$$

Thus, a very-high CMRR can be achieved. In addition, the PSRR will be increased since it is directly related to the gain [12]. To further improve the CMRR, the common-mode gain (A_{cm}) of the logarithmic amplification topology must perform very-high attenuation on all common-mode signals applied at the input of the LPGA module.

To calculate the A_{cm} of the perfectly balanced differential amplifier shown in Figure 4, its small-signal equivalent half circuit is extracted, where we ignored the body-effect transconductance (g_{mb}) [13]. However, as this perfectly balanced amplifier is symmetric, the calculation is greatly simplified by using the superposition theorem on the circuit shown in Figure 5. Firstly, we found the responses to the small signal currents in term of the pure common-mode input V_{ic} of each branch, and adding all currents at summation node A to obtain the total common-mode gain $A_{cmTotal}$, i.e., $A_{cmTotal} = V_{oc}/V_{ic}$. For the four branches of the circuit of Figure 5 and considering our optimization of this circuit, the values of r_{ds1} , r_{ds2} , r_{ds5} , and r_{ds6} are very small and for ideal case $g_{m1} = g_{m5}$, $g_{m2} = g_{m6}$, and $g_{m4} = g_{m7}$. Thus, the drain currents of each branch can be expressed by:

$$I_{d1} = \frac{V_{ic}g_{m1}}{1 + 2R_{tail}g_{m1}} \tag{13}$$

$$I_{d2} = \frac{V_{ic}g_{m2}}{1 + g_{m2}r_{ds4} - 2R_{tail}r_{ds4}g_{m2}g_{m4}} \tag{14}$$

$$I_{d5} = \frac{V_{ic}g_{m5}}{1 + 2R_{tail}g_{m5}} \tag{15}$$

$$I_{d6} = \frac{V_{ic}g_{m6}}{1 + g_{m6}r_{ds7} - 2R_{tail}r_{ds7}g_{m6}g_{m7}} \tag{16}$$

where $I_{ds1} = -I_{ds5}$ and $I_{ds2} = -I_{ds6}$, thus $I_{ds1} + I_{ds2} = -(I_{ds5} + I_{ds6})$. Consequently, the total common-mode gain at the summation node A can be expressed as

$$A_{cmTotal} = A_{cm1} + A_{cm2} = \frac{2}{g_{m3}} \left(\frac{g_{m1}}{1 + 2R_{tail}g_{m1}} + \frac{g_{m2}}{1 + g_{m2}r_{ds4} - 2R_{tail}r_{ds4}g_{m2}g_{m4}} - \frac{g_{m5}}{1 + 2R_{tail}g_{m5}} - \frac{g_{m6}}{1 + g_{m6}r_{ds7} - 2R_{tail}r_{ds7}g_{m6}g_{m7}} \right) = 0 \tag{17}$$

where g_{m3} is the transconductance of the active load of each stage and A_{cm1} and A_{cm2} are the common-mode gain of the N modules and P modules, respectively.

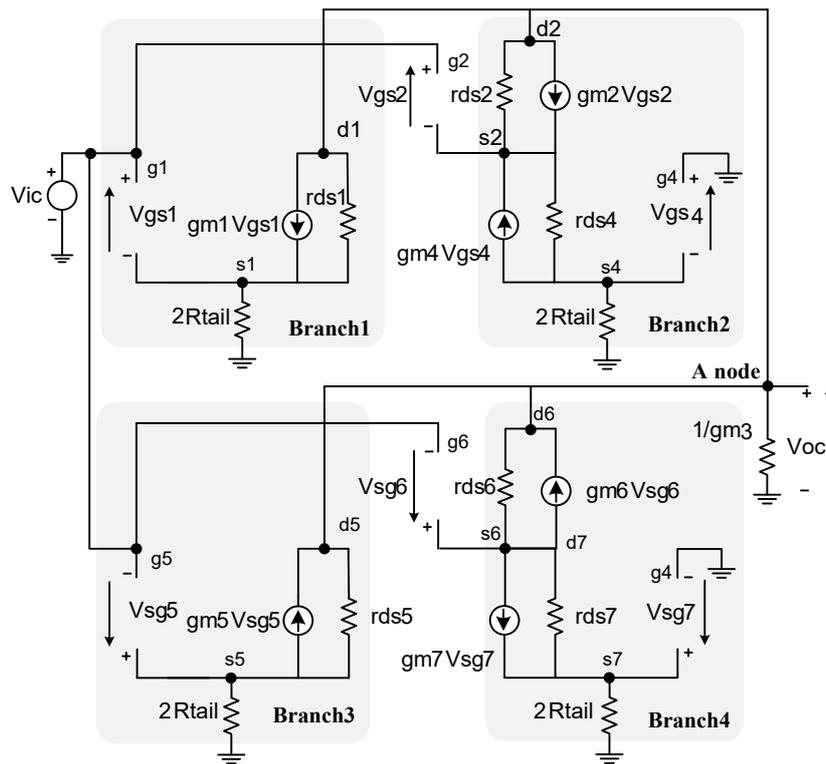


Figure 5. Small-signal equivalent half circuit of the LGA.

3.1.2. Programming Logic

To fit the EEG signal into ADC’s input dynamic range, a programming approach is proposed which is based on the variation of the tail current transistor width of each stage. To program the gain of the one dual low-gain stage, the tail currents of the N and P type LPGA stages must be reduced consecutively. By turning off the switches of In1 and Ip1 in the programming ladders, the node voltage (Vk1) increases, Vgs1/Vgs2 decreases, Vds1/Vds2 increases, Vgs3/Vgs4 decreases, and I1, I2, I5 and I6 decrease. Accordingly, the gain A and the dynamic range $2^3(A + 1)$ decrease. The logic diagram shown in Figure 6 is employed to program the gain of the LPGA. It has been implemented using a shift register, which receives a series input and produces n parallel outputs to tune the N modules. In addition, complementary n outputs have generated (through inverters) to tune the P modules.

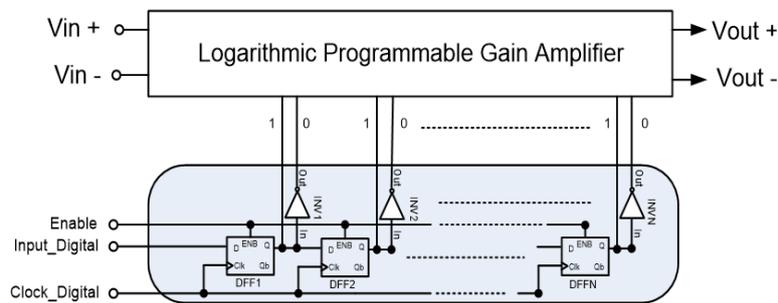


Figure 6. Programming logic diagram of the LPGA.

3.1.3. Rail-to-Rail Output Stage

To get the maximum SNR at the output, the LPGA is required to achieve a rail-to-rail output swing, which is realized by class-AB architecture shown in Figure 7 and connected at the output of the last stage of the LPGA. This architecture consists of two transconductances (G_{mn}, G_{mp}) and a pair of complementary common-source amplifiers (M9 and M10). The output is connected to the inverting

input terminal (V_{out}) and the input signal is applied to the non-inverting input terminal (V_{in}). It is noted that the small resistors of the demodulator's switches, in which the LPGGA needs to drive them, make the primary motivating factor to use class-AB buffer as output stages to achieve low-output distortion [14]. M2 and M8 are directly connected to VDD and GND, respectively, to have an active load of zero, thus not amplify the feedback signal. The balancing of the bias currents for the differential pairs is done by means of the feedback topology. When the non-inverting input voltage is decreased, the gate voltages of M9 and M10 are increased. As a result, M10 starts to discharge the output node. When the output voltage reaches the level that the voltage difference between the input and output is almost zero, M10 stops discharging the output node [14]. Similarly, when the input voltage (V_{in}) is increased, M9 charges the output load until the output voltage almost equals the input voltage. The single-ended amplifier incorporates a complementary differential pair as the input stage does, to obtain a full input voltage swing.

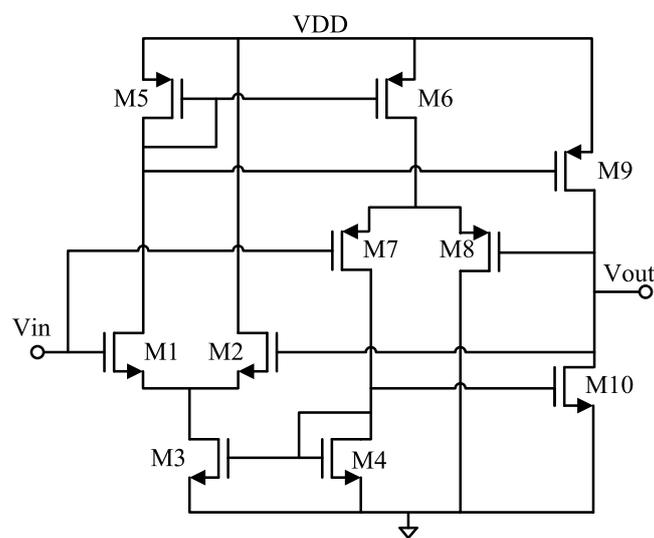


Figure 7. Circuit schematic of single-ended Class AB buffer.

4. Measurement Results

A die photograph of the proposed LPGGA and CLPGA circuits implemented in TSMC 180 nm CMOS process is shown in Figure 8, where they occupy an active area of 0.4 mm^2 and 0.52 mm^2 , respectively. The post-layout simulations were done with Spectre under Cadence platform, and the fabricated chip was tested in our Polystim Neurotech Laboratory. The DC transfer function of the CLPGA is shown in Figure 9. For an input DC voltage of 15 mV, the simulated output DC voltage is approximated as 0.67 VPP. Figure 9a demonstrates the simulated transfer function of the CLPGA, while the bode transfer function of the simulated CMRR is shown in Figure 9b. The simulated values depict the high ability of the CLPGA to reject the common-mode interference (50/60 Hz) ambient signal coming from the main source coupled to the patient's body as well as any signal noise and DC offset electrodes applied to CLPGA differential input. Simulation results of the CLPGA bode transfer for different gains at 1 dB step and for a maximum gain of 44 dB are presented in Figure 10a. The transient simulation results are given in Figure 10b, which shows the step-down output magnitude of the CLPGA controlled by the digital part at each rising edge of the clock signal right after the falling edge of the enable signal as well the spike voltage due to charge analog switches. The chopping frequency is 1 kHz, while 0.5 kHz clock is used for the chopper spike filter. The measurements have been performed in a closed-loop configuration shown in Figure 11 [15,16]. Based on this method, the LPGGA is configured with a signal gain of -1 V/V using $R_1 = R_2 = 10 \text{ k}\Omega$ and the LPGGA has been supplied by $\pm 0.9 \text{ V}$ and it is acting as a preamplifier for its own error signal with $R_3 = 1 \text{ M}\Omega$ and a variable resistor (R_4) of $2 \text{ k}\Omega$ used as a voltage divider at the inverting input. A $20 \text{ }\mu\text{F}$ ceramic capacitor,

C_1 , is connected across R_3 to filter the low amplitude error signals from noise. Furthermore, to reduce the effect of finite output impedance of the LPGA-under-test and the effect of feed-through due to the feedback path of the test set-up, a general purpose amplifier configured as a voltage buffer is used in the feedback loop [16]. Note that the passive elements and the buffer shown in Figure 11 are off-chip components. The open-loop gain obtained from the set-up is calculated as:

$$\frac{V_{out}}{In_Test} = Gain_{LPGA} \frac{R_4}{R_1 + R_3} V_{in} \quad (18)$$

This open-loop gain was measured using a sine wave input of 5 V_{PP} and a frequency of 100 Hz. Figure 12a shows approximately 500 mV_{PP} output signal swing, for the differential input error voltage magnified by a factor of 100, with a maximum value less than or equal to 5 mV_{PP}. The measured open-loop gain is at least 37 dB at 100 Hz. The CMRR is measured by connecting the differential input of the LPGA to a sine wave of 1 V_{PP} at 100 Hz. Figure 12b shows the measured peak-to-peak value of the LPGA differential output, where a 1 V_{PP} input signal has been applied and we obtained the mean values of V_{out+} and V_{out-} , which are found to be 252 μ V and 258 μ V, respectively. Then, the differential signal (7.44 μ V) is obtained by subtracting V_{out+} and V_{out-} . Therefore, the common mode gain is calculated as $20 \text{ Log } (7.44 \mu\text{V}/1 \text{ V})$, which results in 103 dB. The high CMRR value is the sum of the common-mode gain (≈ 103 dB) and the differential gain (≈ 37 dB), making the capacity of LPGA to reject any common noise signal applied to its differential input. The input-referred noise voltage is measured by connecting the LPGA inputs to ground and performing spectrum analysis of the output signal. Figure 13a shows the measured linear RMS value of the differential output under various input amplitudes and frequencies (75.39 μ V_{rms}@ 0.1 Hz, 3 mV_{rms}@ 50/60 Hz, and 42.11 μ V_{rms}@ 100 Hz). Consequently, the measured input-referred noise voltage of the LPGA is determined by dividing the previous values by the linear gain (100 V/V). The input-referred offset voltage of the LPGA is measured by operating the LPGA as comparator and applying a ramp of 1 V_{PP} at V_{IN+} , and the ground at V_{IN-} . The measured input-referred offset voltage that it must be put on the input V_{IN+} to set the DC differential output of the LPGA to zero is 78.13 μ V, as shown in Figure 13b. In addition, this figure depicts the measured maximum differential output swing of the LPGA, around 616 mV_{PP}.

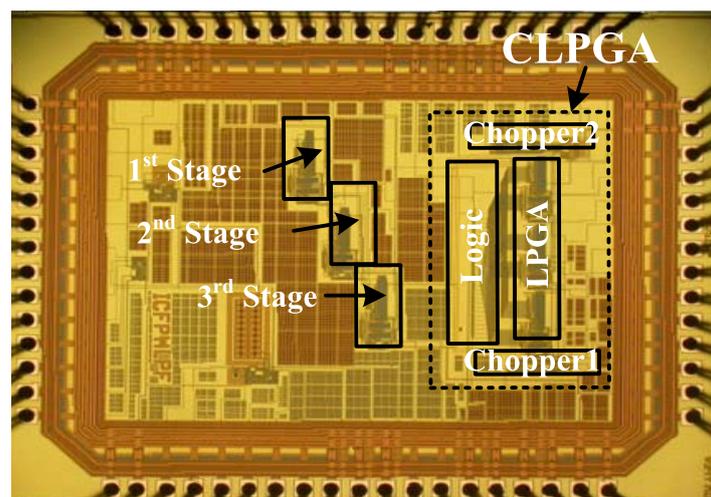


Figure 8. Die micrograph.

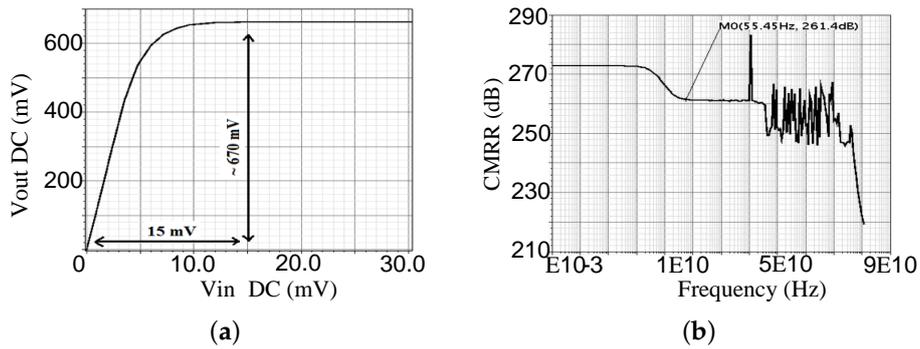


Figure 9. (a) Simulated Transfer Function of the CLPGA; and (b) bode transfer function of the simulated CMRR.

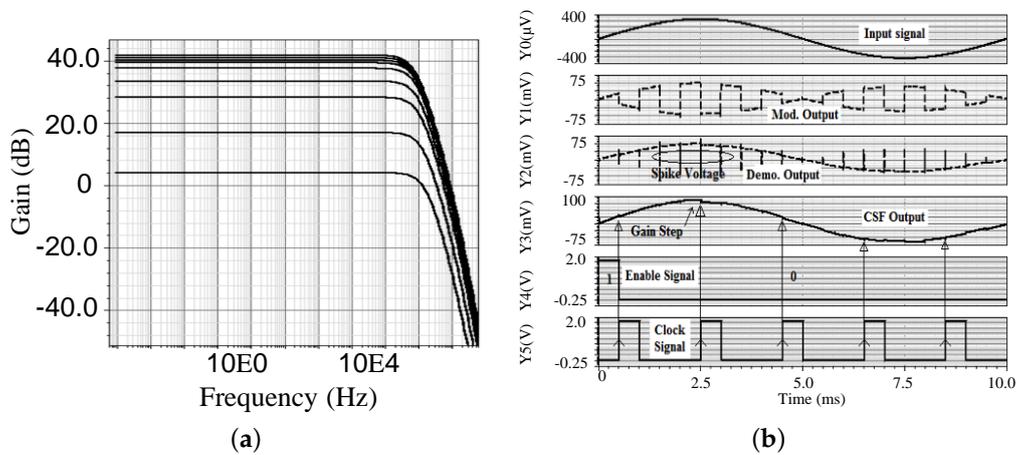


Figure 10. CLPGA simulation results: (a) bode transfer function for different gains; and (b) control of the $f_{CLK} = 0.5$ kHz and input sine wave of $360 \mu\text{V}$ and 100 Hz.

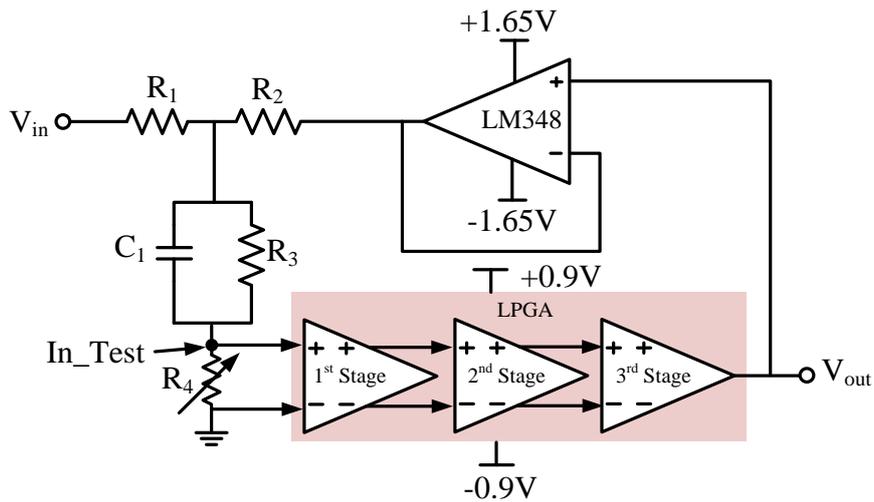
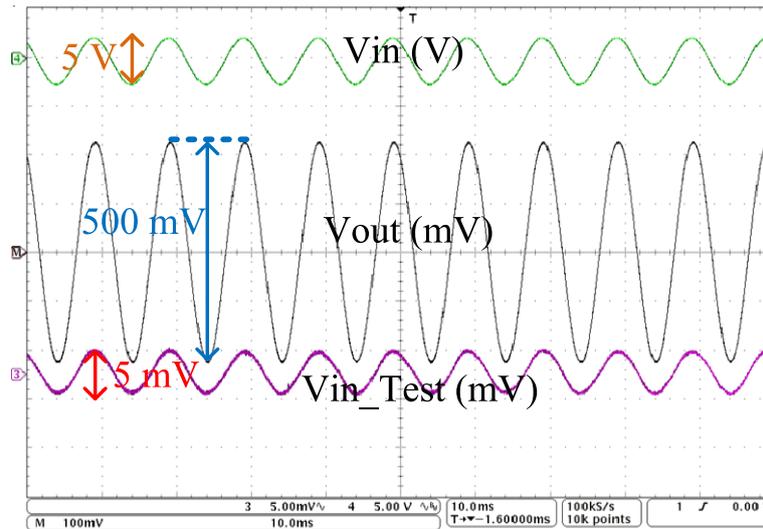


Figure 11. Experimental set-up for LPGA open-loop gain measurement.

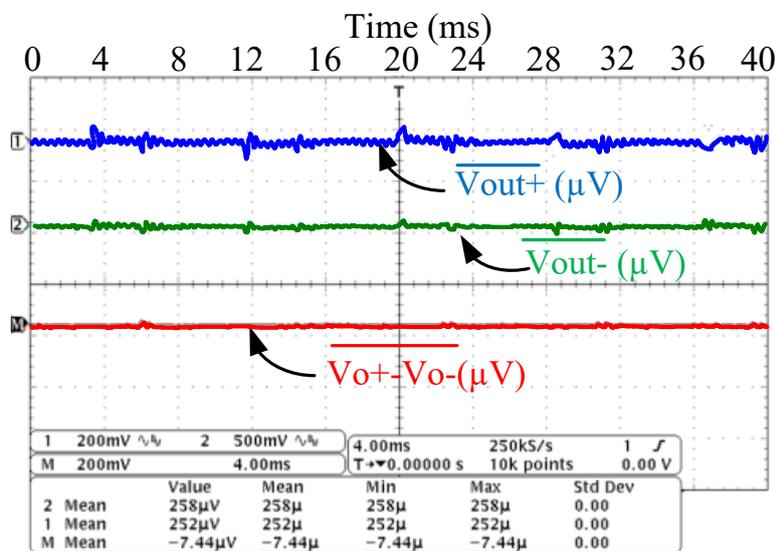
To amplify the signals, grouping offset, detected by the mismatched EEG electrodes and avoid severe distortion in the LPGA performance as well unity gain bandwidth (UGBW) variation, the measured input voltage range of the complementary LPGA can range from -200 to 200 mV, as presented in Figure 14, where a sine wave signal at 100 Hz is increased gradually at the differential input until the output signal begins to distort. Measurement results of the LPGA are summarized in

Table 1 for a resistive and a capacitive load of 10 MΩ and 95 pF, respectively. Although the proposed design achieves high-CMRR, it consumes relatively large amount of power compared to similar designs, as a result of using three amplification stages to increase the CMRR. Therefore, and to provide a fair comparison, we considered a figure of merit (FOM), which is the noise efficiency factor (NEF) as shown in Equation (17) [17]. The NEF of the proposed design is 29.8.

$$NEF = V_{rms,in} \sqrt{\frac{2 \cdot I_{tot}}{\beta \cdot U_T \cdot 4KT \cdot BW}} \tag{19}$$

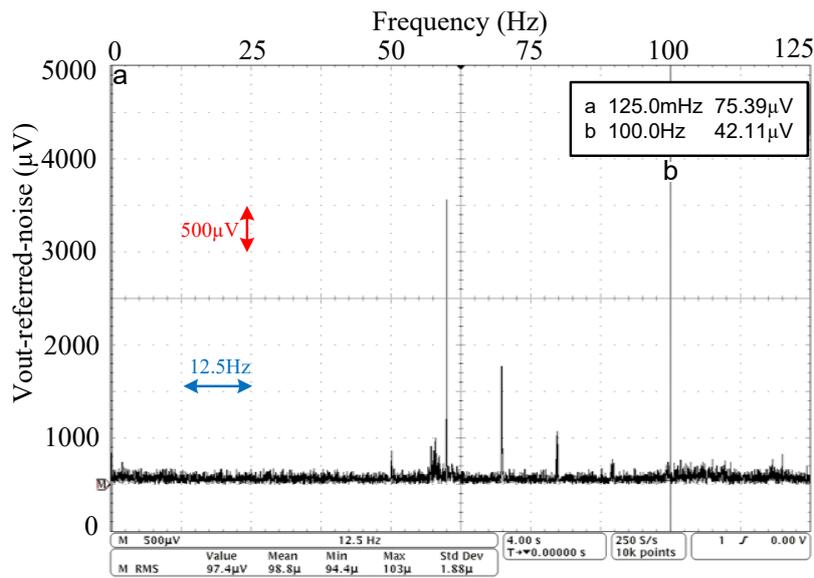


(a)

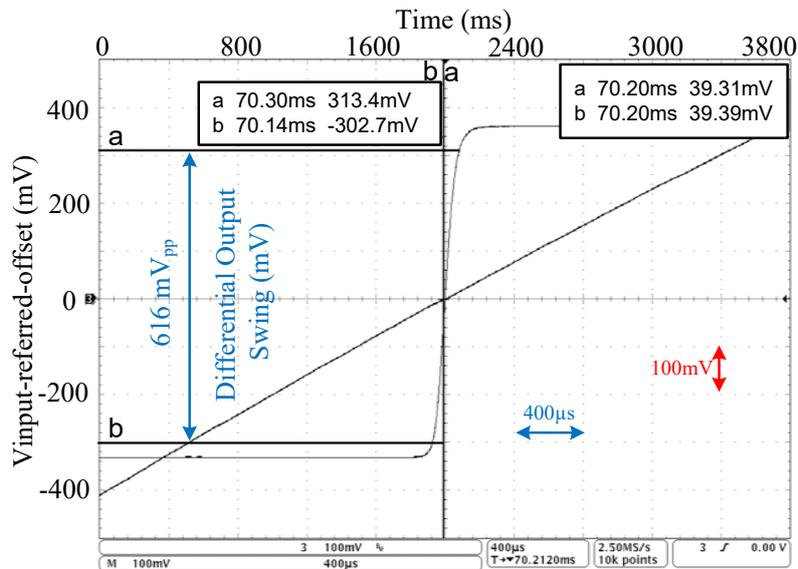


(b)

Figure 12. Measured open loop ($R_{load} = 10\text{ M}\Omega$ and $C_{load} = 95\text{ pF}$): (a) voltage gain of the LPGA at 100 Hz for $V_{in} = 5\text{ V}_{pp}$; and (b) CMRR (140 dB) of the LPGA at 100 Hz for $V_{in} = 1\text{ V}_{pp}$.



(a)



(b)

Figure 13. Measured open loop ($R_{load} = 10\text{ M}\Omega$ and $C_{load} = 95\text{ pF}$): (a) output-referred noise of the LPGA at 0.1 Hz, 50/60 Hz, and 100 Hz; and (b) input-referred offset voltage and maximum differential output swing of the LPGA for an input ramp of 1 V_{PP} at 100 Hz

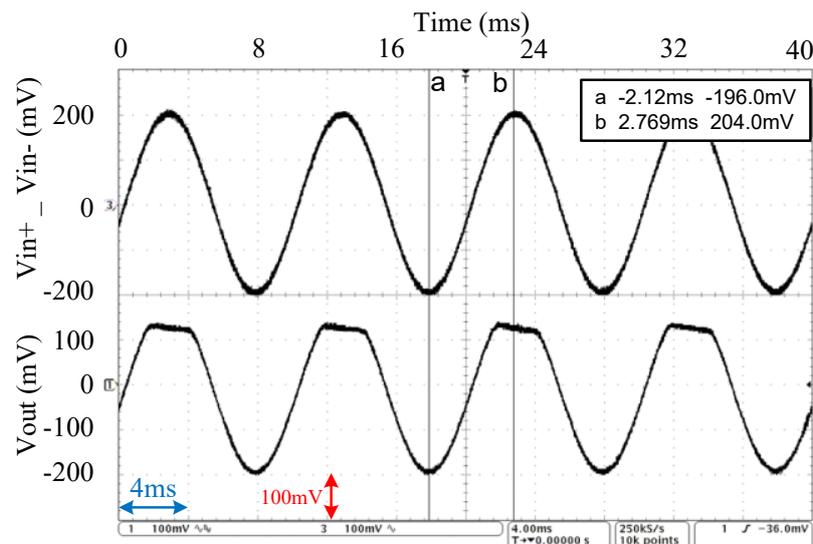


Figure 14. Measured open loop ($R_{load} = 10 \text{ M}\Omega$ and $C_{load} = 95 \text{ pF}$) input voltage range using an input sine wave at 100 Hz.

Table 1. LPGA Performance Summary and Comparison.

Reference	[18]	[19]	[20]	[21]	[4]	This Work
Technology (CMOS)	180 nm	65 nm	180 nm	180 nm	180 nm	180 nm
Supply Voltage (V)	1.2	0.8	1.5	1.8	1.8	± 0.9
Gain (dB)	58	15	0	NA	11–101	37
CMRR (dB)	>100	NA	97	102	84	140
Noise	$1.3 \mu\text{V}_{\text{rms}}$	$0.99 \mu\text{V}_{\text{rms}}$	$1 \mu\text{V}_{\text{rms}}$	$0.65 \mu\text{V}_{\text{rms}}$	$1.75 \mu\text{V}_{\text{rms}}$	$0.754 \mu\text{V}_{\text{rms}}$
Bandwidth (Hz)	0.5–500	0.1–500	0.25–250	0.5–100	0.5–100	0.1–100
Power Consumption (μW)	9.24	0.8	5.5	104	82	189
PSRR@50/60Hz (dB)	NA	NA	NA	NA	NA	145
Area (mm^2)	1.2 a	0.024	2.25 a	15.8 a	17.55 b	0.4
THD (%)	0.082	NA	NA	NA	NA	0.045
NEF	6.15	1.81	4.67	19.1	45.6	29.8

a, chip area, including ADC; b, chip area.

5. Conclusions and Future Work

A fully integrated logarithmic programmable gain amplifier (LPGA) dedicated to EEG acquisition systems is introduced in this paper. It features low-noise and high common-mode rejection ratio performance. A proposed logarithmic amplification topology that exhibits low common-mode gain is presented. To further improve the CMRR, three amplification stages were cascaded. Moreover, a chopper stabilization technique was adopted to reduce the $1/f$ noise and the inherent DC offset voltage of the input transistors. The generated spikes from the chopping process were canceled by employing a chopper spike filter. Furthermore, a rail-to-rail output stage realized by class-AB architecture was used to maximize the SNR at the output. The proposed circuit was designed and fabricated in 180 nm CMOS technology. Complete experimental characterization was performed to validate the functionality of the presented preamplifier circuit. The LPGA achieved 140 dB CMRR and an input-referred noise of $0.754 \mu\text{V}_{\text{rms}}$. It consumes 189 μW from 1.8 V power supply and occupies an active area of 0.4 mm^2 .

To further improve the proposed LPGA, more optimizations will be performed to decrease its power consumption. Besides, a fully integrated EEG acquisition channel including the ADC implementation is our next step.

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