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Design of a Wide-Band Voltage-Controlled Ring Oscillator Implemented in 180 nm CMOS Technology

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Abstract: The design of a wide-band voltage-controlled oscillator (VCO) modified as a VCO with programmable tail currents is introduced herein. The VCO is implemented by using CMOS current-mode logic stages, which are based on differential pairs that are connected in a ring topology. SPICE simulation results show that the VCO operates within the frequency ranges of 2.65–5.65 GHz, and when it is modified, the VCO with programmable tail currents operates between 1.38 GHz and 4.72 GHz. The design of the CMOS differential stage is detailed along with the symbolic approximation of its dominant pole, which is varied to increase the frequency response in order to achieve a higher oscillation frequency when implementing the ring oscillator structure. The layout of the VCO is described and pre- and post-layout simulations are provided, which are in good agreement using CMOS technology of 180 nm. Finally, process, voltage and temperature variations are performed to guarantee robustness of the designed CMOS ring oscillator.

Keywords: VCO; current-mode logic; MOSFET; PVT variations; Layout

1. Introduction

Originally, current mode logic (CML) was used as a mean to design VLSI logic gates to accomplish nanosecond delays. CML emerged with bipolar junction transistors (BJT) [1], and the aim was focused on eliminating the emitter-coupled logic (ECL) drawbacks at that time, such as large power consumption and excessive heat generation [2]. When CMOS technology was used to design CML stages, it was introduced with the adaptive pipeline technique to compensate for deviations in the MOS device's parameters and in the operating environment, which in turn was used to compensate for clock skew and to decrease the power dissipation [3]. It was shown that CML has many advantages, including high speed symmetric operation, equal noise margins, equal rise and fall times, requirement of relatively few components and low power dissipation. The symmetric operation feature allows an operation with a lower logical swing, thus improving the operating speed even more. That way, several CML blocks have been used for the implementation of various topologies and logic gates, such as, buffers, latches, flip-flops, XOR gates, and push–pull topologies, among others. In this manner, this article introduces the design of a wide-band voltage-controlled oscillator (VCO) that is implemented using CML stages connected in a ring topology. It is worth mentioning that designing VCOs is a challenge [4–6]; besides, one can find guidelines to deal with modern design issues, such as ultra-low-power requirements [7]. Other important applications require robust VCOs, such as in designing analog-to-digital converters [8,9] or phase-locked loops [10]. Some VCOs are designed using

complex devices such as negative differential resistances [11], and others such as the one introduced herein use blocks connected in a ring topology [12].

Designing a VCO with a ring structure and using differential CML stages has the advantage of great immunity to supply disturbances [13]. Other desired features in designing a VCO are associated to accomplish low-power consumption, minimum layout area, large output frequency range and wide tuning range. Those target specifications become difficult to achieve due to the continuous down scaling of silicon technology. On the one hand, VCOs can be implemented using LC-tank structures, which can tune transistors to operate at higher frequencies than ring oscillators, are relatively immune to power supply noise [14], and have outstanding phase noise and jitter performance [13]. On the other hand, designing VCOs in a ring topology is frequently a more attractive alternative because of its wider tuning range, small layout area, higher gain, low cost, robustness to variations, simplicity and scalability in deep nanoscale processes [15,16]. One challenge of VCOs based on ring topologies is reducing the deterministic jitter induced by power supply noise [14]. That way, some authors explore the use of compensation techniques to reduce the sensitivity to supply noise and also the current consumption at high switching frequencies.

The oscillation frequency of a VCO can be evaluated using Equation (1), and, to vary such a frequency, a CMOS CML stage with active load is usually employed, as shown herein. In this manner, the CMOS CML stage has a P-type MOS transistor as load, which operates in the triode region and its associated resistance is controlled by a voltage source V_{ctrl}. The associated resistance of the active load is connected with a load capacitor in which both give rise to a time constant τ, so that varying V_{ctrl} makes varying the oscillation frequency [16], and depending on the number of CML stages N, one can use Equation (1). Extending the oscillation frequency in a wider range that can be controlled by varying V_{ctrl}, requires a good design methodology. For instance, one must consider the number of stages that must be connected in a ring topology, as well as the delay of each CMOS CML stage. At first sight, one can think on reducing the number of stages and their associated delay to increase the oscillation frequency. However, the main effects are that decreasing N yields a reduction in gain, which may result in the oscillation eventually stopping. In this manner, this article shows that deriving the symbolic approximation of the dominant pole of the CMOS CML stage, through the use of the high-frequency small-signal equivalent model of the MOS transistor [17], can help to enhance the oscillation frequency.

$$f_{osc} = \frac{1}{2N \cdot \tau} \tag{1}$$

The rest of this article is organized as follows: Section 2 describes the considerations taken for the design of both the CMOS CML stage and the VCO, and the analyses carried out to measure its performance characteristics. The design of a VCO using CMOS differential stages with programable tail currents is detailed in Section 3. Section 4 describes the layout design of the CMOS differential stages and the VCO. Finally, Section 5 summarizes the conclusions.

2. VCO-Based on CMOS Differential Stages

2.1. CMOS Differential Stage with Passive Load

The main objective in designing a CMOS differential stage that is used for the implementation of a VCO, is oriented to achieve the highest oscillation frequency. In this manner, the first task is identifying the design issues to increase the frequency response of the CML block, which is shown in Figure 1. Its sizing considers that, according to Equation (1), the oscillation frequency is inversely proportional to both the number of CML stages N and the propagation delay τ. Therefore, to achieve a high oscillation frequency, the delay must be reduced [16,18]. It can be approximated by Equation (2), so that, varying the transistors dimensions [15,18,19], the delay can be reduced by augmenting g_{ds} and reducing the equivalent capacitance, where C_L could be the dominant one. On the one hand, augmenting the MOS transistors dimensions leads to larger parasitic capacitance values. Therefore, the

sizing is focused on reducing the dimensions of the differential-pair transistors. On the other hand, the load resistance R_L affects the delay and it also modifies the value of the dominant pole [20], described as ω_p. In integrated circuit design, ω_p is directly proportional to the gain-bandwidth-product (GBW), and considering the trade-off between GBW and the open-loop gain A_{OL}, the most important issue is enhancing GBW [21,22].

$$\tau = \frac{C_L R_L}{1 + g_{ds} R_L} \tag{2}$$

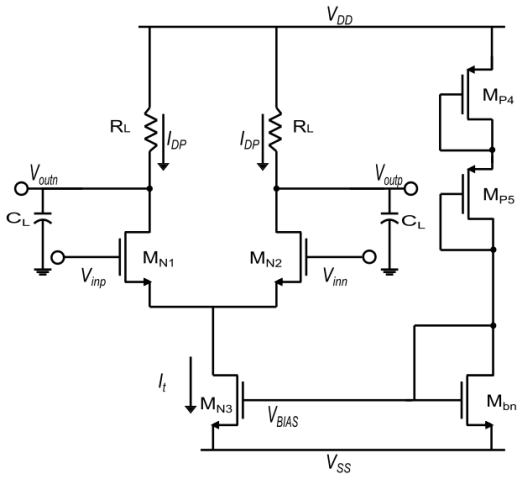


Figure 1. CMOS current-mode logic stage with passive load.

To find the appropriate load resistor value one can use $R_L = (V_{DD} - V_{out})/I_{DP}$. If the MOS transistors should be in saturation, one must accomplish $|V_{DS}| > |V_{GS}| - |V_{TH}|$ and $|V_{GS}| > |V_{TH}|$. For instance, setting $I_t = 4mA$, $V_{DD} = -V_{SS} = 0.9V$, and $|V_{TH}| \approx |0.5V|$, then $R_L = 450\ \Omega$. The overdrive voltages take into account that small size dimensions are desirable, and the ratios are calculated by Equation (3) that is obtained from the quadratic model equation. In this manner, using CMOS technology of 180 nm from UMC, the sizes are set to $W_{MN1} = W_{MN2} = 70\ \mu m$, $W_{MN3} = 600\ \mu m$, $W_{MP4} = W_{MP5} = 800\ \mu m$, and $W_{Mbn} = 200\ \mu m$.

$$\left(\frac{W}{L}\right) = \frac{2I_D}{\mu_n C_{ox}(|V_{GS}| - |V_{TH}|)^2} \tag{3}$$

Since the VCO is desired to operate at high frequencies, the MOS high-frequency model shown in Figure 2 [22] is used. An input voltage V_{FV} is connected to the node labeled V_{inp}, and node V_t is associated to the sources of the differential pair, so that performing nodal analysis results in the matrix formulation given in Equation (4), where: $a = s(C_{gs1} + C_{gd1} + C_D)$, $b = sC_{gd1}$, $c = sC_D$, $d = sC_{gs1}$, $e = -sC_{gd1} + gm_1$, $f = s(C_{gd1} + C_L + C_D + C_{db1}) + gds_1 + \frac{1}{R_{L1}}$, $g = gm_1 + gmb_1 + gds_1$, $h = sC_D$, $i = s(C_{gd2} + C_D + C_{db2}) + gds_2 + \frac{1}{R_{L2}}$, $j = gm_2 + gmb_2 + gds_2$, $k = sC_{gs1} + gm_1$, $l = gds_1$, $m = gds_2$, $n = s(C_{gs1} + C_{sb1} + C_{sb2} + C_{gd3} + C_{db3} + C_{gs2}) + gm_1 + gmb_1 + gds_1 + gm_2 + gds_2 + gds_3 + gmb_2$. Applying the work in [23,24], the compact and second-order symbolic expression that approaches the dominant pole can be expressed by $\omega_p = Denom/Numer$, where: $Numer = 7.3786e14(1.6695e25gm_2 - 1.4135e37C_L - 1.4599e39C_Lgm_2 - 5.5999e38C_Dgm_2 + 1.5623e37C_L - 2.5912e40C_Lgm_2^2 - 2.5912e40C_Dgm_2^2 + 6.8467e+49C_L^2 + 9.3800e38C_Lgm_2 + 9.9525e39C_Lgm_2^2 + 3.1681e51C_L^2gm_2 + 1.2127e24)$ and $Denom = (8.8495e15C_L + 1.2183e17C_Lgm_2 + 3.8782e28C_L^2)(1.2199e26 - 4.3726e27gm_2 + 5.3461e38C_L + 1.6794e27gm_2 - 9.4497e25)$. It is notorious that the dominant pole value heavily depends on both C_L and gm_2, the values of which are proportional to the transistor's sizes [20]. That way, the reduction of transistor's sizes leads to an

increase of ω_p. To verify the symbolic approximation, the Bode magnitude given in Figure 3 compares the complete or original transfer function (TF) with the approximated TF.

$$\begin{bmatrix} a & -b & -c & -d & -1 \\ e & f & 0 & -g & 0 \\ -h & 0 & i & -j & 0 \\ -k & -l & -m & n & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{inp} \\ V_{outn} \\ V_{outp} \\ V_t \\ I_{FV} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_{FV} \end{bmatrix} \quad (4)$$

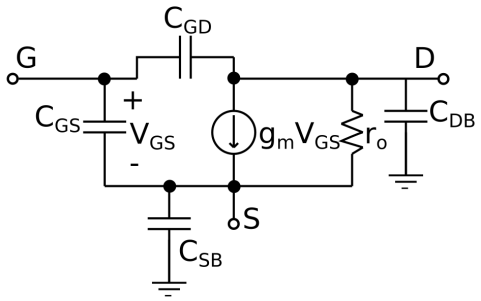


Figure 2. High-frequency MOSFET model [22].

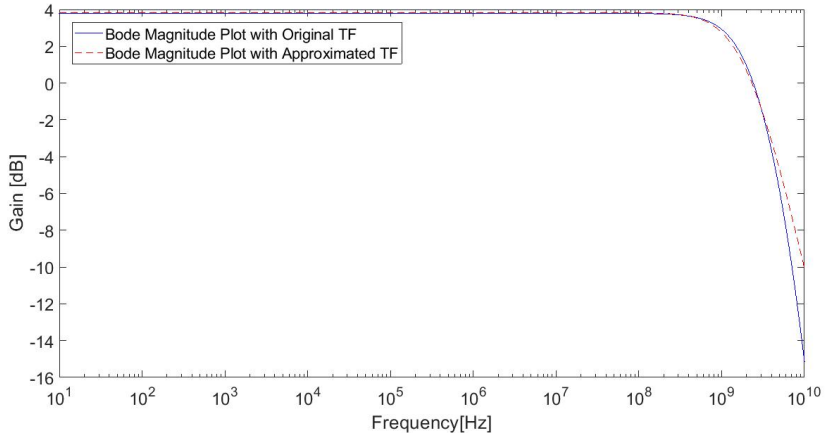
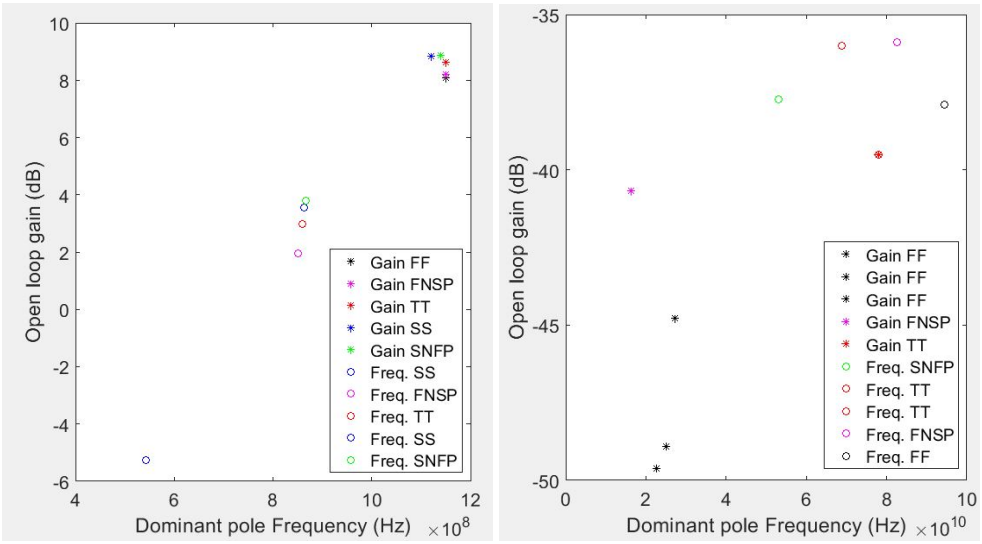


Figure 3. Bode magnitude of the current-mode logic stage shown in Figure 1, simulated using CMOS technology of 180 nm, and comparing the original TF versus the symbolic approximation.

The CMOS CML stage can be characterized measuring the open-loop gain A_{OL} and the dominant pole ω_p. The gain-bandwidth product GBW is the frequency at which A_{OL} becomes 0 dB [25]. The load capacitor is selected under the supposition that a CML stage must be capable of driving three stages, therefore we assume $C_L = 3C_{gs}$, where C_{gs} is obtained from the .lis file generated from the SPICE circuit simulation. The design is tested under process, voltage and temperature (PVT) variations. A robust design must have a low PVT sensitivity, and it is performed considering five process corners: TT (typical–typical), SS (slow–slow), SNFP (slow–fast), FNSP (fast–slow) and FF (fast–fast). The test considers three voltage variations of $\pm 10\%$ of $\pm V_{supply} = 0.9V$, and three temperature variations from $T- = -20$ °C, $T = 60$ °C and $T+ = 120$ °C [26]. Figure 4 summarizes the higher and lower values resulting from the PVT variations for $R_L = 450\ \Omega$. The dependence of the gain and dominant pole values under PVT variations depicted in this figure show that there is a wide variation in both parameters, where the high gain cases occur mostly for lower dominant pole frequencies and viceversa. Table 1 summarizes the measured A_{OL} and ω_p values, for each PVT variation. Due to the huge variations, this design is unsuitable for designing a VCO. Therefore, a CMOS CML stage with active load is detailed in the next subsection.

Table 1. Open-loop gain and dominant pole values over PVT variations with $R_L = 450\ \Omega$.

Corners	Temperature	T−			T			T+		
	Voltage	V−	V	V+	V−	V	V+	V−	V	V+
TT	A_{OL} (dB)	2.98	8.64	4.05	7.07	−1.7	−36	2.25	−26	−39.5
	ω_p (Hz)	860 M	1.2 G	2.3 G	1.1 G	3.1 G	68.7 G	1.7 G	21 G	78.1 G
SS	A_{OL} (dB)	−5.3	3.8	8.84	3.55	7.18	3.23	5.31	4.24	−20.1
	ω_p (Hz)	543 M	870 M	1.1 G	863 M	1.1 G	1.81 G	993 M	1.4 G	12 G
SNFP	A_{OL} (dB)	3.81	8.88	−3.5	6.81	−4.4	−34.3	0.41	−22.9	−37.7
	ω_p (Hz)	866 M	1.1 G	4.6 G	1.1 G	4 G	49.8 G	1.8 G	15.3 G	53 G
FNSP	A_{OL} (dB)	1.94	8.21	8.02	6.96	3.12	−35.9	4.4	−26	−40.7
	ω_p (Hz)	850 M	1.2 G	1.7 G	1.1 G	2.1 G	82.6 G	1.5 G	24.6 G	16.4 G
FF	A_{OL} (dB)	8.08	4.43	−45	−4.5	−38	−48.9	−29	−42	−49.6
	ω_p (Hz)	1.2 G	2.3 G	27 G	4.6 G	94 G	25.1 G	28 G	16.6 G	22.6 G



(**a**) (**b**)

Figure 4. (**a**) Higher and (**b**) lower gains and dominant pole frequencies with $R_L = 450\ \Omega$.

2.2. CMOS Differential Stage with Active Load

Figure 5 shows the CMOS differential stage with active loads implemented by P-type MOS transistors (M_{P3} and M_{P4}) that must operate in the triode region. The value of the equivalent resistance is controlled by varying the voltage at the gates of the PMOS transistors, which is called control voltage V_{ctrl} [16,27]. The output conductance of the PMOS transistor can be approached as $1/g_o = 1/\mu C_{ox}(|V_{ctrl} - V_s| - |V_{th}|)$. The sizing of M_{P3}-M_{P4} must accomplish $|V_{DS}| < |V_{GS}| - |V_{TH}|$ and Equation (5) [28]. To achieve a wide range of control-voltage, the sizes are: $W_{MN1} = W_{MN2} = 60\ \mu$m, $W_{MP3} = W_{MP4} = 40\ \mu$m, $W_{MN5} = 500\ \mu$m, $W_{Mbn} = 200\ \mu$m, and $W_{MP6} = W_{MP7} = 800\ \mu$m, in all cases $L = 0.18\ \mu$m.

$$I_D = \mu C_{ox} \frac{W}{L}[(|V_{GS} - V_{TH}|)\,|V_{DS}| - \frac{1}{2}|V_{DS}|^2] \tag{5}$$

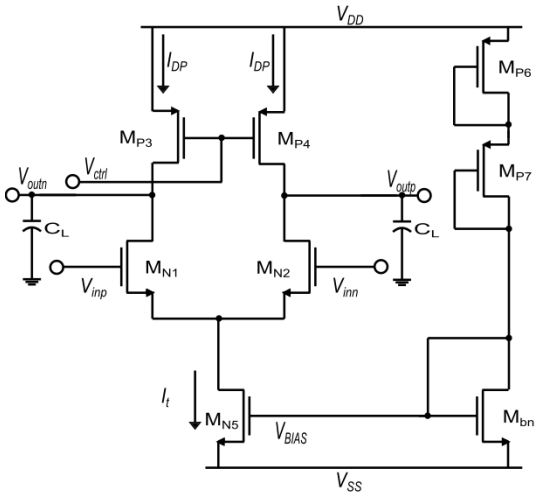


Figure 5. CMOS differential stage with active load and voltage control.

The approximation of the dominant pole is performed in the same way as done for the CML stage with passive load, and it can be approached by Equation (6). The comparison of the Bode magnitude of both the original and the approximated transfer functions (TF) is shown in Figure 6. Again, it can be appreciated that the dominant pole depends on both C_L, g_m of the differential pair, and g_{ds} of the active load [24], so that the reduction of the transistor's sizes leads to an increase of ω_p.

$$\omega_p = \frac{3.29e54(C_D+C_{db2}+C_{db4}+C_L)+2.43e44(gds_2+gds_4)+1.46e56gm_2(C_D+C_L)+3.86e45(gds_4gm_2)+2.51e58(C_Lgds_4gm_2)}{3.29e54(gds_2+gds_4)+1.46e56(gds_4gm_2+gds_2gds_4+gds_4gmb_2)} \quad (6)$$

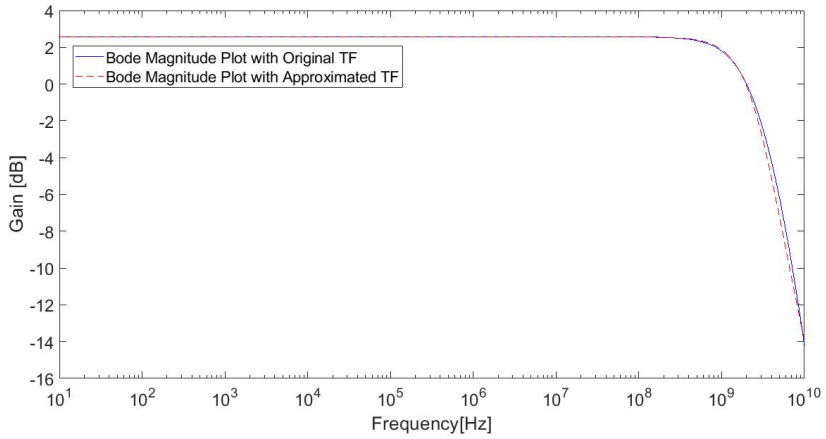
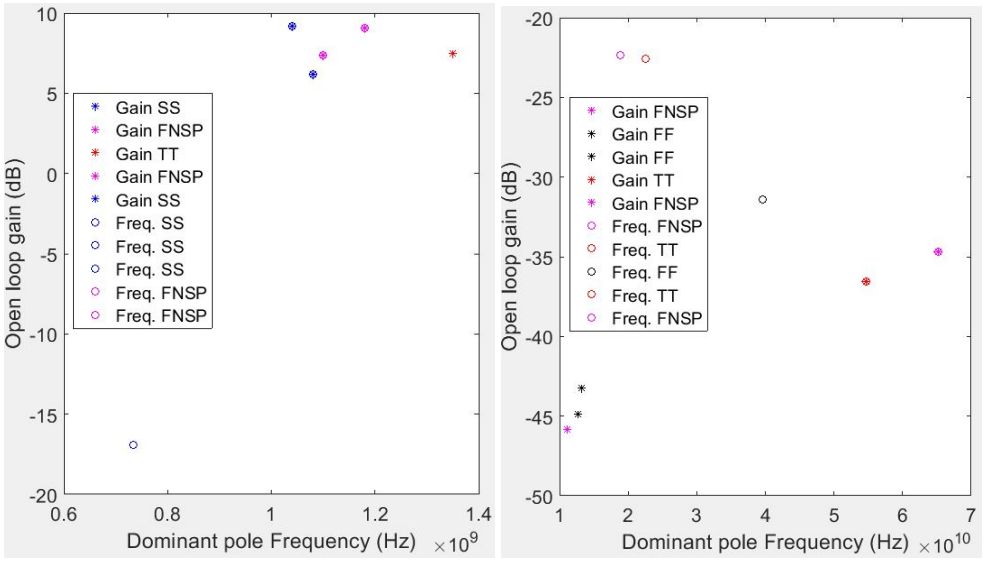


Figure 6. Bode magnitude of the CMOS differential stage shown in Figure 5, simulated using CMOS technology of 180 nm, and comparing the original TF versus the symbolic approximation.

The characterization of the CMOS differential stage with active load provides the results given in Section 4, where one can see the comparison between the performances with and without post-layout simulations. The PVT variations are simulated setting $V_{ctrl} = -0.2V$, considering five process corners (TT, SS, SNFP, FNSP and FF), three voltage variations ($\pm 10\%$ of $\pm V_{supply} = 0.9V$), and three temperature variations ($T- = -20$ °C, $T = 60$ °C and $T+ = 120$ °C) [26]. The higher and lower gain and frequency values are shown in Figure 7. One can see that the higher dominant pole frequencies are achieved in the FNSP and TT process corners; however, the FNSP corner also presents some of the lowest dominant pole values along with the SS corner. Table 2 summarizes the PVT simulation results.

Table 2. Open-loop gain and dominant pole frequency over PVT variations with $V_{ctrl} = -0.2$ V.

Corners	Temperature	T−			T			T+		
	Voltage	V−	V	V+	V−	V	V+	V−	V	V+
TT	A_{OL} (dB)	−9.4	−2.1	5.19	−0.4	7.49	−22.6	4.99	−2.8	−36.5
	ω_p (Hz)	1.7 G	2.4 G	2.1 G	1.9 G	1.4 G	23 G	1.3 G	3.5 G	55 G
SS	A_{OL} (dB)	−16.9	−7.94	−1.12	−5.38	0.3	9.17	−0.29	6.16	−6.43
	ω_p (Hz)	734 M	1.6 G	2.2 G	1.4 G	1.7 G	1 G	1.4 G	1.1 G	4.4 G
SNFP	A_{OL} (dB)	−9.3	−2.4	4.47	−1.2	4.86	−1.59	1.39	3.97	−17.7
	ω_p (Hz)	1.8 G	2.6 G	2.2 G	2 G	1.6 G	3.5 G	1.6 G	1.5 G	11.1 G
FNSP	A_{OL} (dB)	−9.7	−1.97	5.58	0.15	9.08	−34.7	7.36	−22.3	−45.9
	ω_p (Hz)	1.6 G	2.3 G	2 G	1.7 G	1.2 G	65.2 G	1.1 G	18.8 G	11.1 G
FF	A_{OL} (dB)	−3.5	3.45	−7.1	5.4	−10.6	−43.2	3.05	−31.4	−44.9
	ω_p (Hz)	2.6 G	2.5 G	10 G	1.7 G	9.7 G	13.3 G	2.5 G	39.6 G	12.7 G



(**a**) (**b**)

Figure 7. (**a**) Higher and (**b**) lower gains and dominant pole frequencies, for the CMOS differential stage with active load and $V_{ctrl} = -0.2$ V.

2.3. Voltage Controlled Oscillator Based on CMOS Differential Stages

The CMOS differential stage with active load is used herein to design a four-differential stages VCO, as shown in Figure 8. In this case, the sizes of the MOS transistors are varied to reach the highest oscillation frequency, so that they were established as $W_{MN1} = W_{MN2} = 40$ µm, $W_{MP3} = W_{MP4} = 30$ µm, with $C_L = 50fF$, thus resulting in oscillations between the frequencies 2.65 GHz and 5.65 GHz, which require control voltages in the range between -0.2 V and -0.9 V. The oscillating frequency of 5.65 GHz with a control voltage of -0.9 V is shown in Figure 9, for which the average power consumption was 39 mW. The control voltage range can be appreciated in Figure 10.

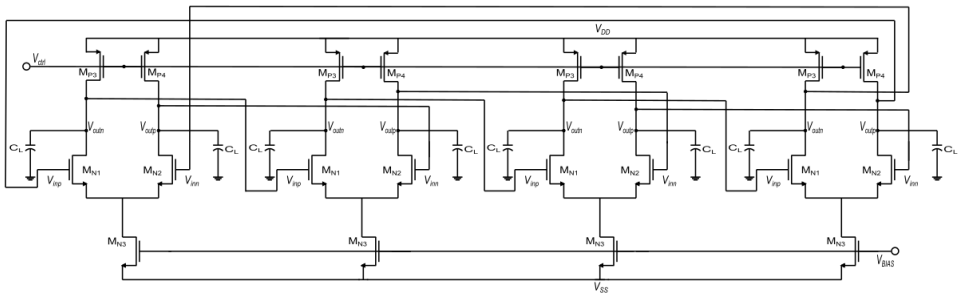


Figure 8. Voltage controlled ring oscillator consisting of four-differential stages with active loads.

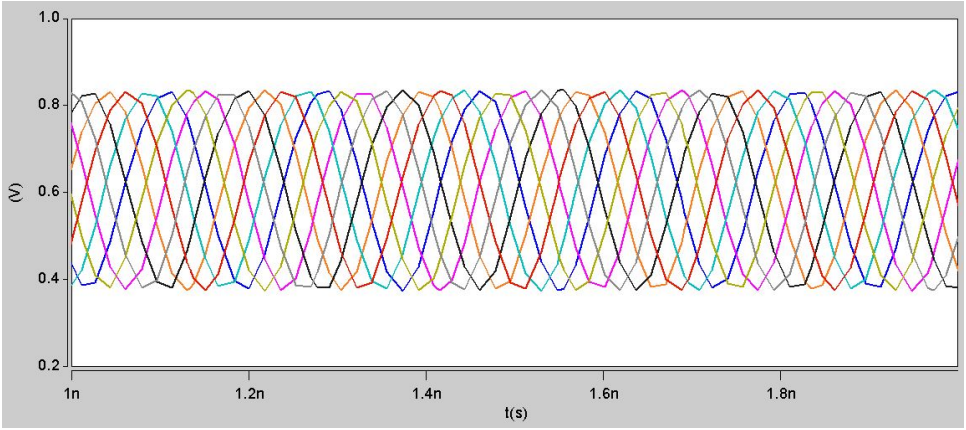


Figure 9. VCO response when $V_{ctrl} = -0.9$ V and f_{osc} = 5.65 GHz.

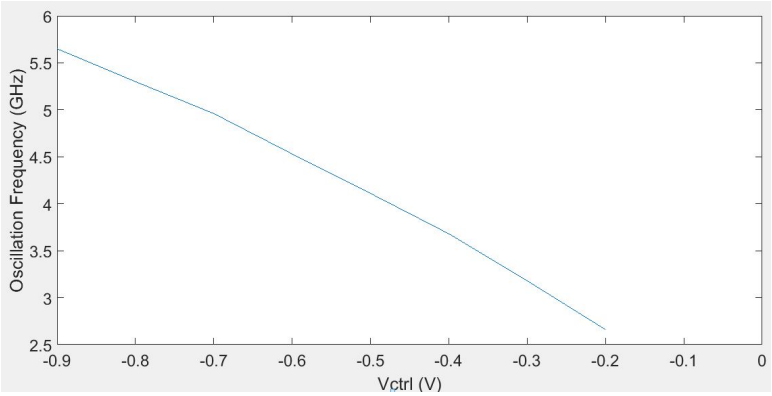


Figure 10. Oscillation frequency vs. control voltage variation.

The static supply sensitivity of the VCO is very important, and it is measured observing the change in the oscillation frequency due to a 10% supply voltage variation [29]. Figure 11 shows the frequency variations produced by the changes in the supply voltage. The results show a static supply sensitivity of $0.11\%/1\%V_{supply}$. Table 3 shows a comparison between the proposed VCO and other CML-based VCOs already published in the literature. As one can see, the three VCOs are designed using CMOS technology of 180 nm and voltage supplies of 1.8 V. Other VCOs implemented in CML-based ring structure have been designed and applied in analog-to-digital converter [30] and pseudo-random bit sequence generator [31]. However, they are not listed in Table 3 due to lack of information such as number of stages, supply voltage, tail current, load capacitance, and power dissipation. Besides, the VCO in [30] was implemented using CMOS technology of 90 nm and the one in [31] using 180 nm. These VCOs provide frequency tuning ranges of 1–7.2 and 2.7–3.3 GHz and voltage tuning ranges of 0.32–0.62 and 0–1.1 V, respectively. On the other hand, the proposed VCO uses four stages and a higher load capacitance compared to the one in [15,32], and it provides the higher frequency tuning range while maintaining an acceptable control-voltage range, power dissipation and supply sensitivity.

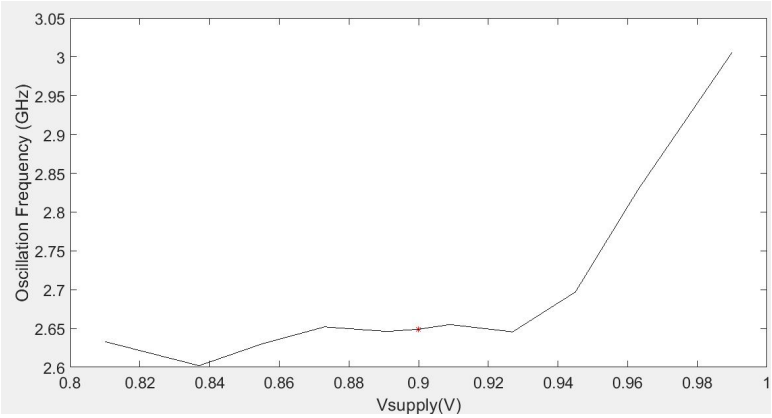


Figure 11. VCO's oscillation frequency vs. supply voltage.

Table 3. Comparison among the proposed VCO and related designs.

	This Work	**[15]**	**[32]**
Technology (nm)	180	180	180
Number of stages	4	4	9
Supply voltage (V)	±0.9	1.8	1.8
Tail current (mA)	4	1.4	0.145–0.859
Load capacitance (fF)	50	19.7	-
Freq. tuning range (GHz)	2.65–5.65	2.2–2.7	0.292–1.54
Volt. tuning range (V)	−0.2 to −0.9	-	0.6 to 1.8
@-0.9 V Power Diss. (mW)	44.2	10.1	0.895
Supply sensitivity	$0.11\%/1\%V_{DD}$	$0.045\%/1\%V_{DD}$	-

3. VCO with Programmable Tail Currents

Based on the VCO design shown in Figure 8, this section shows its programmable version by designing a logic that controls the flow of the tail current. The programmability of the tail current can be performed using different number of switches; in this section, four switches are used, as shown in Figure 12. Basically, the sizes of the MOS transistors are calculated to control the current flow, which can also be replaced by a variable current source when setting the V_{ctrl} to a constant value. In this case, the control-voltage is fixed to the value that allows the widest current variation to achieve a wide programmable current range, while keeping the transistors working in the desired operation region. It resulted in $V_{ctrl} = -0.55$ V to have the oscillation frequency shown in Figure 13, which is associated to a current variation between 3 and 8 mA, approximately.

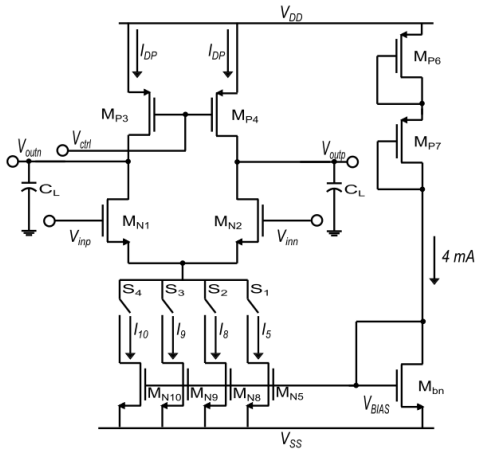


Figure 12. Programmable tail currents in the CMOS differential stage using four switches.

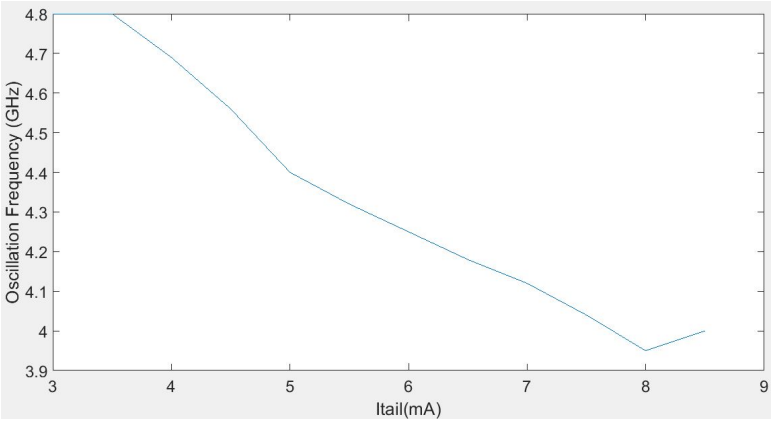


Figure 13. Oscillation frequency vs. tail current @ $V_{ctrl} = -0.55$ V.

The four switches shown in Figure 12 allow a discrete variation of the current that can be programmed using four bits. Each MOS transistor is sized differently to provide a fraction of the current that will flow in the tail of the differential pair. That way, the programmable current ranges can be established to be between 3 mA and 7.5 mA, and the current flowing through the bias transistors M_{P6}, M_{P7}, M_{bn} is defined to be 4 mA. Therefore, to be able to program the tail current with discrete values, the MOS transistors M_{N5}, M_{N8}, M_{N9} and M_{N10} are sized to drive a current of 4 mA, 2 mA, 1 mA and 0.5 mA, respectively. The sizes of those MOS transistors are the following: $W_{MN5} = 800$ µm, $W_{MN8} = 400$ µm, $W_{MN9} = 200$ µm and $W_{MN10} = 100$ µm. In this case, the logic states of the switches are programmed as shown in Table 4, which summarizes the logical values needed to produce each tail current, where a logical 1 is produced with a pulse of 0.9 V and a logical 0 with a pulse of 0 V, the pulses are mean that the corresponding switch must be closed and open, respectively. It is worth mentioning that the design of the switches must be done carefully to mitigate the on parasitic resistance and capacitances of the MOS transistors. Figure 14 shows the programmable tail currents in the VCO's output waveforms generating an oscillation frequency $f_{osc} = 4.72GHz$ for a 3 mA tail current. The tendency of the oscillation frequency to decrease with an increasing tail current coincides with the programmable VCO's results shown in Figure 13.

Table 4. Programmable switches to provide bias currents in the range from 3 to 7.5 mA, in steps of 0.5 mA.

Current (mA)	s4	s3	s2	s1
3	0	1	1	0
3.5	0	1	1	1
4	1	0	0	0
4.5	1	0	0	1
5	1	0	1	0
5.5	1	0	1	1
6	1	1	0	0
6.5	1	1	0	1
7	1	1	1	0
7.5	1	1	1	1

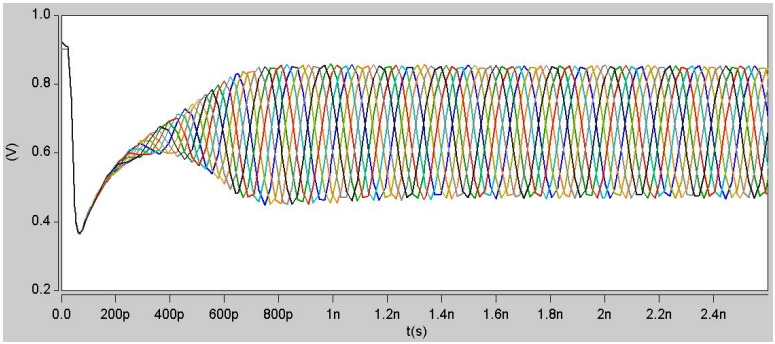


Figure 14. VCO's output waveforms for a programmed current of 3 mA.

4. Layout Design of the VCO Based on CMOS Differential Stages with Active Load

The minimum width and length sizes of the MOS transistors for a 180 nm UMC technology are 0.24 µm and 0.18 µm, for the NMOS and PMOS transistors, respectively. The minimum diffusion area is 0.1936 µm^2, the minimum poly to diffusion spacing is 0.22 µm, and the minimum $N+$ implant overhang of diffusion equals 0.22 µm. The sizes for the SPICE simulations are slightly modified to achieve a highly symmetrical layout in order to reduce mismatches [25]. The MOS transistors are placed with the same orientation and maintaining the NMOS and PMOS accommodated in different areas of the chip, but trying to use minimum silicon area. The placement of each transistor is the first task to get a symmetrical layout; after this, electromigration rules are taken into account to determine the minimum amount of fingers, which are necessary for the desired current to flow through each metal without damaging the integrated circuit. In this manner, the efficient placement is to maintain NMOS transistors at the bottom block and the PMOS transistors at the top block, to achieve a good matching between the differential pair transistors, which are placed in an interdigitated structure and over M_{bn}. The layout of one CMOS differential stage with active load is shown in Figure 15, which occupies an area of 6377 µm^2, including the power grid.

The sizes of the CMOS differential stages consider dimensions with multiplicities to ensure that the post-layout simulations provide the same or a best range of control-voltage and oscillation frequency. Table 5 summarizes the comparison of the simulation results of the CMOS differential stage performing post-layout characterization, which has a power consumption of 32 mW. This table shows that there are very minor changes in the characterizations of the CMOS differential stage in the post-layout simulation.

Table 5. Pre- and post-layout characterization of the CMOS differential stage.

Characteristic	Pre Layout	Post Layout
A_{OL} (dB)	2.49	2.49
ω_p (Hz)	1.15 G	1.15 G
GB (Hz)	1.02 G	1.02 G
$PhaseMargen$ (°)	129	129
$A_{common-mode}$ (dB)	−9.92	−9.92
$CMRR$ (dB)	12.41	12.41
$PSRR+$ (dB)	11.54	11.54
$PSRR-$ (dB)	−2.5	−2.5
$SlewRate+$ (V/µs)	349	350
$SlewRate-$ (V/µs)	−278	−277
V_{inmax} (V)	0.85	0.85
V_{inmin} (V)	−0.11	−0.11
t_{rise} (ps)	220.1	220.1
t_{fall} (ps)	638.2	634.8
t_{pHL} (ps)	999.9	999.9
t_{pLH} (ps)	0.05	0.05
$SettlingTime$ (s)	2.3n	2.3n
V_{outmax} (V)	0.75	0.75
V_{outmin} (V)	−0.1	−0.1

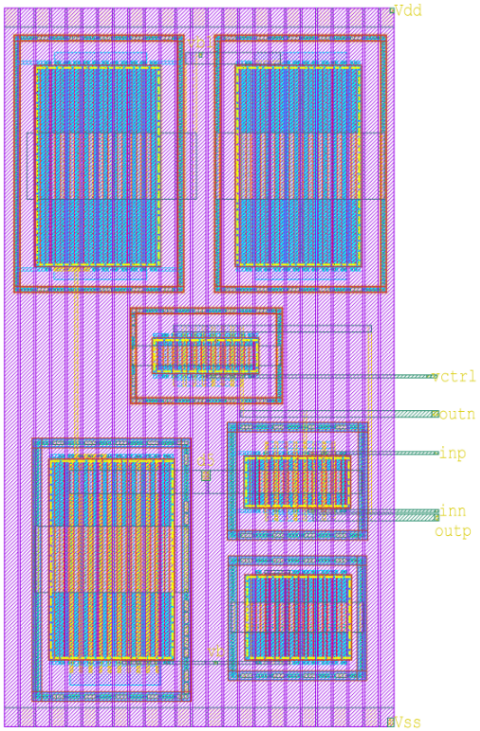
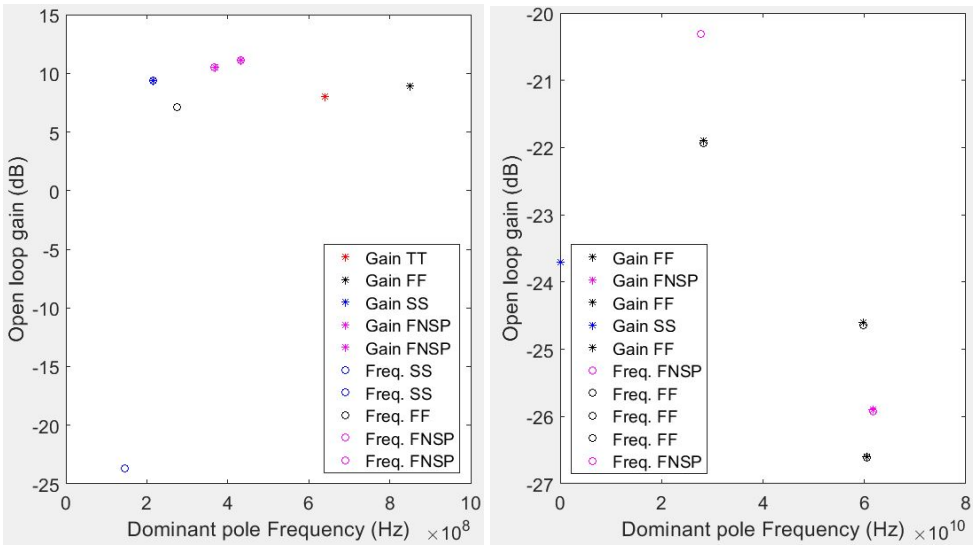


Figure 15. Layout of a CMOS differential stage implemented in Tanner from Mentor graphics using UMC 180 nm technology.

PVT variations are simulated for five corners and setting $V_{ctrl} = -0.2$ V, so that the higher and lower gain and frequency values for the post-layout VCO are shown in Figure 16. The higher dominant pole frequencies are achieved in the FNSP and the FF process corners, however, the FNSP corner also presents some of the lowest dominant pole frequency values along with the SS corner. Table 6 summarizes the measured A_{OL} and ω_p values for each PVT variation.



(**a**) (**b**)

Figure 16. (**a**) Higher and (**b**) lower gains and dominant pole frequencies of the CMOS differential stage with active load under PVT variations and setting $V_{ctrl} = -0.2$ V.

Table 6. Post-layout open-loop gain and dominant pole frequency values under PVT variations and setting $V_{ctrl} = -0.2$ V.

Corners	Temperature	T−			T			B		
	Voltage	V−	V	V+	V−	V	V+	V−	V	V+
TT	A_{OL} (dB)	−10.7	−2.8	4.5	−0.54	8.03	−5.11	5.53	1.62	−20
	ω_p (Hz)	839 M	1.3 G	1.3 G	1 G	641 M	4.2 G	623 M	1.1 G	20 G
SS	A_{OL} (dB)	−23.7	−14	−5.1	−9.3	−2.7	4.31	−2.8	3.52	9.36
	ω_p (Hz)	145 M	132 M	969 M	580 M	841 M	832 M	666 M	696 M	215 M
SNFP	A_{OL} (dB)	−10.7	−3.2	3.1	−1.96	3.68	3.9	0.12	3.15	−3.8
	ω_p (Hz)	871 M	1.3 G	1.4 G	1.1 G	919 M	497 M	936 M	569 M	1.5 G
FNSP	A_{OL} (dB)	−10.2	−2	6.34	0.85	11.1	−20	10.5	−18	−26
	ω_p (Hz)	837 G	1.3 G	1.1 G	969 M	432 M	28 G	368 M	16 G	62 G
FF	A_{OL} (dB)	−0.07	8.89	−13	7.1	−15	−25	−8.4	−22	−27
	ω_p (Hz)	1.6 G	851 M	17 G	276 M	16 G	60 G	4.5 G	28 G	60 G

The complete layout of the four-stage VCO based on CMOS differential stages is shown in Figure 17. It reuses the layout of the CMOS stage shown in Figure 15, and the complete layout is also designed with the goal of obtaining a highly symmetrical layout. The silicon area of the complete VCO including the power grid is 17,019 μm^2.

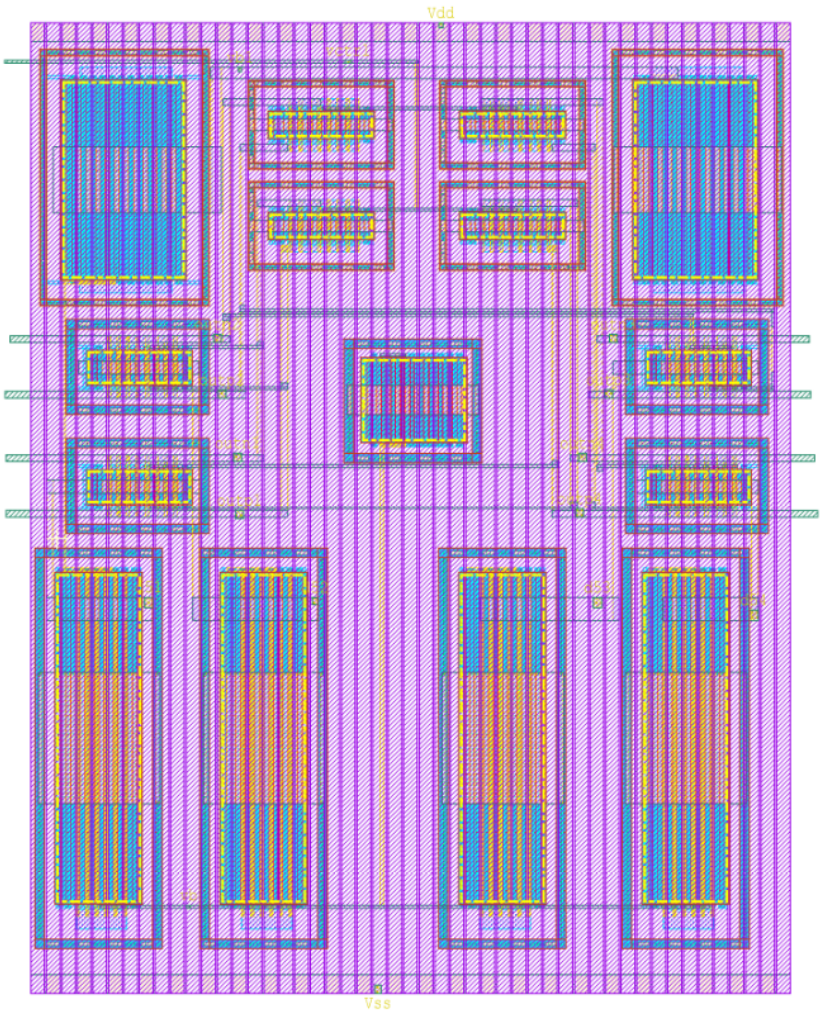


Figure 17. Complete layout of the VCO based on four CMOS differential stages, implemented in Tanner from Mentor graphics using UMC technology of 180 nm.

The post-layout oscillation frequencies are between $f_{osc} = 4.72$ GHz and $f_{osc} = 1.84$ GHz, for control voltages between -0.9 V and -0.2 V. Figure 18 shows the comparison between the pre- and post-layouts of the VCO based on four CMOS differential stages. An amplified view of the post-layout output signals for control voltages of -0.9 V and -0.2 V is shown in Figure 19. The average power consumptions of both cases is 42 mW.

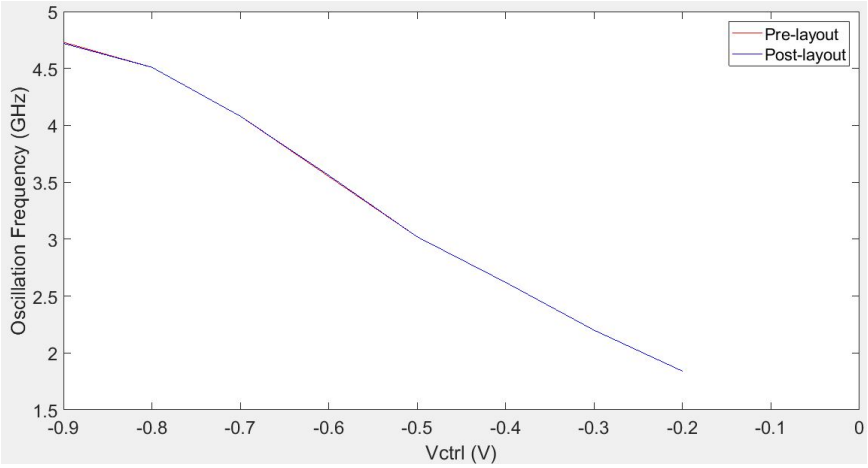


Figure 18. Comparison of the oscillation frequency vs. control voltage for the pre- and post-layout simulations of the VCO.

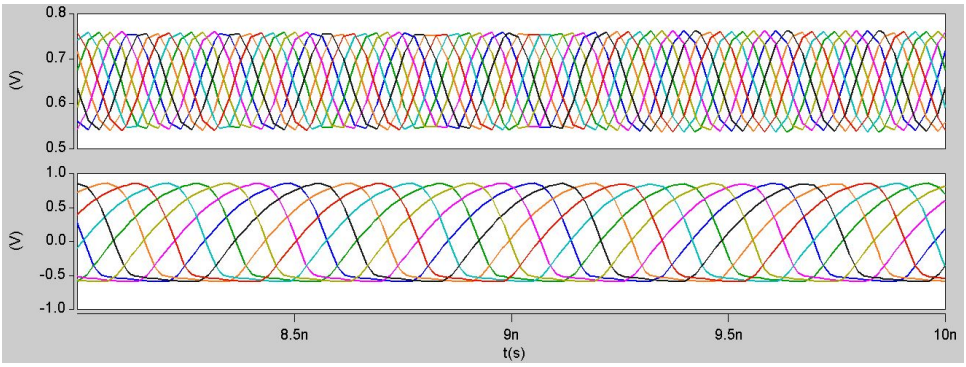


Figure 19. Post-layout output waveforms of the VCO for $V_{ctrl} = -0.9$ V (**top**) and $V_{ctrl} = -0.2$ V (**bottom**).

To measure the static supply sensitivity of the VCO, the change in the oscillation frequency due to a 10% supply voltage variation is measured [29], and the results are shown in Figure 20 for both the pre- and post-layout VCOs. The results show a static supply sensitivity of $0.54\%/1\%V_{supply}$ and $1.63\%/1\%V_{supply}$ for the VCO and the post-layout VCO, respectively.

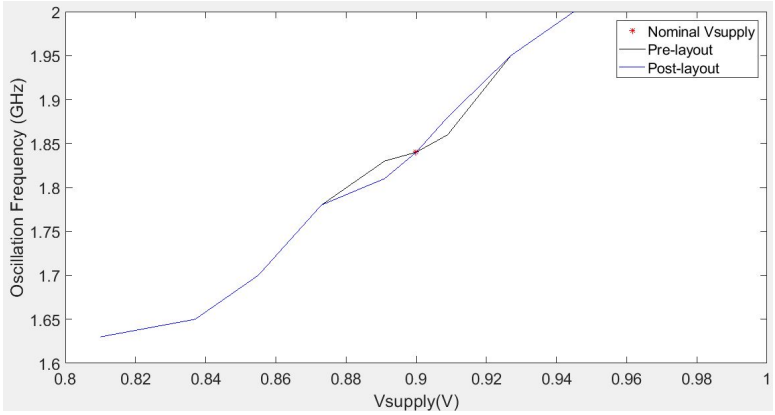


Figure 20. Frequency variations produced by the changes in the supply voltage of the VCO.

5. Conclusions

The design of a VCO based on four CMOS differential stages connected in a ring topology is presented. Analytical expressions were derived applying symbolic analysis to identify the requirements to extend the frequency of oscillation. As a result, the theoretical simulations provided a range of control-voltage between −0.2 V and −0.9 V, which corresponds to an oscillation frequency in the range between 2.65 GHz and 5.65 GHz. This range is wider compared to similar topologies reported in the literature. In addition, the post-layout simulation results verified that the design of the proposed VCO was successful. The VCO was modified to program the tails currents using four switches for a current range between 3 mA and 7.5 mA, which provided an oscillation frequency within the range from 1.38 GHz to 4.72 GHz. This range is very close to the one measured before layout, thus showing the suitability of the CMOS differential stage to be used in the design of a VCO.

Finally, as stated by Equation (1), the oscillation frequency is inversely proportional to the number of stages, so that a reduction of stages leads to a reduction in the gain, and augmenting the stages leads to a reduction in the frequency range. For instance, performing simulations using six CMOS differential stages instead of four, the frequency range of the VCO is reduced from 2.65–5.65 GHz to 1.81–3.7 GHz. That way, using four stages is a good number to increase the range of frequency and voltage-control.

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