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A Two-Module Linear Regulator with 3.9–10 V Input, 2.5 V Output, and 500 mA Load

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Abstract: A linear regulator with an input range of 3.9–10 V, 2.5 V output, and a maximal 500 mA load for use with battery systems was developed and presented here. The linear regulator featured two modules of a preregulator and a linear regulator core circuit, offering minimized power dissipation and high-level stability. The preregulator delivered an internal power voltage of 3 V and supplied internal circuits including the second module (the linear regulator core). The preregulator fitted with an active, low-pass filter provided a low-noise reference voltage to the linear regulator core circuit. To ensure operational stability for the linear regulator, error amplifiers incorporating the Miller compensation technique and featuring a large slewing rate were employed in the two modules. The circuit was successfully implemented in a 0.25 μm, 5 V complementary metal-oxide semiconductor (CMOS) process featuring 20 V drain-extended MOS (DMOS)/bipolar high-voltage devices. The total silicon area, including all pads, was approximately 1.67 mm^2. To reduce chip area, bipolar rather than DMOS transistors served as the power transistors. Measured results demonstrated that the designed linear regulator was able to operate at an input voltage ranging from 3.9 to 10 V and offer a maximum 500 mA load current with fixed 2.5 V output voltage.

Keywords: linear regulator; low noise; wide input range; high voltage (HV); high stability; large current load; bandgap; protection circuits

1. Introduction

Today, high-voltage (HV) battery-powered systems with wide input ranges play major roles in energy storage for portable/palm notebook computers, battery chargers, wireless communication equipment, and so on [1,2]. To ensure safety, long life, and reliable operation of lithium ion batteries, an integrated circuit (IC) is generally required to manage their charging and discharging process. An IC must feature a power management circuit converting a high input voltage to a stable low voltage that supplies other IC circuits. A power management circuit featuring a cascaded DC–DC converter and low-dropout regulator (LDO) with a high system power efficiency is typically termed as a voltage regulator; however, a DC–DC converter may create large voltage ripples and, thus, reduce output voltage accuracy [3,4]. Also, the design complexity of a DC–DC converter is much higher than that of a linear regulator. The use of a linear regulator for power management affords design simplicity, less silicon area, low cost, and no ripple [5–12].

Consequently, an HV linear regulator for power management implemented by an HV-LDO alone, even with a lower power efficiency, becomes attractive for constructing power management circuits used in high-accuracy output battery-powered systems. Generally, HV-LDO composed of high-voltage DMOS or bipolar transistors (BJTs) only has a significantly high power consumption and large silicon area [13–15]. Additionally, the linear regulator applied in HV battery-powered systems must be capable of bearing a high current load in a wide input voltage range. Although the HV-LDOs presented in [13–15] are able to operate in a wide input voltage range, they cannot afford a high current load.

Therefore, we designed a novel, two-module HV-linear regulator based on CMOS, DMOS, and bipolar transistors, which was able to operate in a wide input voltage range (3.9–10 V) and achieved a high load current (500 mA) with ensured stability under various conditions. The paper is organized as follows: Section 2 introduces the configuration of our HV linear regulator circuit, Section 3 describes the implementation thereof, Section 4 demonstrates the test results, and Section 5 contains conclusions.

2. Configuration of the Proposed HV Linear Regulator Circuit

Figure 1 shows the configuration of the proposed HV linear regulator, consisting of a bandgap reference, an over-temperature protection (OTP) circuit, an over-current protection (OCP) circuit, a preregulator, and a linear regulator core circuit. The preregulator and linear regulator core constitute two distinct modules. The preregulator converts a high input voltage to a stable low voltage (Vdd = 3 V) used for supplying most other circuits, as shown in Figure 1. High-voltage DMOS transistors were used as the power transistor in the preregulator and wherever high voltage existed in the circuit design. All other devices employed were either normal CMOS transistors, for the purposes of easier control, better matching, and lower quiescent current, or bipolar transistors in the output stage of the linear regulator for supporting high voltage and delivering a higher power with a smaller chip area. A high-precision bandgap reference was used to provide reference voltage for the preregulator circuit [16,17]. The OTP and OCP circuits can be used to safeguard regulator operation [18]. At an input voltage ranging from 3.9 to 10 V, the design adopted a 0. 25 µm 5 V CMOS process combined with 20 V DMOS/bipolar devices to implement the circuit. To avoid interference between the preregulator and the core linear regulator, the preregulator featured an active low-pass filter to provide a low-noise, high-precision reference voltage ($Vref1$) to the linear regulator core, as shown in Figure 1. The typical output voltage of the proposed HV linear regulator was 2.5 V.

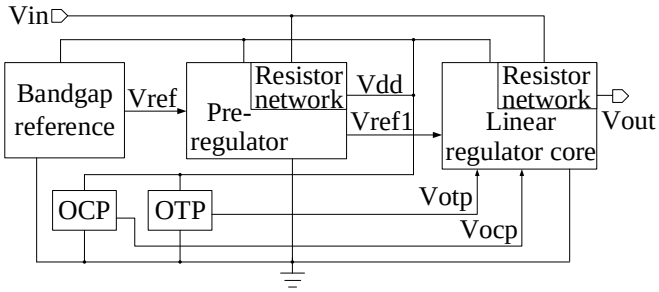


Figure 1. The configuration of the proposed design.

3. Implementation of the Proposed HV Linear Regulator

3.1. The Preregulator Featuring an Active Low-Pass Filter

Figure 2 shows the preregulator consisting of an error amplifier, a start-up circuit, a resistor network circuit, and the active, low-pass filter. The start-up and resistor network circuits that operate at high input voltages were implemented by DMOS transistors (DM1–DM5). The start-up circuit ensured that the preregulator attained the desired operating conditions. As shown in Figure 2, when *Vin* is applied with power supply, resistor *R1*, with proper resistance, forces node *Vout1* to increase with *Vin*.

Then, a current is generated in DM1, DM3, and *R3*, which ensures that other components quickly recover. Finally, a negative feedback loop consisting of the error amplifier, DM1–DM3, and *R2–R4* forces the preregulator to work in a stable condition. In addition, diode-connected transistors DM4 and DM5 were used to reduce fluctuation at node *Vout1*. With deliberately selected resistance for the resistor network circuit, a 3 V internal power voltage (*Vdd*) was obtained, and a low-noise, high-precision reference voltage (*Vref*1) for the linear regulator core was generated after the active filter. Given the high direct current (DC) gain of the error amplifier, *Vref*1 and *Vref* are ideally identical. The internal power supply voltage *Vdd* can be expressed as

$$Vdd \approx \frac{R2 + R4}{R4} * Vref + V_{GS,M1}, \tag{1}$$

where transistors M1 and M2 work in the subthreshold region, and the drain current I_D can be expressed by [19]

$$I_D \approx \frac{W}{L} I_0 exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \tag{2}$$

where $I_0 = \mu C_{ox}(\eta - 1)V_T^2$, and μ, V_{TH}, V_T, η, and C_{ox} represent the carrier mobility, the threshold voltage of the transistor, the thermal voltage, the subthreshold slope factor, and the gate-oxide capacitance, respectively. *W* and *L* are width and length of the transistor, respectively. The value of the resistor R_{eq} in M2 is dictated by the current flowing in transistor M2 ($I_{D,M2}$) and the drain-source voltage thereof (*Vref*1 − *Vfb*), as follows:

$$R_{eq} = \frac{Vref1 - Vfb}{I_{D,M2}} - R5. \tag{3}$$

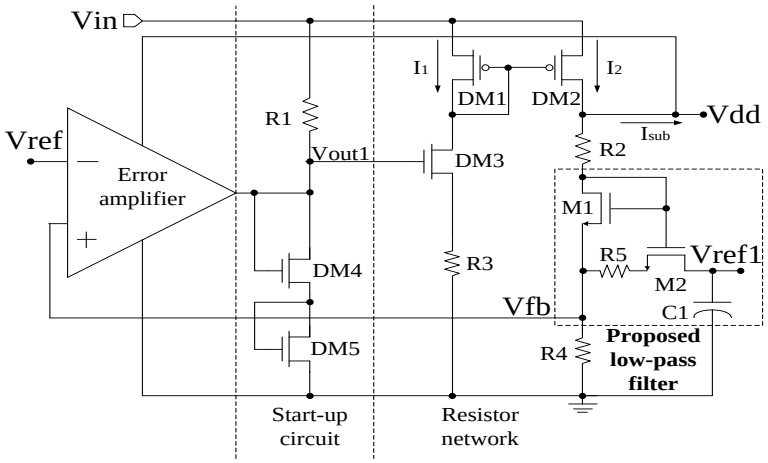


Figure 2. Preregulator with an active low-pass filter.

Thus, an active RC low-pass filter implemented using a mirror circuit (NMOS transistors M1 and M2) is included, as shown in Figure 2. It can effectively reduce noise with significantly reduced chip area when compared to a real resistive polyresistor with similar resistance, and the cut-off frequency f_c of the active RC low-pass filter is

$$f_c = \frac{1}{2\pi R_{out,f} C1} = \frac{1}{2\pi\left(R_{out1} + R5 + R_{eq}\right)C1}, \tag{4}$$

where R_{out1} is the output resistance viewed at point *Vfb*. Therefore, the final output reference voltage *Vref*1(f) is:

$$Vref1(f) = \frac{Vref1(0)}{1 + j\frac{f}{fc}}, \tag{5}$$

where *Vref*1(0) is approximately equal to *Vfb*. To ensure an appropriate cut-off frequency, the equivalent resistance of R_{eq} is controlled by a simple mirror circuit consisting of NMOS transistors M1 and M2, as shown in Figure 2. Given the M2:M1 (width/length) ratio of 1:4000, the M2 current (I_D) is low. In other words, high-frequency noise is well filtered from the output reference voltage. Table 1 lists the size of components used in the preregulator, and the simulated spectral density of noise at the output reference node (*Vref*1) versus frequency is shown in Figure 3, where an approximately 625 nV/ $\sqrt{\text{Hz}}$ of noise density at 100 Hz is obtained.

Table 1. Component sizes of the preregulator.

Components	Value	Components	Value
DM1(*W*/*L*)	40 µm/0.4 µm	M1(*W*/*L*)	200 µm/0.5 µm
DM2(*W*/*L*)	600 µm/0.4 µm	M2(*W*/*L*)	1 µm/10 µm
DM3 (*W*/*L*)	20 µm/0.45 µm	*C1* (pF)	5.3
DM4, DM5(*W*/*L*)	20 µm/5 µm	*R1*/*R2*/*R3*/*R4*/*R5* (kΩ)	1800/320/1/400/75

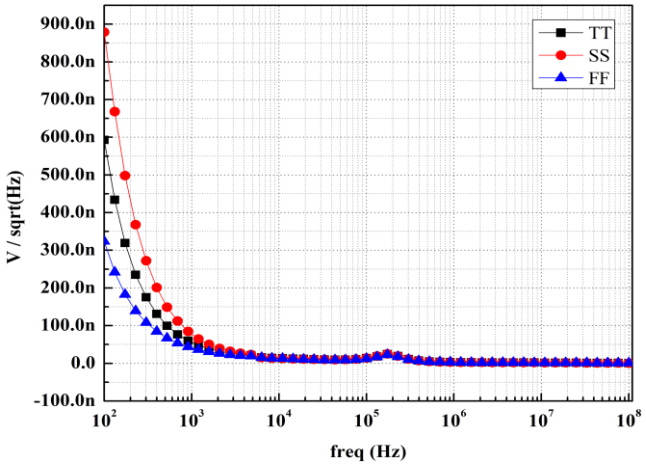


Figure 3. Simulated noise of *Vref*1 versus increasing frequency.

As shown in Figure 2, drain currents I_1 I_1 and I_2 I_2 flow through DM1 and DM2, respectively, and I_{sub} I_{sub} is the supply current for other subsequent circuits. So $(I_2 - I_{\text{sub}})$ $(I_2 - I_{sub})$ is the current flowing through network resistors (*R2*, *R5*, and *R4*). Since DM1 and DM2 are matched in a current mirror, and $I_2 \approx (W/L)_{DM2}/(W/L)_{DM1} I_1$ $I_2 \approx (W/L)_{DM2}/(W/L)_{DM1} I_1$, the total current consumption of the resistor network can, therefore, be calculated as $(I_1 + I_2 - I_{\text{sub}})$ $(I_1 + I_2 - I_{sub})$.

3.2. The Core Linear Regulator

Figure 4 shows the linear regulator core circuit featuring an error amplifier and a feedback resistor network circuit. The low-noise reference voltage *Vref*1 is provided by the preregulator described in the previous section. R_{load} is the load resistor, and a 22 μF off-chip capacitor with an equivalent series resistance (ESR) of 10 mΩ was used to ensure linear regulator core stability and to reduce over-under-shoot voltage. *R4* and *R5* form the feedback resistor network, and DMOS transistors (DM1–DM3) constitute the driver to provide the base current for the power transistor Q1. Supplied by the preregulator, the error amplifier with PMOS/NMOS-input pairs and an output push–pull stage

significantly improved the transient response speed of the linear regulator core. As shown in Figure 4, the tail current (M6) in the NMOS differential–input pair was biased by the current–mirror transistor M4 of the PMOS differential–input pair; this improved the speed of the linear regulator core as well. For supplying a maximum load current of 500 mA, a power DMOS transistor would require a significantly large area of silicon. Thus, we used a smaller-sized and high-voltage NPN bipolar transistor Q1 as the power transistor, which enhanced the driving ability of the linear regulator and improved areal efficiency. The width/length ratio k between DM2 and DM1 was set to 400 to ensure efficient driving of power transistor Q1 in this study. Table 2 lists the sizes of the main components of the linear regulator core.

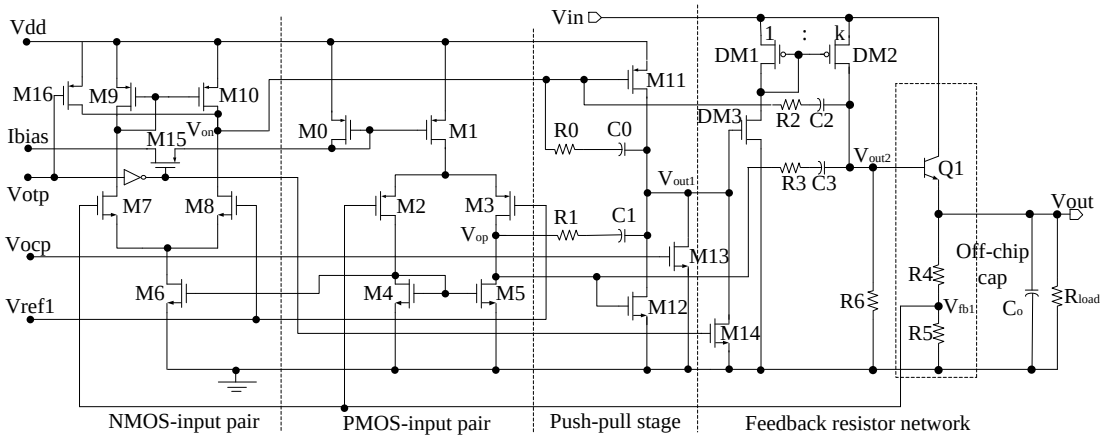


Figure 4. Implementation of the linear regulator core circuit.

Table 2. Main component sizes of the linear regulator core circuit.

Components	*C0,1/R2,3* (pF)	*R0,1/R2,3* (kΩ)	DM1 (Width/Length)	*k*	DM3 (Width/Length)	Q1 (Number)
Value	1.3/3.0	45/22.5	40 µm/800 nm	400	400 µm/450 nm	984 (5 µm × 5 µm)

To ensure the stability of the linear regulator core circuit, we used the Miller compensation technique in the design. As can be seen from Figure 4, $C0 - C3$ and $R0 - R3$ are Miller capacitors and resistors, respectively. Figure 5a is a small-signal model of the linear regulator core. Both the PMOS and NMOS input pairs could be taken as separate, single-stage operational amplifiers and, thus, exhibited single dominant poles at output nodes V_{op} and V_{on}, respectively. R_{op} and R_{on} are the equivalent output resistances of the PMOS and NMOS input pairs, respectively. C_{op} and C_{on} are the equivalent output parasitic capacitances of the PMOS and NMOS input pairs, respectively. C_{op} was derived principally from the C_{GS} of M12, whereas C_{on} was attributable mainly to the C_{GS} of M11. Given the small sizes of transistors M11 and M12, C_{op} and C_{on} had minimal capacitances. G_{mp} and G_{mn} are the transconductances of PMOS and NMOS input pairs, respectively, where $G_{mp} = g_{mp2,3}$ and $G_{mn} = g_{mn7,8}$ [16]. $g_{mp2,3}$ is the transconductance of M2 and M3 (assuming that M2 and M3 are matched), and $g_{mn7,8}$ is the transconductance of M7 and M8 (assuming that M7 and M8 are matched), as shown in Figure 4. At an appropriate bias current, correct sizes of the PMOS and NMOS input pairs ensured that g_{mp} and g_{mn} were equivalent: $G_{mp,n} = g_{mp,n} = g_{mp2,3} = g_{mn7,8}$. C_{p1} is the parasitic capacitance of the push–pull stage output, attributable principally to C_{GS} of DM3.

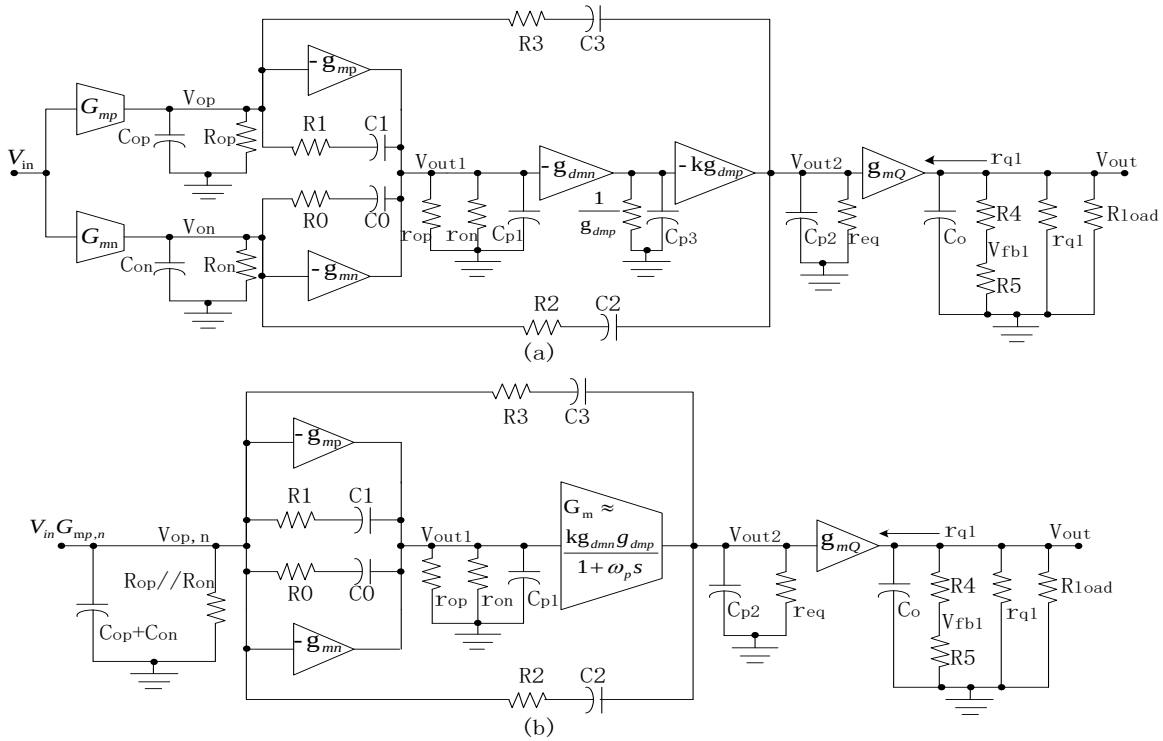


Figure 5. (**a**) Small-signal model of the proposed linear regulator core; (**b**) simplified small-signal model.

As the DMOS transistor DM3 (width = 400 µm, length = 450 nm) was large, the capacitance of C_{p1} was greater than that of both C_{op} and C_{on}. The transconductances of M11 and M12 are g_{mp} and g_{mn}, respectively. g_{dmn} is the transconductance of DM3, whereas DM2 and DM1 generate a transconductance of kg_{dmp} due to their width/length ratio of k. $1/g_{dmp}$ and C_{p3} are the equivalent output resistance and the parasitic capacitance of the mirror node between DM1 and DM2, respectively. Therefore, the DM1–DM3 combination could be considered to exhibit a large $G_m = kg_{dmn}g_{dmp}/\left(1+\omega_p\right)$, as shown in the simplified small-signal model of Figure 5b. The frequency of ω_p was high given its low resistance ($1/g_{dmp}$) and capacitance (C_{p3}); thus, it did not affect the loop stability of the linear regulator core. g_{mQ} is the transconductance of Q1; r_{q1} is the equivalent output resistance viewed at the emitter node of Q1; C_o is the off-chip capacitor; and R_{load} is the load resistor. As shown in Figure 5, V_{op} and V_{on} of Figure 5a can be merged into the single node $V_{op,n}$ of Figure 5b, where $R_{op}//R_{on}$ and $C_{op}+C_{on}$ are the lumped resistance and capacitance. Thus, the DC gain of the core linear regulator is:

$$A_v \approx \left[G_{mp,n}R_{op}//R_{on}\right]\times\left[g_{mp,n}\left(r_{op}//r_{on}\right)\right]\times\left(G_m r_{eq}\right)\times\left(g_{mQ}R_{out}\right), \tag{6}$$

where the equivalent output resistor $R_{out} = r_{q1}//R_{load}//(\mathrm{R4}-R5)$ Obviously, four principal poles were produced at nodes $V_{op,n}$ (ω_{p1}), V_{out1} (ω_{p4}), V_{out2} (ω_{p3}), and V_{out} (ω_{p2}) of the stability loop. Miller capacitors C0 and C1 with identical capacitances (C0, 1) split the poles between nodes V_{out1} and $V_{op,n}$; the two poles can be expressed as [16]

$$\begin{aligned}\omega_{pM1} &\approx \frac{1}{\left(1/g_{mp,n}\right)\left[C_{p1}+\mathrm{C0},1\right]},\\ \omega_{pM2} &= \frac{1}{\left(R_{op}//R_{on}\right)\mathrm{C0},1\,g_{mp,n}\left[r_{op}//r_{on}\right]}.\end{aligned} \tag{7}$$

Similarly, Miller capacitors $C2$ and $C3$ with identical capacitances $C2,3$ split the poles between nodes V_{out2} and $V_{op,n}$; the two poles can be expressed as [16]

$$\begin{aligned} \omega_{pM3} &\approx \frac{1}{\left(1/g_{mQ}\right)\left[C_{p2}+C2,3\right]}, \\ \omega_{pM4} &\approx \frac{1}{\left(R_{op}//R_{on}\right)C2,3g_{mp,n}\left[r_{op}//r_{on}\right]G_m r_{eq}}. \end{aligned} \tag{8}$$

A low-frequency pole developed at node $V_{op,n}$ given the chosen Miller compensation; this is the dominant pole ω_{p1} of the stability loop, expressed as:

$$\omega_{p1} \approx \frac{1}{c_{outp,n}r_{outp,n}}, \tag{9}$$

where the equivalent capacitor $c_{outp,n}$ and the resistor $r_{outp,n}$ at node $V_{op,n}$ can be expressed as:

$$c_{outp,n} \approx C0,1g_{mp,n}\left(r_{op}//r_{on}\right)+C2,3g_{mp,n}\left(r_{op}//r_{on}\right)G_m r_{eq}, \tag{10}$$

$$r_{outp,n} \approx R_{op}//R_{on}. \tag{11}$$

The equivalent capacitor $c_{outp,n}$ was amplified by the inter amplifiers of the stability loop. As transistor DM3 had a smaller parasitic capacitor than that of power transistor Q1, the pole at node V_{out1} was of higher frequency than the pole at node V_{out2} ($\omega_{p4} = \omega_{pM2} > \omega_{p3} = \omega_{pM3}$). As the off-chip capacitor C_o had a capacitance of 22 μF, a second dominant pole was generated at output node V_{out}, given by

$$\omega_{p2} \approx \frac{1}{c_o R_{out}} \approx \frac{1}{c_o\left[r_{q1}//R_{load}//(\mathrm{R4}+R5)\right]}. \tag{12}$$

Thus, the four poles may be ordered as $\omega_{p4} > \omega_{p3} > \omega_{p2} > \omega_{p1}$. Also, two left half-plane (LHP) zeros, ω_{z1} and ω_{z2}, featuring appropriate resistors and capacitors, were used to compensate for phase shifts caused by the poles of the stability loop [16].

The external ESR and output off-chip capacitor (C_o) generated a third LHP zero to compensate for the negative phase shift caused by the low-frequency nondominant pole [20]. Consequently, four poles and three LHP zeros were generated in the loop of the linear regulator core. Appropriate sizing of the compensation resistors and capacitors ensured that the linear regulator core was stable in various operating conditions.

Figure 6 shows the simulated loop response results at different current loads (0, 10, 100, 250, and 500 mA) under different input supply voltages (3.9 and 10 V). As the current load changes, the output equivalent resistor values vary, slightly affecting the DC gain of the linear regulator core loop. Figure 7 shows the simulated phase margins (PMs) and unity gain frequencies versus load current under various conditions of different input voltages (3.9 and 10 V), process corners (TT, SS, and FF), and temperatures (−40 to 85 °C). It is clearly seen that the PMs were over 30° in all simulated cases. In most cases, the PMs were over 50°, ensuring linear regulator core stability over large input voltage and current load ranges.

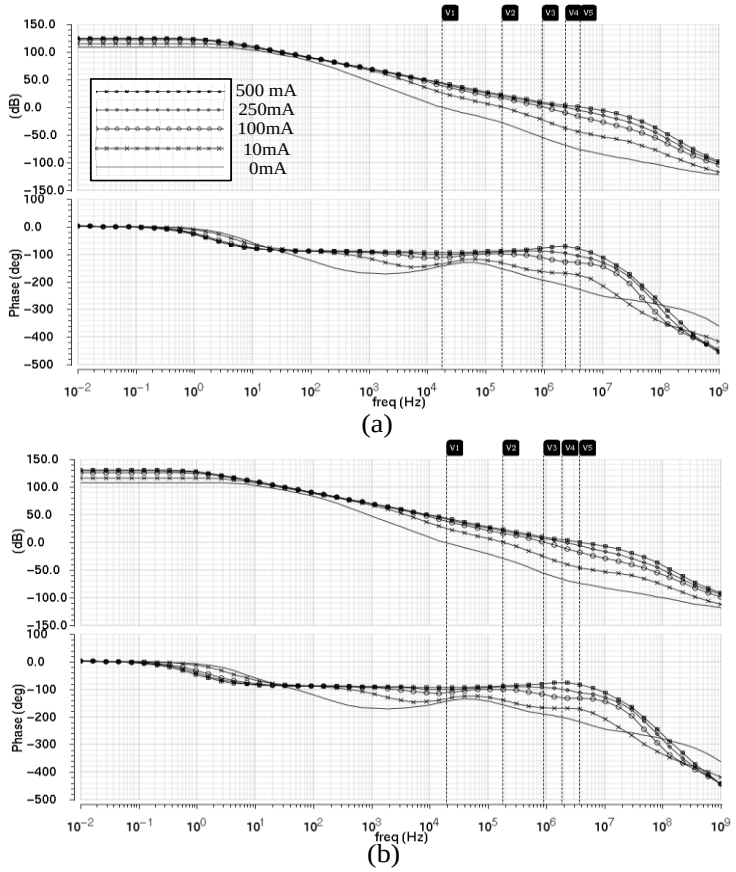
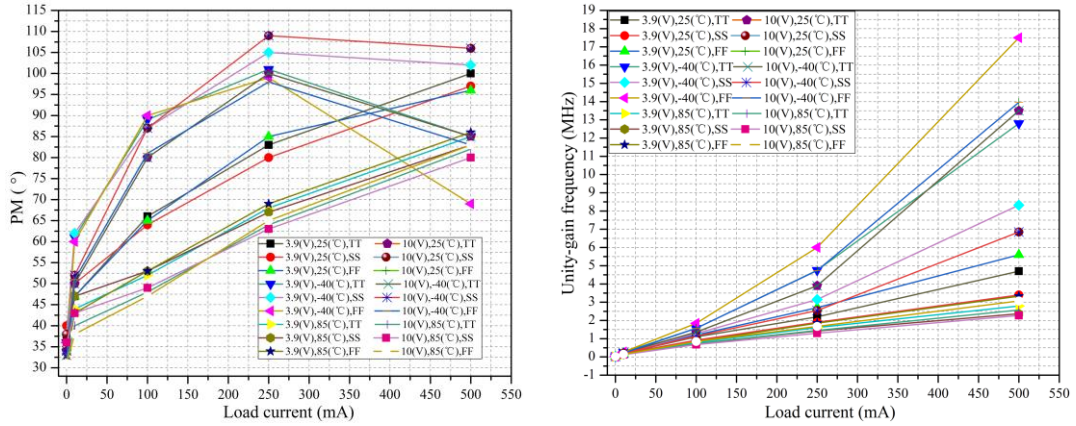


Figure 6. Simulated loop response results of the linear regulator core with different current loads; (**a**) supply voltage of 3.9 V; (**b**) supply voltage of 10 V.



(**a**) (**b**)

Figure 7. The simulated phase margins (PMs) and unity gain frequency with different cases; (**a**) PMs; (**b**) unity gain frequency.

3.3. Bandgap and Protection Circuits

Figure 8a shows the bandgap core circuit in this study, which provided reference voltages and bias currents for other subsequent circuits. The operational amplifier forced nodes *Vp* and *Vn* on virtual ground, and the resistor *R4* and the capacitor *C1* formed a low-pass filter for the output reference voltage. The output reference voltage $Vref \approx ln(N)\Delta V_{BE}R1, 3/R2 + V_{BE}$, where $R1,3 = R1 = R3$, and *Vref* has a low-temperature coefficient (TC). The simulated temperature coefficient (TC) of the

bandgap reference voltage is shown in Figure 8b, where an approximate 3.4 ppm/°C TC under different CMOS processes over temperatures ranging from −40 to 85 °C was achieved.

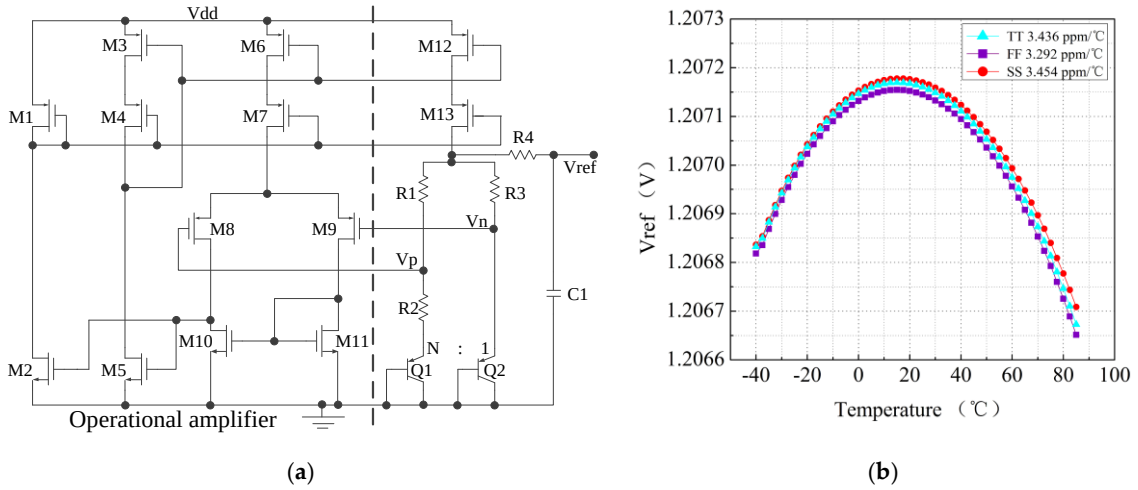


Figure 8. (**a**) Bandgap core circuit; (**b**) simulated temperature coefficient of *Vref*.

Figure 9 shows protection circuits including an OCP circuit and an OTP circuit. As shown in Figure 9a, *Vref* was provided by the bandgap circuit, the operational amplifier (OP) with *R1*, and M1–M3 produced a low TC bias current for M4. Transistors M4–M7 with the same sizes were in current mirror. DMOS transistors DM1–DM3 were used to avoid damage to transistors M5–M7, due to the high supply voltage *Vin*. Bipolar transistor Q0 mirrored with Q1 was adopted to sense the load current, where Q1 with *R4* and *R5* was a part of linear regulator core, and the ratio of Q0 and Q1 was 1/984. When the load current was too high (in an over-current condition), the mirrored current flowing Q0 generated a larger voltage difference on *R6*. In this case, the drain current in DM5 will be smaller than the drain current in DM4, so that M7 with the same size of M6 is forced to work in the linear region. In other words, an over-current signal *Vocp* was generated, and it was used to lower the base current for both Q0 and Q1, leading to a reduced output current and, thus, over-current protection.

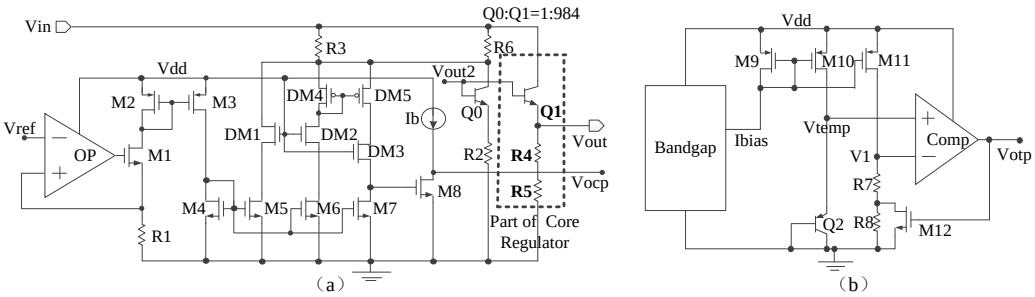


Figure 9. Protection circuits; (**a**) over-current protection (OCP) circuit; (**b**) over-temperature protection (OTP) circuit.

Figure 9b presents the OTP circuit, where the bias current *Ibias* is provided by the bandgap circuit. The base-emitter voltage of Q2 ($V_{BE,Q2} = V_{temp}$) was applied to the positive input node of the comparator (Comp), while a reference voltage *V1* generated by M11, *R7*, and *R8* was applied to the negative input node of the comparator. By selecting a proper *V1*, the comparator can keep a high output (*Votp*) in a wide temperature range. As the base-emitter voltage of Q2 (V_{temp}) decreased versus an increasing temperature, V_{temp} became lower than *V1* at a high temperature "T1", which was the critical temperature. The comparator produced a low-output *Votp*, which turned off the switch M12, and a higher voltage *V1* was generated. The linear regulator core circuit will be shut down by the signal of *Votp*. Until the temperature drops to a certain value "T2", a high *Votp* enables the linear regulator

core again. "T1−T2" is the temperature window, which can be well defined by selecting proper M11, *R7*, and *R8*. The temperature window can effectively avoid a constantly changing condition near the critical temperature.

4. Measurements

Figure 10 shows the layout of the linear regulator circuit fabricated via a standard 0.25 µm CMOS process with 20 V DMOS and bipolar devices. The CMOS transistors operated at a supply voltage of 5 V, and the DMOS devices could correctly work at a maximum drain-source voltage of 20 V. The total chip area including the BGR, OCP, and OTP circuits (and all pads) was approximately 1.67 mm^2 (1140 × 1485 µm). To minimize process mismatching, we used the common-centroid technique to layout the active MOS and bipolar transistors of the bandgap circuit. Additionally, we added dummy transistors to improve matching. As the load current was large, two pads were employed for the connection of Q1 to the output to reduce the parasitic resistance in the current paths.

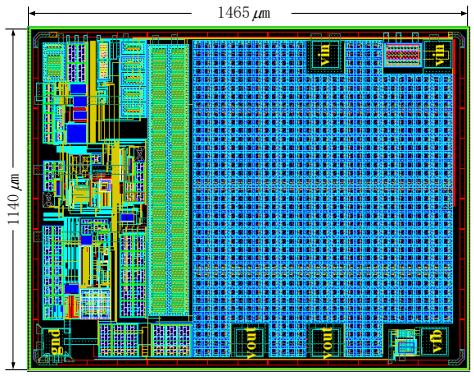
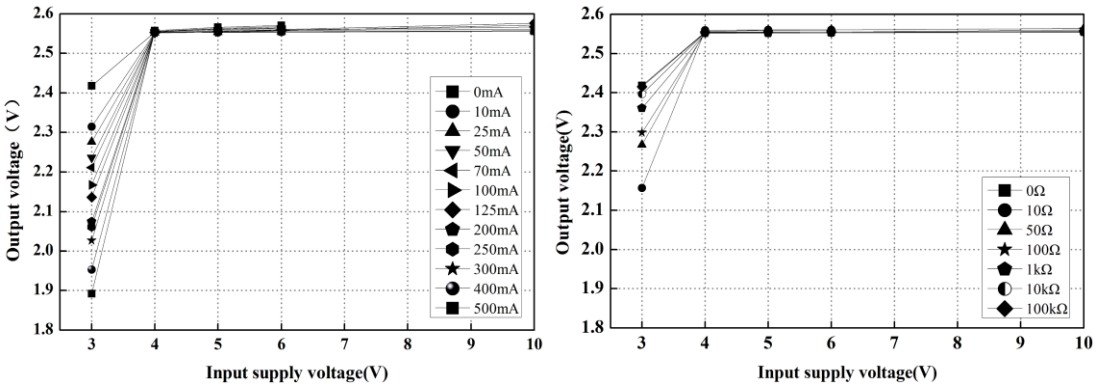


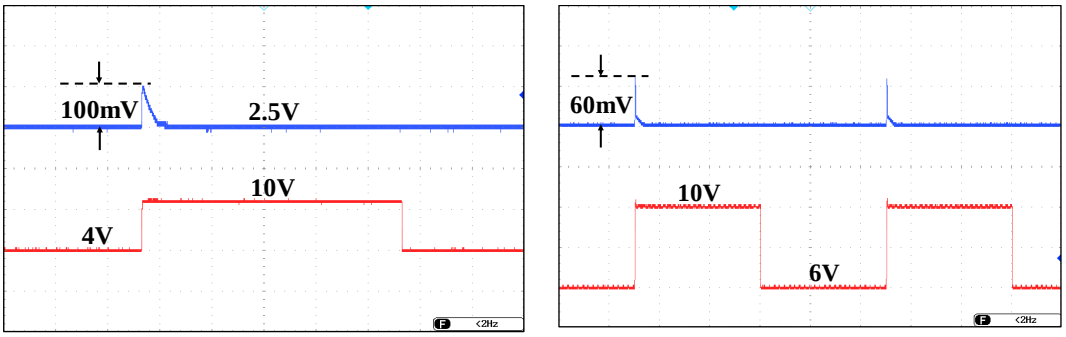
Figure 10. Layout of the proposed regulator with pads.

Figure 11 shows the measured output voltages as the input supply voltage increased under different loads. Figure 11a shows the output voltages at different current loads (0–500 mA), and Figure 11b shows the output voltages at different resistance loads (0–100 kΩ). The regulator operated well as the supply voltage varied from 3.9 to 10 V with a fixed output voltage of 2.5 V. Figure 12 shows the line transient performance; Figure 12a shows that the output voltage was 2.5 V under a load current of 10 mA and an input supply voltage ranging from 4 to 10 V. Figure 12b shows the results with a load current of 50 mA and an input supply voltage ranging from 6 to 10 V. In two cases, overshoot voltages were 100 and 60 mV, respectively.



(**a**) (**b**)

Figure 11. Measured output voltage versus input supply voltage (**a**) with different current loads and (**b**) with different resistance loads.



(**a**) (**b**)

Figure 12. Measured transient line performance of the proposed linear regulator. (**a**) load current is 10 mA; (**b**) load current is 50 mA.

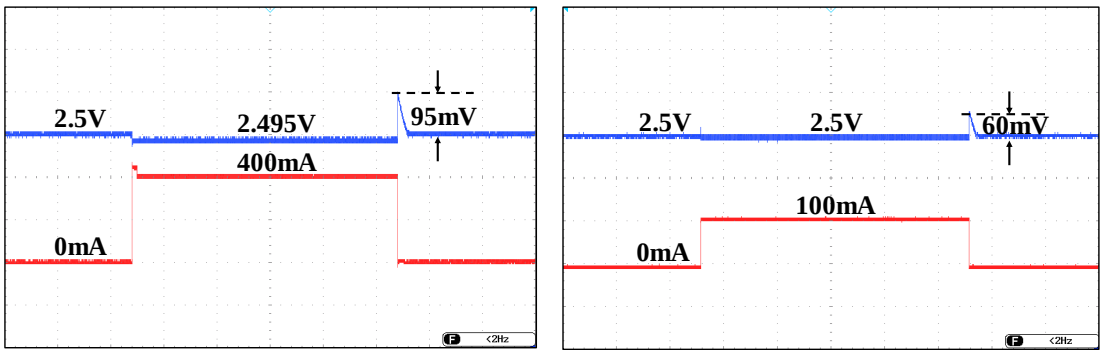
Figure 13 shows the transient load performance of the output voltage. Figure 13a demonstrates the measured results under transient loads from 0 to 400 mA, and Figure 13b presents the results under transient loads from 0 to 100 mA at a supply voltage of 4 V. Figure 14 gives further details on transient load performance. Figure 14a shows the results as the transient load changed from 0 to 450 mA, and Figure 14b shows the results as the transient load varied from 0 to 200 mA at a supply voltage of 6 V. A figure of merit FOM^1 was adopted to compare the transient response of different regulators, and it is defined as [6]

$$FOM^1 = C_L \frac{\Delta Vout}{I_{L,max}} \times \frac{I_q}{I_{L,max}}, \tag{13}$$

where C_L is the load capacitor, $\Delta Vout$ is the maximum transient output-voltage variation, I_q is the quiescent current, and $I_{L,max}$ is the maximum load current. Considering the transient response induced by input supply voltage variation, a new figure of merit (FOM^2) was defined to express the performance of different regulators, and it is given by

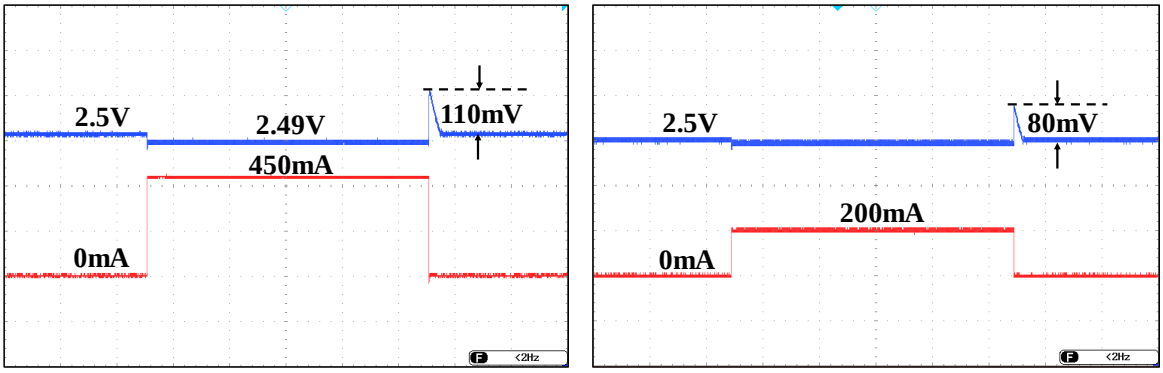
$$FOM^2 = FOM^1 \times LineR, \tag{14}$$

where $LineR$ is line regulation [21]. Table 3 summarizes the performance of the proposed regulator; the results were compared to those of other studies. At a quiescent current of 350 μA and a supply voltage of 3.9 to 10 V, our proposed linear regulator including bandgap and protection circuits delivered a maximum current of 500 mA. The proposed linear regulator without voltage ripples achieved competitive load regulation, line regulation, current efficiency, FOM^1, and FOM^2.



(**a**) (**b**)

Figure 13. Measured transient load performance of the proposed linear regulator with supply voltage of 4 V. (**a**) Load current step is from 0 to 400 mA; (**b**) load current step is from 0 to 100 mA.



(**a**) (**b**)

Figure 14. Measured load transient performance of the proposed linear regulator with supply voltage of 6 V. (**a**) Load current step is from 0 to 450 mA; (**b**) load current step is from 0 to 200 mA.

Table 3. Performance summary and comparisons of other studies.

Research.	Ref. [3]	Ref. [6]	Ref. [12]	Ref. [13]	Ref. [15]	Ref. [22]	This Work
Input voltage range Vin (V)	6–18	1.4–1.8	1.8–2.2	4–40	3.5–24	1.2–1.8	3.9–10
Typical output voltage Vout (V)	1.8–3.3	1.2	1.6	2.5–5	3	1.0	2.5
Dropout voltage (mV)	-	200	200	>200	>200	200	>200
Quiescent current (μA)	-	1.6–200	71–101	8	3.7	135.1	350 (Including BGR, OCP and OTP)
Load Regulation (mV/mA)	-	0.1	-	5.3	0.067	0.075	0.0328 @ (0-450 mA)
Line Regulation (mV/V)	-	5.5	131	10	0.88 @ 5 V	22.7	0.2 @ (5–10 V)
Max. load current (mA)	450	50	100	30	150	100	500
Current Efficiency (%)	-	99.6	99.9	99.9	99.9	99.8	99.9
FOM^1 (ns)	-	1.92	0.21	0.182	0.592	0.439	3.388
FOM^2 (ns)	-	10.56	27.51	1.82	0.521	0.935	0.6776
Topology	DC–DC converter+LDO	LDO	LDO	HV-LDO	HV-LDO	LDO	Two-module linear regulator
System ripple	10 mV	no	no	no	no	no	no
Technology	0.35 μm HV CMOS	0.18 μm CMOS	0.18 μm CMOS	0.6 μm CMOS with DMOS device	0.35 μm Bi-CMOS	0.18 μm CMOS	0.25 μm CMOS with DMOS device
Chip area (mm^2)	6.4 (including BGR and pads)	0.0285	0.033	0.3 (including pads)	0.7912 (including BGR pads)	0.024	1.67 (including pads, BGR, OCP and OTP)

CMOS—complementary metal-oxide semiconductor; FOM—figure of merit; HV-LDO—high-voltage, low-dropout regulator.

5. Conclusions

We designed a linear regulator for battery systems; the input voltage ranged from 3.9 to 10 V, and the maximum load current was 500 mA. The regulator featured a preregulator and a linear regulator core for minimizing power dissipation and maximizing operation stability. The error amplifiers with the Miller compensation technique were adopted to ensure the stability of both the preregulator and the linear regulator core circuit. The circuit was implemented in a 0.25 μm 5 V CMOS process with 20 V DMOS devices, and the total silicon area was 1.67 mm^2. The linear regulator was able to afford a stable output voltage of 2.5 V under a maximum load current of 500 mA over a supply voltage range

of 3.9–10 V. Measurements showed that a load regulation of 0.0328 mV/mA and a line regulation of 0.2 mV/V were obtained. FOM^1 and FOM^2 were 3.388 and 0.6776 ns, respectively.

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