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# A PVT-Robust Super-Regenerative Receiver with Background Frequency Calibration and Concurrent Quenching Waveform

Yadong Yin <sup>1,\*</sup>, Ximing Fu <sup>2</sup> and Kamal El-Sankary <sup>2</sup>

<sup>1</sup> School of Physics and Information Engineering, Fuzhou University, Fuzhou 350002, Fujian, China; yinyadong@fzu.edu.cn

<sup>2</sup> Department of Electrical and Computer Engineering, Dalhousie University, Halifax B3H 4R2, Canada; xm954365@dal.ca (X.F.); kamal.el-sankary@dal.ca (K.E.-S.)

\* Correspondence: yinyadong@fzu.edu.cn; Tel.: +86-591-2286-5132

Received: 26 August 2019; Accepted: 30 September 2019; Published: 4 October 2019

**Abstract:** A process-voltage-temperature (PVT)-robust, low power, low noise, and high sensitivity, super-regenerative (SR) receiver is proposed in this paper. To enable high sensitivity and robust-PVT operation, a fast locking phase-locked-loop (PLL) with initial random phase error reduction is proposed to continuously adjust the center frequency deviations of the SR oscillator (SRO) without interrupting the input data stream. Additionally, a concurrent quenching waveform (CQW) technique is devised to improve the SRO sensitivity and its noise performance. The proposed SRO architecture is controlled by two separate biasing branches to extend the sensitivity accumulation (SA) phase and reduce its noise during the SR phase, compared to the conventional optimal quenching waveform (OQW). The proposed SR receiver is implemented at 2.46 GHz center frequency in 180 nm SMIC CMOS technology and achieves better sensitivity, power consumption, noise performance, and PVT immunity compared with existent SR receiver architectures.

**Keywords:** concurrent quenching waveform (CQW); phase-locked loop (PLL); super regenerative oscillator (SRO); sensitivity

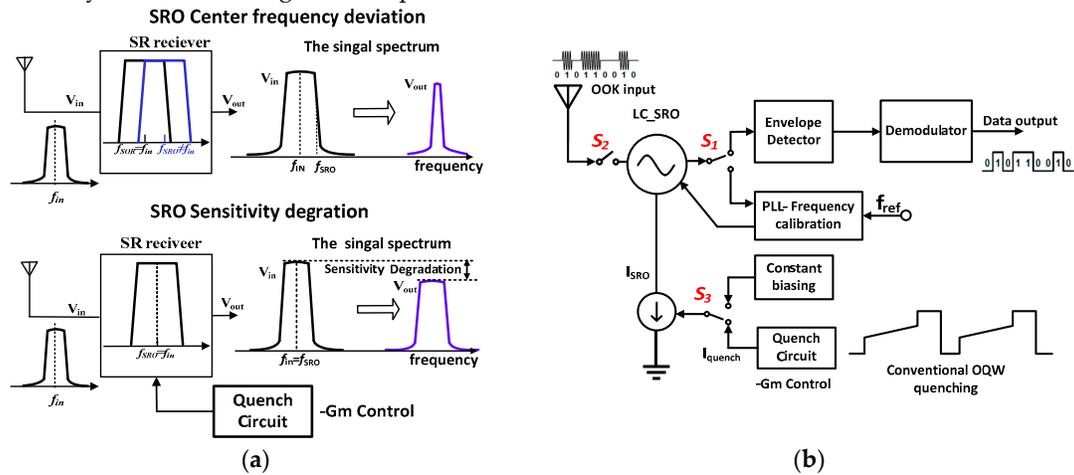
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## 1. Introduction

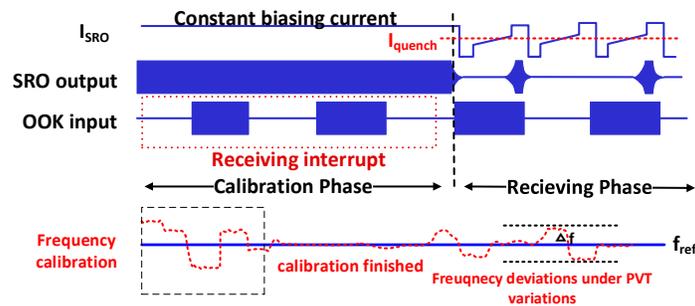
The low complexity and low power consumption characteristics make super-regenerative (SR) receivers, mainly composed of a LC-tank super regenerative oscillator (SRO), an envelope detector (ED), and a demodulator, a suitable alternative for short-range wireless communications. Unlike linear receivers which tend to be more robust to PVT variations [1,2], SR receivers are nonlinear and hence are inherently more prone to PVT variations. The in-band SRO gain is simultaneously affected by the frequency deviations between the carrier frequency of the input OOK signal and SRO's center frequency and the design of its quenching waveform as shown in Figure 1a. Any deviation in the center frequency or the shape of its quenching waveform will result in selectivity and sensitivity degradations. To achieve high performance under low power consumption, a frequency calibration circuit is required to adjust the SRO center frequency and an optimal quenching waveform (OQW) [3] is needed to optimize the SRO performance.

Recently, several frequency calibration techniques have been proposed for SR receivers using a phase-locked-loop (PLL) [4,5] or a counter-based frequency-locked-loop (FLL) [6] as shown in Figure 1b. Although these techniques can calibrate the SRO to the expected center frequency, they have to interrupt receiving of the input OOK data stream. For example, the frequency calibration loop in Reference [4] uses a charge-pump based PLL to compensate for the frequency deviations of

the SRO at start-up; however, it is not able to continuously track the frequency deviation under PVT variations. During normal operation while receiving the input data, any frequency deviation with respects to the SRO nominal center frequency  $f_{SRO}$  will cause degradation of the SRO performance (as illustrated in Figure 1a). Due to the initial phase error between the reference clock and SRO's feedback clock at the start of each calibration cycle, the conventional PLL or FLL-based methods need a considerable time exceeding the quenching cycle to overcome this initial phase error and that causes error in the frequency calibration (refer to Section 2.1.1). As a result, it is not feasible to use the conventional techniques to calibrate the SRO frequency in background (refer to Figure 2). In contrast, a novel initial phase error reduction is proposed in this paper to shorten the frequency detection time to less than the quenching cycle. That offers the proposed calibration the capability to continuously adjust the SRO center frequency in every quenching cycle to compensate for the SRO selectivity deviation during normal operation.



**Figure 1.** Challenges in the design of SRR: (a) SRO's selectivity and sensitivity under PVT (process-voltage-temperature) variations, and (b) the conventional frequency calibration for SR (super-regenerative) receiver with OQW (Concurrent Quenching Waveform).



**Figure 2.** The timing diagram of the conventional frequency calibration.

The sensitivity of the SR receiver is determined mainly by its quenching signal design. An optimal quenching waveform (OQW), shown in Figure 1b, was proposed in Reference [1] to optimize the sensitivity of the SRO. This quenching signal places the SRO into two regions, namely the sensitivity accumulation (SA) region and the super-regenerative (SR) region. In this paper, a concurrent quenching waveform (CQW) technique is presented to extend the SA region over the entire quenching period to allow maximum sensitivity accumulation and alleviate the requirement on the slope shape of the OQW under PVT variations. In addition, the proposed CQW reduces the SRO noise substantially and improves its signal-to-noise ratio (SNR) during the SR region.

This paper is organized as follows: Section 2 firstly presents the SRO theoretical background analysis and important design parameters, and then introduces the proposed background frequency calibration and concurrent quenching waveform techniques. Section 3 includes the simulation results. Section 4 concludes this paper.

## 2. Materials and Methods

### 2.1. SRO Theoretical Background Analysis

#### 2.1.1. PLL with Random Initial Phase Error

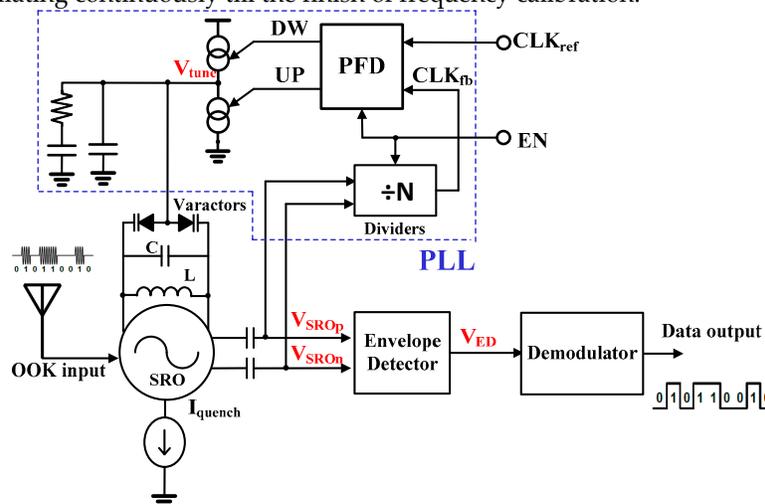
To improve the SR receiver selectivity, compensation of its center deviation is required. There are several methods currently used to calibrate the oscillating frequency of the SRO using PLL [4,5] and FLL [6]. However, all of them are infeasible to conduct background frequency calibration as the reason described below.

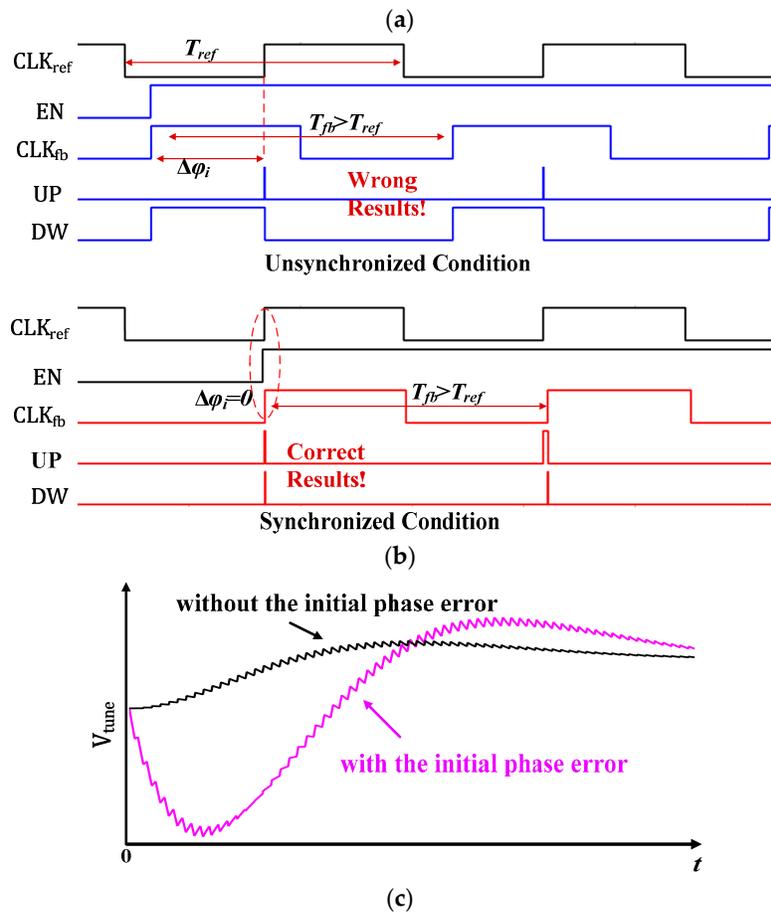
Figure 3a illustrates the schematic of the SR receiver with a conventional PLL-based frequency calibration. In contrast with the continuous operation of a normal PLL used for clock synchronization, a PLL used for SRO oscillating frequency calibration operates in intermittent mode. When the input enable signal EN is high, PLL is activated to detect the phase error between the reference clock  $CLK_{ref}$  and the feedback clock  $CLK_{fb}$ , and converts this phase error into the pulse width on the outputs UP and DW of the phase-frequency detector (PFD), and accordingly drive the charge pump to adjust the varactors' tuning voltage  $V_{tune}$  to tune the oscillating frequency of SRO  $f_{SRO}$  to be the desired one. When EN is low, the PLL must freeze its operation. Since  $CLK_{ref}$  and  $CLK_{fb}$  are unsynchronized when EN turns active, there exists a random phase error between  $CLK_{ref}$  and  $CLK_{fb}$  as shown in Figure 3b.

The phase difference between  $CLK_{ref}$  and  $CLK_{fb}$  can be expressed as follows:

$$\Delta\varphi = \int_0^{t_{PD}} (f_{ref} - f_{fb}) dt + \Delta\varphi_i \quad (1)$$

where  $f_{ref}$  and  $f_{fb}$  are the frequencies corresponding to  $CLK_{ref}$  and  $CLK_{fb}$  the reference clock and the PLL loop's feedback clock respectively,  $\Delta\varphi_i$  is the initial phase error between these two clocks at the start of the detection, and  $t_{PD}$  is the detecting time. As shown in Figure 3b, although the period of the reference clock  $T_{ref}$  is smaller than the feedback clock's period  $T_{fb}$ ,  $\Delta\varphi_i$  will result in incorrect values at the PFD's output signals on UP and DW, which causes increasing  $T_{fb}$  by PLL instead of decreasing it. That will increase substantially the PLL's settling time (as indicated by the settling time of  $V_{tune}$  in Figure 3c), therefore, it is hard for the conventional PLL-based calibration to adapt SRO's intermittent operation because the quenching cycle is too short for PLL to acquire correct phase error detection. As a consequence, the SR receiver has to interrupt its receiving process and keep SRO oscillating continuously till the finish of frequency calibration.

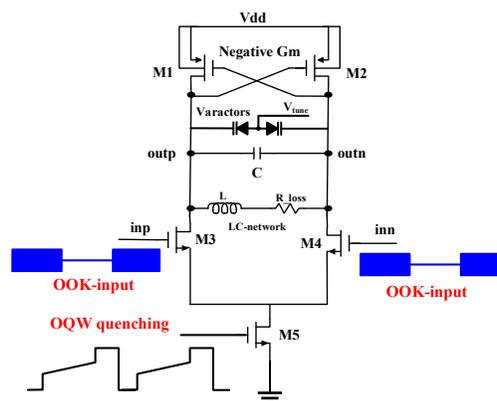




**Figure 3.** The challenges of conventional PLL-based frequency calibration: (a) the schematic of the SR receiver with the PLL-based calibration (b) the impacts of the unpredictable initial phase error on the phase error detection and (c) on the settling time of PLL.

### 2.1.2. Quenching Signal Analysis under PVT Variations

To optimize the sensitivity of the SRO, an optimal quenching waveform (OQW) is proposed in Reference [1] as shown in Figure 4. The OQW offers clearly better performance compares with conventional quenching waveforms such as square wave, sawtooth, and sinusoidal quenching. The OQW signal places the SRO into 2 regions, the sensitivity accumulation (SA) region and the super-regenerative (SR) region, to optimize the SRO sensitivity (Figure 5).



**Figure 4.** The conventional SRO architecture with OQW.

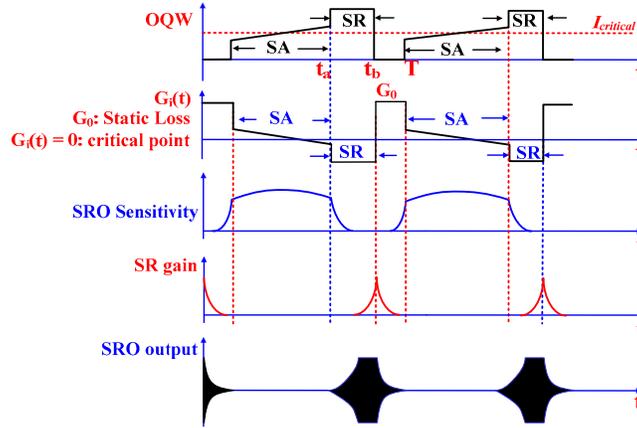


Figure 5. The timing diagram of the conventional SRO architecture with OQW.

According to Reference [1], the expression of the SRO voltage output can be written as:

$$V_{out}(t) = 2k_0\delta_0\omega_0 e^{-\omega_0 \int \delta(\tau) d\tau} * \int_0^t I_{in}'(t) e^{\omega_0 \int \delta(\tau) d\tau} \sin(\omega_0(t - \tau)) dt \quad (2)$$

where  $k_0, \delta_0, \omega_0$  represents the passive gain, quiescent damping factor, center frequency of the SRO respectively.  $\delta(t)$  is the dynamic damping factor for the entire system and  $I_{in}'(t)$  is the first derivative of the input current. The dynamic damping factor is given:

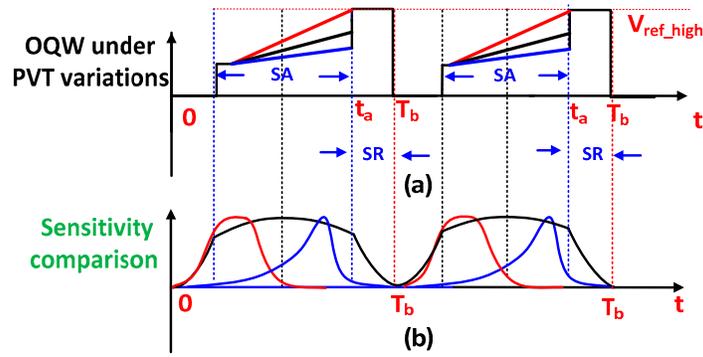
$$\delta(t) = \frac{G_0 - G_m(t)}{2\omega_0 C} \quad (3)$$

where  $G_0$  represents the SRO static loss,  $-G_m(t)$  is the transient value of the negative transconductance.  $C$  is the total capacitance of the LC-tank and  $G_i(t) = G_0 - G_m(t)$  represents the instantaneous transconductance due to the quenching controller. The sensitivity and SR gain functions extracted from Equation (2) are:

$$\text{Sensitivity:} \quad s(t) = e^{\omega_0 \int_0^{t_a} \delta(\tau) d\tau} \quad (4)$$

$$\text{SR gain:} \quad u(t) = e^{-\omega_0 \int_{t_a}^{t_b} \delta(\tau) d\tau} \quad (5)$$

As it is shown in the timing diagram of the OQW based SRO in Figure 5, the sensitivity reaches its maximum value when the SRO biasing current is equal to a critical current  $I_{critical}$  (equivalently when the instantaneous transconductance  $G_i(t) = 0$ ). However, once the oscillation starts to build up in the SR region, the SRO will not respond to the input signal because the sensitivity rapidly decays afterwards in the SR region (refer to Figure 5). Since the maximum sensitivity of the SRO is achieved only when the OQW crosses  $I_{critical}$  in the middle of SA region, any change in the OQW's slope due to PVT variations in the SA region will cause sensitivity degradation as shown in Figure 6. At the end of the SA region, the OQW is stepped up to a maximum value  $V_{ref\_high}$  to place the SRO in the SR region and regenerate the output signal. In the SR region, the SRO regenerative gain is dramatically reduced because the sensitivity decays to 0 (refer to Figure 6b), therefore, the input referred noise will dramatically increase which will degrade the SNR.

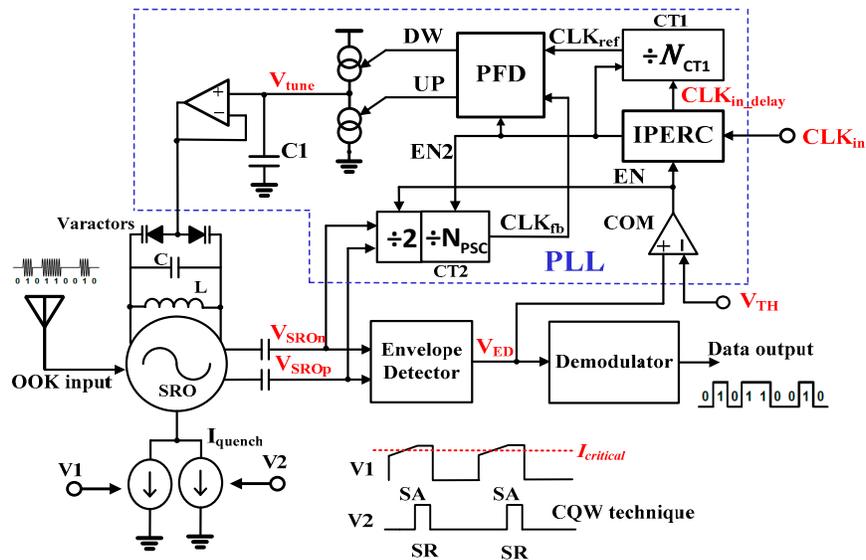


**Figure 6.** Optimal quenching waveform under PVT variations: (a) OQW slope variations and (b) sensitivity variations under slope variations.

## 2.2. Proposed SR Receiver with Background Frequency Calibration and Concurrent Quenching Waveform

### 2.2.1. SR Receiver Architecture Overview

The block diagram of the proposed SR receiver is illustrated in Figure 7. This receiver consists of an SRO quenched by the proposed CQW and a PLL with the initial phase error reduction, built around the SRO for frequency calibration. Beside the components illustrated in Figure 3a, the proposed PLL includes an initial phase error reducing circuit (IPERC), a comparator (COM) used to trigger frequency calibration periodically, a divider (CT1) employed to generate a synchronized reference clock  $Clk_{ref}$  from the input clock  $Clk_{in}$ , and an analog OTA-based buffer to drive the varactors and hold the charge on the capacitor  $C_1$ . Unlike the above mentioned PLL or FLL techniques in References [4,6] that interrupt the receiving phase to perform frequency calibration, the proposed PLL can perform frequency calibration without disturbing the data receiving. When the envelope detector output  $V_{ED}$  goes high, exceeding a preset threshold voltage  $V_{TH}$ , the output EN of comparator COM in PLL turns high accordingly to enable PLL to detect the frequency difference between the SRO output frequency and the desired one, and tune the SRO center frequency via the voltage  $V_{tune}$ . Meanwhile, the proposed CQW technique is applied to the SRO to achieve noise reduction and sensitivity enhancement robust to PVT variations.



**Figure 7.** The block diagram of the proposed SR receiver with background frequency calibration and CQW technique.

### 2.2.2. Fast Frequency Calibration Using PLL with Initial Phase Reduction

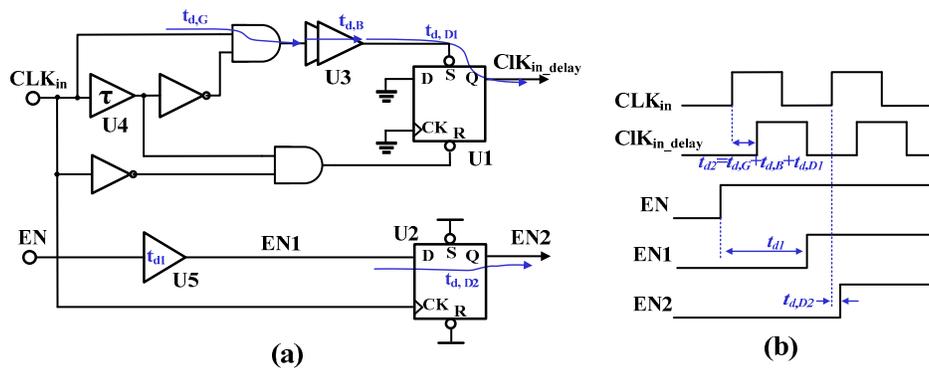
As shown in Figure 7, the proposed PLL is composed mainly of a phase detector, a high-speed analog divider ( $\div 2$ ) combined with a pulse-swallow counter (CT2) for RF signal frequency division, a counter (CT1) for the reference clock generation, an initial phase error reduction circuit (IPERC), and a comparator (COM). IPERC is used to eliminate the initial phase error  $\Delta\varphi_i$  between the reference clock ( $\text{Clk}_{\text{ref}}$ ) and the feedback clock ( $\text{Clk}_{\text{fb}}$ ) stemming from SRO's output. After initial phase error reduction, the actual phase error between  $\text{Clk}_{\text{ref}}$  and  $\text{Clk}_{\text{fb}}$  is detected by the phase detector and converted into the pulse width on the phase detector's output UP and DW. Then, UP and DW drive the charge pump to charge or discharge the capacitor  $C_1$  to adjust its voltage  $V_{\text{tune}}$ . Finally, the voltage on  $C_1$  is buffered and fed to the varactors to tune SRO's oscillating frequency.

The required frequency calibration time per quenching cycle for the proposed intermittent frequency calibration technique is much shorter than conventional techniques mentioned in Reference [1–2,4] owing to the initial phase error reduction. Equation (6) shows the design parameters which will influence the calibration time. The phase detector output  $\varphi_n$  represents the frequency detecting accuracy and can be derived as:

$$\varphi_n = \int_{T_{n-1}}^{T_n} (f_{\text{ref}} - f_{\text{fb}}) dt + \Delta\varphi_{i,n} = \int_{T_{n-1}}^{T_n} \left( \frac{f_{\text{in}}}{N_{\text{CT1}}} - \frac{f_{\text{SRO}}}{N} \right) dt + \Delta\varphi_{i,n} \quad (6)$$

where  $\Delta\varphi_{i,n}$  is the initial phase error occurring in the  $n$ th cycle,  $(T_n - T_{n-1})$  represents the phase detecting time,  $N = 2 * N_{\text{PSC}}$  is the overall division ratio including the ratio of the analog divider ( $\div 2$ ) and  $N_{\text{PSC}}$  from CT2 respectively;  $f_{\text{ref}}$  and  $f_{\text{fb}}$  are the frequency of  $\text{Clk}_{\text{ref}}$  and  $\text{Clk}_{\text{fb}}$ , respectively, and  $\text{Clk}_{\text{ref}}$  is the result of dividing  $\text{Clk}_{\text{in}}$  by  $N_{\text{CT1}}$  the division ratio of CT1.  $(f_{\text{ref}} - f_{\text{SRO}}/N)$  is defined as the calibration resolution which represents the difference between the desired SRO oscillating frequency and the current SRO oscillating frequency. As indicated, the ultimate phase error  $\varphi_n$  includes the unpredictable  $\Delta\varphi_{i,n}$  and the actual phase error between  $\text{Clk}_{\text{ref}}$  and  $\text{Clk}_{\text{fb}}$ .

Compared with the conventional counterparts in the state-of-art design, IPERC is the essential of the proposed PLL. Figure 8 shows the schematic of the IPERC and its signal propagation delay diagram, while Figure 9a illustrates its timing diagram.



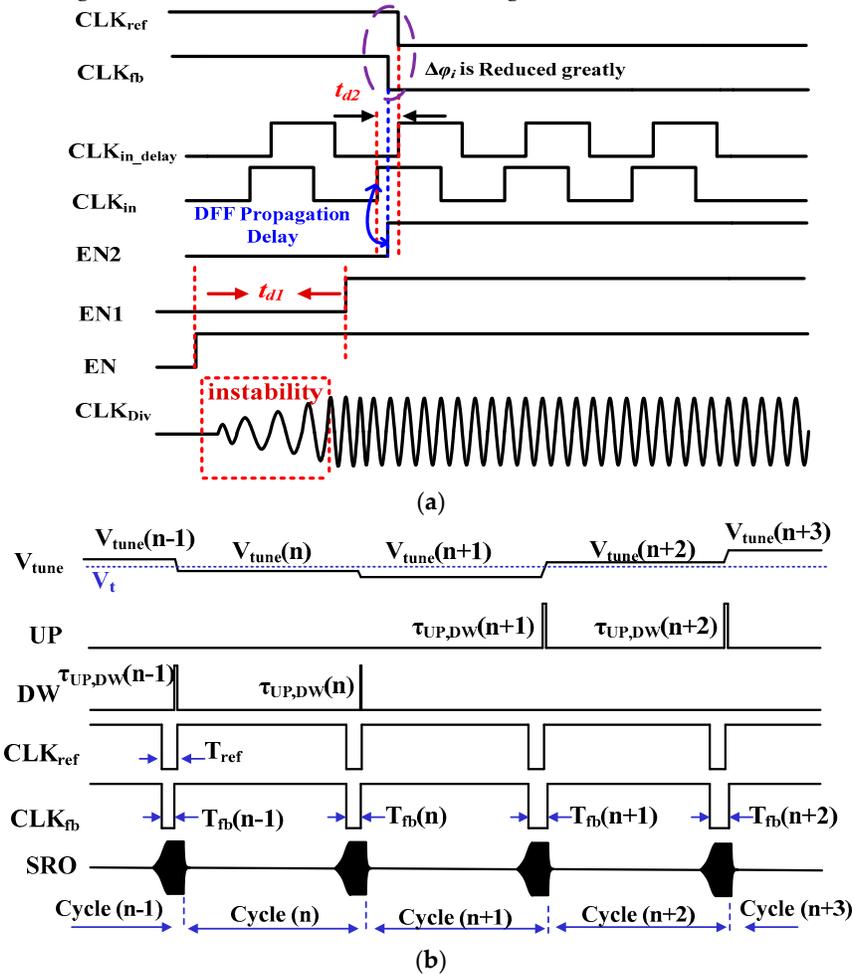
**Figure 8.** The initial phase error reduction principle: (a) the schematic and (b) its signal propagation delay.

In conjunction with those figures, the working principle of IPERC is explained as follows. This circuit includes two identical DFF-type latches, U1 and U2, with a set (S) and a reset (R) inputs. The latch U1 along with a buffer chain (U3), a delay cell (U4), two AND2 gates and two inverters are used to generate  $\text{Clk}_{\text{in\_delay}}$  which is a delayed version of the input  $\text{Clk}_{\text{in}}$ . The input EN is delayed by  $t_{d1}$  through the delay cell U5 to generate the signal EN1 which is sampled in U2 by  $\text{Clk}_{\text{in}}$  to generate the output EN2. As shown in Figure 8b, the rising edges of  $\text{Clk}_{\text{in\_delay}}$  will lag behind the corresponding rising edges of  $\text{Clk}_{\text{in}}$  by a delay of  $t_{d2}$  calculated by:

$$t_{d2} = t_{d,G} + t_{d,B} + t_{d,D1} \quad (7)$$

where  $t_{d,G}$  is the AND gate’s propagation delay,  $t_{d,B}$  is the buffer chain’s delay, and  $t_{d,D1}$  is the latch’s propagation delay from its input S to its output Q.

Simultaneously, the rising edge of EN2 will lag behind the rising edges of  $Clk_{in}$  by a delay of  $t_{d,D2}$ , the latch U2’s propagation delay from its clock input CK to its output Q. The delay of  $t_{d1}$  on EN2 is aimed at preventing the division ratio  $N$  from the instability of the analog divider during the initial start-up phase as shown in Figure 9a. To avoid the degradation of detecting accuracy caused by the instability, the value of  $t_{d1}$  must be set greater than the settling time of the analog divider. The duration of the instability varies with PVT variation, and its worst-case scenario is about 5 ns in the proposed design, hence  $t_{d1}$  is set to 10 ns in this design.



**Figure 9.** The timing diagram of the proposed PLL calibration with IPRC: (a) the timing diagram of the initial phase error reduction, and (b) the critical signals in the proposed PLL (assuming quasi-periodic steady state).

As shown in Figure 7, EN2 is used to enable the dividers CT1 and CT2 at the same time to synchronize the generation of  $Clk_{ref}$  and  $Clk_{fb}$ , and consequently eliminate their initial phase error  $\Delta\phi_i$ . According to Equation (7), the rising edge of EN2 will always lead the rising edge of  $Clk_{in\_delay}$  by a value of  $(t_{d2} - t_{d,D2})$ . That prevents CT1 from missing the first rising edge of  $Clk_{in\_delay}$  when EN2 turns high. Since  $t_{d,D1}$  approximately equals  $t_{d,D2}$ ,  $(t_{d2} - t_{d,D2})$  can be set by the buffer chain U3 to provide synchronization between  $Clk_{ref}$  with  $Clk_{fb}$ . As a result,  $\Delta\phi_i$  can be reduced from tens nanoseconds to less than 1 ns despite PVT variations.

Figure 9b presents the timing diagram of the main signals in the proposed PLL. The PLL operates on cycle by cycle basis by detecting the frequency error between  $Clk_{ref}$  and  $Clk_{fb}$ , and adjusting the tuning voltage  $V_{tune}$  and consequently the oscillating frequency of SRO in each cycle.

To systematically analyze its performance, the following hypotheses are considered: (1) the PLL operated in a quasi-periodic steady state mode; (2) The transient charging or discharging behavior of the charge pump is neglected. After calibration, the negative pulse width  $T_{fb}$  of  $\text{Clk}_{\text{fb}}$  approximately equals  $T_{ref}$ , the counterpart of  $\text{Clk}_{ref}$ ; while the tuning voltage  $V_{tune}$  will approach the desired level  $V_t$ . Therefore, the following equations can be found:

$$\left\{ \begin{array}{l} T_{fb}(n) = T_{ref} + \Delta T_{fb}(n) \\ \Delta \tau_{UP,DW}(n) = \Delta T_{fb}(n) + \frac{1}{2\pi} \Delta \varphi_i(n) \\ V_{tune}(n) = V_t + \Delta V_{tune}(n) \\ V_{tune}(n) = V_{tune}(n-1) + \frac{I_{CP}}{C_1} \Delta \tau_{UP,DW}(n-1) \\ f_{SRO}(n) = f_o - kV_{tune}(n) \\ f_{SRO}(n)T_{fb}(n) = N \end{array} \right. \quad (8)$$

where  $\Delta \varphi_i(n)$  is the initial phase error in the cycle  $n$ ,  $\Delta \tau_{UP,DW}(n)$  is the pulse width of PFD's outputs;  $I_{CP}$  is the current of the charge pump;  $C_1$  is the capacitance of C1; and  $k$  is the voltage-to-frequency gain of SRO (assumed to have a negative value),  $f_{SRO}$  is the oscillating frequency of SRO while  $f_o$  is its initial value. Those equations can be combined as:

$$(f_o - kV_t)T_{ref} - kT_{ref}\Delta V_{tune}(n) + (f_o - kV_t)\Delta T_{fb}(n) - k\Delta V_{tune}(n)\Delta T_{fb}(n) = N \quad (9)$$

It is notable that  $(f_o - kV_t)$  equals the target frequency  $f_{TF}$  which is expected to be  $N/T_{ref}$ . Additionally,  $\Delta V_{tune}(n)\Delta T_{fb}(n)$  is sufficiently small compared to other terms in Equation (9), and can be neglected. The Equation (9) can be rewritten as:

$$\Delta V_{tune}(n) \approx \frac{f_{TF}}{kT_{ref}} \Delta T_{fb}(n) \quad (10)$$

Substituting Equation (10) into Equation (8) yields:

$$[\Delta T_{fb}(n) - \Delta T_{fb}(n-1)] = \frac{I_{CP}T_{ref}k}{C_1f_{TF}} \left[ \Delta T_{fb}(n-1) + \frac{1}{2\pi} \Delta \varphi_i(n-1) \right] \quad (11)$$

By applying Z-domain analysis to Equation (11), the transfer function of the PLL can be written as:

$$H(z) = \frac{\Delta T_{fb}(z)}{\Delta \varphi_i(z)} = \frac{\frac{I_{CP}T_{ref}k}{2\pi C_1 f_{TF}} z^{-1}}{1 - \left(1 + \frac{I_{CP}T_{ref}k}{C_1 f_{TF}}\right) z^{-1}} \quad (12)$$

As implied by Equation (12), the necessary and sufficient condition for the stability of the proposed PLL is:

$$\left| 1 + \frac{I_{CP}T_{ref}k}{C_1 f_{TF}} \right| < 1 \rightarrow \beta = \left| \frac{I_{CP}T_{ref}k}{C_1 f_{TF}} \right| < 2 \quad (13)$$

The step response of the system can be written as:

$$h(n) = 1 - (1 - \beta)^n \quad (14)$$

From the above equation, it can be observed that a larger  $\beta$  can lead to a faster system's convergence but results in a larger ripple on  $\Delta T_{fb}$ . In this design,  $\beta$  is set to 0.27 to guarantee accurate frequency calibration as it is discussed in section 3.

### 2.2.3. SRO with Concurrent Quenching Waveform

The proposed SRO architecture and its timing diagram are shown in Figure 10 and Figure 11 respectively. In contrast to conventional SRO architectures, the SA and SR regions in the proposed one are separately controlled by M5 and M6 which perform the proposed CQW operation. M5 is controlled by  $V_1$  and is on for the entire quenching period (case when  $V_1 = V_{1a}$  in Figure 11). M6 is controlled by  $V_2$  and is on only during the SR region. When M5 is on, the SRO is always operating

in the vicinity of  $I_{critical}$  and accumulates sensitivity during the entire quenching phase. When M6 is on, the SRO performs super-regeneration and sensitivity accumulation simultaneously, while the conventional SRO architecture with OQW loses sensitivity accumulation during SR region. When the transistors M5–6 are both on, the SRO is in SR region and concurrently regenerates the SRO output and samples the input signal for the entire quenching cycle.

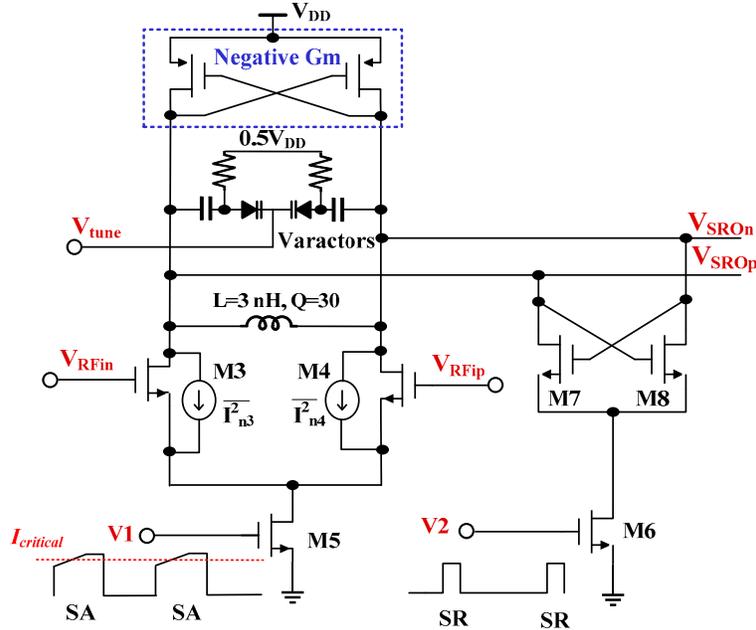


Figure 10. The proposed SRO architecture with CQW technique.

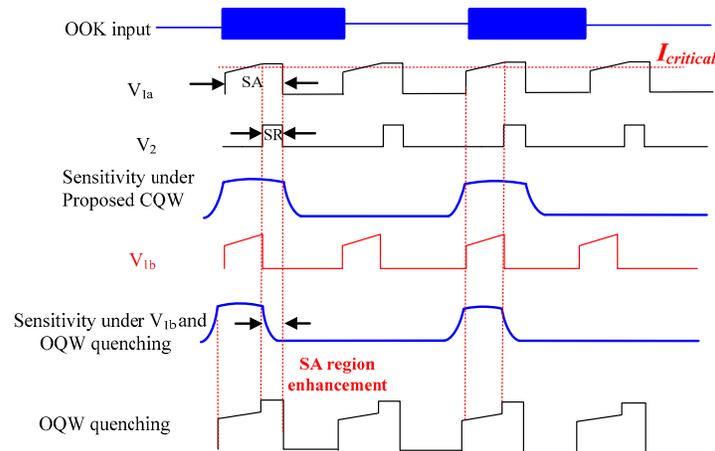


Figure 11. Comparison between the conventional OQW and the proposed CQW techniques.

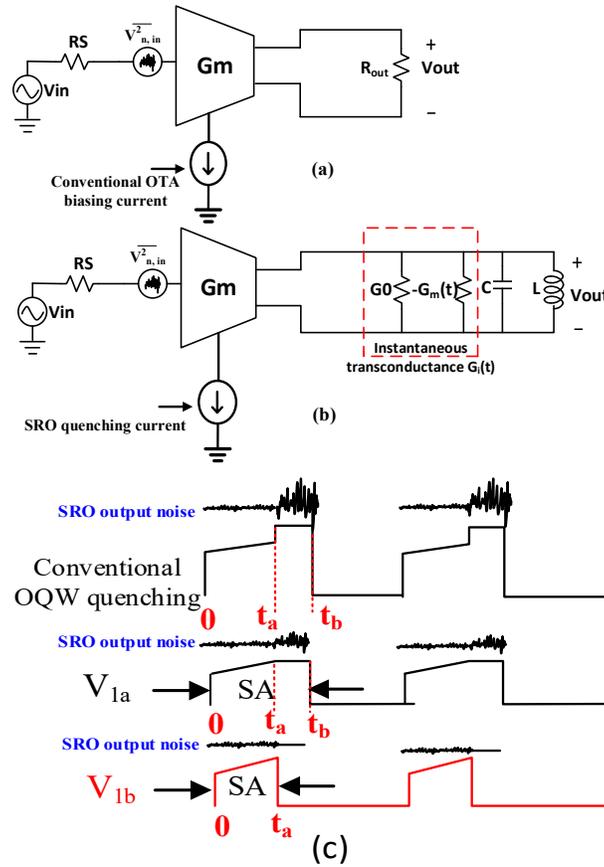
Splitting the quenching signal into  $V_1$  and  $V_2$  allows optimizing the noise performance in addition to improving the accumulated sensitivity compared to OQW as will be explained later. Figure 12c shows the SRO output noise with different  $V_1$  waveforms,  $V_{1a}$  and  $V_{1b}$ , along with OQW scheme. For  $V_1 = V_{1a}$ , M5 is on for the entire quenching period to improve sensitivity and noise compared to OQW. For  $V_1 = V_{1b}$  M5 is turned off to improve more the noise performance compared to the case of  $V_1 = V_{1a}$  while achieving same sensitivity as OQW.

To understand how to optimize the noise of the SRO it is instructive to compare the noise performance of an OTA and an SRO as shown in Figure 12a,b. The small signal model of an OTA and SRO are different by the type of load. Additionally, the OTA is biasing using constant current

while an SRO is biased using its customized quenching waveform. The output referred noise of an OTA can be analyzed as follows:

$$\overline{V_{n,out}^2} = V_{n,in}^2 A_v^2 \tag{15}$$

where  $\overline{V_{n,in}^2}$  and  $\overline{V_{n,out}^2}$  are the input and output referred noise respectively. Gain of an OTA,  $A_v$  simply equals  $G_m R_{out}$ . Since the biasing current is a constant value which means that the  $G_m$  maintains a constant value. In conventional linear receivers with OTA placed as the front-end signal detector, increasing the biasing current will cause input referred noise to decrease because the current thermal noise of a MOS transistor is proportional to  $G_m$  while the input referred noise is inversely proportional to  $A_v^2$ .



**Figure 12.** Noise analysis comparison between conventional OTA and SRO: (a) small signal model for OTA, and (b) SRO; (c) SRO quenching strategy and noise performance comparison.

Similarly, the input referred noise of the SRO can be intuitively analyzed also by starting from the SRO gain  $A_v$  [7,8] as the following:

$$A_v = k_0 k_r u(t) \tag{16}$$

with

$$k_r = \delta_0 \omega_0 \int_0^{t_b} s(\tau) d\tau \tag{17}$$

where  $k_r$  is the SRO regenerative gain and  $u(t)$  is the SR gain as given in Equation (5).

$$\overline{V_{n,out}^2} = V_{n,in}^2 A_v^2 \Delta f_{ENB} \tag{18}$$

The gain  $A_v^2$  can also be written as the following:

$$A_v^2 = k_r^2 u(t)^2 \frac{G_{meff}^2}{G_0^2} \quad (19)$$

where  $\Delta f_{ENB}$  is the equivalent noise bandwidth (ENB) of the SRO frequency response.  $G_{meff}$  and  $G_0$  refer to the effective transconductance of M3–4 in Figure 10 and static loss of the SRO. For practical design purposes, in Equations (16)–(19) the SRO regenerative gain  $k_r$  is much greater than the SR gain  $u(t)$  for the SRO to achieve good sensitivity. The noise bandwidth in Equation (18) is determined by the selectivity of the SRO.

As we can notice, the major difference for the noise analysis between conventional OTA-based receivers and SR receiver is that the gain  $A_v$  of an SRO consists of 3 different components, namely static loss, regenerative gain, and super-regenerative gain corresponding to  $k_0$ ,  $k_r$ ,  $u(t)$  respectively. For the proposed CQW scheme applied as quenching signal for the SRO under  $V_{1a}$ , the sensitivity region has been extended over the entire quenching cycle and the SRO is always responding to the input OOK signal for both SA and SR regions. Therefore, the major contribution of the SRO gain  $k_r$  is not degrading through the entire quenching cycle and hence reducing the input referred noise and improving the SNR. In contrast, for the SRO under OQW quenching, the SR region is only responsible for generating the oscillation envelope, in response to the SA region, while  $k_r$  is dramatically reduced because the sensitivity decays to 0 (refer to Figure 11). Therefore, the input referred noise will dramatically increase and hence degrade the SNR. It is straightforward to find that the SRO frequency response has narrower noise bandwidth for the proposed CQW technique compared with the conventional OQW quenching because the proposed CQW technique extends the sensitivity for the SRO in time domain and therefore, it automatically reduces the  $\Delta f_{ENB}$  to reduce the noise.

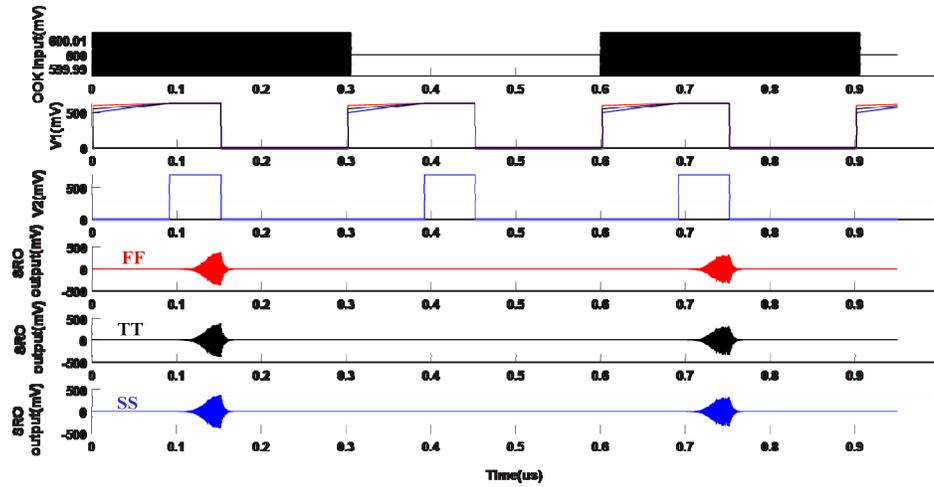
The dominant noise source of the SRO circuits is stemmed from the input transistors (M3–4 in Figure 10); when  $V_1 = V_{1b}$  the transistors M3–M4 are turned off in SO region to reduce the noise as highlighted in red in Figure 12c. That will maintain the same SA region compared with the OQW while reducing the biasing current completely in the SR region for the input transistors M3–4 to maximize the SNR for the SRO under the trade-off of lower sensitivity accumulation compared to the case of  $V_1 = V_{1a}$ .

### 3. Simulation Results and Discussion

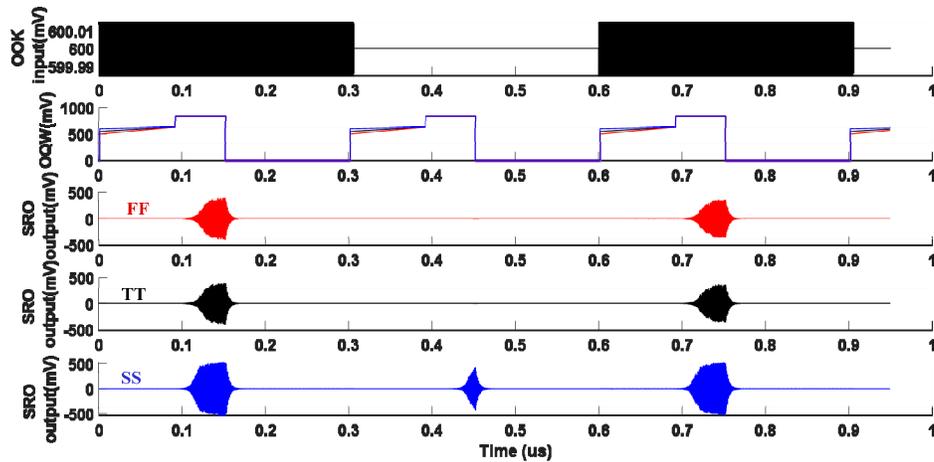
The proposed SR receiver with PLL frequency calibration and CQW technique is implemented in at transistor level using 180 nm SMIC CMOS technology. An inductor of 3 nH with a quality factor (Q) of 30 and a pair of varactors with a nominal capacitance of 0.5 pF (at  $V_{tune} = 0.5V$ ) are used to set the SRO resonance frequency around 2.46 GHz. A Gm-booster crossing-coupled PMOS pair with an aspect ratio of 450/0.18 is used to provide sufficient negative transconductance under a supply voltage of 1 V. The aspect ratio of input pair (M3/M4/M7/M8) in Figure 10 is 150/0.18.

Figure 13 is the simulation results to illustrate the operating principle of the proposed SRO with CQW technique. The CQW extends the SA region during the control voltage  $V_1$ , while  $V_2$  is only used to generate fast start-up oscillation. As a result, the effect of the process variation on slope changes can be reduced. As shown, the process variations does not degrade the sensitivity accumulation because the SA region has been extended over the entire quenching cycle and the SRO is able to detect the input signal correctly with different slopes of the voltage  $V_1$ .

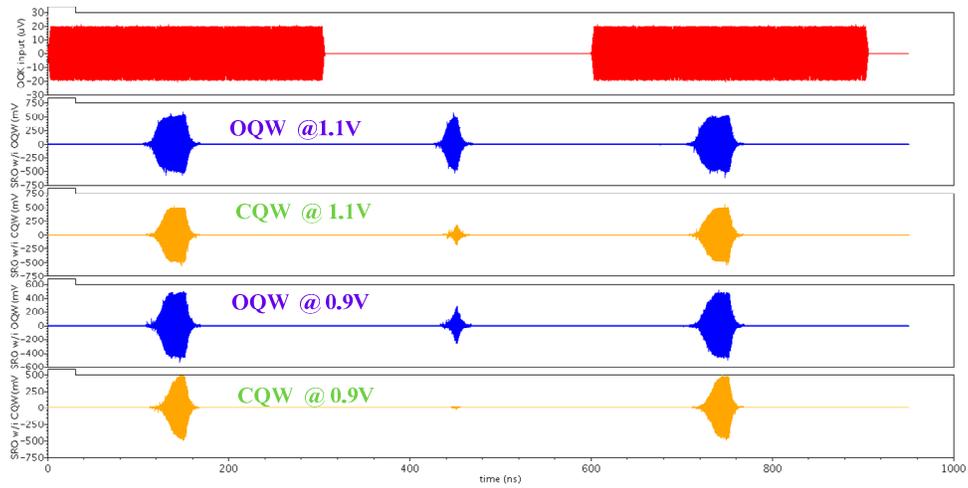
In contrast to Figure 13, Figure 14 show how the conventional OQW suffers under process variations which dramatically reduce the sensitivity of the SRO. That is indicated from the oscillation at the SRO output during the absence of input OOK signal. Figures 15 and 16 show the immunity of the proposed the proposed CQW architecture against voltage and temperature variations respectively. Figure 17 shows how the proposed CQW architecture can reduce the oscillation at the SRO output during the absence of input signal with the presence of noise compared with OQW. That is indicated by reducing the oscillation at the SRO output during the absence of input OOK signal.



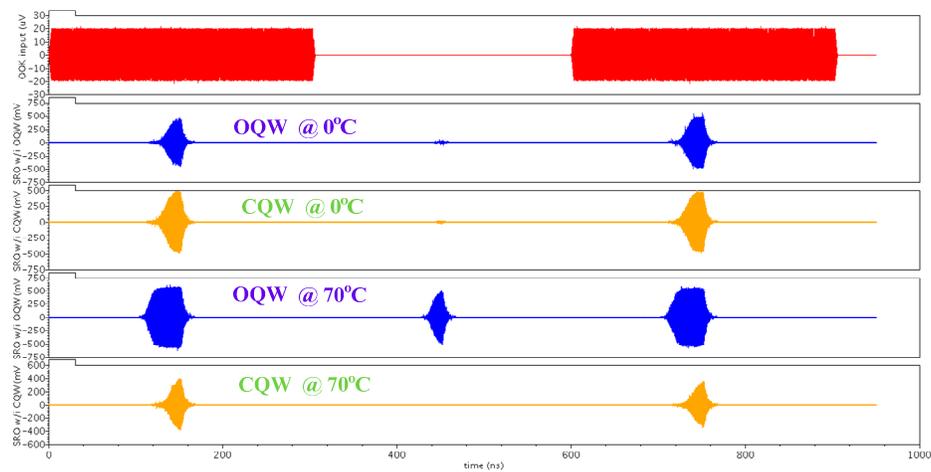
**Figure 13.** The simulation results illustrating the SRR’s immunity against process variations when the proposed quenching waveform is applied. From top to bottom: the input OOK signal, the proposed CQW voltage  $V_1$  under process variations, the proposed CQW voltage  $V_2$ , and the SRO output signals under process variations (the red line for the fastest-speed process corner (FF), the black is for the typical (TT), and the blue is for the slowest one (SS)).



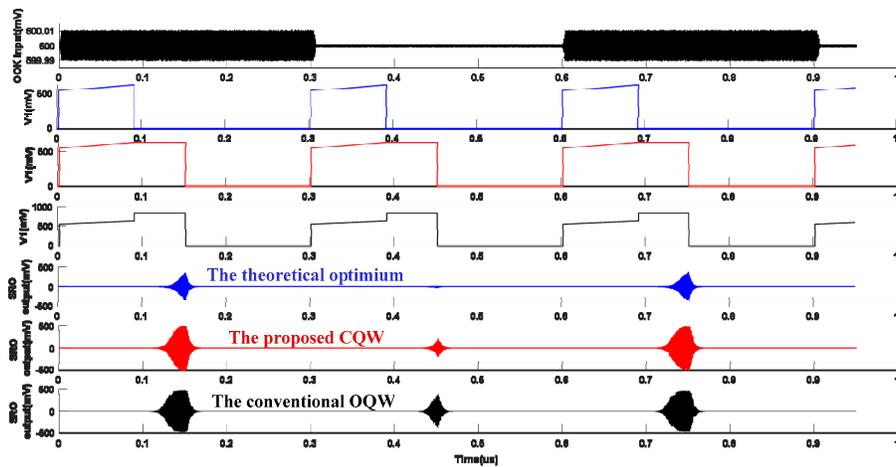
**Figure 14.** The simulation results illustrating the SRR’s immunity against process variations when the conventional optimal quenching waveform is applied. From top to bottom: input OOK signal, the combined CQW waveform, and the SRO output signals under process variation (the red line for the fastest-speed process corner (FF), the black is for the typical (TT), and the blue is for the slowest one (SS)).



**Figure 15.** The simulation results illustrating the SRR’s immunity against supply voltage variations. From top to bottom: the input OOK signal, the OQW @ 1.1V, the proposed CQW @ 1.1V, the OQW @ 0.9V, and the proposed CQW @ 0.9V.

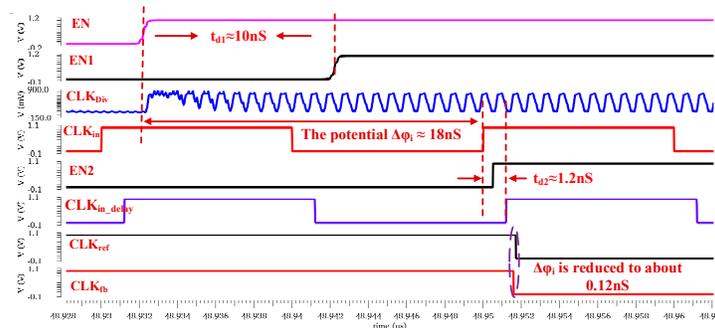


**Figure 16.** The simulation results illustrating the SRR’s immunity against temperature variations. From top to bottom: the input OOK signal, the OQW @ 0 °C, the proposed CQW @ 0 °C, the OQW @ 70 °C, and the proposed CQW @ 70 °C.

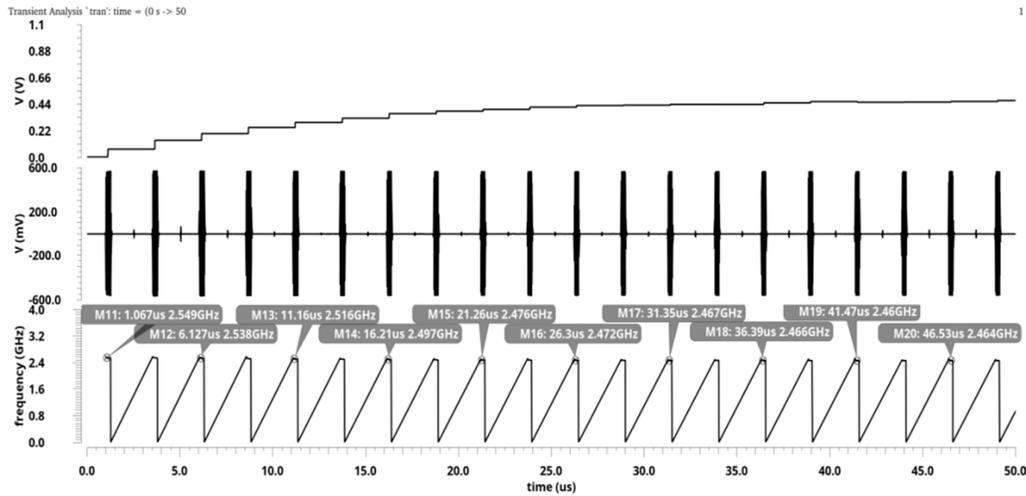


**Figure 17.** The simulation results illustrating noise analysis comparison between the proposed CQW technique and the conventional OQW technique. From top to bottom: the input OOK signal, the proposed CQW quenching voltage  $V_{1b}$ , the proposed CQP quenching voltage  $V_{1a}$ , the conventional OQW quenching voltage, and the SRO output signals corresponding with different quenching waves.

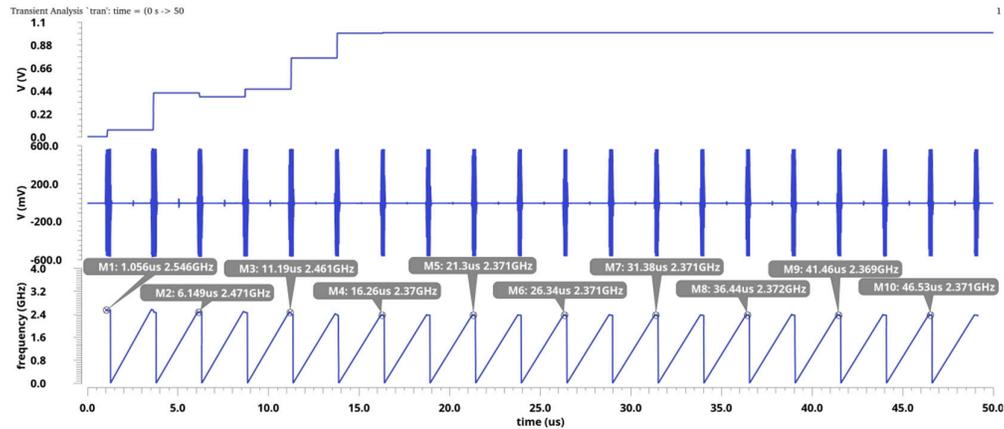
Figure 18 shows the proposed PLL with initial phase error reduction.  $Clk_{in}$  is set to 50 MHz and the division ratio of  $N_{CT1}$  and  $N_{PSC}$  are 5 and 123 respectively to expect a final  $f_{SRO}$  of 2.46 GHz. As Figure 16 indicates, due to the random initial phase  $\Delta\phi_i$  between EN and  $Clk_{in}$ , the time shift can be up to 18 ns. However, by applying the proposed initial phase error reduction, the actual phase error can be shortened to be around 0.12 ns. Therefore, the proposed PLL can differentiate the small frequency deviation between  $Clk_{ref}$  and  $Clk_{fb}$  and then adjust the voltage  $V_{tune}$  in each calibration cycle. Figure 19 illustrates the proposed frequency calibration process during SR receiver's receiving. In simulations, each quenching cycle lasts 1.25  $\mu$ s to match a data rate of 800 kbps wherein the SR phase only occupies a length of 300 ns. Despite the short SR phase, the proposed PLL is still able to adjust the oscillating frequency from 2.55 GHz to 2.46 GHz with a frequency error of less than 10 MHz as shown. In contrast, when the initial phase error reduction is disabled, the PLL fails to obtain sufficiently precise frequency error detection, and the initial phase error misleads the adjustment of  $V_{tune}$ . As a result, the PLL finally settles down to a wrong  $f_{SRO}$  as shown in Figure 20.



**Figure 18.** The simulation results of the proposed phase error reduction under clock synchronization and delay compensation.



**Figure 19.** The simulation results of the proposed background frequency calibration, sequentially including: the control voltage, SRO’s output signal, and the frequency calibration results (the calibration results in each quenching cycle have been labeled).



**Figure 20.** The simulation results without the proposed initial phase error reduction, sequentially including: the control voltage, SRO’s output signal, and the frequency calibration results (the calibration results in each quenching cycle have been labeled).

In the following simulation the immunity of the proposed PLL is evaluated under technology process variations. The SRO’s frequency versus voltage curves are tested with corners variation as shown in Figure 21. The frequency variation can be up to 50 MHz with a fixed  $V_{tune}$  due to the process variation while the voltage-to-frequency gain is about  $-267$  MHz/V at  $f_{SRO} = 2.46$  GHz under the TT process corner. Figure 22a shows the settling behavior of PLL is with different values of  $\beta$  changed by selecting different  $I_{CP}$  according to Equation (13). As shown in Figure 22a, when  $\beta$  is less than 2, all waveforms of  $V_{tune}$  gradually converge but with ripple due to the random  $\Delta\phi_i$  in each cycle. A larger  $\beta$  leads to a faster convergence, but more ripples. To achieve a precise frequency calibration,  $\beta$  is set to 0.27. In this case, the settling time of PLL is about 35  $\mu$ s, and the ripple of  $V_{tune}$  is limited to less than 25 mV which corresponds to a frequency variation of 6.7 MHz. Figure 22b shows the settling behavior under various process corners with  $\beta = 0.27$ . It can be seen that the waveforms can converge regardless of the process variation with a maximum voltage ripple less than 25 mV.

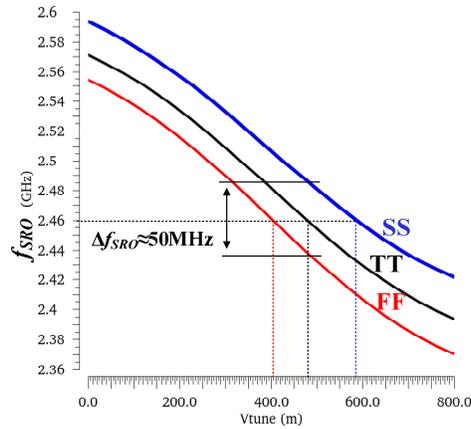


Figure 21. The simulation curves of  $f_{SRO}$  vs  $V_{tune}$  under different process corners.

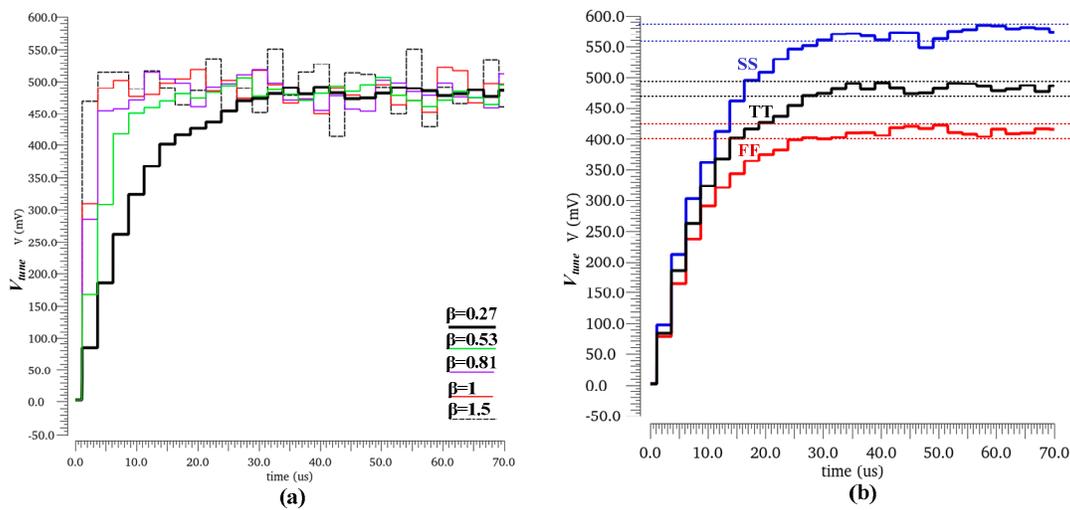
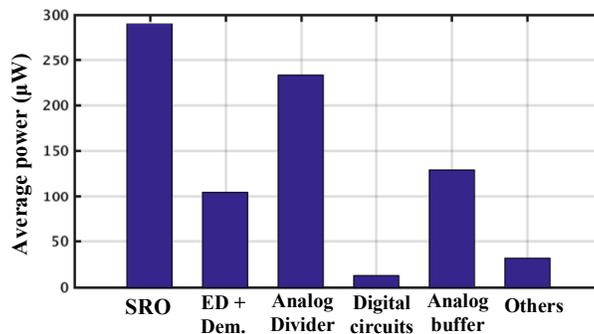


Figure 22. The simulated settling waveforms of  $V_{tune}$  (a) with different values of  $\beta$ , and (b) under process variation with a constant  $\beta = 0.27$ .

Figure 23 shows the breakdown power consumption of the proposed SR receiver. The total power consumption of the receiver is about 802  $\mu\text{W}$ , including the main blocks of the receiver: the SRO, the envelop detector (ED), and the demodulator (Dem.), contributes a power consumption of about 395  $\mu\text{W}$ ; while the PLL consumes a power of 407  $\mu\text{W}$  in average. Table 1 summarizes the performance of this work in comparison with the state-of-arts. The main features of the proposed design are the ability to achieve background frequency calibration with a good sensitivity and less power consumption compared to the counterparts.



**Figure 23.** The simulated power consumption summary.**Table 1.** Performance table and comparison to the prior works.

	[4]	[5]	[6]	This work <sup>1</sup>
Process (nm)	130	180	40	180
Frequency band (GHz)	2.4	0.4	0.9	2.4
Calibration Technology	Analog PLL	Digital PLL	Digital PLL	Analog PLL
Background Calibration	No	No	No	Yes
Sensitivity (dBm)	−90	−83	−86	−87
Data rate (Mbps)	0.5	1	1	0.8
Quench Signal	Internal digital	Internal digital	Internal analog	External CQW
Supply (V)	1.1–1.3	1.5	0.65	1
Power (mW)	2.8	5.5	0.32	0.8

<sup>1</sup> Simulation results, others are from measurements.

#### 4. Conclusions

This paper proposed a new background frequency calibration and quenching techniques to improve the sensitivity and selectivity of SR receiver. In this work, the importance of cancelling of the initial phase error is discussed and frequency calibration using a PLL with the initial phase error reduction has been proposed to calibrate the SRO center frequency without interrupting the incoming data stream and simultaneously improving the selectivity of the SR receiver. The proposed architecture achieves much shorter phase detecting time to support discrete frequency calibration compared with conventional techniques. Moreover, the proposed CQW quenching technique allows the sensitivity accumulation region to be enlarged through the entire quenching cycle which improves the SRO sensitivity, noise performance, and reduce the power consumption compared with conventional SRO architecture. Meanwhile, immunity to PVT variations has also been improved due to the SA region extension.

**Author Contributions:** All the authors contributed substantially to this paper. The conceptualization, methodology, validation, and formal analysis of PLL, Y.Y.; The conceptualization, methodology, validation, and formal analysis of CQW, F.X. and K.E-S; investigation, Y.Y.; writing—original draft preparation, Y.Y., and F.X.; writing—review and editing, Y.Y and K.E-S; funding acquisition, Y.Y., and K.E-S.

**Funding:** This research was partly funded by THE FUJIAN PROVINCIAL NATURAL SCIENCE FOUNDATION OF CHINA, grant number 2017J01760, and 2017J01734, and THE NATURAL SCIENCE AND ENGINEERING RESEARCH COUNCIL OF CANADA.

**Conflicts of Interest:** The authors declare no conflicts of interest.

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