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Model-Based Quasi-Sliding Mode Control with Loss Estimation Applied to DC–DC Power Converters

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Abstract: This paper presents the experimental implementation of a buck converter with quasi-sliding mode control combined with a loss estimator function. An online loss estimator is developed to estimate, in real time, the parasitic resistances of the converter and variations of the resistance in the load. The estimated loss resistance and the resistance of the load are embedded, in real time, into the model equations of the controller using Zero Average Dynamics and Fixed Point Induction Control techniques (ZAD-FPIC) to improve the control robustness to resistive parameter variations. Details of the experimental setup are presented to show developed electrical and electronic circuits, and experimental techniques are described to ensure the successful digital implementation of closed-loop control of the buck power converter. The proper shielding of electrical wiring in power electronics allows improvement to the quality of the measures by removing noise induced by electromagnetic interference. A trigger signal is used to implement the Pulse-Width Modulation (PWM) with centered pulse and to synchronize the sampling of analogical signals from the buck converter. Such synchronization allows the use of a lower sampling frequency and ensures the measurements at the right instant in time. Experimental results are in good agreement with numerical simulations, showing the effectiveness of the control approach.

Keywords: buck converter; ZAD-FPIC; control parameters; sliding mode control; recursive least squares

1. Introduction

A buck converter is a DC–DC power converter that is applied in a wide range of low-voltage technological applications. This converter can be modeled as a piecewise linear system [1], where the theory and models can be found in ref. [2]. However, the converter presents significant voltage variations when different types of loads are connected [3].

A good mathematical model derives from an appropriate balance between simplicity and accuracy. An approach that combines theoretical, simulated, and experimental tests is pertinent to find the best balance. Advances in electronics have allowed the development of rapid control prototyping (RCP) platforms [4,5], where real-world systems can be automatically connected with mathematical models [6]. By integrating theoretical, simulated, and experimental methods, the best model can be identified and its control strategy validated at the same time.

Besides, in ref. [7], the steady-state limit cycles in PWM-controlled converters were evaluated and, to avoid oscillations, some conditions were imposed on the control law and the quantization resolution.

On the other hand, the Fixed-Point Induction Control (FPIC) technique allowed the stabilization of unstable orbits [8]. Recent control techniques applied to the buck converter are the Zero Average Dynamics (ZAD) and FPIC, which have shown good results for controlling the output voltage [9].

The internal parameters of an electronic converter may vary depending on the operating conditions. In addition, load variations or the aging of components may occur. Ignorance of these parameters in real time can cause inaccuracies in the design of the controllers [10], which causes instability throughout the system [11]. Therefore, adaptive and self-adjusting controllers based on parameter identification are being investigated. Power losses in the circuit must be considered to accurately represent similar results between simulation and experimental tests. In the literature, some authors have focused on estimating power losses in the switching process of the metal– oxide– semiconductor field-effect transistor (MOSFET) [12]. In addition, the power losses in the core of an inductor in a PWM converter are estimated [13]. Furthermore, other elements in the circuit produce power losses, such as the capacitor, current sensor, and feeding source, which is why parameter estimation must identify those not considered in the simulation test. The most commonly used methods to estimate the parameters are conventional least squares [14,15] and recursive least squares (RLS) [16,17]; both techniques help to obtain accurate results when loads are fixed or vary slowly [10]. Due to the above, the RLS technique is used in this work to estimate these parameters in the circuit.

In ref. [18], the parameters estimation of a buck converter with digital PWM control and ZAD strategy is presented. A visualization approach was applied in [19], where the output voltage of a buck power converter is controlled by means of a quasi-sliding scheme. There, the authors introduced the load estimator by means of least mean squares to make the ZAD-FPIC control feasible in load variation conditions, and comparative results for the buck converter with different control strategies (including: Sliding Mode Control (SMC), Proportional–Integral–Derivative (PID) and ZAD-FPIC) were presented.

In ref. [19], the FPIC technique is used for the control design based on (ZAD) strategy, including load estimation by means of the Least Mean Squares (LMS) method. In ref. [20], an adaptive ZAD-FPIC strategy is formulated for motor speed control. The system involves a buck power converter, a permanent magnet DC motor (PMDC motor) [21], and a dSPACE platform; the load torque and the friction torque are considered unknown so that they lead to an uncertain parameter that is estimated by means of a least mean squares (LMS) mechanism, which is formulated and tested on the real system.

A comparative analysis that represents the advantages and drawbacks is presented in Table 1. This table lists the four applications of ZAD, FPIC, ZAD-FPIC, and ZAD-FPIC with the recursive least squares (RLS) method. ZAD-FPIC with the RLS method has more advantages over the other combinations because it inherits the advantages of the ZAD-FPIC controller and is also robust against changes in the internal parameters of the converter and changes in the load. Therefore, this article shows the development of ZAD-FPIC with the RLS method where parasitic resistance and load resistance are measured.

Table 1. Advantages and drawbacks of the ZAD and FPIC techniques.

Technique	Advantages	Drawbacks
ZAD	Fixed switching frequency, low steady state error, and robustness to load disturbances.	Not robust to changes in system parameters and real-time processing requires a high sampling rate and synchronization of signal sensing with a CPWM output.
FPIC	Useful for chaos control and stabilization of orbits of a higher period and order.	Not robust to changes in the system parameters and does not have feedback of the controlled variables.
ZAD-FPIC	It presents fixed switching frequency under steady-state error (meaning it permits the control of variables even if there are time delays in the system), and it allows control of chaos and oscillations in the controlled variable.	It inherits the same issues of ZAD and FPIC, which makes it not robust due to variation of internal system parameters and load. Furthermore, the steady-state error increases if there is variation in the system parameters.
ZAD-FPIC with RLS method	Inherits the advantages of ZAD-FPIC and is robust to changes in the internal parameters of the system and load variations.	Does not measure parameters that present high-speed changes and the system must be linear with respect to the parameter to be estimated.

Additionally, previous works do not estimate losses related to parasitic resistance, which changes due to heating. Besides, neither a description is made of how the experiments were performed and nor is it explained how the sampling and signal synchronization was made with the firing signal given by the Centered Pulse Width Modulation (CPWM) signal. Therefore, this paper presents a detailed method to perform both the experimental test and the synchronization of sampling signals and the effects of parasitic resistance losses, in addition to the real-time controller.

2. Materials and Methods

2.1. Buck Converter Model

Figure 1 displays a diagram of the buck converter with an integrated control that uses the ZAD and FPIC techniques. The converter has a power source with voltage E, internal source resistor r_s, an N-Channel MOSFET IRFP350 working as a switch S, an internal MOSFET resistance r_M, a diode with forward voltage V_{fd}, a filter LC, an internal resistance of the inductor r_L, a resistance used to measure current r_{Med}, and a resistance R that represents the load of the circuit.

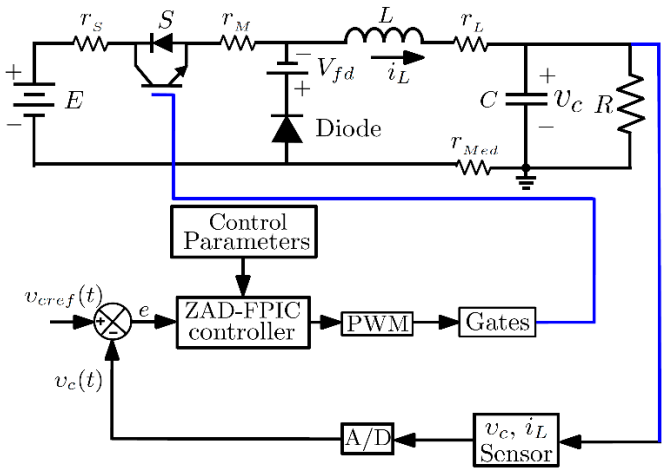


Figure 1. Buck converter controlled by Zero Average Dynamics and Fixed Point Induction Control (ZAD-FPIC).

From the circuit in Figure 1, the output voltage v_c and the inductor current i_L are measured in discrete time at each sampling period T. These measures are the inputs for the ZAD-FPIC control law used to regulate the output signal v_c. The control requires adjusting the reference voltage $x_{1ref} = v_{cref}$ and the control parameters K_s and N. These parameters are responsible for the system dynamics and stability regions.

The output signal of the controller enables the CPWM, which drives the change of state in switch S, between ON and OFF, providing the inductor input with a voltage E or $-V_{fd}$, respectively, as depicted in Figure 2. This voltage modulator combined with the switch S, the DC power source, and in conjunction with the filter LC and the diode D, must supply to the load R an average voltage v_c during a switching period.

The inductor input signal when using a CPWM gate command is shown in Figure 2, where the duty cycle d is calculated for each period T, and E is the voltage magnitude. Herein, when the output signal of the CPWM yields the gate command $u = 1$ and the switch S is enabled (state ON), the mathematical model is described by Equation (1):

$$\begin{bmatrix} \dot{v}_c \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & \frac{-(r_s+r_M+r_{Med}+r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} E, \tag{1}$$

which can be simplified in the form:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a & h \\ m & p_2 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} E, \tag{2}$$

where $a = -1/RC$, $h = 1/C$, $m = -1/L$, and $p_2 = -(r_s + r_M + r_{Med} + r_L)/L$. The term x_1 is the capacitor voltage v_c and x_2 is the inductor current i_L:

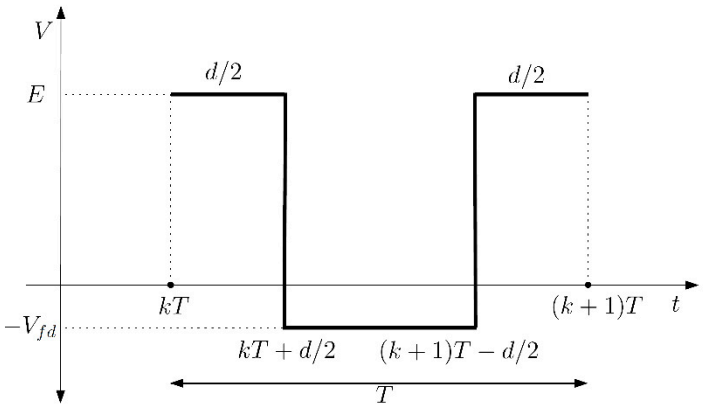


Figure 2. Voltage signal supplied to LC filter when using a CPWM command to drive the MOSFET transistor (switch S).

When the output signal of the CPWM indicates the value $u = 0$, the switch S is disabled (state OFF) and, in this condition, the system can be modeled by Equation (3):

$$\begin{bmatrix} \dot{v_c} \\ \dot{i_L} \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & \frac{-(r_{Med}+r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{-1}{L} \end{bmatrix} V_{fd}. \tag{3}$$

Analogously, Equation (3) can be simplified in the form:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a & h \\ m & p_3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{-1}{L} \end{bmatrix} V_{fd}, \tag{4}$$

where the terms $a = -1/RC$, $h = 1/C$, $m = -1/L$, and $p_3 = -(r_{Med} + r_L)/L$.

Thus, to describe the dynamical system during a complete period T, Equations (2) and (4) can be combined as shown in Equation (5), where $\dot{x} = \left[\dot{x}_1, \dot{x}_2\right]' = \left[\frac{dx_1}{dt}, \frac{dx_2}{dt}\right]'$:

$$\dot{x} = \begin{cases} A_1 x + B_1 E & \text{if } \; kT \le t \le dT/2 \\ A_2 x + B_2 V_{fd} & \text{if } \; kT + \frac{dT}{2} \le t \le kT + T - dT/2 \\ A_1 x + B_1 E & \text{if } \; kT + T - \frac{dT}{2} \le t \le kT + T \end{cases}. \tag{5}$$

The control goal is to ensure the output voltage v_c provided to the load R corresponds to a desired reference voltage, namely $x_{1\text{ref}}$. The regulation must be performed at each period T by computing the proper duty cycle ($d \in [0, T]$), to be applied at the next iteration. Thus, the switch S must be driven according to the CPWM signal, remaining closed for the duration of the duty cycle or when $u = 1$.

2.2. ZAD Control Strategy

The ZAD approach was proposed in ref. [22] and studied also in refs. [19,23,24]. The idea behind the method is to define a sliding error function and force the average error to zero at each sampling

period [23]. Then, suppose that $e = x_1 - x_{1ref}$ is the tracking error and $s(t) = e + k_s\dot{e}$ is the sliding surface; thus, it can be represented as a piecewise linear function of the state as given by Equation (6):

$$s(x(kT)) = \begin{cases} s_1(kT) + (t-kT)\dot{s}_+ & \text{if } kT \le t \le kT + dT/2 \\ s_2(kT) + (t-kT-dT/2)\dot{s}_- & \text{if } kT + \frac{dT}{2} \le t \le kT + T - dT/2 \\ s_3(kT) + (t-kT-T+dT/2)\dot{s}_+ & \text{if } kT + T - \frac{dT}{2} \le t \le (k+1)T \end{cases}, \tag{6}$$

where

$$\dot{s}_+ = \left(\dot{x}_1 + k_s\ddot{x}_1\right)\Big|_{x=x(kT),\ \text{S=ON}}, \dot{s}_- = \left(\dot{x}_1 + k_s\ddot{x}_1\right)\Big|_{x=x(kT),\ \text{S=OFF}}, s_1(kT) = x_1 - x_{1ref} + k_s\left(\dot{x}_1 - \dot{x}_{1ref}\right)\Big|_{x=x(kT),\ \text{S=ON}}, s_2(kT) = \tag{7}$$

In this paper, $\dot{x}_{1ref}$ is assumed to be zero. During a complete sampling period, as shown in Figure 3, the slopes are calculated from the values of the state variables at the instant of sampling $t = kT$ as shown in Equations (6) and (7). The slopes are then used to compute the duty cycle to be applied in the next control iteration.

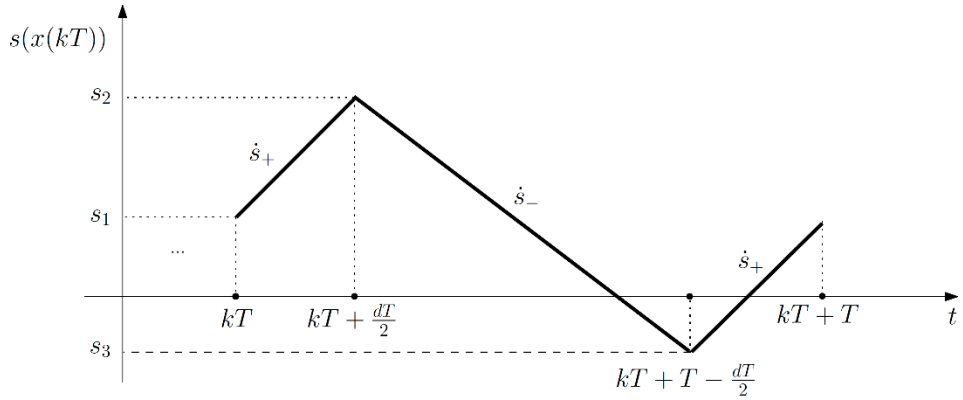


Figure 3. Piecewise description of the sliding surface in a complete period considering the commutation events generated by a CPWM signal of duty cycle d and period T.

In this equation, $k_s = K_s\sqrt{LC}$, consider that K_s is a constant of the ZAD. Thus, the mathematical description for the condition of zero average dynamics is given by Equation (8). Herein, the first and third slopes in Figure 3 have the same values, and to build the piecewise function $s(x(kT))$ it is necessary to obtain information from the state values x_1 and x_2 at instant kT :

$$\int_{kT}^{(k+1)T} s(x(kT))dt = 0. \tag{8}$$

Equation (8) is solved to obtain the duty cycle d_k at each sampling time, which ensures the condition of zero average dynamics when applied to the system through switch S. The duty cycle was obtained in refs. [8,22] and can be expressed by Equation (9):

$$d_k = \frac{2s_1(kT) + T\dot{s}_-(kT)}{T(\dot{s}_-(kT) - \dot{s}_+(kT)}. \tag{9}$$

In the experimental test, the state variables are measured to calculate the CPWM with a sampling frequency of 10 kHz and a one-period delay. Thus, the duty cycle used experimentally is given by Equation (10), which means that the actual control law in the current period k is calculated with the values of state variables measured at the previous iteration $(k-1)$; therefore, instantaneous application is not possible:

$$d_k = \frac{2s_1((k-1)T) + T\dot{s}_-((k-1)T)}{T(\dot{s}_-((k-1)T) - \dot{s}_+((k-1)T)}. \tag{10}$$

2.3. FPIC Technique

This control technique was proposed in ref. [25], numerically tested in ref. [26], and experimentally tested in ref. [8]. Then, the ZAD-FPIC technique applied to the buck converter obtains a new duty cycle expression as shown in Equation (11):

$$d_{ZAD-FPIC} = \frac{d_k + Nd^*}{N+1}. \tag{11}$$

Herein, N is the control parameter of the FPIC, the term d_k is obtained from (10), and d^* can be calculated at the beginning of each period as in Equation (12); then, Equation (13) is obtained:

$$d^* = d_k|_{steady\ state}, \tag{12}$$

$$d^* = \left[\frac{x_{1ref}\left(1 + \frac{r_{Med}+r_L}{R}\right) + V_{fd}}{-x_{1ref}\left(\frac{r_s+r_M}{R}\right) + E_{sensed} + V_{fd}} \right]. \tag{13}$$

Assuming a duty cycle greater than zero and less than 1, a saturation function given by Equation (14) is applied; therefore, the expression of the duty cycle for the ZAD-FPIC controlled system is as Equation (14). A complete description on the ZAD-FPIC technique can be found in refs. [26,27]:

$$d = \begin{cases} d_{ZAD-FPIC} & if\ 0 < d_{ZAD-FPIC} < 1 \\ 1 & if\ 1 < d_{ZAD-FPIC} \\ 0 & if\ d_{ZAD-FPIC} \leq 0 \end{cases}. \tag{14}$$

2.4. Parasitic Resistance (or Loss) Estimator

This subsection addresses the problem of parameter uncertainty and proposes a solution to improve the control technique by including a parameters estimation function. In particular, attention is focused on the estimation of parasitic resistances, which are included in the model equations used by the control strategy. In so doing, computation of the duty cycle is improved as well as the control performance.

An online loss estimator is designed and tested in order to have an accurate estimate of losses in the elements of the buck converter. In this case, the RLS estimation method [28] is used to design the loss estimator. When the switch is ON, the system operates as described in Equation (1) and all losses are estimated from the remaining series circuit. Additionally, the variables must be sensed once the switch is ON and the time is a multiple of kT. Thus, the inductor current dynamics is given by:

$$\frac{di_L(t)}{dt} = -\frac{1}{L}v_c(t) - \frac{r_s + r_M + r_{Med} + r_L}{L}i_L(t) + \frac{E}{L}. \tag{15}$$

Let us introduce $r_p = r_s + r_M + r_{Med} + r_L$ as the total resistance parameter. By applying first-order Euler discretization method to Equation (16) at the k-th sampling period, the following discrete expression is obtained:

$$i_L(\mathrm{k}) - i_L(\mathrm{k}-1) = T_s\left[-\frac{1}{L}v_c(\mathrm{k}) - \frac{r_p}{L}i_L(\mathrm{k}) + \frac{E(k)}{L}\right], \tag{16}$$

where T_s is the digital controller sampling period. Organizing the expression (16), a new equation is obtained as presented in Equation (17), which has been arranged to have the standard form $F = \phi^T\theta$,

which is useful to apply the RLS algorithm [28]. Here, θ is the unknown scalar parameter to be identified, which corresponds to a combined resistance in series:

$$\underbrace{\frac{T_s E(k)}{L} - \frac{T_s v_c(k)}{L} - i_L(k) + i_L(k-1)}_{F} = \underbrace{\frac{T_s}{L} i_L(\mathrm{k})}_{\phi^T} \underbrace{r_p}_{\theta}. \tag{17}$$

The recursive algorithm to obtain the estimated $\hat{\theta}$ of parameter θ is described in Appendix A [28]. Moreover, applying the first-order Euler integration method, the recursive equation to estimate θ is given by:

$$\hat{\theta}(\mathrm{k}) = \hat{\theta}(k-1) + \gamma\phi(\mathrm{k})\Big[F(k) - \phi^T(\mathrm{k}-1)\hat{\theta}(\mathrm{k}-1)\Big], \hat{\theta}(1) = \theta_0, \quad k = 1,\ 2,\ 3, \ldots \mathrm{n}, \tag{18}$$

where the term γ is a constant that defines the convergence velocity of the estimator [28] and θ_0 is the initial (nominal) value for estimated parameter. Replacing the terms from Equation (17) into Equation (18), the recursive estimation of parameter r_p is given by:

$$\hat{r_p}(\mathrm{k}) = \hat{r_p}(k-1) + \gamma\phi(\mathrm{k})\Big[F(k-1) - \phi^T(\mathrm{k}-1)\hat{r_p}(\mathrm{k}-1)\Big], \hat{r_p}(1) = r_{p0}, \tag{19}$$

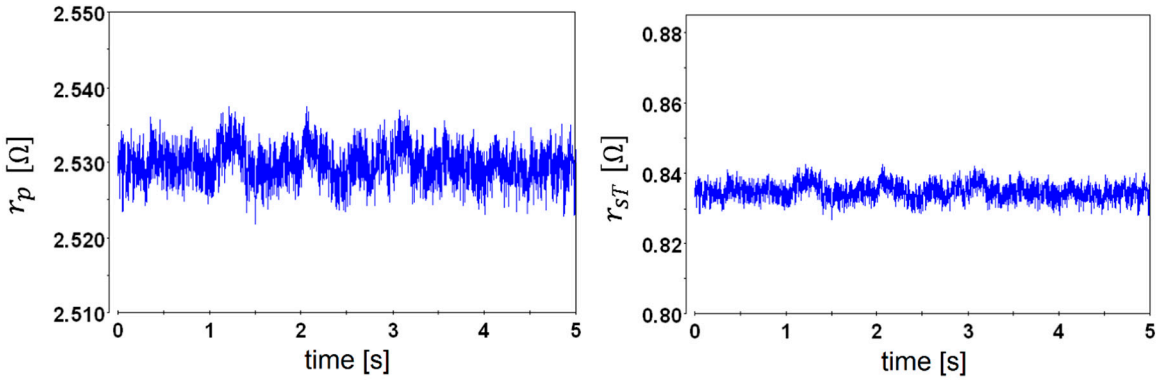
with

$$\phi(\mathrm{k}) = \frac{T_s}{L} i_L(\mathrm{k}), \tag{20}$$

$$F(k) = \frac{T_s E(k)}{L} - \frac{T_s v_c(k)}{L} - i_L(k) - i_L(k-1), \tag{21}$$

$$\phi^T(\mathrm{k}-1) = \frac{T_s}{L} i_L(\mathrm{k}-1). \tag{22}$$

Implementing the estimator in the Simulink-MATLAB software, the total parasitic resistance was measured and expressed as r_p in Figure 4a. Now, the total resistance in the inductor and current measurement is $r_{LT} = r_{Med} + r_L = 1.695\ \Omega$ and the total resistance in the MOSFET and source is $r_{sT} = r_s + r_M = 0.84\ \Omega$ as shown in Figure 4b.



(**a**) Total loss estimator r_p (**b**) Loss estimation in the source r_{sT}

Figure 4. Experimental results of total loss estimator r_p and loss estimation in the source r_{sT}.

2.5. Load Estimator

Finally, in order to further improve the performance of the controller, a load estimator is included in the system.

The RLS estimation [28] method was also used to design the load estimator. From Equation (1), the voltage capacitor equation is given by:

$$\dot{v}_c = \frac{-1}{RC} v_c + \frac{1}{C} i_L. \tag{23}$$

By applying the first-order Euler discretization method to Equation (23) at the k-th sampling period, the following discrete expression is obtained:

$$v_c(\mathrm{k}) - v_c(\mathrm{k}-1) = T_s\Big[-\frac{1}{RC} v_c(\mathrm{k}) + \frac{1}{C} i_L(\mathrm{k})\Big], \tag{24}$$

which can be written in the form:

$$\underbrace{T_s i_L(k) + C v_c(k-1) - C v_c(k)}_{F(k)} = \underbrace{T_s v_c(k)}_{\phi^T(k)} \underbrace{\frac{1}{R}}_{\theta(\mathrm{k})}. \tag{25}$$

Applying the same method as the previous section and considering that the parameter R is the inverse of θ, the recursive estimation of the parameter $\hat{R}(k)$ is given by [28]:

$$\hat{R}(k) = \frac{1}{\hat{\theta}(k)}, \tag{26}$$

$$\hat{\theta}(k) = \hat{\theta}(k-1) + \gamma\phi(\mathrm{k})\Big[F(k-1) - \phi^T(\mathrm{k}-1)\hat{\theta}(\mathrm{k}-1)\Big],\ \hat{\theta}(1) = \theta_0,$$

where the estimated load R is calculated as $\hat{R}(k) = \frac{1}{\hat{\theta}(k)}$ and γ is a constant similar to in the previous section.

2.6. Hardware Development

Figure 5 shows the block diagram of the implementation and control of the system with ZAD-FPIC. The blocks on the left side are implemented using dsPACE technology (Paderborn, Germany), in particular, the digital implementation of proposed control strategy is developed in the DS1104 board, while the blocks on the right side include the system hardware. The digital part implemented in the DS1104 board performs the following tasks: acquires signals; converts them from analog to digital; executes the control strategy at each iteration; calculates the duty cycle and generates CPWM signals. The output signal is sent to the opto-coupling circuit, which enables/disables the MOSFET power transistor, to finally feed the Buck Converter. The output signals of the circuit are measured and conditioned by a proper circuit.

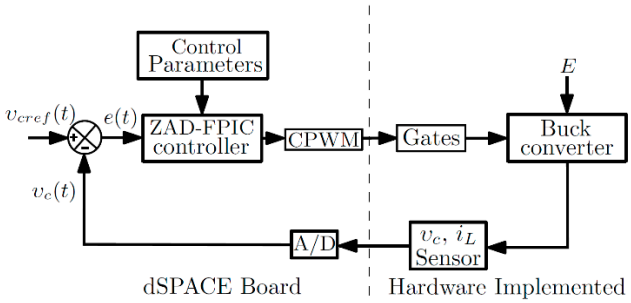


Figure 5. Block diagram of the implementation and control of the system with ZAD-FPIC.

Figure 6 shows the hardware implemented to control the converter using the ZAD-FPIC. The implemented triggering circuit is shown to control the ON and OFF states of the IRFP350 MOSFET that acts as a switch for the power converter. This circuit is designed to work up to 100 kHz

switching frequencies and the CPWM can be configured. Through the use of an HCP-J312 optocoupler, high-frequency isolation is achieved with good switching and response time characteristics.

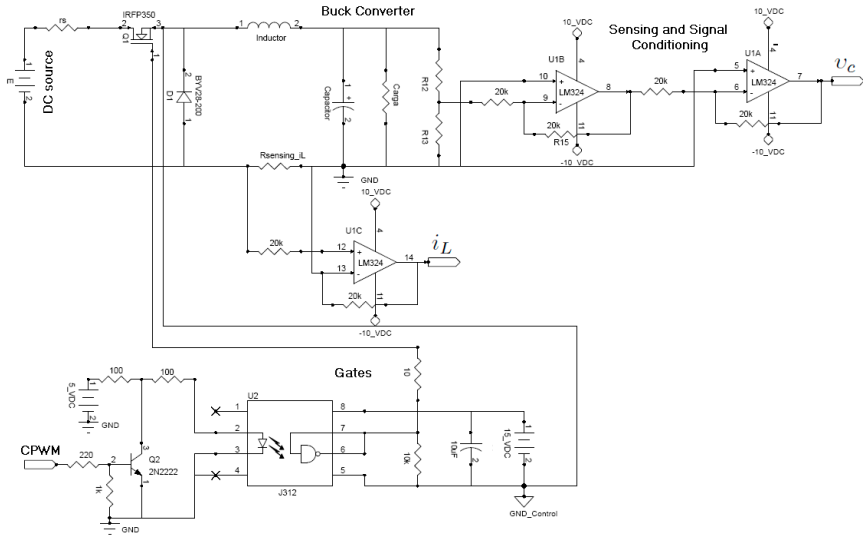


Figure 6. Hardware implemented for the analogic circuit.

2.7. Electric Circuit

The buck converter was implemented with the elements shown in Figure 7. The power supply is fully regulated and consists of a switched source used for laboratory practices with the possibility of having a variable voltage from 0 to 60 volts with a current up to 6 A. The fact that the power supply used in this work is regulated does not imply that this requirement is met in the actual application. In ref. [29], it was shown experimentally that when using an unregulated power supply, the regulation error was the same as with a regulated source and this was less than 1% in both cases. This occurred due to the FPIC control that includes the value of the source. The DC source and switch on the left have an internal resistance r_s = 0.3887 Ω, which was measured in the laboratory by considering full-load and open-circuit tests.

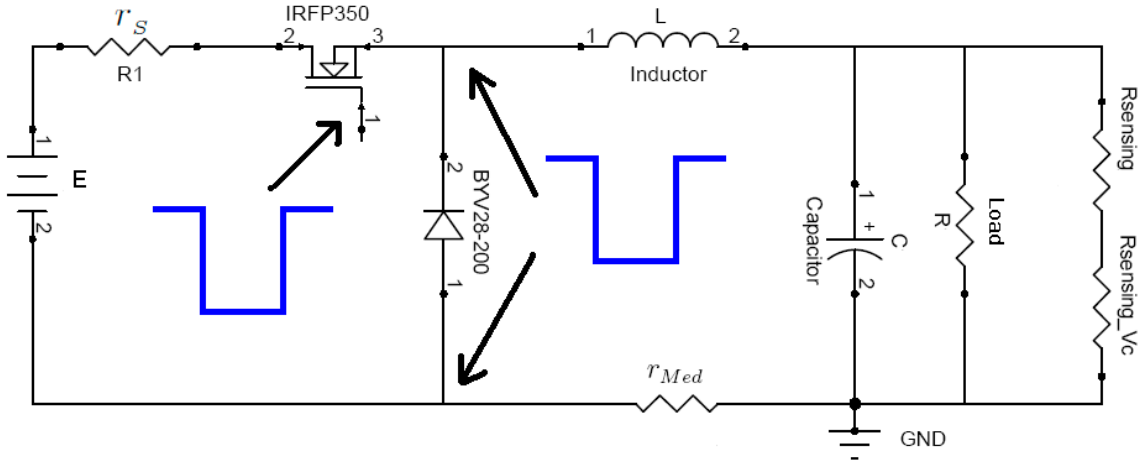


Figure 7. Electric circuit of the buck converter.

In series with the source a switch is connected that operates to the desired frequency (for this application, 10 kHz). This device is the IRFP350 MOSFET, which has an internal resistance of r_M = 0.3 Ω taken from the data reported in ref. [30]. In addition, it has the switching and response time characteristics given in Table 2, taken from ref. [30], where it can be seen that it also meets the required specifications.

Table 2. Commutation time of the solid-state switch (N-channel MOSFET) and optocoupler.

Device	Symbol	Definition	Type	Units
Switch IFRP350	t_{on}	Turn-on delay time	0.8	ns
	t_{off}	Turn-off delay time	0.6	ns
	t_r	Rise time	0.1	µs
	t_f	Fall time	0.1	µs
Optocoupler HCP-J312	t_{on}	Turn-on delay time	16	ns
	t_{off}	Turn-off delay time	87	ns
	t_r	Rise time	49	ns
	t_f	Fall time	47	ns

The diode will conduct when there is a positive current in the coil and the transistor is OFF. This diode (BYV28-200) is of the ultra-fast recovery type (30 ns) and is used in applications of very fast rectification as is the case of switched power sources. The inductor was built in the laboratory and has several advantages. Because it has a ferrite core, it is able to work in the range of a few Hz up to 100 kHz. It has 10 taps, which allows it to obtain 45 values of inductance ranging from 1 mH to 74.21 mH with a current of up to 3 A. The capacitor used is one of the electrolytic type. The load connected is a resistive load and was built in the laboratory; it is composed of 24 resistance of 10 Ω connected two in parallel and then placed in series, in such a way that different resistance values can be obtained with values from 4.863 Ω to 58.641 Ω with the power dissipation shown in Table 3.

Table 3. Possible values for the resistive load.

R (Ω)	P (W)	R (Ω)	P (W)	R (Ω)	P (W)
4.8630	40	24.404	200	43.888	360
9.7340	80	29.326	240	48.782	400
14.591	120	34.200	280	53.708	440
19.447	160	39.092	320	58.641	480

2.8. Sensing and Adequation of Signals

Because there are voltage signals in the load greater than 10 V and the current and voltage signals are disturbed by electromagnetic interferences caused by the switching of the transistor [31], two circuits were implemented as shown in Figure 8. Then, the signals were adapted in order to acquire them through the analog-to-digital conversion devices of the DS1104 board (ADC converters).

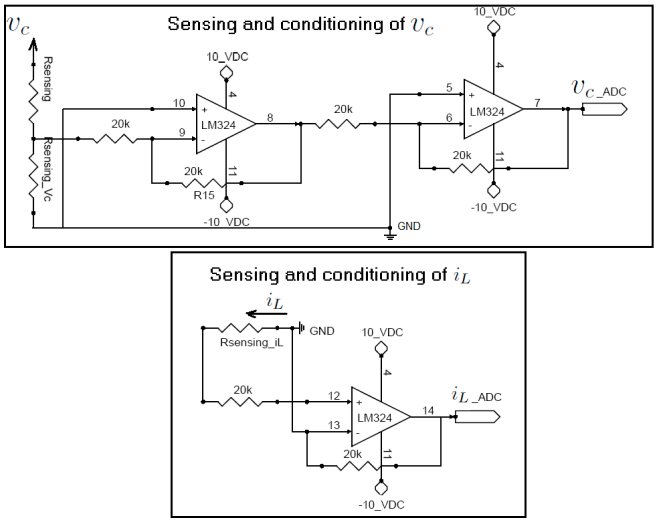


Figure 8. Sensing and adaptation of analog signals.

To sense the voltage, a resistive divider was used in which the voltage signal at the output is attenuated by the gain av. The resistors used to sense voltage (Rsensing and Rsensing_*Vc*) have high values compared with the load resistance to minimally alter the dynamics of the system and are also precision resistances. Because this voltage signal is carried to the DS1104 by one of its analog/digital inputs, it is necessary that the voltage value av v_c does not exceed the value of +10 volts because it is the maximum range allowed by the ADC inputs of the DS1104. To ensure that they do not exceed this voltage value, it is necessary to pass the analog signals through a buffer amplifier with operations supplied with ±10 V.

To sense the current, a resistor in series of 1.007 Ω is used from which the value of its voltage drop is taken as the value of the current i_L. This resistor is composed of four resistors of 10 W in order to avoid heating and errors in the measurements. The signal was adapted as shown in Figure 9 in order to remove the radiated and driven noise present due to commutation [31]. These voltage and current signals are carried by shielded cable to the ADCHx inputs as shown in Figure 9, because in practice it was found that by switching the MOSFET there is radiated and conducted noise that adds to the real signals [31,32]. For this reason, it was ensured that these signals were fully shielded from the output of the sensors to the inputs of the DS1104 with the configuration shown in Figure 9.

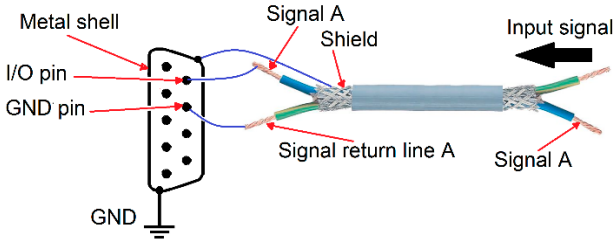


Figure 9. Shielding of signals sensitive to noise [33].

2.9. Software Development

Simulink is an environment for multi-domain simulation and is designed based on models for dynamic and embedded systems. It provides an interactive graphic environment and a set of block libraries that allows designing, simulating, implementing, and testing a wide variety of linear and non-linear systems in continuous or discrete time or a hybrid of the two, and it even works with different time sampling [34]. The system under study, which includes the buck converter controlled with the control technique ZAD-FPIC, forms a non-linear system because there are two topologies for each sampling period; it is also a hybrid because it has to work in continuous and discrete time.

The DS1104 board is used to control the system and allow implementation of a rapid control prototype (RCP) because the hardware has a power PC microprocessor with I/O interfaces [33]. The DS1104 is programmed in the Simulink-MATLAB platform with an interface that captures and visualizes the sensed and processed signals. ControlDesk was the tool used in this work to capture and store signals taken from the physical system.

2.10. Acquisition, Synchronization, and Interruption

For implementation of the ZAD-FPIC control technique, it is necessary to know some values of constant parameters such as L, C, r_s, r_{Med}, r_M, r_L, F_s, F_C, K_s, and N. In addition, the values of voltage in the capacitor (v_c) and current in the inductor (i_L) are also considered for sampling. The values of the parameters are measured from the electrical circuit and placed in the respective inputs of Figure 10.

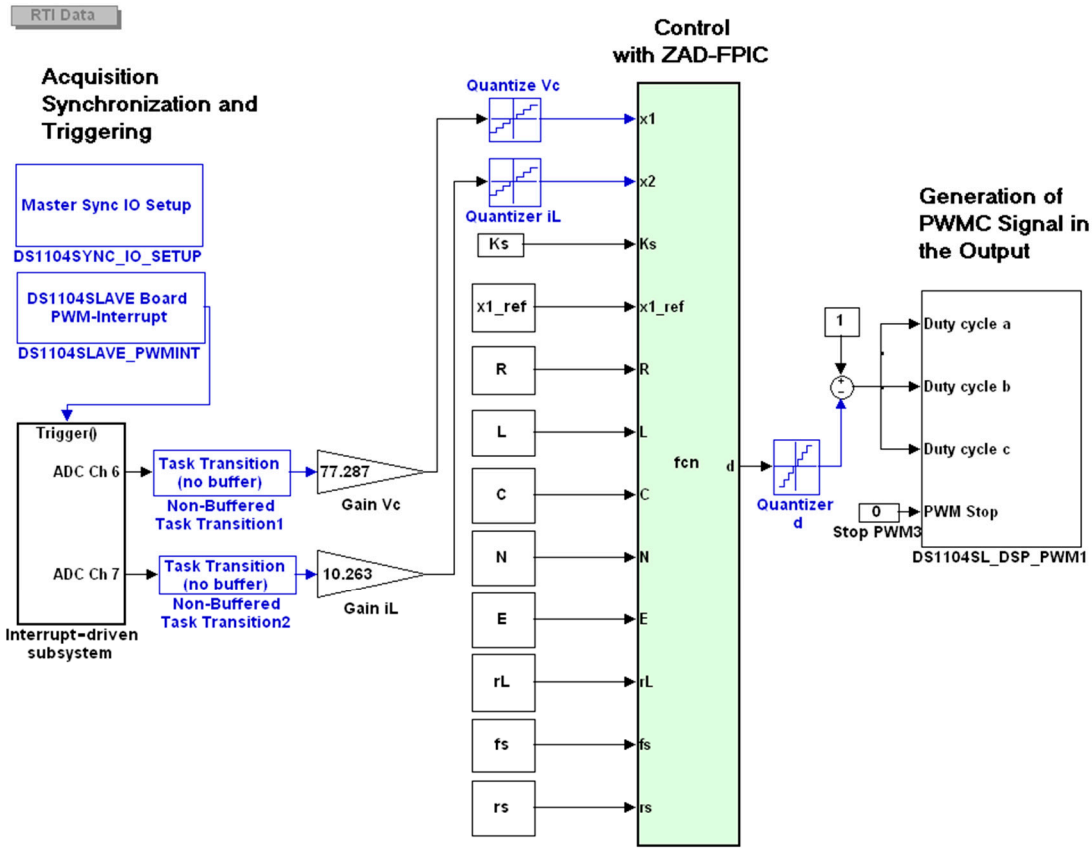


Figure 10. Software developed in Simulink to control the buck converter.

Measurement of the state variables v_c and i_L is carried out by means of a block DS1104 Slave Board PWM-Interrupt whereby an interruption is configured with a trigger signal provided by the Master Sync I/O setup, which is triggered at the beginning of the generation of each signal CPWM. The Master Sync I/O setup block is configured to synchronize the acquisition and processes with the trigger signal. Then, through proportional gains, the v_c and i_L signals are amplified to obtain the correct voltage and current values needed to execute the control technique.

2.11. Control with ZAD-FPIC

Implementation of the ZAD-FPIC control technique was performed using the embedded MATLAB function block from Simulink. The control block is shown in Figure 10. This block considers the values of the constant parameters and the state variables of the real system, with which the duty cycle defined by the corresponding Equations (11) and (13) is calculated.

In practice, it is necessary to limit the duty cycle (d) obtained by applying the corresponding Equation (14) so that if the cycle is above 1, then it is necessary to saturate it to 1 and if it is below 0, then it is necessary to adjust it to zero.

2.12. Generation of CPWM in the Output

Using the configuration shown in the right part of Figure 10, the same duty cycle is entered into the three inputs of the CPWM generation block in order to have only one CPWM output and its inverted CPWM signal (CPWMinv). The outputs CPWM and CPWMinv have the following characteristics among many others: they are complementary, centered, of constant switching frequency in the range of 1.25 Hz to 5 MHz, they are signals of the TTL type, they are protected by a dead time (deadband), and their initiation mode and its stop time are controllable. Figure 11 shows that CH1 is the CPWM output, CH3 is the CPWMinv, and CH2 corresponds to the duty cycle d and changes proportionally with time.

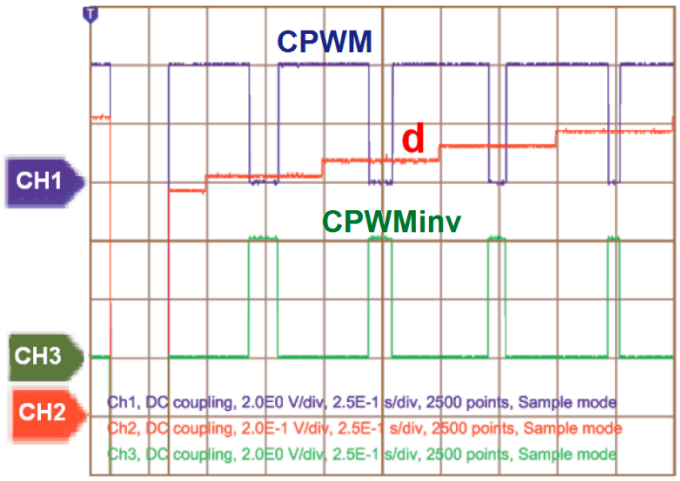


Figure 11. Outputs CPWM and CPWMinv controlled with *d* with one delay period (1Tp).

When performing sampling synchronization via the ADC channels with a trigger signal obtained from the digital PWM output, a one-delay period (1Tp) is presented. This phenomenon is illustrated in Figure 12, which shows the following signals: the signal generated CPWM in blue (CH1); the duty cycle (green signal), which corresponds to a sawtooth signal produced by a signal generator; and the signal (sampled) (CH4) that corresponds to the duty cycle sampled at a frequency given by the trigger signal (CH2) for, in this case, 10 kHz.

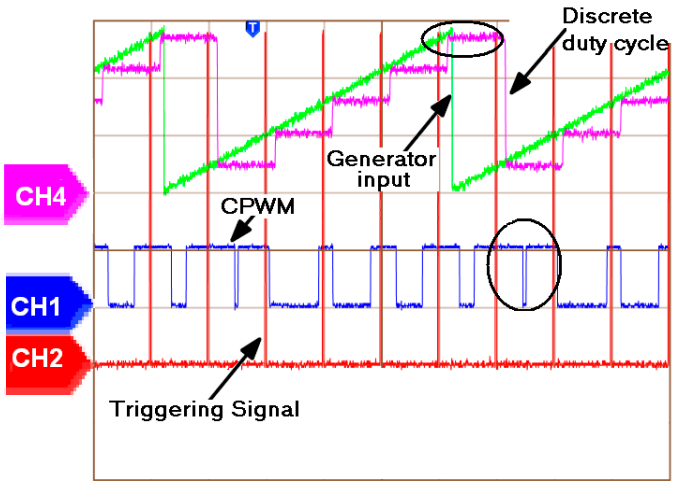


Figure 12. Generation of the CPWM signal with one delay period (1Tp).

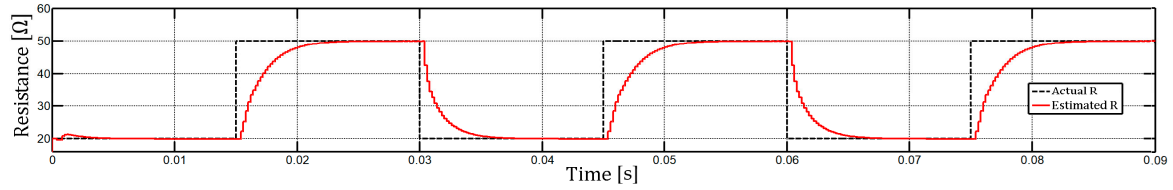
Thus, Figure 12 shows clearly that when sampling an external signal (Generator Input) at a given switching frequency, and with it generating the CPWM pulse train, a full delay period is presented (1Tp). Therefore, in the rest of the document, all results, both numerical and experimental, are made, taking into account that the time required to sense a signal and then execute the control action is equal to one sampling period (1Tp). This means that there is a delay period equal to the inverse of the switching frequency in all signals sensed at the input. The main consequence of having a delay period is the presence of chaos and instability in the controlled system with only the ZAD control technique, which was demonstrated in refs. [29,35]. Therefore, chaos and instability are controlled with the FPIC control technique [35]. That is why in the rest of the document the system is controlled with the ZAD-FPIC control technique.

3. Results

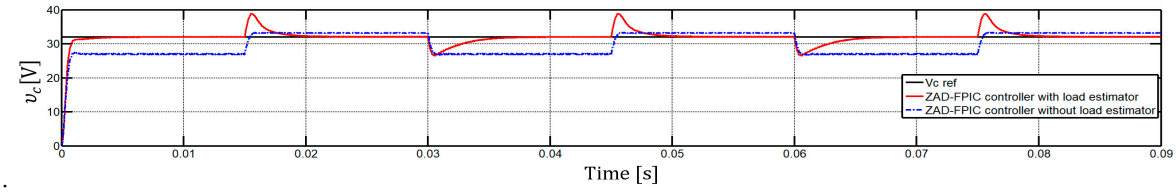
Table 4 shows the parameters obtained with an exact measurement to perform the simulation and experimental tests according to the losses and load estimations performed in Sections 2.4 and 2.5.

To show the advantages of the ZAD-FPIC with the RLS method over the conventional ZAD-FPIC, the behaviors of the two controllers are presented with variations in the load. Figures 13 and 14 illustrate the simulation for cases of the circuit with and without the estimator when the load varies from $R = 20\ \Omega$ to $R = 50\ \Omega$, and from $R = 30\ \Omega$ to $R = 150\ \Omega$, respectively. From Figures 13a and 14a, it can be seen that the controlled variable v_c for the ZAD-FPIC controller without the load estimator has a greater overshoot and a longer establishing time than the controller without the load estimator because the RLS method has a delay time for high-speed changes signals.

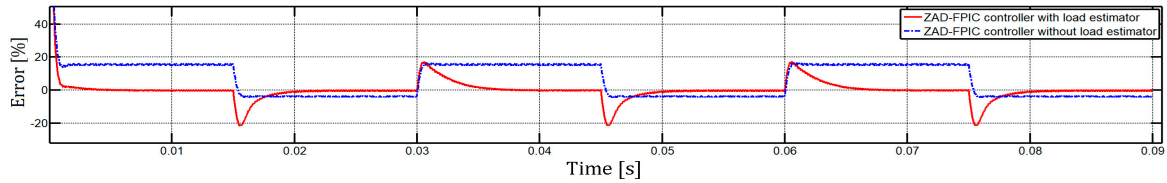
Table 5 shows the steady-state error for the controlled voltage v_c for both ZAD-FPIC with and without load estimator. From Figures 13a and 14a, it is concluded that when the load estimator R is used, the system presents less steady-state error for the different values of the load resistance. When ZAD-FPIC with load estimator is used, it is observed that the error increases directly with the increase in the load resistance. This is because the estimated resistance for large values of R does not reach the current resistance value. When ZAD-FPIC without load estimator is used, it is observed that the error tends to be greater at lower and higher resistance values because the controller parameters required a constant resistance value of 40 Ω; therefore, for values close to 40 Ω, the error tends to be smaller.



(**a**) Actual and estimated resistance R in the simulation

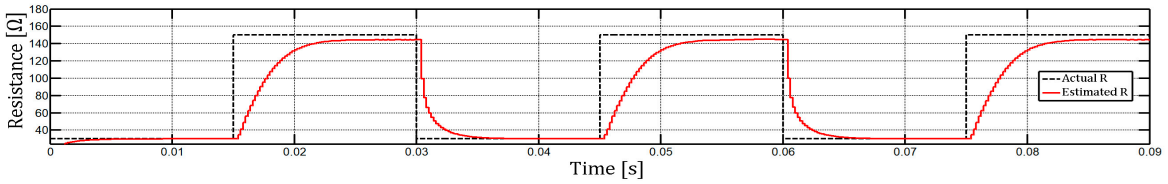


(**b**) v_c controlled voltage signal

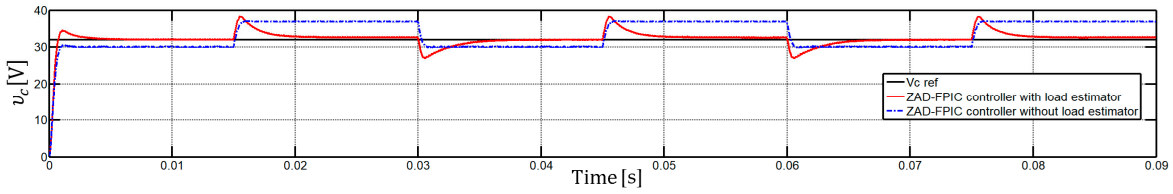


(**c**) Error in the controlled voltage signal

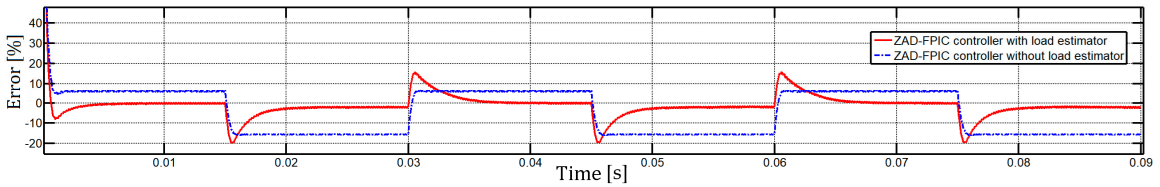
Figure 13. Simulation results to show the comparison of both controller when considering R variations, $R = [20,\ 50]\ \Omega$.



(**a**) Actual and estimated resistance R in the simulation



(**b**) v_c controlled voltage signal



(**c**) Error in the controlled voltage signal

Figure 14. Simulation results to show the comparison of both controller when considering R variations, $R = [30, 150]\ \Omega$.

Table 4. New parameters for the buck converter and the controller according to the loss estimation.

Parameter	Description	Value
x_{1ref}	Reference voltage	32 V
E	Input voltage	40.086 V
R	Resistance of the load	Variable
C	Capacitance	46.27 µF
L	Inductance	2.473 mH
r_{LT}	Total resistance in the inductor and current measurement	1.695 Ω
r_{sT}	Total resistance of the MOSFET and source	0.84 Ω
V_{fd}	Polarizing voltage of the diode	1.1 V
N	Control parameter of FPIC	1
K_s	Bifurcation parameter	5
F_C	Switching frequency	10 kHz
F_s	Sampling frequency	10 kHz
T_s	Digital controller sampling period	10 kHz
1Tp	One-delay period	100 µs
bits ADC	Number of bits ADC	12 bits
bits d	Number of bits of duty cycle	10 bits

Table 5. Error in the controlled signal.

Controller	20 Ω	30 Ω	50 Ω	150 Ω
ZAD-FPIC with load estimator	0.1%	0.2%	0.4%	2.5%
ZAD-FPIC without load estimator	18%	7%	3%	16%

To validate the performance of the parameter estimation approach with simulation and experimental tests, instantaneous load changes are made in order to test the estimator of R. Table 6 shows the times and the load connected to the converter to test the estimator with $\gamma = 1$. The parameters of the converter and controller are shown in Table 4 and the control parameters are fixed as $N = 1$ and $K_S = 5$. The switching and sampling frequencies are assigned at 10 kHz. The results are shown in Figures 15 and 16.

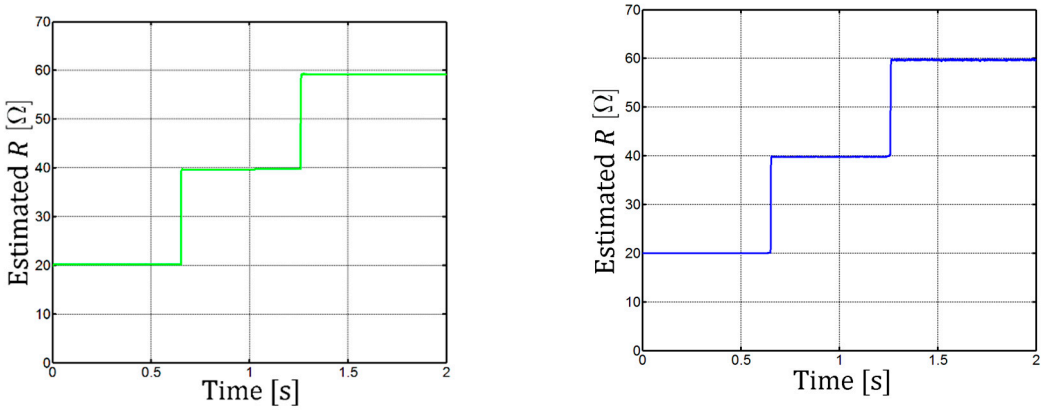
Figure 15e,f show that the ZAD-FPIC controller regulates the output voltage v_c well, with errors below 2%. Regarding the duty cycle in both the numerical and experimental tests (Figure 15g,h, respectively), it can be seen that it is not saturated; therefore, the system has fixed computation frequency in both cases.

Table 7 shows the numerical and experimental errors when using the ZAD-FPIC controller without load estimator. From the experimental results it is observed that for smaller values of the load resistance, the error tends to increase because there are losses in the experimental circuit and these still need to be estimated.

Figure 16 shows the behavior of the system when irregular changes in the load are presented. After large changes in the load, the output voltage remains close to the reference value $x_{1ref} = 32$ V. It is observed that the system is stable to changes in the load. The voltage v_c remains fixed while the current i_L varies considerably and, in all cases, the error is less than 2%. Finally, in Figure 16g,h, it is observed that for the positive and negative growth of the load resistance the system regulates the controlled signal v_c well and presents low steady-state error.

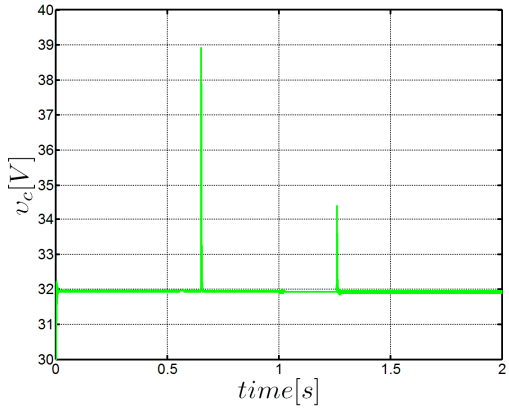
Table 6. Changes in the load R.

Range of Time (s)	R
(0.4, 0.6515)	20 Ω
(0.6515, 1.2598)	39.8 Ω
(1.2598, 1.6)	59.7 Ω

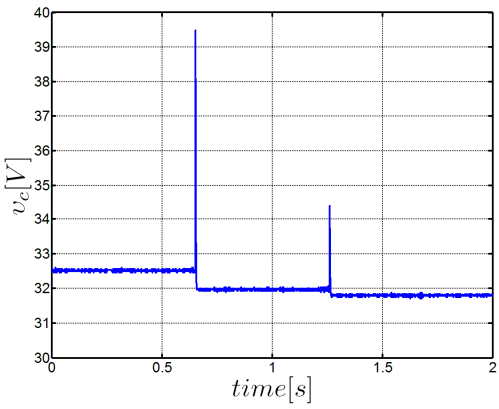


(**a**) R estimated in the simulation (**b**) R estimated in the experiment

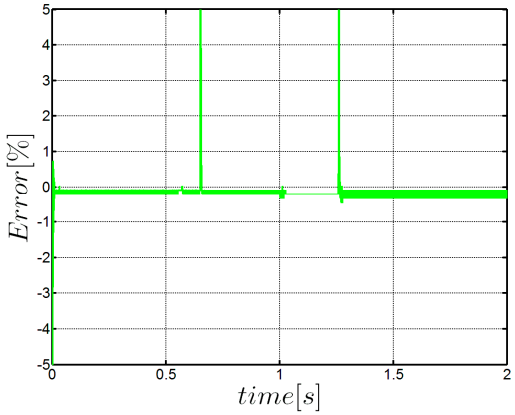
Figure 15. *Cont.*



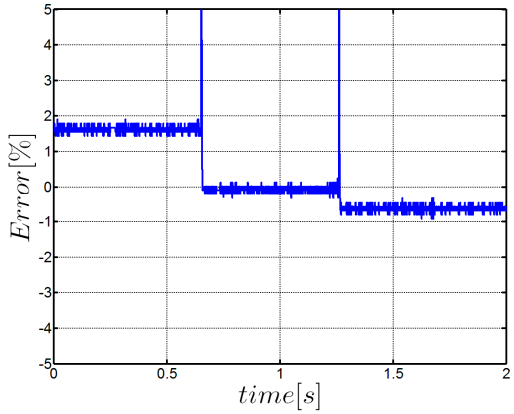
(**c**) v_c in the simulation



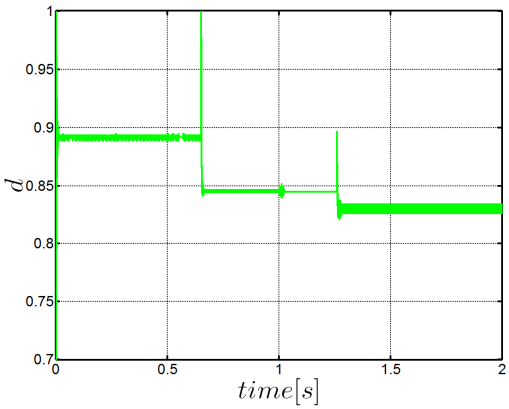
(**d**) v_c in the experiment



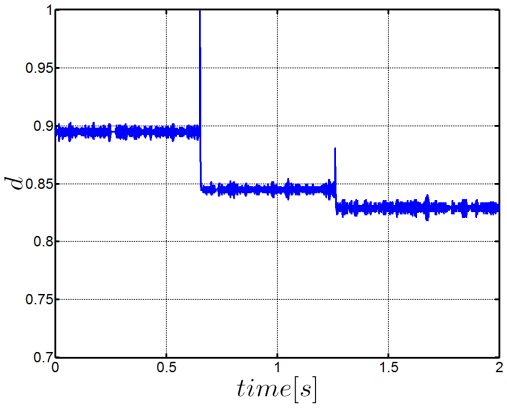
(**e**) Error in the simulation



(**f**) Error in the experiment

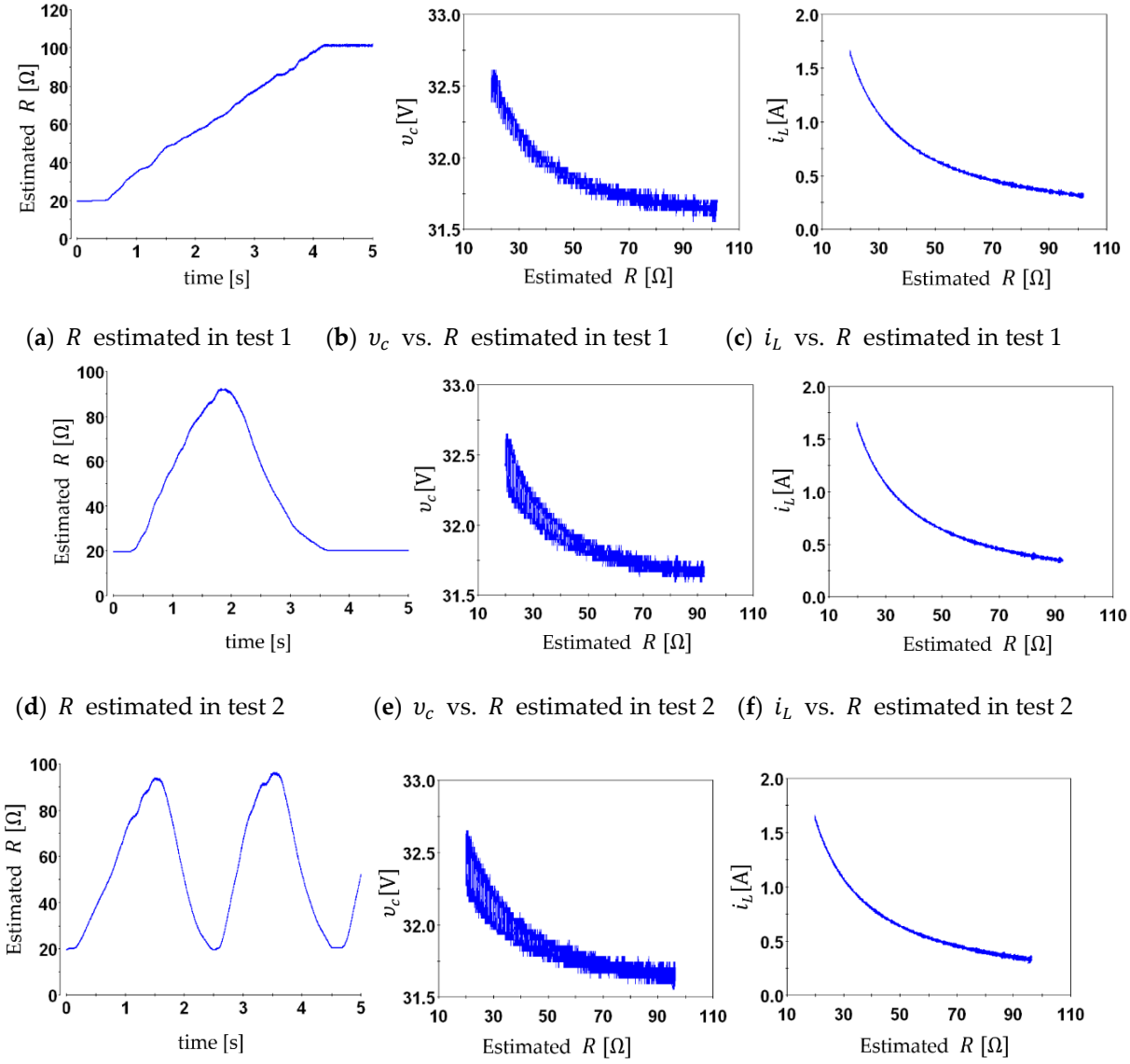


(**g**) d in the simulation



(**h**) d in the experiment

Figure 15. Behavior of the load estimator R when the values change according to Table 4 for the buck converter controlled by ZAD-FPIC without load estimator, one delay period, $K_s = 5$, $N = 1$, and $\gamma = 1$.



(**a**) R estimated in test 1 (**b**) v_c vs. R estimated in test 1 (**c**) i_L vs. R estimated in test 1

(**d**) R estimated in test 2 (**e**) v_c vs. R estimated in test 2 (**f**) i_L vs. R estimated in test 2

(**g**) R estimated in test 3 (**h**) v_c vs. R estimated in test 3 (**i**) i_L vs. R estimated in test 3

Figure 16. Behavior of the load estimator load R in the experimental test when the load changes for the buck converter controlled with ZAD-FPIC, with one-delay period, $K_s = 5$, $N = 1$, and $\gamma = 1$.

Table 7. Error in the controlled signal.

ZAD-FPIC without Load Estimator	20 Ω	40 Ω	60 Ω
Simulation	0.1%	0.2%	0.3%
Experimental	1.7%	0.2%	0.8%

4. Conclusions

This paper presented the development of a buck converter controlled with a quasi-sliding mode control combined with a loss estimator function to compensate internal losses in the buck converter. Detailed electric and electronic circuits were presented that describe the triggering of the power transistor (N-Channel MOSFET IRFP350) and shielding of wires for reduction of electromagnetic interference to measure voltage and current signals in the capacitor and inductor, respectively. The digital controller is implemented in real time using dSPACE technology (DS1104 board) to manage properly the digital and

analogic signals that drive the power system. A detailed description was presented to build the PWM signal with pulse at the center and to ensure proper synchronization in the real-time implementation. In so doing, signals from the buck converter are sampled at each period of time, avoiding measurement uncertainties when sampling on the Poincarè surface. Experimental results showed the effectiveness of the experimental implementation and, of course, the good performance of the model-based control law with loss estimator function to compensate internal losses in the buck converter.

The same control methodology presented in this paper can be applied to other power converters such as the boost and buck boost. For both cases, it is necessary to write the mathematical models to compute the duty cycle. Additionally, for both cases, a suitable regression method can be identified to estimate the unknown parameters and implement them in real-time to obtain the parameters separately, which will avoid problems with estimator convergence. It was verified numerically that the RLS method does not measure parameters that present high-speed changes. Additionally, it was observed that for lower load resistance, values of the steady-state error increase because it is possible to have parameters in the circuit that still have not been modeled. In the experimental results, it was observed that for smaller values of the load resistance, the error tends to increase because some power losses still require to be estimated.

Author Contributions: C.I.H.V. contributed to control design and estimator design, control strategy implementation, and data analysis; J.E.C.-B. reviewed the theory, performed simulations, and analyzed the data; and F.E.H. conceived the theory, wrote the manuscript, performed the experiments, and developed the data analysis.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

ADC	Analog-to-digital converter
CPWM	Centered pulse width modulation
CPWMinv	Inverted CPWM signal
DC	Direct current
FPIC	Fixed point induction control
LMS	Least mean squares
MOSFET	Metal–oxide–semiconductor field-effect transistor
PID	Proportional integral derivative
PMDC	Permanent magnet DC motor
PWM	Pulse-width modulation
RCP	Rapid control prototyping
RLS	Recursive least squares method
SMC	Sliding mode control
ZAD	Zero average dynamics

Notation

1Tp	One-delay period
C	Capacitance
D	Diode
d	Duty cycle
d^*	Duty cycle calculated with FPIC

$d_{ZAD-FPIC}$	Duty cycle calculated with ZAD-FPIC
E	Input voltage
F_C	Switching frequency
F_s	Sampling frequency
i_L	Current in the inductor
K_s	Control parameter of the ZAD
L	Inductance
N	Control parameter of the FPIC
R	Resistance of the load
r_L	Resistance in the inductor
r_{LT}	Total resistance in the inductor and current measurement
r_M	Internal MOSFET resistance
r_{Med}	Resistance used to measure current
r_s	Internal resistance of the source
r_{sT}	Total resistance of the MOSFET and the source
S	Switch of the circuit
T	Sampling period
t_f	Fall time
t_{off}	Turn-off delay time
t_{on}	Turn-on delay time
t_r	Rise time
u	Output signal of the controller
v_c	Capacitor voltage and output voltage of the circuit
v_{cref}	Voltage reference
V_{fd}	Polarizing voltage of the diode
x_1	Capacitor voltage
x_2	Inductor current

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