

Article

A Highly Selective and Compact Bandpass Filter with a Circular Spiral Inductor and an Embedded Capacitor Structure Using an Integrated Passive Device Technology on a GaAs Substrate

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Abstract: As one of the most commonly used devices in microwave systems, bandpass filters (BPFs) directly affect the performance of these systems. Among the processes for manufacturing filters, integrated passive device (IPD) technology provides high practicality and accuracy. Thus, to comply with latest development trends, a resonator-based bandpass filter with a high selectivity and a compact size, fabricated on a gallium arsenide (GaAs) substrate is developed. An embedded capacitor is connected between the ends of two divisions in a circular spiral inductor, which is intertwined to reduce its size to $0.024 \lambda_g \times 0.013 \lambda_g$ with minimal loss, and along with the capacitor, it generates a center frequency of 1.35 GHz. The strong coupling between the two ports of the filter results in high selectivity, to reduce noise interference. The insertion loss and return loss are 0.26 dB and 25.6 dB, respectively, thus facilitating accurate signal propagation. The filter was tested to verify its high performance in several aspects, and measurement results showed good agreement with the simulation results.

Keywords: integrated passive device technology; bandpass filter; circular spiral inductor; air-bridge structure; GaAs substrate

1. Introduction

The development of communication technology has resulted in the creation of many new microwave devices in the past decade, and has attracted public attention. Such devices have greatly improved our lives, and promoted the advancement of society. The widespread urban communication system requires a variety of components to transmit the required amounts of information. Thus, products such as amplifiers, mixers, baluns, and power dividers are being more extensively used. The proper operation of these complex systems demands filters to block unwanted noise and interference within selected frequency ranges. Bandpass filters (BPFs) are among the most essential components for applications on the microwave frequency bands, and their performances affect the operation of complete systems. As an electronic interface unit, the BPF allows the transmission of signals in a specific frequency range to reduce interference. Besides performance requirements, the increasingly complex structure and diverse uses of communication devices demand miniaturization to meet consumer expectations [1].

Different methods of designing BPFs have been proposed to meet diverse requirements. A common method consists of using parallel coupled lines or structures based on this classical

prototyping [2,3], and its simplicity prevents high costs and provides devices with wide and flat passbands. Other methods adopt stub-loaded resonators for fabricating BPFs that are capable of controlling the resonant modes, thus easily enabling multiband response and control of the center frequency [4–6]. However, the length of the conventional transmission lines limits miniaturization when employing these methods. To overcome this shortcoming, several manufacturing processes have been proposed. Designs based on three-dimensional multilayer structures like liquid-crystalline polymer substrate [7] or low temperature co-fired ceramic technology [8] can greatly optimize the design, but they cannot be applied to mass production, given the high prices and large time consumption. Other designs use complementary metal-oxide-semiconductor transistor (CMOS) technology [9], and although it enables miniaturization, some parameters remain to be improved. For these reasons, integrated passive device (IPD) technology is preferred for designing microwave passive devices. IPD technology is a newly developed manufacturing technology that realizes an ideal integrated packaging system and provides complete module solutions at the same time. This technique can be used not only to process bandpass filters, lowpass filters or other filters, but also to process biosensors [10], power dividers [11], and couplers [12]. IPD technology can provide technical support for the growing chip market, with the help of its wide application in the processing of different devices.

In this study, we developed a compact on-chip BPF with a circular spiral inductor and an embedded capacitor. The filter is fabricated by using a gallium arsenide (GaAs) substrate at a center frequency of 1.35 GHz, and it was simulated by using a three-dimensional electromagnetic simulator for more accurate results. After analysis of the structure, we present the IPD process that is used to fabricate the filter. IPD technology allows for the simultaneous achievement of compact size, low cost, and excellent performance. In fact, the dimensions of the proposed BPF are 1.54 mm × 0.81 mm, which is ideal for the telecom industry, whose devices require a high degree of integration and accuracy. Moreover, we were able to generate circular patterns, which was relatively hard to process before, owing to inadequate processing techniques. Measurement results with an insertion loss of 0.26 dB and a return loss of 25.6 dB are provided and compared with results from similar works.

2. Materials and Methods

Many approaches are available for designing BPFs, from which the inductor-capacitor (LC) resonant structure employed in this study is easy to implement, compared to other methods, while providing the required effectiveness. The schematic of the proposed BPF is shown in Figure 1a, where the resonant frequency is mostly determined by the inductor and capacitor, which have circular shapes to allow the capacitor to be located exactly in the space between the two divisions of the inductor. The performance of the inductor is enhanced by mutual inductance from the intertwined and overlapped circular lines with air bridges. An air bridge is depicted in the enlarged view at the upper right corner of Figure 1a in four vertical directions. Five similar air-bridge structures are present in the proposed BPF, one at the upper side, two symmetrically located at the left and right sides, and the remaining two at the lower side. As depicted in the enlarged view at the bottom right corner of Figure 1a, r_1 and r_2 are the radii of the two small circles in the innermost ring of the embedded capacitor. A sector structure with a diameter of 100 μm in the middle can enhance coupling between the different parts. The line width and spacing of the outer ring are 20 μm and 14 μm , respectively, and both the line width and spacing of the inner ring are 10 μm . The combination of the left and right transmission lines can improve matching with the terminal, and current flows without distortion or interference by the elimination of excessive sharp turns that mitigates impedance loss.

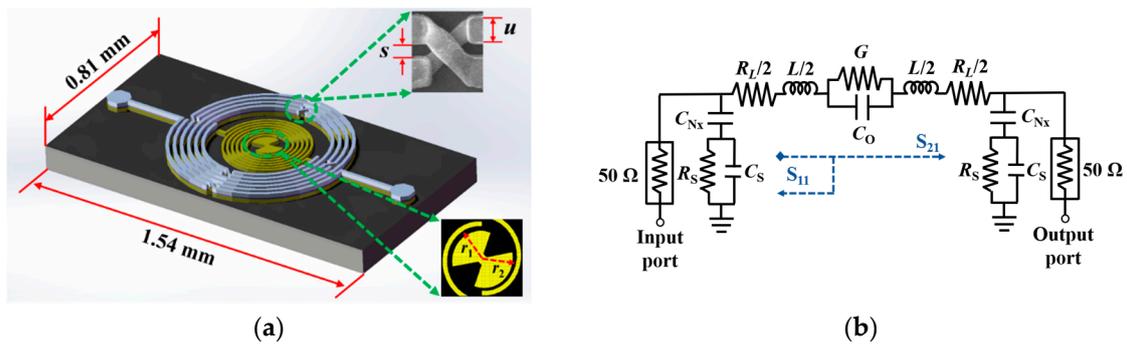


Figure 1. Proposed bandpass filter (BPF): (a) layout ($u = 20 \mu\text{m}$, $s = 14 \mu\text{m}$); (b) equivalent circuit.

The exact realization of an ideal element is difficult. Neglecting some small values of feedthrough capacitance, the equivalent circuit of the proposed LC-type BPF is shown in Figure 1b. The model mainly consists of the inductor, capacitor, and its associated parasitic lumped elements. Variables R_L and G denote the loss resistance and impedance in the inductor (L) and capacitor (C_O), respectively, and C_{N_x} , C_S , and R_S represent the capacitance and resistance associated with the SiN_x layer and the ground. The above parameters can be estimated as [13,14]:

$$R_L = \frac{\rho l}{w\delta(1 - e^{-t/\delta})} \tag{1}$$

$$C_S = \frac{1}{2}lwC_{\text{sub}} \tag{2}$$

$$R_S = \frac{2}{lwG_{\text{sub}}} \tag{3}$$

$$C_{N_x} = \frac{1}{2}lw \frac{\epsilon_{N_x}}{t_{N_x}} \tag{4}$$

where ρ is the resistance coefficient, l is the length of the circle, w is the metal width, δ is the skin depth in the conductor, t is the thickness of the conductor line, C_{sub} and G_{sub} are the capacitance and conductivity per unit area of the GaAs substrate, respectively, and ϵ_{N_x} and t_{N_x} are the dielectric constant and thickness of the SiN_x layer for passivation, respectively. Although many factors affect the performance of the BPF, the center frequency is mainly determined by the circular spiral inductor and capacitor in the proposed design. The inductance of the circular inductor can be derived as in [15]:

$$L = \frac{\mu n^2 d_A}{2} [\ln(2.46/\eta) + 0.20\eta^2] \tag{5}$$

with:

$$d_A = \frac{(d_{\text{out}} + d_{\text{in}})}{2} \tag{6}$$

$$\eta = \frac{d_{\text{out}} - d_{\text{in}}}{d_{\text{out}} + d_{\text{in}}} \tag{7}$$

where μ is the magnetic permeability, n is the number of turns of the inductor, $d_A = 862 \mu\text{m}$ is the average diameter of the outer and inner ring of the inductor, and the value of η is approximately 0.22. The linear function between the capacitance of the concentric pattern and radius of the innermost circle can be used to obtain the capacitance. The capacitance value is solely determined by the material properties for a fixed width of the annular ring and the spacing between two adjacent rings [16,17]. Thus, a capacitor model that should be optimized through a simulation can be designed, because a capacitive effect exists between the metal layers and the ground.

The simulations and optimization were performed on the Agilent Advanced Design System Momentum version 2016.01 (Keysight Technologies, Inc., Santa Rosa, CA, USA) to confirm and support the results and theoretical analysis in this study. The simulated Y parameter of the inner spiral line is depicted in Figure 2a. From this curve, a value of 0.405 pF at a resonant frequency of 1.35 GHz was calculated as in [18]:

$$C = \frac{\text{imag}(Y_{11})}{2\pi f} \quad (8)$$

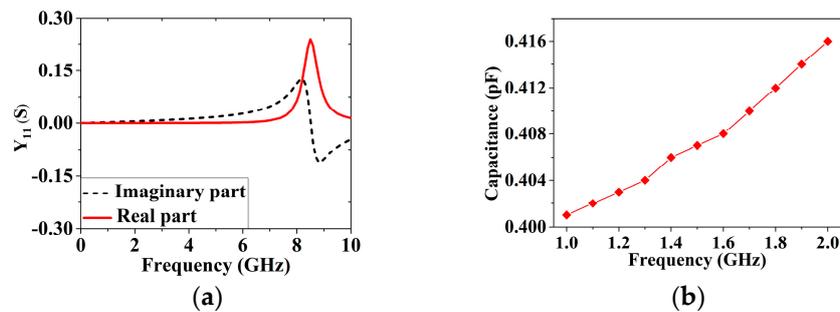


Figure 2. Simulation results of capacitance for optimization. (a) Y parameter of the inner spiral line; (b) Calculated capacitance value.

As shown in Figure 2b, in the L band, where most of the satellite communication systems operate, the capacitance value is stable as only minor differences can be observed. The inductor and capacitor are connected in series, and the center frequency related to the total inductance and capacitance can be expressed as in [18]:

$$f_c = \frac{1}{2\pi\sqrt{LC_0}} \quad (9)$$

the error between the calculated and designed resonant frequencies does not exceed 2.3%.

A representative cross-section of the technology used for the proposed design is illustrated in Figure 3a, where the dimensions are not to scale. The structure is mainly composed of a GaAs substrate and metal layers. Only three metal surfaces, which are the Leads layer, Text layer, and Bond layer from top to bottom, are presented to make the design and processing more concise. The relatively inexpensive copper/gold metal is preferred for slowing down oxidation. The seed metal is selectively added to increase adhesion. A thin SiN_x layer is deposited on the 200 μm thick GaAs substrate, to form a flat surface, and top metal for long-term protection, with a thickness of 100 nm [19–21]. The dielectric constant (ε_r) of GaAs is 12.85, with a loss tangent of 0.006. The finest line width can be processed to 10 μm, with a thickness of 1.8 μm as a middle metal layer. Small gaps between the two metal layers can be used to build an air bridge. More details on the processing are detailed in Figure 3b. After cleaning, plasma-enhanced chemical vapor deposition is used to deposit the SiN_x layer on the substrate. The thickness of Cu/Au is 4.5/0.5 μm, as the bottom metal and the top metal. A plasma etcher (SF₆:O₂ = 45:5 sccm) is adopted after depositing a dielectric layer to remove the unnecessary parts of SiN_x. A 100 nm thick Ti/Au seed metal deposition is followed by etching to avoid shorting, and another mask can be selectively used on the protective film of the top metal to form the specific area of the final SiN_x layer.

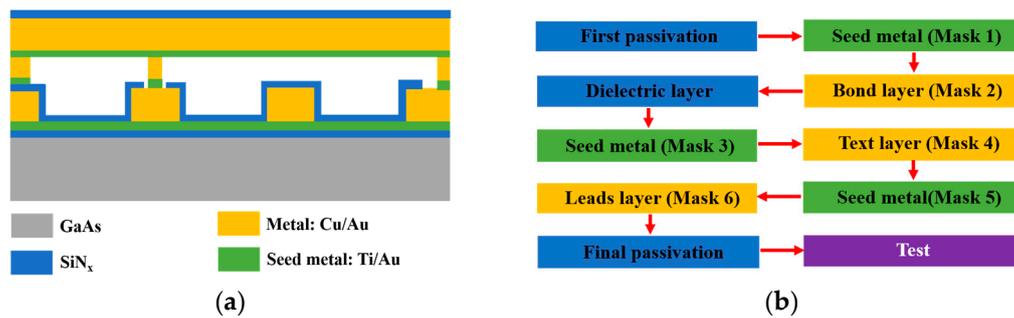


Figure 3. Employed advanced integrated passive device (IPD) technology. (a) Stack-up of device on GaAs substrate; (b) Flowchart of the IPD fabrication process.

3. Results

For testing, the signal from the chip was directed outside through the gold leads on both sides, as shown in Figure 4a, and the chip was attached to a sub-board, as shown in Figure 4b. Figure 4c shows a cubic aluminum block with edges of 2 cm, placed on the bottom of the printed circuit board. The aluminum block provides a flat measuring environment and noise reduction. Figure 4d shows the Agilent 8719ES vector network analyzer that was used to perform measurements on the fabricated BPF.

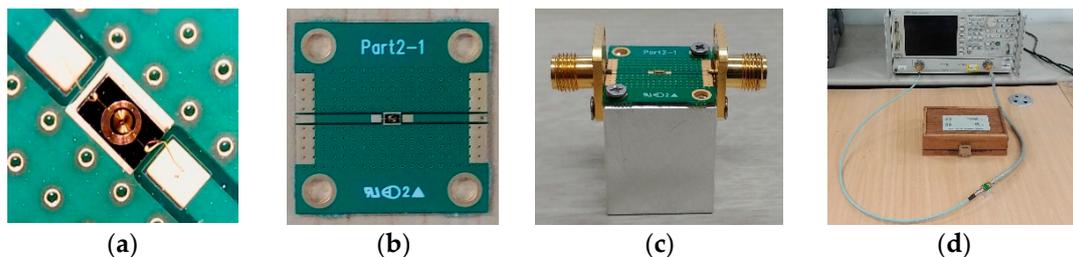


Figure 4. Measurement setup. (a) Enlarged view of on-chip BPF with Au wire bonding; (b) Packaged device on a printed circuit board; (c) Side view of the final product with connectors; (d) Test setup.

The total size of the proposed BPF is $1.54 \text{ mm} \times 0.81 \text{ mm}$, which corresponds to a size of $(2.4 \times 10^{-2} \times 1.3 \times 10^{-2}) \cdot \lambda_g$, where λ_g denotes the guided wavelength at a center frequency of 1.35 GHz. Figure 5a shows the scanning electron microscopy image that is used to verify whether the processing is defective or not, as this would be difficult to observe with the naked eye. The simulated current density around the resonant frequency is shown in Figure 5b, which indicates the current flowing through the center of the filter, and reflects the internal workings of the central region of the filter at resonance. The Q-factor represents the amount of energy that is lost on the filter, with higher values indicating greater loss. The Q-factor of the BPF can be calculated as:

$$Q = \frac{f_c}{f_H - f_L} \quad (10)$$

where f_H and f_L are passband-edge frequencies in the upper and lower bands, respectively. As shown in Figure 6a, a 10 dB fractional impedance bandwidth of 29% was achieved, the fractional bandwidth is calculated by $(f_H - f_L)/f_c$ [18]. The insertion loss is as low as 0.26 dB, and the return loss is above 25.6 dB within the passband. A transmission zero is designed to locate at 3.7 GHz, where the admittance parameter Y_{21} equals zero, with a magnitude of S_{21} to be 36 dB in the rejection band. The location of transmission zero can be slightly changed with the dimension; however, it should be noted that it may affect the variations of other parameters, such as bandwidth and selectivity [18,21]. A sharp roll-off is obtained both in the lower and upper bands, from 20 dB to 3 dB attenuation points, which confirms the good skirt performance. A relatively constant group delay over the entire passband

is plotted in Figure 6b, indicating the small distortion of the BPF. The negligible differences between the measurement and simulation results may be due to losses in the measuring instruments.

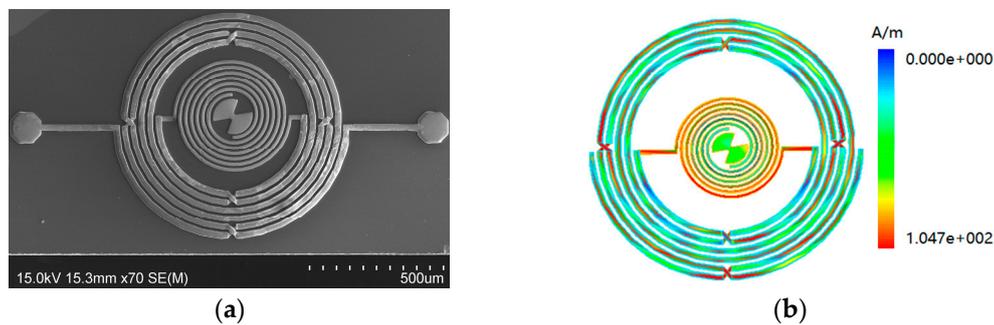


Figure 5. Final processed on-chip BPF. (a) Scanning electron microscopy image of proposed BPF; (b) Simulated current density over proposed BPF.

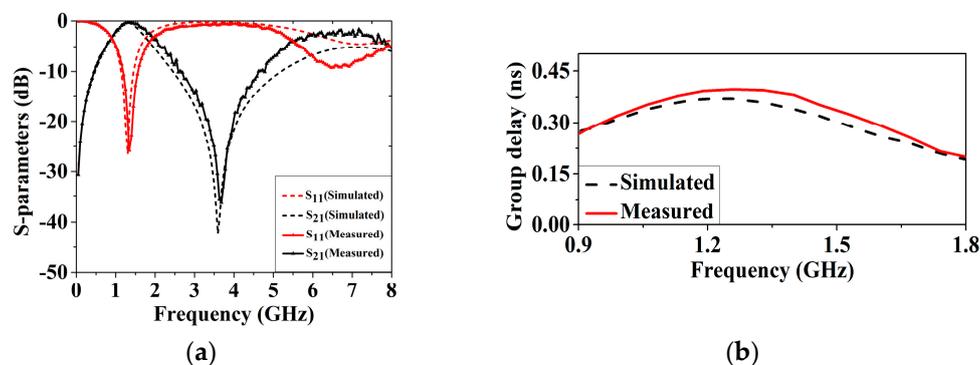


Figure 6. Simulation and measurement results: (a) Parameters S_{11} and S_{21} ; (b) Group delay.

4. Discussion

Research on BPFs mainly aims for their application to wired and wireless communication systems. In addition, IPD technology is used to meet the high demands of modern communication equipment regarding micromachining. Moreover, GaAs, a high mobility material, is usually applied as a substrate because its process is more mature than most other processes, and there is no excess passivation film on the GaAs surface. Long transmission lines designed in the pattern improve processing precision, which further ensures the stability of the filter. In this study, a simple inductor–capacitor series equivalent circuit is used for analysis. Problems can be found in time in low-order circuit and be modified easily. Then, after repeated simulations and measurements, loss was reduced and a wide bandwidth was achieved. Finally, fabricated BPF was checked to confirm that there is no problem through the scanning electron microscopy images.

Many studies have been focused on improving the performance of BPFs in recent years. Table 1 compares on-chip filters based on different processes with the proposed BPF, which provides higher performance with fewer metal layers than a low temperature co-fired ceramic BPF [8] or a glass IPD BPF [22]. The return loss above 20 dB of the proposed BPF indicates that almost no reflected signal occurs at the center frequency, and the best insertion loss was obtained among the compared BPFs [8,21–25]. GaAs can provide better insulation and less signal loss than silicon substrate; in addition, the working power of GaAs is higher than glass [26]. A circular spiral pattern is used in series with the inductor, and the stability of the capacitance value is ensured by the simple structure in a limited space. A relatively high self-resonant frequency of the capacitor, which is approximately equal to 8.1 GHz, enables the capacitor to work over a wide frequency range. The overall size of fabricated chip is small, especially the circular structure that makes the short side more compact.

Table 1. Comparison of this study to similar works.

Work	Technology	f_c (GHz)	Insertion Loss (dB)	Return Loss (dB)	Area ($\lambda_g \times \lambda_g$)	FBW (%) (10-dB)	Metal Layers
[8]	LTCC	1.57	2.7	>30	0.063×0.048	5	4
[22]	Glass IPD	2.6	0.6	>30	0.023×0.012	17	4
[23]	Si IPD	1.5	2.54	20	0.046×0.026	16	2
[24]	GaAs IPD	2.27	0.8	26.1	0.024×0.019	27	2
[25]	GaAs IPD	1.96	0.27	26.8	0.019×0.023	28	2
[21]	GaAs IPD	1.71	0.50	32.1	0.024×0.020	27	3
This work	GaAs IPD	1.35	0.26	25.6	0.024×0.013	29	3

LTCC, low temperature co-fired ceramics; FBW, fractional bandwidth.

5. Conclusions

We propose a simple design of an IPD-based BPF for L-band applications. A circular spiral inductor with an embedded capacitor is used to reduce the chip size to 1.25 mm^2 . High performance in terms of return loss and insertion loss with values of 25.6 dB and 0.26 dB, respectively, were measured throughout the passband. The theoretically predicted values are in good agreement with the actual measured values. By fabrication on a GaAs substrate, it is possible to perform a relatively high Q-factor and a compact spiral circular pattern. Additionally, fabrication costs and time can be saved with this simple IPD processing technology, by using three layers of metal. IPDs can effectively combine plenty of passive components together to save more space and achieve more features than discrete passive devices.

IPD technology whose substrate possesses good insulation properties and high electron mobility in a high frequency range will have broad application prospects in medical, lighting, and wireless communication markets. In our future work, the chip will be packaged to prevent damage and overheating by adopting a SOT-6 packaging process, which also provides waterproofing and easy handling. Considering these advantages along with its high selectivity, the proposed BPF seems promising for applications in wireless communication systems.

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