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Performance Evaluation of a Semi-Dual-Active-Bridge with PPWM Plus SPS Control

Ming Lu  and Xiaodong Li * 

Faculty of Information Technology, Macau University of Science and Technology, Taipa, Macau 999078, China; 1409853pii30001@student.must.edu.mo

* Correspondence: xdli@must.edu.mo; Tel.: +853-8897-2195

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Abstract: In this paper, a semi-dual-active-bridge (S-DAB) DC/DC converter with primary pulse-width modulation plus secondary phase-shifted (PPWM + SPS) control for boost conversion is analyzed in detail. Under the new control scheme, all effective operation modes are identified at first. Then, the working principle, switching behaviour, and operation range in each mode are discussed. Compared with conventional secondary phase-shifted control, PPWM + SPS control with two controllable phase-shift angles can extend the zero-voltage switching (ZVS) range and enhance control flexibility. In addition, an effective control route is also given that can make the converter achieve at the global minimum root-mean-square (RMS) current across the whole power range and avoid the voltage ringing on the transformer secondary-side at a light load. Finally, a 200 W prototype circuit is built and tested to verify correctness and effectiveness of theoretical results.

Keywords: DC–DC conversion; zero-voltage switching (ZVS)

1. Introduction

With the development of modern technology, there is a constant rise in energy use. Therefore, the concerns regarding the availability of fossil energy and the associated pollution in the mining and consumption process is continuously growing too. In order to alleviate the energy crisis and environmental pollution, the use of renewable energy (solar energy, wind energy, etc.) has developed rapidly around the world. As an important component for the application of renewable energy, the DC/DC converter with higher performance has been one of the most popular research fields [1–5]. So far, a number of DC/DC converter topologies have been proposed according to the various application requirements. In these converters, the phase-shift full-bridge converter is more attractive due to high power density, electrical isolation, easy to realize soft-switching commutation, high efficiency and low electromagnetic interference (EMI) [6–13]. However, it still suffers from high voltage ringing, reverse recovery on the secondary-side rectifier diodes, limited zero-voltage switching (ZVS) range and duty cycle loss.

To extend the ZVS range, a series of the full-bridge converters with various resonant tanks are presented. Among them, the converters with LC or LLC resonant tank are more attractive [14–19]. Nevertheless, the parameters of resonant tank should be selected carefully to achieve higher performance. Meanwhile, the design of magnetic components becomes complicated. On the other hand, when the phase-shift full-bridge converter works at high-output voltage and high-power case, the reverse-recovery problem of the rectifier diodes becomes more serious. In order to solve this problem, two active switches are introduced into the secondary-side rectifier of the converter, which is named the semi-dual-active-bridge (S-DAB) converter [20–22]. On this basis, two modified

S-DAB topologies in [23,24] are proposed to only reduce the voltage stress on primary-side and secondary-side semiconductor devices, respectively. Furthermore, the S-DAB converter with an LC resonant tank is also presented in [25,26]. However, when the S-DAB converters work in a discontinuous-current mode (DCM) for boost operation, the voltage ringing phenomenon is generated on the transformer secondary-side. In particular, at the high switching frequency, high power and voltage levels, the excessive ringing might result in strong EMI, distorted gating signals and abnormal high peak voltages across the switches. In addition, the amount of power loss from snubber/parasitic capacitor will also increase during the ringing process [27,28]. Although a customized RC snubber is helpful to alleviate this problem, extra loss will be introduced in continuous-current mode (CCM) operation and the overall efficiency would be lower.

To the authors' best knowledge, the voltage ringing problem in S-DAB has yet to be resolved. In this paper, PPWM + SPS control is applied on an S-DAB converter for boost operation to further improve performance, which also avoids the voltage ringing problem. The rest of this paper is organized as follows: in Section 2, each steady-state mode of an S-DAB converter with PPWM + SPS control is analyzed comprehensively, including working principle, switching behaviour, and operation range. In Section 3, an effective control route across the whole power range is presented in order to achieve minimum root-mean-square (RMS) current and no voltage ringing. Experimental results are provided in Section 4. Conclusions are drawn in Section 5.

2. Operation Principle of an S-DAB Converter with PPWM + SPS Control

2.1. Basic Operation Principle

The schematic of an S-DAB converter is shown in Figure 1. The primary H-bridge consists of four switches ($M_1 - M_4$), while the secondary H-bridge is realized by a diode leg (D_{S1} and D_{S2}) and a switch leg (M_5 and M_6). The high frequency transformer T with a turns ratio of $n_t : 1$ not only provides galvanic isolation, but also matches voltage level. The voltage gain is defined as $M = n_t V_o / V_{in}$, and $M > 1$ refers to boost operation. The inductor L_s includes the leakage inductance of the transformer and an external inductance. The filter capacitor C_o is connected in parallel with the load R_{load} to depress the output voltage ripple. In this paper, PPWM + SPS control with two phase shift angles is employed on an S-DAB converter. All switches operate at the same frequency f_s with 50% duty cycle, and switches in each switch leg are turned on/off complementarily. α is defined as the inner phase-shift by which the gating signal of M_4 lags that of M_1 . Similarly, ϕ is defined as the outer-phase-shift by which the gating signal of M_6 lags that of M_1 . Two pulse-width-modulated voltages v_{AB} and v_{CD} are generated by the two bridges, respectively. The pulse-width of v_{AB} is determined by α solely. However, the waveform of v_{CD} is associated with not only phase-shift angles but also the load level.

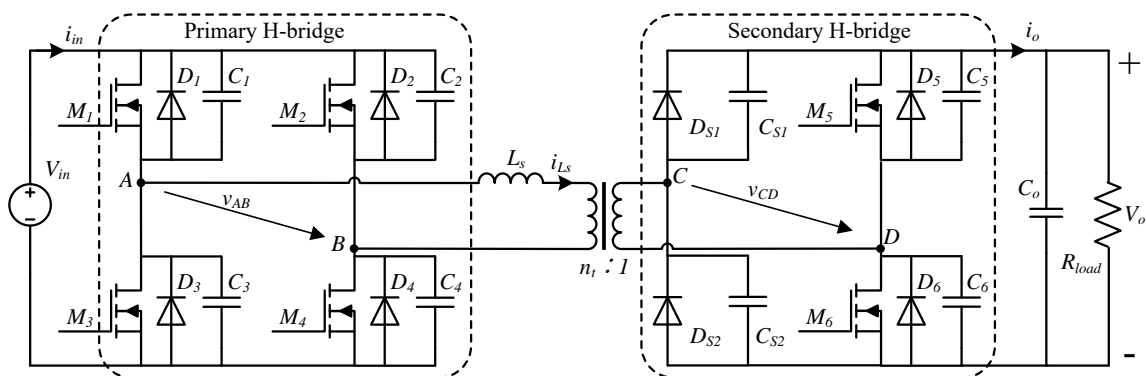


Figure 1. The circuit configuration of a S-DAB converter.

Depending on the relationship between two phase-shifts, an S-DAB converter with PPWM + SPS control can operate in three steady-state working modes, including one CCM (Mode A) and two DCMs, (Mode B and C). In the following part, each mode will be analyzed in detail one by one. In order to simplify the analysis process, four assumptions are made as follows:

1. All components, such as switches, diodes are ideal and lossless.
2. The magnetizing inductance of the transformer is infinity.
3. The snubber/parasitic capacitors and dead-times influence are neglected.
4. The filter capacitor is large enough to maintain constant voltage on the load.

2.2. Steady-State Analysis of Continuous-Current Mode

The ideal steady-state waveforms in Mode A are shown in Figure 2, where β denotes the first zero-crossing points referred to the turn-on moment of M_1 . It can be seen that Mode A is featured with $\alpha < \beta < \phi < \pi$; and there are eight different intervals in one switching period. The corresponding equivalent circuits of the first four intervals are presented in Figure 3, respectively. The other four intervals are almost the same except for the directions of voltage/current and involved conducting devices.

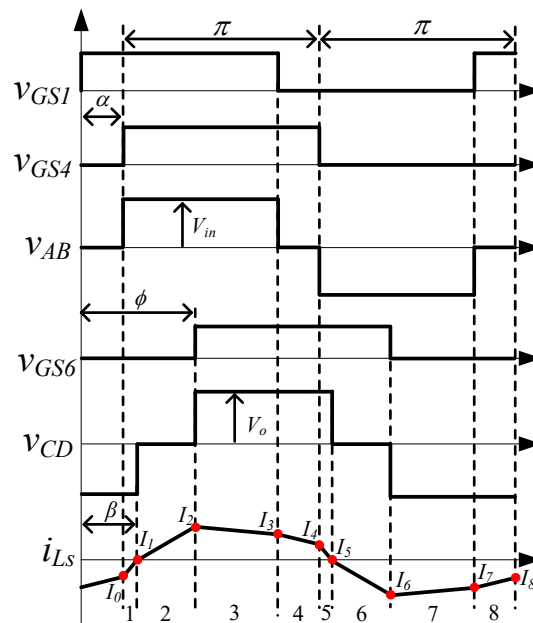


Figure 2. Steady-state waveforms in Mode A.

Interval 1 [Figure 3a]: At the beginning, M_2 is turned off and M_4 is turned on with ZVS. In this interval, the conducting devices are M_1 and M_4 , M_5 and D_{s2} . Thus, the voltage across the inductor is clamped at $(V_{in} + n_t V_o)$, the value of i_{Ls} decreases linearly from the negative value I_0 to I_1 . The power stored in the inductor is delivered to input DC power and load during this interval:

$$I_1 = I_0 + \frac{V_{in} + n_t V_o}{2\pi f_s L_s} (\beta - \alpha) = 0. \quad (1)$$

Interval 2 [Figure 3b]: At $\beta - \alpha$, the polarity of i_{Ls} is changed, the current flowing diode-leg is shifted naturally from D_{s2} to D_{s1} , i.e., D_{s2} is turned off with zero current. The secondary-side of transformer is shorted now by M_5 and D_{s1} . Meanwhile, the primary current flows from V_{in} to L_s through primary switches M_1 and M_4 . Thus, the voltage across the inductor is clamped at V_{in} ,

the value of i_{L_s} increases linearly from I_1 to the positive maximum I_2 . The power is being stored in the inductor L_s during this interval:

$$I_2 = I_1 + \frac{V_{in}}{2\pi f_s L_s} (\phi - \beta). \quad (2)$$

Interval 3 [Figure 3c]: At $(\phi - \alpha)$, M_5 is turned off and M_6 is turned on with ZVS. In this interval, the situation on the primary side does not change; the secondary current is shifted to D_{s2} and M_6 , flowing to the load. Thus, during this interval, the voltage across inductor is clamped at $(V_{in} - n_t V_o)$, and the power is transmitted to the load. Due to $(V_{in} < n_t V_o)$, the value of i_{L_s} starts to decrease linearly from I_2 to the positive value I_3 :

$$I_3 = I_2 + \frac{V_{in} - n_t V_o}{2\pi f_s L_s} (\pi - \phi). \quad (3)$$

Interval 4 [Figure 3d]: At $(\pi - \alpha)$, M_1 is turned off and M_3 is turned on with ZVS. In this interval, the primary side is shorted by M_3 and M_4 ; and no change happens on the secondary side. Thus, the voltage across inductor is clamped at $-n_t V_o$. During this interval, the value of i_{L_s} starts to decrease linearly until it reaches $-I_0$. The power stored in the inductor is delivered to load:

$$I_4 = I_3 - \frac{n_t V_o}{2\pi f_s L_s} \alpha = -I_0. \quad (4)$$

Based on Equations (1)–(4), the instantaneous current values at the moments of transition can be calculated as functions of α and ϕ . Furthermore, the output power P_o and the inductor RMS current $I_{L_s, rms}$ can be obtained too. These results are listed in Table 1, where the current and power values are normalized by the following base values:

$$I_b = \frac{V_{in}}{2\pi f_s L_s}, P_b = \frac{V_{in}^2}{2\pi f_s L_s}. \quad (5)$$

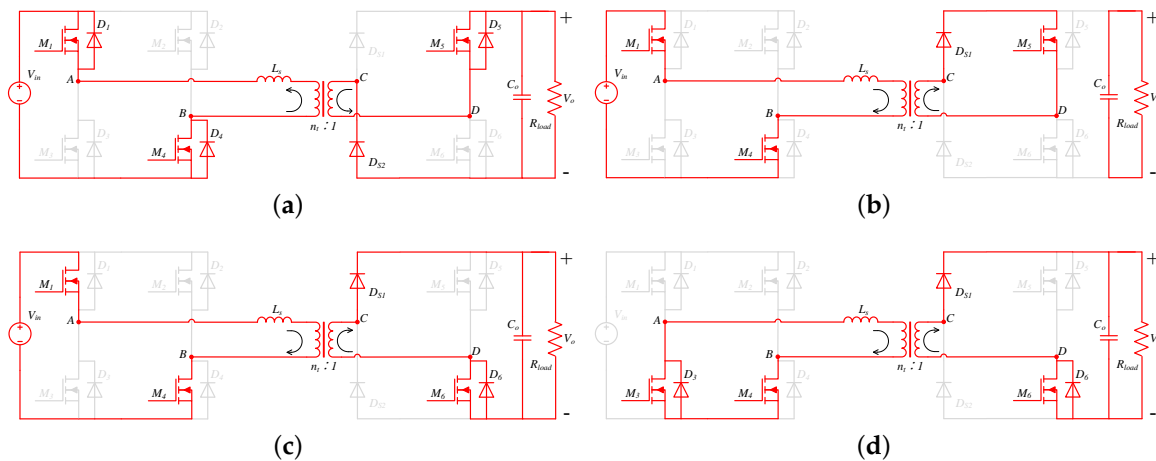


Figure 3. Equivalent circuits corresponding to the first four intervals in Mode A: (a) Interval 1 $[0, \beta - \alpha]$; (b) Interval 2 $[\beta - \alpha, \phi - \alpha]$; (c) Interval 3 $[\phi - \alpha, \pi - \alpha]$; (d) Interval 4 $[\pi - \alpha, \pi]$.

Table 1. Theoretical values of inductor current and output power in Mode A.

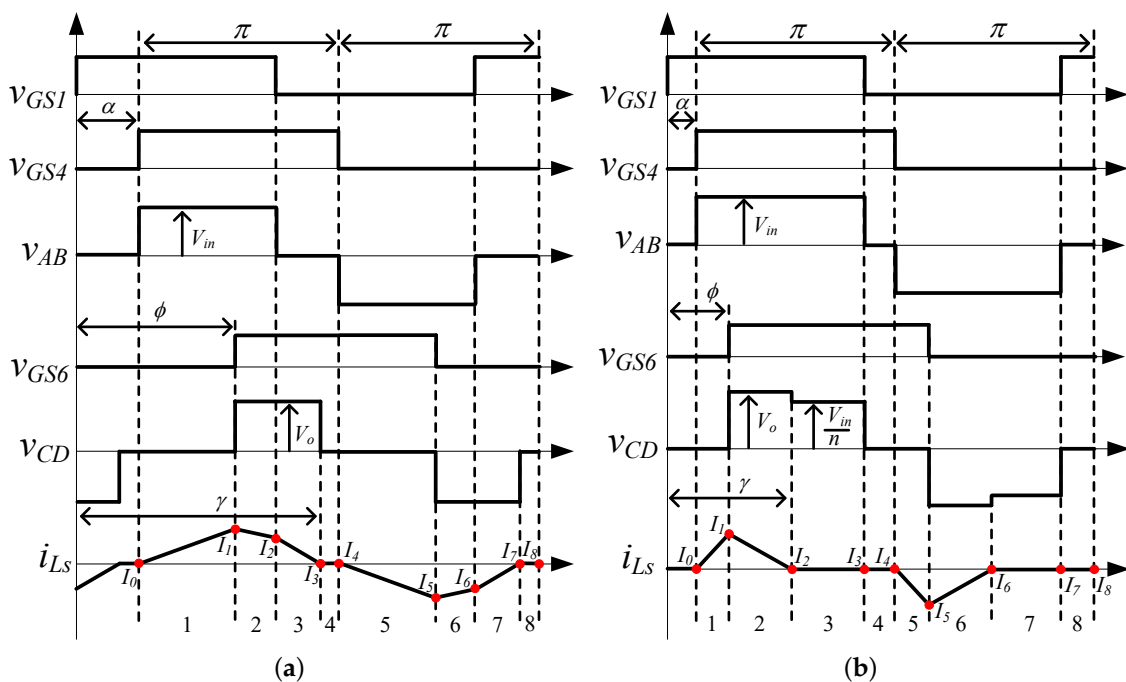
Value	Expression
$I_{0,pu}$	$\frac{(1+M)(\alpha-\pi+\alpha M-\phi M+\pi M)}{2+M}$
$I_{1,pu}$	0
$I_{2,pu}$	$\pi - \frac{\alpha-2\phi+3\pi}{2+M}$
$I_{3,pu}$	$\pi + (\pi - \phi)(1 - M) - \frac{\alpha-2\phi+3\pi}{2+M}$
β	$\frac{\pi+\alpha+\phi M-\pi M}{2+M}$
$P_{o,pu}$	$\frac{M}{2\pi(2+M)^2} \left(\begin{aligned} &2\alpha\phi M^2 + 4\pi\phi M^2 + 4\alpha\phi M - \alpha^2 M^2 - 2\pi\alpha M^2 - 2\phi^2 M^2 - 2\pi^2 M^2 \\ &+ 4\pi\phi M + \pi^2 M - 4\phi^2 M - 3\alpha^2 M - 2\pi\alpha M \\ &+ \pi^2 + 4\alpha\phi + 4\pi\phi - 3\alpha^2 - 2\pi\alpha - 4\phi^2 \end{aligned} \right)$
$I_{Ls,rms,pu}$	$\frac{1}{\sqrt{3\pi(M+2)^2}} \sqrt{\begin{aligned} &M^3\alpha^3 - 3M^3\alpha^2\phi + 3M^3\alpha^2\pi + 3M^3\alpha\phi^2 - 6M^3\alpha\phi\pi \\ &+ 3M^3\alpha\pi^2 - 2M^3\phi^3 + 6M^3\phi^2\pi - 6M^3\phi\pi^2 + 2M^3\pi^3 \\ &+ 3M^2\alpha^3 - 6M^2\alpha^2\phi + 3M^2\alpha^2\pi + 3M^2\alpha\phi^2 - 3M^2\alpha\pi^2 \\ &- 2M^2\phi^3 + 6M^2\phi^2\pi - 3M^2\pi^3 + 4M\alpha^3 - 6M\alpha^2\phi + \\ &6M\alpha\phi^2 - 6M\alpha\phi\pi - 4M\phi^3 + 6M\phi^2\pi + 2\alpha^3 - 3\alpha^2\pi + \pi^3 \end{aligned}}$

2.3. Steady-State Analysis of Discontinuous-Current Mode

Different from CCM, the inductor current i_{Ls} in DCM remains at zero for a small duration in each switching period. Steady-state waveforms of two DCMs are shown in Figure 4, where γ denotes the second zero-crossing points referring to the turn-on moment of M_1 . It can be found that the difference between those two DCMs can be concluded as: $\alpha < \phi < \pi < \gamma$ for Mode B and $\alpha < \phi < \gamma < \pi$ for Mode C.

Mode B [Figure 4a]

According to the steady-state waveforms in Mode B, the equivalent circuits in the first four intervals are shown in Figure 5. It can be seen that the first three intervals in Mode B are almost the same as Intervals 2–4 in Mode A, except that the inductor current at the end of Interval 3 (Mode B) can arrive again at zero.

**Figure 4.** Steady-state waveforms in: (a) Mode B; (b) Mode C.

Interval 4 [Figure 5d]: After $\gamma - \alpha$, all secondary diodes are reversed biased, which will result in the secondary-side of transformer being open-circuited. Meanwhile, the primary switches M_3 and M_4 are still conducting. Thus, the transformer secondary voltage is clamped at 0, and i_{Ls} is kept at zero. This interval ends up with M_2 turned on at zero current. In this zero-current interval, there is no power transferring in the converter.

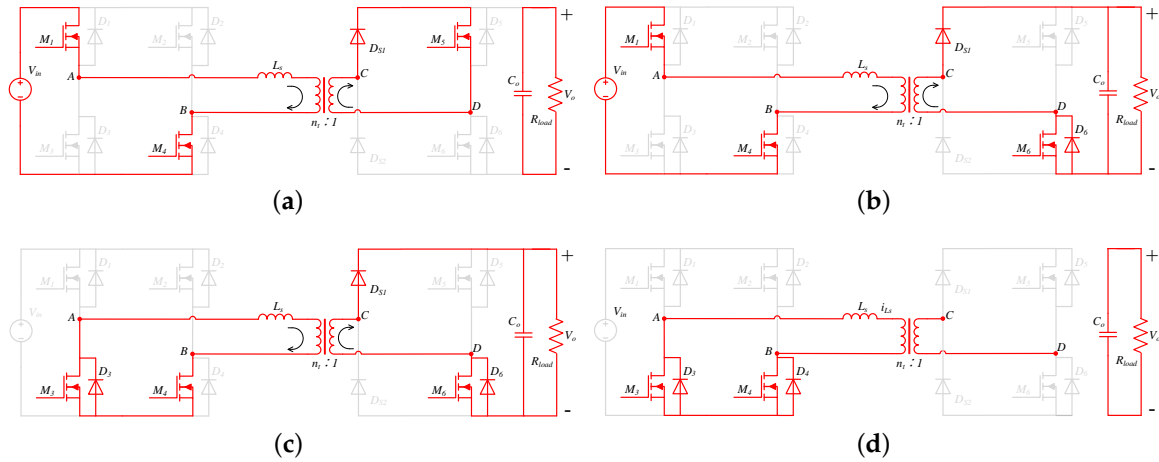


Figure 5. Equivalent circuits corresponding to the first four intervals in Mode B: (a) Interval 1 $[0, \phi - \alpha]$; (b) Interval 2 $[\phi - \alpha, \pi - \alpha]$; (c) Interval 3 $[\pi - \alpha, \gamma - \alpha]$; (d) Interval 4 $[\gamma - \alpha, \pi]$.

Mode C [Figure 4b]

Similarly, the equivalent circuits corresponding to first four intervals in Mode C are shown in Figure 6, respectively. It can be seen that the first second intervals in Mode C are almost the same as Intervals 2 and 3 in Mode A, except that the inductor current at end of Interval 2 (Mode C) can arrive again at zero.

Interval 3 [Figure 6c] in Mode C is different from those aforementioned intervals. Although the input DC source V_{in} is applied on the primary-side of transformer by the switches M_1 and M_4 , there is no flowing current in the converter. The secondary-side of transformer is open-circuited since all secondary diodes are reversed biased. Thus, the secondary-side transformer voltage is clamped at $\frac{V_{in}}{n}$. Interval 3 ends up with M_3 turned on at zero current. This interval also belongs to the zero-current interval, and there is no power transferring. Interval 4 is the same as Interval 4 in Mode B.

Based on the steady-state analysis in each DCM, the instantaneous current values at the moment of transition can be calculated. Similarly, the output power and RMS current across inductor can be also obtained. These theoretical results are listed in Table 2.

Table 2. Theoretical values of inductor current and output power in DCM.

Value	Mode B	Mode C
$I_{0,pu}$	0	0
$I_{1,pu}$	$\phi - \alpha$	$\phi - \alpha$
$I_{2,pu}$	$\pi - \alpha + \phi M - \pi M$	0
$I_{3,pu}$	0	0
γ	$\frac{\pi - \alpha + \phi M}{M}$	$\frac{M\phi - \alpha}{M - 1}$
$P_{0,pu}$	$\frac{\alpha^2 + \pi^2 + 2\pi\phi M - 2\pi\alpha - \phi^2 M - \pi^2 M}{2\pi}$	$\frac{M(\phi - \alpha)^2}{2\pi(M - 1)}$
$I_{Ls,rms,pu}$	$\frac{1}{\sqrt{3\pi M}} \sqrt{\frac{3M^2\phi^2\pi - M^2\phi^3 - M^2\phi\pi^2 + M^2\pi^3 - M\alpha^3}{2M\pi^3 - \alpha^3 + 3\alpha^2\pi - 3\alpha\pi^2 + \pi^3}}$	$\sqrt{\frac{M(\phi - \alpha)^3}{3\pi(M - 1)}}$

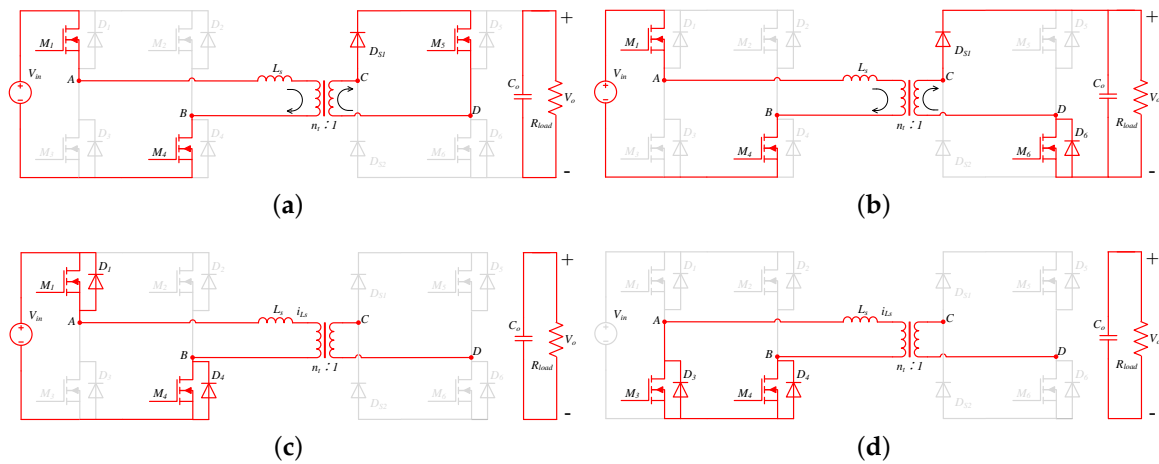


Figure 6. Equivalent circuits corresponding to the first four intervals in Mode C: (a) Interval 1 $[0, \phi - \alpha]$; (b) Interval 2 $[\phi - \alpha, \gamma - \alpha]$; (c) Interval 3 $[\gamma - \alpha, \pi - \alpha]$; (d) Interval 4 $[\pi - \alpha, \pi]$.

2.4. Switching Behaviour

Since the converter may work in three different steady-state modes, the switching behaviour of all switches and diodes also vary with the operation modes. According to the current polarity at switching moment of all switches and diodes, the switching behaviour in each mode are concluded in Table 3. First of all, the diodes in the secondary H-bridge can be turned on/off at zero current in any mode. In Mode A, all switches operate with ZVS and each diode is turned on/off with zero-current. Compared with Mode A, the switching loss in two DCMs is slightly increased due to the partial switch losing ZVS, and the switching loss in Mode C is higher than those in Mode B. Thus, Mode A should be selected as the main operation mode.

Table 3. Switching behavior in different modes.

Mode	M_1, M_3	M_2, M_4	M_5, M_6	D_{S1}, D_{S2}
A	ZVS	ZVS	ZVS	zero-current-on/off
B	ZVS	zero-current-on/off	ZVS	zero-current-on/off
C	zero-current-on/off	zero-current-on/off	ZVS	zero-current-on/off

2.5. Operation Range of Each Mode

Through comparing three steady-state modes, it can be found that Mode B is an in-between mode, and there are two boundary conditions existing between Mode B and the other two modes. Thus, the operating range of two controllable phase-shifts α and ϕ will be different in each mode. Knowing these conditions and range is helpful for the design of the converter.

When $\gamma = \pi$ in Mode B, the converter works at the boundary condition (6) between Mode A and B. At this boundary, the secondary H-bridge works in synchronous rectification mode:

$$\phi = \frac{\alpha + \alpha M + \pi M - \pi}{M}. \quad (6)$$

When $\gamma = \pi - \alpha$ in Mode B, it works at another boundary condition (7) between those two DCMs, in which the second zero-crossing happens at the moment of the switch M_3 being turned on:

$$\phi = \frac{\alpha + \pi M - \pi}{M}. \quad (7)$$

According to both boundary conditions, the operating range of each mode is shown in Figure 7 for $M = 1.5$ and $M = 2$, respectively.

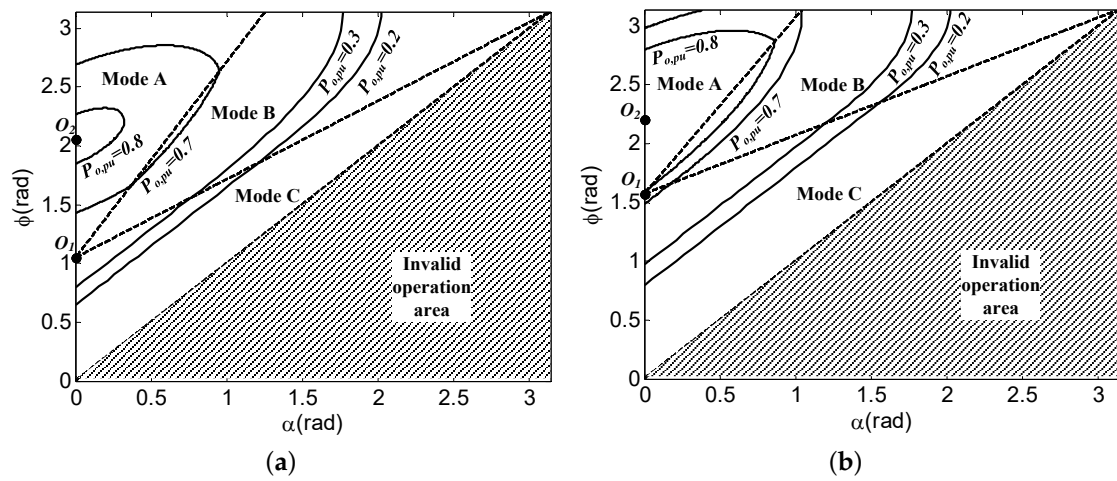


Figure 7. Operating range of each boost mode with suspended power contours for $M = 1.5$ and $M = 2$: (a) $M = 1.5$; (b) $M = 2$.

In Figure 7, the shaded area $\alpha \geq \phi$ represents an invalid operation area. The boundary of the neighboring modes is plotted by two dashed lines using (6) and (7), respectively, and these two boundary lines intersect at the point O_1 . Meanwhile, the power contours with the same normalized power $P_{o,pu}$ value are shown by solid curves, in which the maximum load capacity of the converter is located at the point O_2 , $P_{o,pu,max} = \frac{\pi M(M+1)}{2(M^2+2M+2)}$. The operating range with the conventional secondary phase-shifted control is only along the ϕ -axis. Compared with conventional control, PPWM + SPS can expand regulating range of output power and enhance flexibility of phase-shift control.

3. Proposed Control Route of an S-DAB Converter with PPWM + SPS Control

It is obvious that countless control routes exist from full power at O_2 to zero power at $\phi = \alpha$ for an S-DAB converter with PPWM + SPS control in Figure 7. Therefore, in order to select a reasonable control route, theoretical analysis of the inductor current is carried out to achieve lower conducting loss.

Based on Tables 1 and 2, the relationship between normalized inductor RMS current $I_{Ls,rms,pu}$ and phase-shift α at different power contours are shown in Figure 8, with $M = 1.5$ as an example. It can be found that, at the high power levels, the converter may work in Mode A. $I_{Ls,rms,pu}$ values can arrive at the minimum values when the converter is operated at conventional secondary phase-shifted control from O_2 to O_1 along the ϕ -axis. At the low power levels from O_1 to zero power O_0 , the converter may operate in Mode C, in which $I_{Ls,rms,pu}$ is minimum and constant for the same power level.

In practical application, each switch and diode has its own snubber/parasitic capacitor. It is possible to get the voltage ringing on the transformer secondary-side when the converter is working in a zero-current interval. In Mode C, there are two zero-current intervals (3 and 4) in the half period. Taking a capacitor into account, Interval 3 can be equivalent to the new circuit as Figure 9. In this interval, a resonance circuit is formed by a power inductor and the snubber/parasitic capacitor of the diode leg. Thus, the voltage ringing will be introduced into the transformer secondary-side. However, there is no voltage ringing in Interval 4. The main reason is that the DC source V_{in} in Figure 9 is short-circuited in interval 4. Compared with Mode C, there is only one zero-current interval in Mode B and it is free of voltage ringing, which is same as Interval 4 in Mode C. Considering that voltage ringing will potentially bring up system instability and damage the semiconductor devices, the control route for low power is put on the boundary line between Mode B and C. Thus, the selected route from full power to zero power with PPWM + SPS control is given as Equations (8) and (9), which is a

piecewise function. Under the proposed route control, the converter can achieve at the minimum RMS current for the full power range and is free of voltage ringing across the transformer.

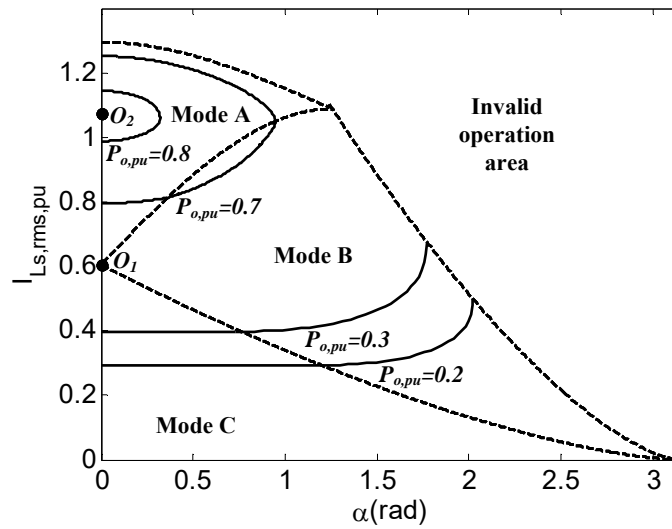


Figure 8. Normalized inductor RMS current vs. phase-shift α at different power contours for $M = 1.5$.

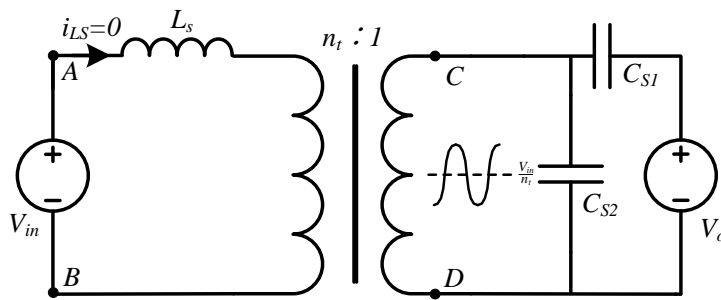


Figure 9. New equivalent circuit corresponding to interval 3 in Mode C.

When $P_{o,pu} \in \left[\frac{\pi(M-1)}{2M}, P_{o,pu,max} \right]$,

$$\begin{cases} \phi = \pi - \frac{(2+M)\sqrt{2\pi M(\pi M^2 + \pi M - 2M^2 P_{o,pu} - 4M P_{o,pu} - 4P_{o,pu})} + X_1}{2M^3 + 4M^2 + 4M} \\ \alpha = 0. \end{cases} \quad (8)$$

When $P_{o,pu} \in \left[0, \frac{\pi(M-1)}{2M} \right]$,

$$\begin{cases} \phi = \pi - \frac{X_2 \sqrt{P_{o,pu}}}{M} \\ \alpha = \pi - X_2 \sqrt{P_{o,pu}} \end{cases}, \quad (9)$$

where $X_1 = 2\pi M^2 + 2\pi M$, $X_2 = \frac{\sqrt{2\pi M(M-1)}}{M-1}$.

4. Experimental Verifications

To verify the theoretical analysis above, a 200 W S-DAB prototype is built, as shown in Figure 10. The specifications of the lab-scale converter are listed in Table 4. The gating signals of S-DAB are implemented using a TMS320F28335 DSP from TI (Texas Instruments, Dallas, TX, USA) and the switching frequency is set at 100 kHz.

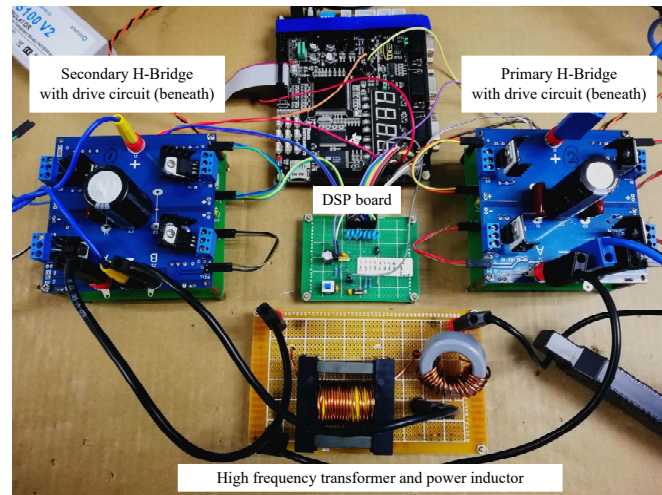


Figure 10. The layout of a 200 W S-DAB laboratory prototype.

Table 4. Specifications of a 200 W S-DAB converter.

Component	Parameter
Input DC voltage V_{in}	80 V
Load DC voltage V_o	120 V
Power inductance L_s	38 μ H, CM400125/MPPcore
Transformer turns ratio n_t	15:15, ETD49/N97
Filter capacitor C_o	470 μ F, 1 electrolytic cap
Switch $M_1 \sim M_6$	STP40NF20, $R_{ds} = 38$ m Ω
Diode D_{s1}, D_{s2}	MBR40250TG, $V_F = 0.86$ V

Based on the analysis of each operation mode in Section 2, a set of experimental waveforms corresponding to three effective modes are obtained and shown in Figure 11, respectively. These experimental results match the theoretical prediction closely. In Figure 11c, the voltage ringing shows up on the transformer secondary-side v_{CD} after i_{Ls} decreases to zero and remains a small duration until $v_{AB} = 0$. As expected, the voltage ringing is not identified in Figure 11b.

A series of experimental tests are then performed along the proposed minimized rms current route. The boundary power between the two stages of the control route is calculated to be 52% load, i.e., 104 W. Thus, the converter works in CCM (Mode A) at the high power of 200 W and 150 W. Two phase-shift angles are calculated as $\alpha = 0^\circ$, $\phi = 90.25^\circ$ (200 W) and $\alpha = 0^\circ$, $\phi = 63.76^\circ$ (150 W) according to (8). Experimental results of 200 W and 150 W are shown in Figure 12a,b, respectively. It can be seen from those two figures that the inductor current i_{Ls} is continuous. The related waveforms satisfy the operation condition of $\phi > \beta > \alpha = 0$ and all switches can operate at ZVS.

When the output power is lower than 52% load, the converter is operated at the boundary between Mode B and C. Using (9), two phase-shift angles are obtained as follows: (1) 100 W, $\alpha = 28.06^\circ$, $\phi = 78.71^\circ$; (2) 50 W, $\alpha = 72.46^\circ$, $\phi = 108.3^\circ$. Experimental results of 100 W and 50 W are shown in Figure 12c,d, respectively. It can be seen that the transition moment of v_{AB} from V_{in} to zero happens at the zero-crossing point of the inductor current and there is a small zero-current duration. The operation conditions of two experimental results match the boundary feature between both DCMs. In addition, the voltage ringing on the waveform v_{CD} is prevented in comparison to DCM under conventional secondary phase-shifted control (Figure 13). Based on these experimental results, the values of the RMS current, peak current, and efficiency are listed in Table 5, where the highest efficiency can arrive at 95.53% for 150 W. For 50 W operation with conventional control in Figure 13, the measured efficiency is 88.46%. It is seen that the efficiency using the proposed control is improved slightly since the current values and the switching behaviour under the two control methods are almost the same and the loss

due to the ringing accounts for a small portion of total loss. However, the removal of the ringing phenomenon depresses EMI so that the risk of distortion in gating signals is reduced and the operation stability is improved consequently.

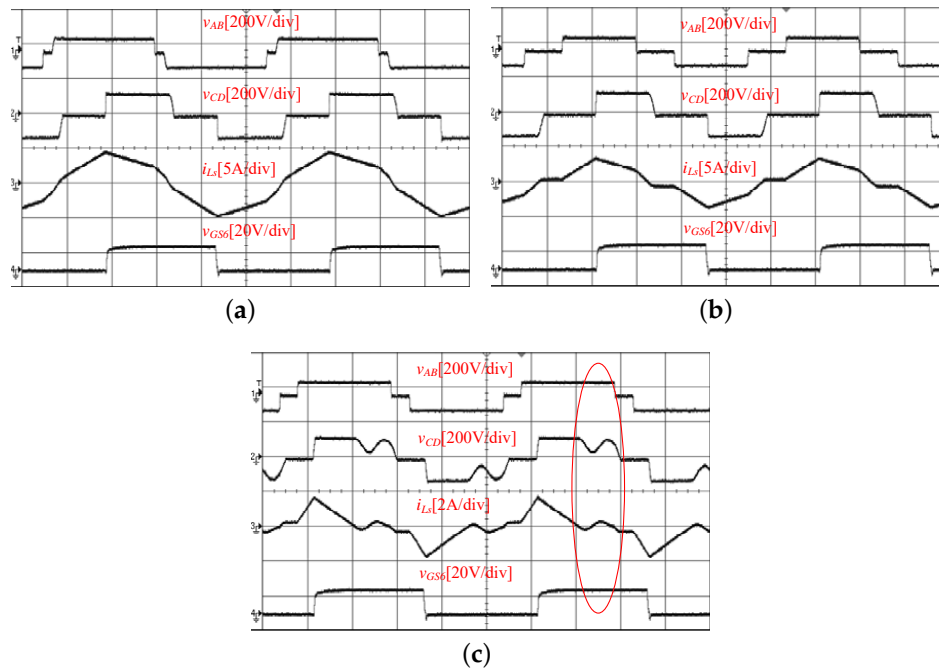


Figure 11. Experimental waveforms of v_{AB} , v_{CD} , i_{LS} and V_{GS6} (from top-bottom), time scale: (2 μ s/div), (a) Mode A; (b) Mode B; (c) Mode C.

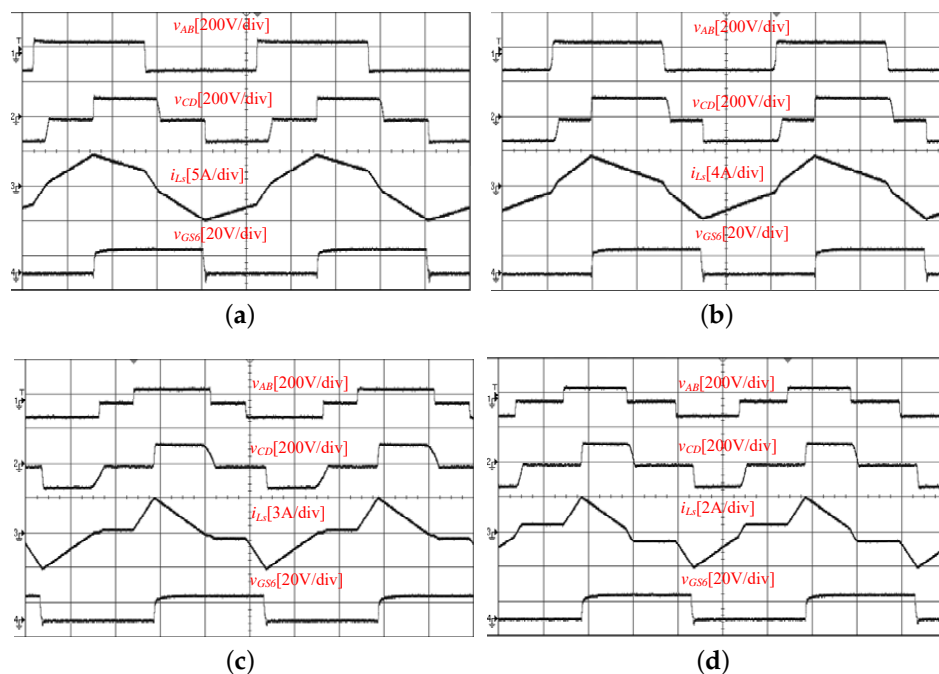


Figure 12. Experimental waveforms at four different power levels under the proposed route for $V_{in} = 80$ V and $V_o = 120$ V, time scale: (2 μ s/div), (a) 200 W; (b) 150 W; (c) 100 W; (d) 50 W.

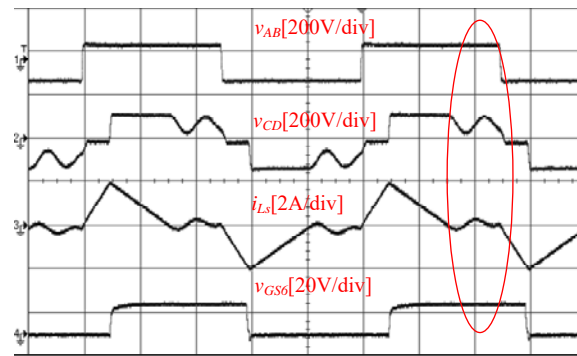


Figure 13. Experimental waveforms at 50 W with conventional secondary phase-shifted control.

Table 5. Measured results at $V_{in} = 80$ V and $V_o = 120$ V.

Power		$I_{Ls,rms}$ (A)	$I_{Ls,peak}$ (A)	η (%)
200 W	theor.	2.9	4.52	-
	exp.	3.08	4.7	94.97%
150 W	theor.	2.14	3.63	-
	exp.	2.19	3.63	95.53%
100 W	theor.	1.57	2.96	-
	exp.	1.58	2.92	92.13%
50 W	theor.	0.94	2.1	-
	exp.	0.95	2.07	88.95%

5. Conclusions

In this work, PPWM + SPS control with two controllable phase-shifts is applied on an S-DAB converter for boost operation and all effective steady-state modes are identified. Based on the characteristics of each mode, a reasonable control route is developed and implemented on a lab-scale S-DAB prototype. The experimental results show the consistency with the theoretical analysis results. Compared with conventional secondary phase-shifted control, the proposed control route not only makes the converter operate with the minimized RMS current for the whole power range, but also eliminates the voltage ringing on the secondary-side of the HF transformer completely. More importantly, the proposed hybrid control can be also applied on the other S-DAB converters in [22–24] to prevent the voltage ringing and improve stability. In addition, other optimization objectives could be developed according to various application requirements.

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