

Article

A Bandwidth-Enhanced Differential LC-Voltage Controlled Oscillator (LC-VCO) and Superharmonic Coupled Quadrature VCO for K-Band Applications

Farman Ullah ^{1,2,3}, Yu Liu ^{1,2,*}, Zhiqiang Li ^{1,2}, Xiaosong Wang ^{1,2},
Muhammad Masood Sarfraz ^{1,2,3} and Haiying Zhang ^{1,2}

¹ Beijing Key Laboratory of Radio Frequency IC Technology for Next Generation Communications, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; farman@ime.ac.cn (F.U.); lizhiqiang@ime.ac.cn (Z.L.); wangxiaosong@ime.ac.cn (X.W.); mmasood@ciitwah.edu.pk (M.M.S.); zhanghaiying@ime.ac.cn (H.Z.)

² Institute of Microelectronics, University of Chinese Academy of Sciences, 19A Yuquan Rd., Shijingshan District, Beijing 100049, China

³ COMSATS University, Wah Campus, G. T. Road, Wah Cantt 47040, Pakistan

* Correspondence: liuyu5@ime.ac.cn; Tel.: +86-108-299-5811

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Abstract: A novel varactor circuit exhibiting a wider tuning range and a new technique for quadrature coupling of LC-Voltage Controlled Oscillator (LC-VCO) is presented and validated on a 25 GHz oscillator. The proposed varactor circuit employs distribute-biased parallel varactors with a series inductor connected at both ends of the varactor bank to extend the tuning range of the oscillator. Similarly, the quadrature coupling is accomplished by employing the 2nd harmonic, explicitly generated in the stand-alone free-running differential oscillator using frequency doubler. As an example, the Differential VCO (DVCO) is tunable between 20 GHz and 31 GHz and exhibits the best Phase Noise (PN) of -100 dBc/Hz at 1 MHz offset frequency. Similarly, the Quadrature VCO (QVCO) covers 42% tuning bandwidth around 25 GHz oscillation frequency, which is significantly wider than other state-of-the-art VCOs at comparable frequencies. In addition, all the oscillators are designed in class-C to further improve their performances both in term of low power and low phase noise. The presented oscillators are designed using high-performance SiGe HBTs of the GlobalFoundries (GFs) 130 nm SiGe BiCMOS 8HP process. The presented DVCO and QVCO draw currents of approximately 10 mA and 21 mA, respectively from a 1.2 V supply.

Keywords: millimeter wave oscillator; wideband VCO; superharmonic coupling; QVCO; oscillation bandwidth; varactor

1. Introduction

Modern wireless communication is transforming into future 5G and the demand for high data-rate communication with increased bandwidth requirements is increasing. Voltage Controlled Oscillator (VCO) as one of the key components is used in modern phase-locked loop (PLL) to provide local frequency signal. It is critical for VCOs that can robustly provide wider tuning range (TR) at mm-wave frequency region with low phase noise. To date, many oscillators featuring low-power consumption (P_{DC}), low phase noise (PN) and wide TR in K-band have been reported [1–8]. However, it is still challenging and uncommon to design VCO with optimized trade-off to simultaneously achieve a wide TR with low PN and low P_{DC} . For example, in [1], two K-band SiGe bipolar VCOs using transformer-coupled varactors are presented. But they can only be tuned from 18.6 to 21.2 GHz and 20.4 GHz to 24.2 GHz, resulting only in 13% and 17% tuning ranges, respectively. Similarly,

triple-couple inductor as part of the LC-Tank, to couple multiple varactors, is implemented to get more linear and wider TR , but only 15.8% TR is achieved at K -band [2]. In [3], the reported differential VCO utilizes current-reuse and transformer-feedback techniques fabricated in the standard bulk 90 nm CMOS process, can only achieve 4.8% tuning bandwidth at K -frequency band. Similarly, various Negative Capacitance (NC) circuits were integrated with traditional LC-VCOs to cancel out the parasitics (produced mainly by the LC-tank and cross-coupled pair) to expand the TR [9,10]. For example, in [9], the NC circuit is used to shift the oscillation frequency from 20.1 to 31.6 GHz, which, although it improves the $TR\%$ from 5.7 to 12.4%, it makes the power consumption too high (590 mW) and worsens the phase noise to -88 dBc/Hz. Similarly, a tunable differential NC circuit was designed in [10] to compensate the parasitic capacitances and is realized by connecting the NC circuit to the source of the cross-coupled transistors of the LC-VCO; however, it affected the start-up condition. Therefore, the NC of [10] only had a small effect on the resonance frequency (f_{RES}) and TR .

Similarly, the Quadrature Voltage Controlled Oscillators (QVCOs) play an important role in many fully-integrated, low cost, radio-frequency transceivers requiring I/Q modulation/demodulation. To provide Quadrature Local Oscillator (LO) signals, various techniques are endorsed. Two approaches are very common for quadrature LO generation: (1) divide-by-two [11] and (2) polyphase filter techniques [12]. However, the earlier is more power hungry since the system oscillator needs to be operated at twice the desired frequency, while the later suffers from low quadrature accuracy as well as requiring an additional buffer to boost the output power. Later, the LC-based QVCOs are presented for the generation of quadrature LO signals without employing divide-by-two or polyphase filters, which resulted in huge reductions in power consumption as well as improved accuracy [13].

LC-based QVCOs are obtained by employing antiphase coupling between two identical differential oscillators. The antiphase connection is realized using a coupling network, either an active or passive coupling. The circuit techniques employing active coupling are parallel coupling (P-QVCO) [13], series coupling (S-QVCO) [3], top- and bottom-series coupling (TS-QVCO and BS-QVCO) [14], sub- and super-harmonic coupling [15,16], body-biased coupling [17], In-phase injection-coupling [18], complementary coupling [19] etc. Similarly, passive coupling techniques like inductor-based superharmonic coupling [20], transformer coupling [21], and coupling using transmission lines [22] are used for quadrature LO generation.

Firstly, we emphasized to attain wider TR at K -frequency band. To realize this, we proposed a novel varactor circuit that consists of two similar branches of varactors, biased at different voltages. They are also cascaded with two inductors, each connected to the common nodes of the varactor bank at both sides. The proposed varactor scheme exhibits wider TR at mm-wave frequency. Besides, the TR of the VCO is enhanced by properly designing the VCO-core and aligning the consecutive frequency tuning characteristics with sufficient overlap margin to avoid blind zones between them. In addition, a novel technique for quadrature generation is proposed in this work. Subsequently, the two similar bandwidth-enhanced differential oscillators that we proposed in our first work are locked in quadrature by implementing the proposed quadrature generation technique. Hence, both the differential and quadrature VCOs cover a minimum of 42% bandwidth around 25 GHz with total power consumptions of 12 mW and 25 mW, respectively from 1.2 V supply.

The rest of the paper is organized as follows. The technical arguments for the selection of an appropriate fabricating technology as well as the LC-oscillator topology based on their inherent PN and power consumption characteristics are outlined in Section 2. Section 3 describes the TR and design implementation of the proposed varactor circuit. Section 4 reports the post-layout simulation results of the differential and quadrature oscillators, both integrated with proposed wideband varactor circuit. The entire work is finally concluded in Section 5.

2. Design Consideration for Low PN and Wideband VCO

2.1. Technology Overview

Moving up with frequency, the losses increase intensively and requirements of the communication systems become more and more rigorous. So, the devices must have higher f_t and higher power handling capabilities in order to meet the stringent requirements of the communication systems. State-of-the-art SiGe BiCMOS technology can stand as the best candidate for its excellent performance, featuring high f_t/f_{max} , high reliability and extended temperature range, making this technology a potential candidate for mm-wave circuit designs.

The VCO, as part of the frequency synthesizer, is a key building block in high performance wireless and wireline communication systems. Previously, integrated mm-wave VCOs have been designed using either GaAs or other III-IV technologies [23,24]. But there has always been an interest to develop Si-based mm-wave VCOs due to its lower fabrication cost and that it can be easily scaled compared to III-IV technologies [25,26]. In addition to the implementation cost and system integration, the SiGe BiCMOS provides the degree of freedom by using MOSFET and HBTs in the same integrated circuits making this technology very appropriate for designing high-performance RF circuits with digital logics on the same substrate. Moreover, SiGe HBTs provide high gain and improved noise performance at extremely low current densities. Also, with lower $1/f$ noise, four times better transconductance and higher breakdown voltage (for the same f_{max}), the BiCMOS technology stands as an appropriate technology for the design of high performance VCOs and power amplifiers etc. The proposed wide TR mm-wave VCO has been designed using 130 nm SiGe BiCMOS technology and is intended to be integrated in a complete frequency synthesizer for K-band applications.

2.2. Class-C

Among several VCO topologies, LC-VCO topology with core transistors operating in Class-B and Class-C are implemented for low PN and wide TR. However, for the same power consumption, 3.9 dB improvement on PN is expected when compared to Class-B [27]. Depicted in Figure 1a, is a typical arrangement of Class-C oscillator in which the base of one transistor in the cross-coupled pair is ac-coupled from the drain of the other, using C_{bias} . In addition, a common dc-bias is applied at the bases of cross-coupled transistors. With this arrangement, the average maximum voltage on the cross-coupled pair can be observed much smaller in Class-C than in Class-B, thereby preventing the core transistors to enter into the saturation region, hence results in better phase noise. However, depending on whether or not the large tail capacitance C_{tail} is connected to the common node of transistors Q1 and Q2, the oscillator is operated fully in Class-C or Class-B [27]. A detailed comparative study of class-B and class-C oscillators has been carried-out in [28].

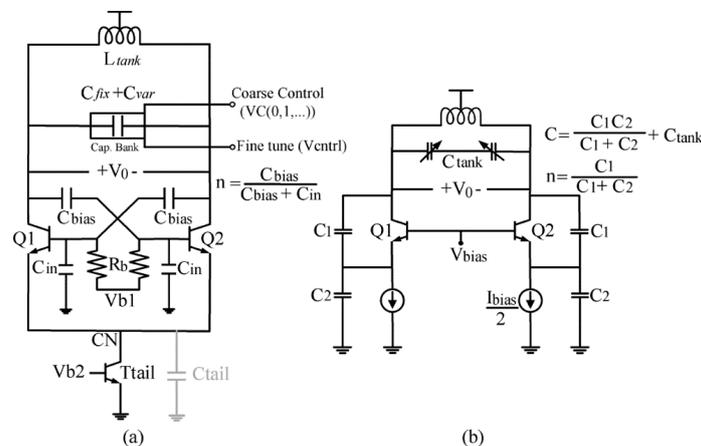


Figure 1. Standard schematics of (a) class-C and (b) differential Colpitts oscillators.

Another oscillator topology that can be widely used for high-frequency applications and particularly in the application of bipolar oscillators, is the Colpitts oscillator (see Figure 1b). A comprehensive analysis of phase noise in bipolar Colpitts oscillator as well as its comparison with Class-B oscillator is conducted in [29]. This comparative study is carried out by assuming the oscillator to operate in current-limited regime for a given tank impedance and bias current. However, when the analysis is extended to maximize the oscillation amplitude, a better phase noise is achieved. Nevertheless, the Colpitts oscillator can also be allowed to decrease its phase noise by setting the feedback factor “ n ” (from tank to the BJT emitter) high; but this would result in large power consumption and less efficiency [30]. Hence, it can be concluded that among the aforementioned topologies we discussed, Class-C LC-Oscillator is a superior topology over others in terms of low power and low PN for a given tank impedance, supply voltage and oscillation frequency, which has been chosen for our design.

Low PN is another significant measure of the oscillator. Single-sideband Phase noise (L) of a generic harmonic oscillator at an offset frequency ($\Delta\omega$) from the carrier can be expressed as (1) [31].

$$L(\Delta\omega) = \left(\frac{\omega_0}{\Delta\omega}\right)^2 \left[\frac{k_B T R_S}{V_0^2} (1 + F) \right] \quad (1)$$

where k_B and T are the Boltzmann constant and temperature, respectively. R_S , V_0 , F and ω_0 denote the inductor’s parasitic series resistance, oscillation amplitude, noise factor and oscillation frequency, respectively. It can be stated by looking at (1) that the phase noise decreases as the dissipated power “ P_{DC} ” is increased at an offset frequency $\Delta\omega$. Moreover, an oscillator topology, yielding low noise factor “ F ” and providing a high amplitude oscillation “ V_0 ” will further help to reduce the phase noise.

3. Circuit Description

The traditional Class-C oscillator arrangement depicted in Figure 1a, consists of a dc-biased cross-coupled transistors pair, a varactor, fix capacitor bank and an inductor. If the differential transconductance produced by the cross-coupled transistors compensates the tank losses, then the frequency of oscillation will be given by (2).

$$f_{RES} = \frac{1}{2\pi \sqrt{L_{tank} \left(\sqrt{C_{Var} + C_{fix}} \right)}} \quad (2)$$

where C_{Var} and C_{fix} represent the capacitances of the varactor and switched-capacitor bank, respectively, that are responsible to coarsely control and finely tune the oscillation frequency. The coarse control of the oscillation frequency can be accomplished using the input control voltage correspond to VC (0, 1, ...), while the fine tuning of the oscillation frequency can be done using V_{ctrl} .

3.1. Varactor

Varactor is employed to tune the oscillation frequency of the oscillator by changing the control voltage across it. For a varactor, the two parameters are very important: (a) the capacitance range i.e., the ratio of the maximum and minimum capacitances that the varactor can provide as the applied voltage is varied, and (b) the quality factor, which is limited by the series resistance within the varactor structure [32]. These two parameters exhibit a trade-off as the frequency goes high, i.e., when the capacitance is increased, the quality factor is decreased. To employ a high Q varactor, the channel length must be minimized. However, for a minimum channel length, the overlap capacitance between the gate and source/drain terminals becomes relatively large, hence limiting the TR . On the other hand, to get the wider TR , the size of the varactor is increased. However, it is not feasible at high frequencies e.g., at 25 GHz, since the contribution of the capacitive part of the tank is more significant in K -band. Particularly, the varactor quality factor degrades intensively if the size of the varactor is set

too high, which may dominate the resonator loss and hence dissatisfy the startup oscillation condition. In order to re-start the oscillation, one may increase the core transistors size, but again, the size of the core transistors cannot be set too large due to the parasitics they add to the tank, which would, in turn, increase the C_{fix} , degrading the TR and tensing the already limited capacitance budget. In summary, it is difficult to achieve high Q and wide TR simultaneously.

Previously, the two types of varactors named as p-n junction diode and n-type accumulation mode-MOS A-MOS varactors are employed for the implementation of wideband VCOs. The p-n diode fundamentally works in reverse bias and it needs to be properly biased with the tank to avoid the forward biasing. One possible formation is shown in Figure 2a, called direct-coupling. However, the critical limitation of this structure is that V_{ctrl} always needs to be higher than the supply voltage to limit the forward biasing. Otherwise, the junction will turn-on and the quality factor will drop significantly. Another type of varactor that is mostly adopted to tune the oscillation frequency is the nMOS varactor. The BiCMOS 8HP process provides a standard thin oxide nMOS varactor for differential circuits. Presented in Figure 2b (left) is the cross-section view and its corresponding differential version of the varactor that can be employed as a variable capacitor. The variable capacitance is achieved as the device is biased from depletion to accumulation [33,34].

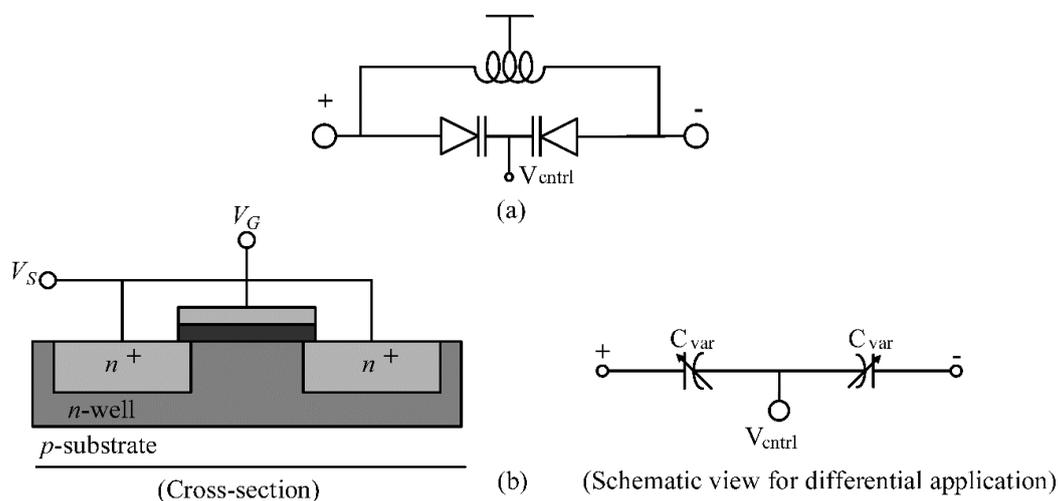


Figure 2. Schematics of (a) tank-coupled p-n diode, (b) n-type A-MOS varactor cross-section and its corresponding schematic view for differential applications.

Regardless the type of varactor used in the oscillator, their conventional structure always suffers from the limited TR .

3.2. Proposed Varactor Circuit Implementation

It is aimed to attain the widest possible TR around 25 GHz oscillation frequency. To realize a wideband VCO, a wideband varactor circuit shown in Figure 3b is proposed exhibiting an extended TR . Unlike the conventional design shown in Figure 3a, the proposed design consists of two similar branches of varactors connected in parallel. Each varactor pair is RC -biased at a different bias voltage generated through the resistive divider circuit. Equal step of biasing voltage is chosen from 1.2 V supply. Hence $Vb1$ and $Vb2$ are chosen as 0.4 V and 0.8 V, respectively. Thus, the steep part of each characteristic curve in the entire TR is centered on its corresponding biasing voltage, thereby presenting a more stretched capacitance over the entire voltage control range. In addition, two inductors each at both ends (in series to the varactor bank) are added to extend the TR . The series connection of inductors improves the C_{max}/C_{min} ratio of the varactor bank and also cancels the parasitic capacitances introduced by the parallel varactor branches leading to achieve even more wider TR . The varactor's series inductors (L_L & L_R) in Figure 3b have significant effects on the VCO's operating frequency as

well as the tuning range, since they are in parallel to the tank inductor (L_{Tank}). The TR can be increased or decreased by respectively increasing or decreasing the value of series inductors. However, a very large value inductor may dissatisfy the startup of the oscillator as well as the desired center frequency able to go lower. Likewise, a very small value inductors exhibit small capacitance and thus presenting narrower tuning range. Therefore, the series inductors need to be decided based on the desired center frequency as well as the required tuning range. In our designed oscillators, 136 pH inductors are selected to optimize the oscillator center frequency around 25 GHz with tuning range from 20 GHz to 31 GHz.

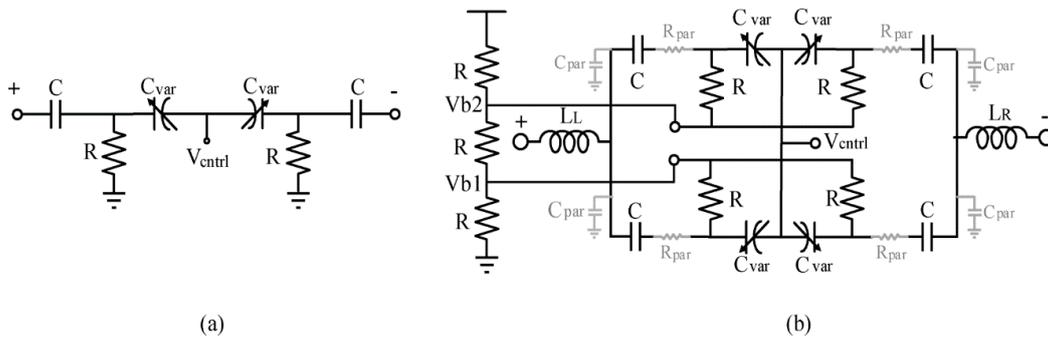


Figure 3. Schematics of the (a) conventional and (b) proposed wideband varactor with parasitics highlighted.

Comparison of the same and single frequency tuning characteristic, based on proposed and traditional varactor circuits, is presented in Figure 4. The proposed tuning circuit when incorporated in class-C LC-VCO (see Figure 7) resulted in an overall wider TR .

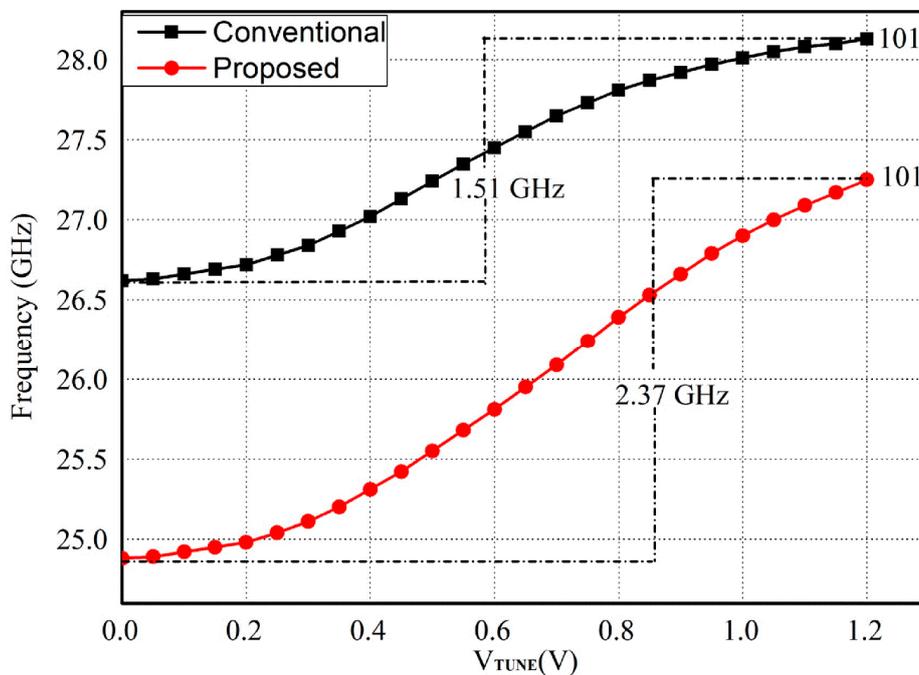


Figure 4. Simulated single frequency tuning characteristic using conventional and proposed varactors.

The simulation result of Figure 4 is performed by first implementing the conventional varactor circuit with two identical branches in parallel with a common biasing voltage. Then, the same number of varactor branches as in conventional design, are implemented in the proposed varactor circuit so that

the overall capacitance in both cases are maintained. By implementing the proposed varactor circuit, the covered frequency range is considerably extended more than the range covered with the traditional varactor circuit. The range covered based on typical and proposed varactors are 1.51 GHz and 2.37 GHz respectively, which is 56% more wider than the baseline TR . These analyses are based on when the input control word to the capacitor bank is 101 which corresponds to VC_0 , VC_1 , VC_2 , respectively. Of course, it will accordingly change as we choose the bottom and top tuning characteristics in the whole TR .

Plots in Figure 5 represent the $F(V)$ curves of the same discrete tuning curve with different biasing voltage combinations applied to the varactors. Based on the most widely covered tuning bandwidth, we chose the varactor biasing voltage as 0.4 V and 0.8 V as V_{b1} and V_{b2} , respectively.

Next, the performance of both the oscillators will be discussed. All simulation results presented in the following section are done with post-layout.

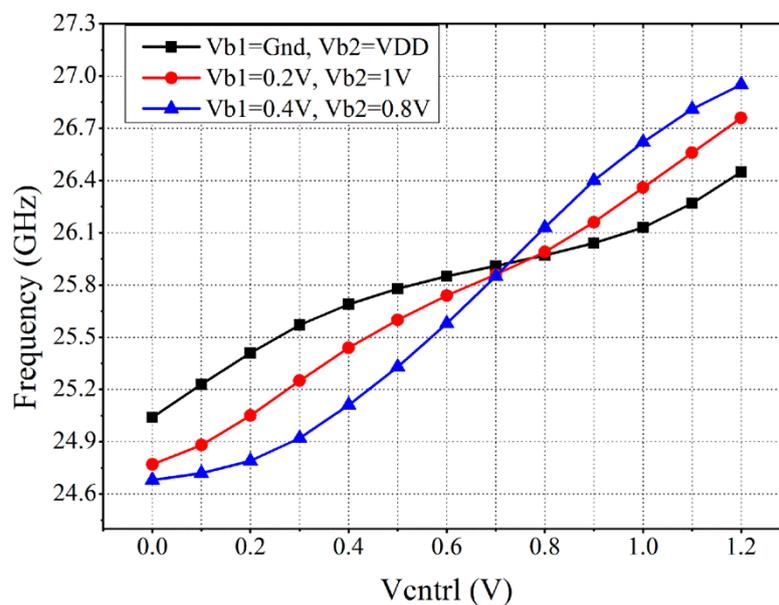


Figure 5. Distributed Biasing of the varactor bank.

4. Post-Layout Simulation Results and Discussion

The designed prototype of differential and quadrature VCOs are presented in Figure 6, with total covered area (including bond pads) of 0.45 mm² and 0.7 mm², respectively. Their corresponding schematic circuits are provided in Figure 7 and Figure 9.

4.1. Differential VCO (DVCO)

A schematic of the proposed differential VCO with integrated wideband varactor circuit is shown in Figure 7. The LC -tank consists of an inductor ($L_{Tank} = 130$ pH), 3-bit switched capacitor bank and the proposed wideband varactor bank. The LC -tank resonator oscillates the desired frequency at the differential output, which is controlled by the control voltage of the varactors (V_{ctrl}). The fine control provides a continuous change in frequency, whereas the coarse control shifts the continuous characteristic up or down. Fixed capacitance is added between the differential outputs (VCO_P and VCO_N) of the oscillator by the NMOS transistor switches (Sw_1 , Sw_2 , Sw_3) as shown in Figure 7 [35]. Depending on the gate voltage applied at $VC(n)/VC(0, 1, 2)$, the switches are turned on or off to add the capacitance in or out from the tank. The switches add parasitic resistance when turned on, thereby degrading the PN of the oscillator. Likewise, add parasitic capacitance when turned off, reducing the TR . The DC -biased cross-coupled transistors (T_1 and T_2) generate the negative transconductance

to cancel the parallel tank-resistance to sustain the oscillation. A large biased tail transistor (T_{tail}) is connected to the common-emitter node (CN) of $T1$ and $T2$ to control current in the circuit.

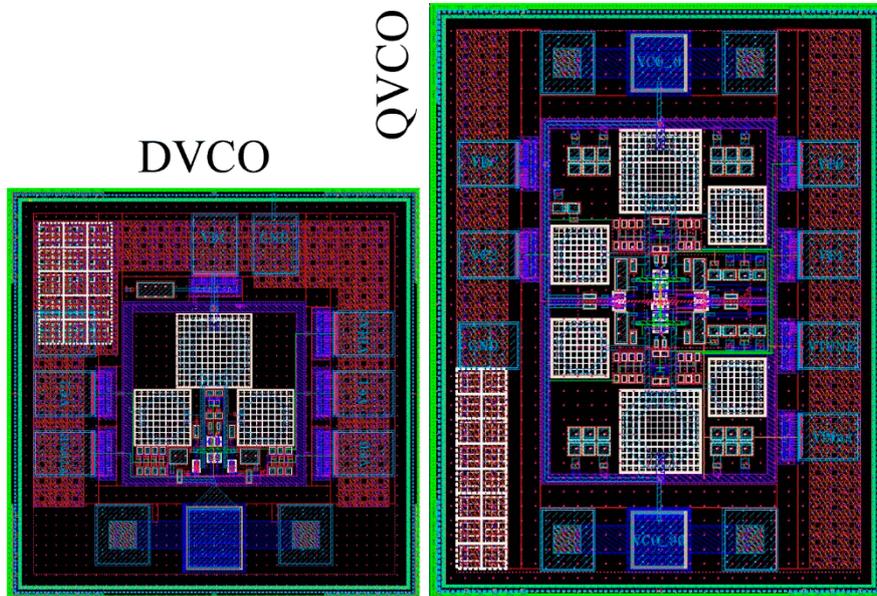


Figure 6. Physical layouts of the designed oscillators.

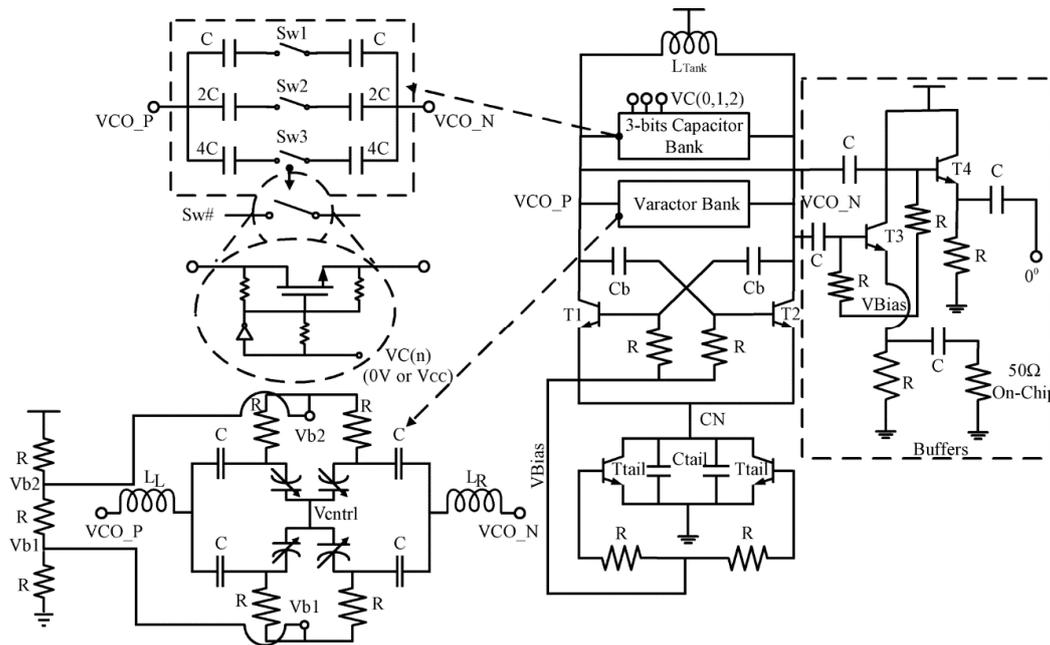


Figure 7. Complete schematic of a Differential Voltage Controlled Oscillator (DVCO) incorporated with proposed wideband varactor circuit.

A differential emitter follower buffer, composed of $T3$ and $T4$ with the input/output capacitances is connected to the differential output of the oscillators in order to prevent the VCO from the loading effect posed by the external circuitry or measuring equipment. The buffer shown in the schematic provides low output impedance to the instrumentation while measuring the output at the emitter, provided that the VCO output is not adversely affected under load. The buffer capacitances (capacitors between the VCO outputs and $T3$ and $T4$) are carefully selected since these capacitances would add

extra parasitic capacitance to the tank and would limit the maximum operating frequency of the VCO. Shown in the proposed VCO schematic, one of the two outputs are terminated with on-chip 50 Ω resistor while the other is left isolated to connect with GSG probe for measurement purpose.

For maximum frequency, the size of the varactor has to be carefully chosen as a trade-off between Q_C and capacitance ratio, since the overall quality factor of the tank is affected both by the inductive and capacitive elements as depicted in (3).

$$\frac{1}{Q_{TOT}} = \frac{1}{Q_C} + \frac{1}{Q_L} \quad (3)$$

At frequencies <10 GHz, usually, the inductor quality factor (Q_L) is the major contributor to the overall tank quality factor (Q_{TOT}). However, at frequencies >20 GHz, Q of the varactor ($Q_C \sim (\omega R_s C)^{-1}$) also decreases significantly, while that of the inductor ($Q_L \sim (\omega L_s / R_s)$) increases with frequency. Also, due to the intrinsic behavior of the varactor, it is difficult to obtain high Q and large C_{max}/C_{min} ratio simultaneously to achieve better VCO performance [36]. The proposed varactor circuit to a large extent breaks the “ Q ” and “ C_{max}/C_{min} ” trade-off and achieves large capacitance ratio. Keeping “ Q ” and “ C_{max}/C_{min} ” trade-off in view, we fixed the varactor size for its optimized performance. In our work, the varactor biasing voltages ($V_{b1} = 0.4$ V, $V_{b2} = 0.8$ V), the capacitance ratio ($C_{max}/C_{min} = 3.88$) branch capacitances (104 fF) and two series inductors, each one of 136 pH are chosen to balance the Q for its widest possible TR at K-band; provided a wider TR from 20 GHz to 31.1 GHz as shown in Figure 8.

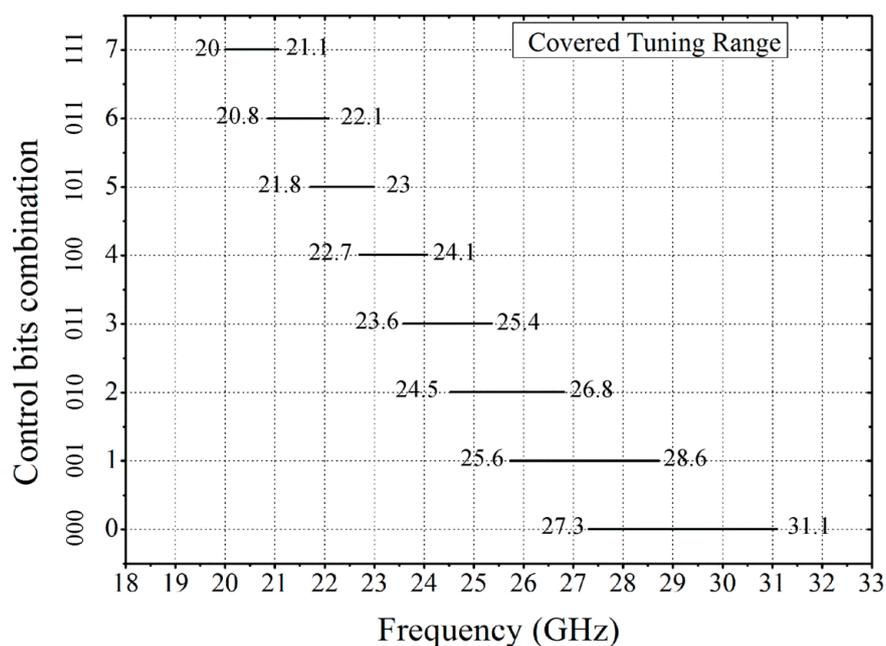


Figure 8. Voltage Controlled Oscillator (VCO) output frequency as a function of the capacitor bank control word.

4.2. Quadrature VCO Using Superharmonic Coupling

The proposed Quadrature VCO (QVCO) is designed using the differential VCO presented in Section 4.1. This section presents the quadrature VCO based on superharmonic coupling. Unlike classical LC-QVCOs, this technique cross-injects the 2nd order harmonic at the oscillator common-mode node to enforce the two free-running differential oscillators oscillate in quadrature, i.e., the 2nd order harmonic generated through oscillator 1 using frequency-doubler is injected at the common-mode node of the oscillator 2 and vice versa.

Intrinsically, the cross-coupled LC-VCOs generate the fundamental and 2nd order harmonic frequency components that appear at the differential path and common-mode nodes of the oscillator, respectively. As stated earlier, numerous techniques are proposed to injection-lock the oscillators using fundamental frequency components. Similarly, if an anti-phase relationship between the two oscillators at the 2nd order harmonic is established, then the oscillators can also be locked in quadrature. As an example of superharmonic coupling [11], the two LC-VCOs are locked to oscillate in quadrature when an anti-phase signal with frequency $2f_0$ is injected at the common-mode node of the coupling oscillators. Hence the QVCO can be understood as an injection-locked frequency divider. However, the technique presented in [11] requires an external signal source running at twice the desired frequency. Unlike the injection-locked LC divider presented in [11], this work employs a SiGe HBT frequency doubler designed by taking the fundamental signal at the base of the transistors (T5 to T9) and generate the 2nd harmonic frequency at their common-emitter nodes. The bases of these transistors are AC-coupled and DC-biased with sufficient voltage. In our design, we applied a common bias voltage to all the biasing points in the circuit in order to maintain low power and allow less number of external DC voltage sources.

The output obtained from common-emitter node of the frequency doubler (T5, T6) in oscillator 1 is injected at the common-emitter node of the cross-coupled transistors (T3, T4) of oscillator 2. Similarly, the same connection is made from oscillator 2 to oscillator 1. Thus, if both LC-VCOs are matched, then owing to symmetry their differential outputs have to be in quadrature.

The presented QVCO is composed of two identical VCOs, each one integrated with the proposed wideband varactor circuits. As discussed in Section 3, the fundamental oscillation is available over a significantly wide frequency bandwidth i.e., 20 GHz to 31 GHz. Since the SiGe HBT frequency doubler also senses the fundamental oscillation of the proposed wideband DVCO, the 2nd order harmonic generated by the doubler is also available over a wide frequency range. So, unlike the LC dividers and injection-locked techniques, the proposed oscillator does not suffer from a limited locking range. Schematic of the proposed QVCO is presented in Figure 9.

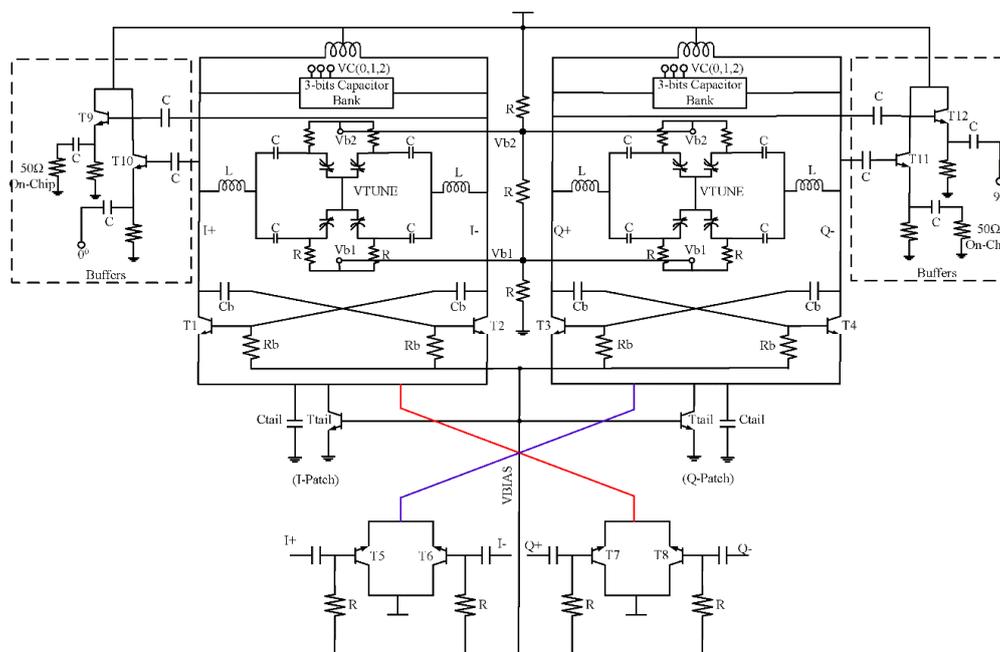


Figure 9. A simplified schematic of the superharmonically coupled Quadrature Voltage Controlled Oscillator (QVCO) with proposed wideband varactor circuits.

Using the proposed coupling technique, the post-layout simulated *PN* of the QVCO demonstrated in Figure 10 is better than its half part. In fact, the *PN* of the QVCO is always better than DVCO in the entire tuning bandwidth as demonstrated in Figure 11. Here, the *PN* values are taken from various frequencies interpreted by various combinations of control voltages applied to the capacitor bank. Hence, it can be established that the *PN* variation in the entire tuning bandwidth is around 7 dB and 3.3 dB and is always less than -93.1 dBc/Hz and -97.5 dB/Hz for DVCO and QVCO, respectively. In addition, the *PN* is better in lower part of the oscillator’s covered bandwidth and it is deteriorated as the oscillator reaches to its maximum attainable frequency.

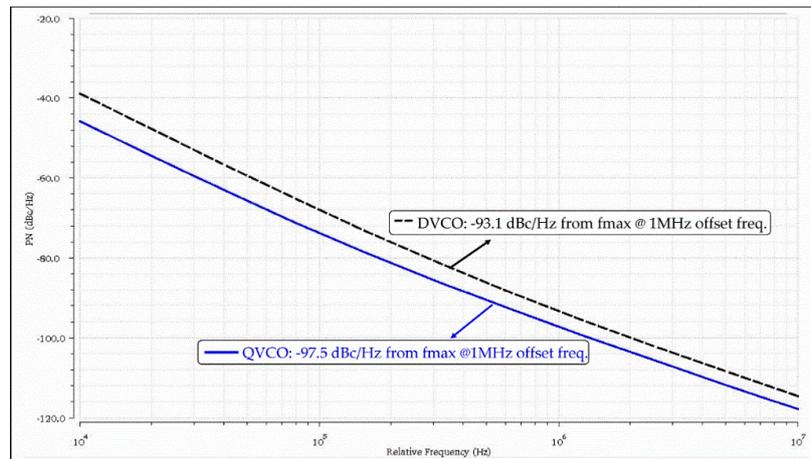


Figure 10. *PN* plot of DVCO and QVCO at an offset range from 10 KHz to 10 MHz highlighting *PN*s from their corresponding maximum carriers.

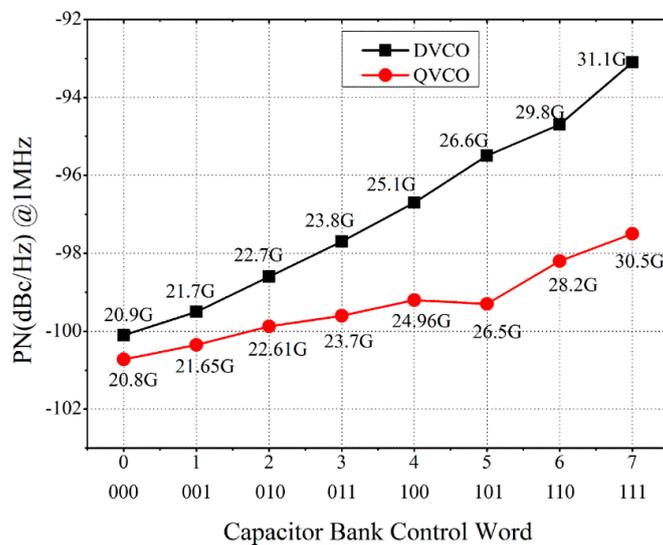


Figure 11. *PN* plot of DVCO and QVCO at 1 MHz offset frequency in the entire *TR*, representing oscillation frequency taken at various capacitor bank control word.

To evaluate the performance of the designed oscillators, a widely accepted Figure-of-Merit (*FoM*) is presented in (4).

$$FoM = L\{\Delta f\} - 20 \log\left(\frac{f_0}{\Delta f}\right) + 10 \log\left(\frac{P_{DC}}{1mW}\right) \quad (4)$$

where Δf , f_0 and P_{DC} are the offset frequency from the carrier, center oscillation frequency and total power, consumed by the core oscillator, respectively.

The FoM is considered to be better with more negative values. In addition to (4), a more widely used expression for FoM is presented to consider the TR of the VCOs as expressed in (5).

$$FoM_T = FoM - 20 \log \left(\frac{FTR(\%)}{10} \right) \quad (5)$$

where the FTR is “Frequency Tuning Range” covered by the oscillator as the tuning voltage is varied, which is calculated using (6).

$$FTR(\%) = \left(\frac{f_{max} - f_{min}}{f_{Center}} \right) * 100\% \quad (6)$$

f_0 or f_{Center} is the oscillator center frequency that can be calculated as

$$f_{Center} = \frac{f_{max} + f_{min}}{2} \quad (7)$$

Getting advantage of wide TR , we calculated FoM with TR (FoM_T) for fair comparison. Tables 1 and 2 summarize this work and other state of the art published K/K_a band oscillators.

Table 1. Comparison of reported K/K_a band DVCOs and this work.

Ref.	f_0 (GHz)	$PN@1$ MHz (dBc/Hz)	P_{DC} (mW)	FTR (%)	FoM_T	Process
[1]	22.7	−114	18	17	−193	SiGe HBT
[2]	20.85	−100.7	8.1	15.8	−181.8	90 nm CMOS
[3]	20.8	−116.4	3	4.8	−191.6	90 nm CMOS
[4]	24.27	−100.33	7.8	2.2	−179	0.18 μ m CMOS
[5]	32.55	−97	19	18.1	−180	0.13 μ m SiGe BiCMOS
[6]	21.5	−113	130	4.6	−171.8	0.25 μ m SiGe
[7]	23	−100	4	2	−181	0.13 μ m CMOS
[8]	24.5	−95.5	1.7	16.8	−185.4	0.18 μ m CMOS
[10]	40	−95	12	27	−184.9	0.13 μ m CMOS
[30]	21	−119	70	20	−194	SiGe BiCMOS
Our Work	25.5	−96	12	43	−186	0.13 μ m SiGe BiCMOS

Table 2. Comparison of reported K/K_a band QVCOs and this work.

Ref.	Coupling Method	f_0 (GHz)	$PN@1$ MHz (dBc/Hz)	P_{DC} (mW)	FTR (%)	FoM_T	I/Q Error	Process
[3]	Series	20.9	−117.2	6.3	3.1	−185.4	n/a	90 nm CMOS
[13]	Parallel	24.7	−111.6	24	4.3	−186	n/a	0.13 μ m CMOS
[21]	Transformer Coupled	20	−111.67	40.32	10.4	−181.5	1.5°	0.18 μ m CMOS
[22]	Transmission Line	33	−99	2.64	-	−183.7	n/a	0.12 μ m SiGe HBT
[25]	Series	25.3	−109	14.4	2.81	−185.5	1.8°	65 nm CMOS
[26]	Parallel	26.1	−114	24	3	−188.5	n/a	0.13 μ m CMOS
Our Work	Superharmonic Coupling	25.3	−99.2	25	42	−185.8	1.2°	0.13 μ m SiGe BiCMOS

5. Conclusions

In this paper, we presented a wideband differential VCO and superharmonically coupled QVCO, designed and simulated in 130 nm SiGe BiCMOS 8HP process for K -band applications. The proposed bandwidth-enhanced varactor circuit is implemented into the LC-VCO that resulted in wider TR . Further, the quadrature locking is accomplished at the common emitter node of the oscillator using BJT frequency doubler. The proposed quadrature technique exhibited better PN performance than its half circuit. Both designs are realized in class-C for improved PN performance. The designed VCOs can cover >42% tuning bandwidth around 25 GHz oscillation frequency, which is substantially wider than the VCOs operating at comparable frequencies. Among the reported VCOs that have been compared, our VCOs demonstrate a competitive FoM_T with the highest tuning bandwidth.

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