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More Discussions on Intrinsic Frequency Detection Capability of Full-Rate Linear Phase Detector in Clock and Data Recovery

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Abstract: The full-rate linear phase detector (PD) has not only phase detection capability but also single-sided frequency detection capability intrinsically. Previously, this fact has been discovered by researching the phase and frequency characteristics of the combined full-rate linear PD and charge pump (CP) under the condition that the ratio of the received data frequency (f_{DATA}) and the recovered clock frequency (f_{CLK}) is set as an integer number. In this paper, for completeness of the theory, the phase and frequency characteristics of the combined full-rate linear PD and CP are studied again while the ratio of f_{DATA} and f_{CLK} is set as a general rational number. Additionally, theoretical analyses of the lock-in range and the lock time of the referenceless single-loop clock and data recovery (CDR) including the full-rate linear PD are newly developed and verified. The calculated lock times by the analysis results agree well with the measured lock times from the MATLAB Simulink simulations.

Keywords: linear phase detector; frequency detection capability; clock and data recovery; CMOS integrated circuits

1. Introduction

To cover the wide range of data rates of the clock and data recovery (CDR) loops and to compensate for the process, voltage, and temperature (PVT) variations of clock frequency from voltage controlled oscillator (VCO), various frequency acquisition techniques have been utilized [1–9] in the serial data interfaces. However, most of these techniques originate from the thought that the phase detectors cannot detect the frequency difference between the received data and the recovered clock in the CDR loops.

Recently, it has been discovered in Reference [10] that the full-rate Hogge linear phase detector (PD) [11] has not only phase detection capability but also intrinsic single-sided frequency detection capability, and such that a referenceless single-loop CDR can be simply implemented by using only the full-rate linear PD without any frequency acquisition techniques. To prove this intrinsic frequency detection capability of the full-rate linear PD, several timing diagrams have been drawn at different clock frequencies specifically when the ratio of the received data frequency (f_{DATA}) and the recovered clock frequency (f_{CLK}) is set as an integer number and the phase and frequency characteristics of the combined full-rate linear PD and charge pump (CP) have been obtained [10]. However, if the ratio of f_{DATA} and f_{CLK} is not an integer number, we could not help but use interpolation between adjacent integer ratios and confirm the interpolated phase and frequency characteristics by providing many supportive MATLAB Simulink simulations. In Reference [10], we have also developed the frequency-locked loop (FLL) analysis to prove that the locking trajectory of the referenceless single-loop CDR utilizing the frequency detection capability of the full-rate linear PD is uniquely represented by

an exponential decay function with a single time constant. However, we could not derive in [10] the closed-form equations of the lock-in range and the lock time of the CDR loop theoretically.

In this paper, for completeness of the theory, the phase and frequency characteristics of the combined full-rate linear PD and CP are to be studied again while the ratio of f_{DATA} and f_{CLK} is not constrained to just an integer but extended to a general rational number. Additionally, theoretical analyses of the lock-in range and the lock time are to be newly developed for the referenceless single-loop CDR implemented by using only the full-rate linear PD without any frequency acquisition aids and verified by comparing the calculated lock times by the analysis results and the measured lock times from the MATLAB Simulink simulations.

Therefore, this paper is organized as follows. In Section 2, the phase and frequency characteristics of the combined full-rate linear PD and CP are presented when the ratio of f_{DATA} and f_{CLK} is set as a general rational number. In Section 3, theoretical analyses of the lock-in range and the lock time of the referenceless single-loop CDR including the full-rate linear PD are developed and verified by using the MATLAB Simulink simulations. The conclusion is given in Section 4.

2. Phase and Frequency Characteristics of the Combined Full-Rate Linear PD and CP

Figure 1 shows the referenceless single-loop CDR architecture including the full-rate linear PD, which is the so-called Hogge PD [11]. If θ is defined as the phase difference between the center of the received data (DIN) and the rising edge of the recovered clock (CLK) as shown in Figure 1, we have shown in Reference [10] that the full-rate linear PD outputs the up (UP) and down (DN) pulses of which pulse widths are $(2n-1)\pi+\theta$ and $n\pi$, respectively, per every n bits when $f_{CLK} = 1/n \times f_{DATA}$ and n is an integer number greater than or equal to 1. As the one bit duration of the received data is 2π, the CP output current can be represented as

$$I_{UP} - I_{DN} = \alpha\, I_{CP} \frac{(2n-1)\pi+\theta}{2n\pi} - \alpha\, I_{CP} \frac{n\pi}{2n\pi} = \alpha\, I_{CP} \frac{(n-1)\pi+\theta}{2n\pi} \text{ for } -\pi < \theta < \pi \quad (1)$$

where I_{UP} is the CP up current, I_{DN} is the CP down current, α is the bit transition density, and the current sources of the CP up and down paths are both equal to I_{CP}. Figure 2a,b show the timing diagrams when $n = 1$ and $n = 2$, respectively, for example. For ease of understanding, the rising and falling edges of the recovered clock are colored in red and green, respectively. In these timing diagrams, we can observe that θ is kept constant from bit to bit as time goes on because n is set as an integer number exactly. In Figure 2a,b, the UP pulse is null during $\pi - \theta$, which is equivalent to the time difference between the rising edge (in red color) of the recovered clock and the next bit transition of the received data. Thus, the UP pulse width is $2n\pi - (\pi - \theta)$ per every n bits. However, the DN pulse width is always $n\pi$ because it is equal to half of the recovered clock period per every n bits.

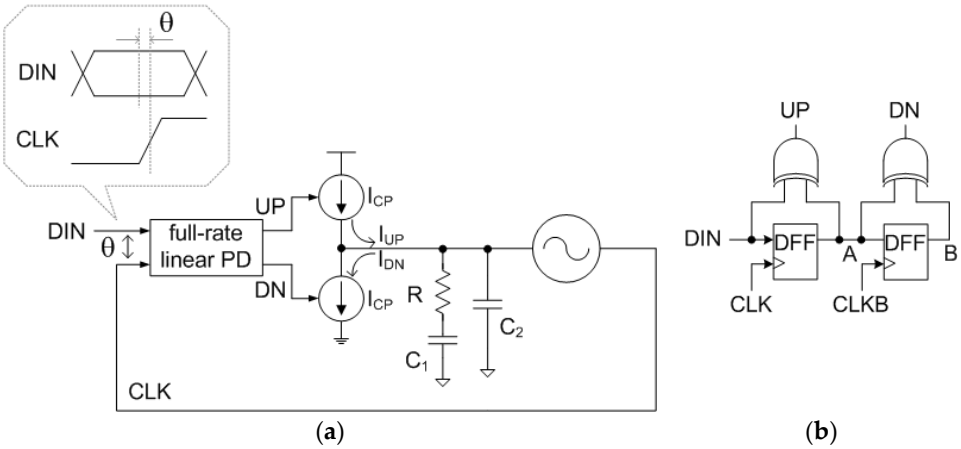

Figure 1. (**a**) The referenceless single-loop clock and data recovery (CDR) architecture including (**b**) the full-rate Hogge linear phase detector (PD).

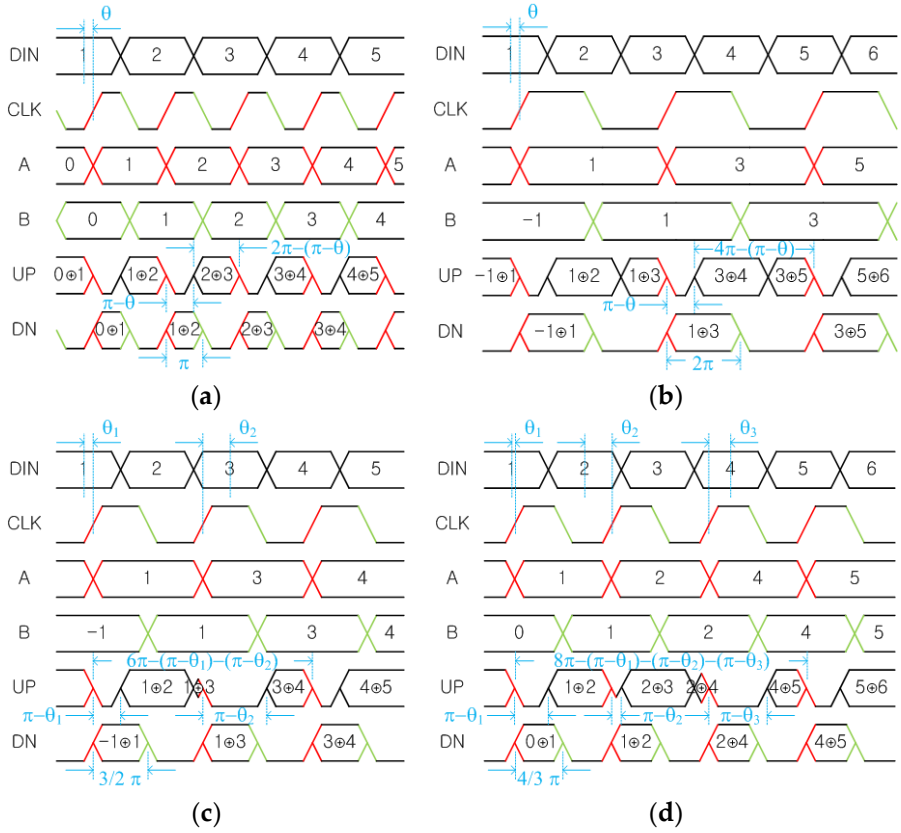

Figure 2. The timing diagrams of the full-rate linear PD when $f_{CLK} = 1/n \times f_{DATA}$ and (**a**) $n = 1$, (**b**) $n = 2$, (**c**) $n = 3/2$ and (**d**) $n = 4/3$.

By following the similar way, we can also derive the CP output current when n is set as a general rational number greater than 1. Since n is now a rational number greater than 1, $n = p/q$, $p > q$, and p and q are relatively prime integers. Then, we can find regularity in the UP and DN pulses by carefully observing the timing diagrams when n is set as rational numbers. Figure 2c,d show the timing diagrams when $n = 3/2$ and $n = 4/3$, respectively, for example. In these timing diagrams, it is interestingly observed that there are exactly q clocks and so q different $\theta \in \{\theta_1, \theta_2, \ldots, \theta_q\}$ in every p bits and that the UP pulse is null during $\pi - \theta$ again. Thus, the UP pulse width is $2\pi \times p - \sum_{i=1}^{q} (\pi - \theta_i)$ per every p bits and the DN pulse width is $\pi \times p$ per every p bits since the DN pulse is always null for half of the recovered clock period. Consequently, the CP output current can be represented in a simple form as follows.

$$I_{UP} - I_{DN} = \alpha\, I_{CP} \frac{2\pi \times p - \sum_{i=1}^{q} (\pi - \theta_i)}{2\pi \times p} - \alpha\, I_{CP} \frac{\pi \times p}{2\pi \times p} = \alpha\, I_{CP} \frac{\pi \times (p-q) + \sum_{i=1}^{q} \theta_i}{2\pi \times p} = \alpha\, I_{CP} \frac{(n-1)\pi + \frac{1}{q} \sum_{i=1}^{q} \theta_i}{2n\pi} \quad (2)$$

For the calculation of $\frac{1}{q} \sum_{i=1}^{q} \theta_i$ in Equation (2), we have to carefully consider the distribution of the rising edges of the recovered clock signals in Figure 3. Since $n = p/q$ is a rational number greater than 1, θ increases linearly within the range of $(-\pi, +\pi)$ as time goes on. Since θ is periodic for every q clocks such that $\theta_{i+q} = \theta_i$, θ is uniformly distributed over one bit period between $-\pi$ and $+\pi$ with the same space of $2\pi/q$ as shown in Figure 3. Accordingly, $\frac{1}{q} \sum_{i=1}^{q} \theta_i$ has the minimum value of $-\pi/q$ if the rising

edges of the clock signals are aligned as shown in Figure 3b and the maximum value of $+\pi/q$ if the rising edges of the clock signals are aligned as shown in Figure 3c. Thus,

$$\frac{1}{q}\sum_{i=1}^{q}\theta_i = -\frac{\pi}{q} + \theta - \left(-\pi + \frac{2\pi}{q}j\right) \text{ for } -\pi + \frac{2\pi}{q}j < \theta < -\pi + \frac{2\pi}{q}(j+1) \quad (3)$$

when $\theta \in \{\theta_1, \theta_2, \ldots, \theta_q\}$ and $j = 0, 1, \ldots, q-1$. Consequently, from Equations (2) and (3), the CP output current is represented by

$$I_{UP} - I_{DN} = \alpha\ I_{CP}\frac{(n-1)\pi - \frac{\pi}{q} + \theta - \left(-\pi + \frac{2\pi}{q}j\right)}{2n\pi} \text{ for } -\pi + \frac{2\pi}{q}j < \theta < -\pi + \frac{2\pi}{q}(j+1) \quad (4)$$

when $\theta \in \{\theta_1, \theta_2, \ldots, \theta_q\}$ and $j = 0, 1, \ldots, q-1$. Additionally, it is worth noting that, if n is an integer number, or equivalently $q = 1$, the derived Equation (4) for a general rational number becomes equal to the previous Equation (1) for an integer number.

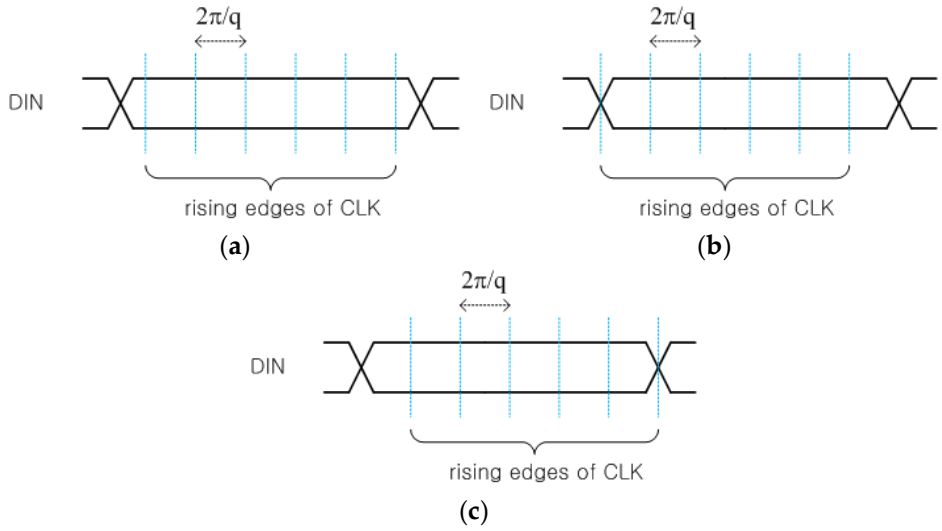

Figure 3. The rising edges of the clock signals when $\sum_{i=1}^{q}\theta_i$ is (**a**) zero, (**b**) minimum, and (**c**) maximum.

Figure 4a,b show the phase characteristics of the combined full-rate linear PD and CP at several rational numbers of n. The solid lines are the calculated values by the derived Equation (4) and the dot points are the simulated values by MATLAB Simulink. As shown in the figures, the calculated and simulated values agree well with each other. The difference between them is due to the randomness of the received data pattern. Figure 4c shows the figure of the general phase characteristic when $n = p/q$ and $n \geq 1$. The general phase characteristic is composed of the same q segments of which the width is $2\pi/q$ and the height is $\alpha\ I_{CP}/p$. The average value of the general phase characteristic becomes the frequency characteristic of the combined full-rate linear PD and CP.

$$I_{avg} = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_{UP} - I_{DN}d\theta = \frac{\alpha\ I_{CP}}{2} \times \left(1 - \frac{f_{CLK}}{f_{DATA}}\right) \text{ if } f_{CLK} < f_{DATA} \quad (5)$$

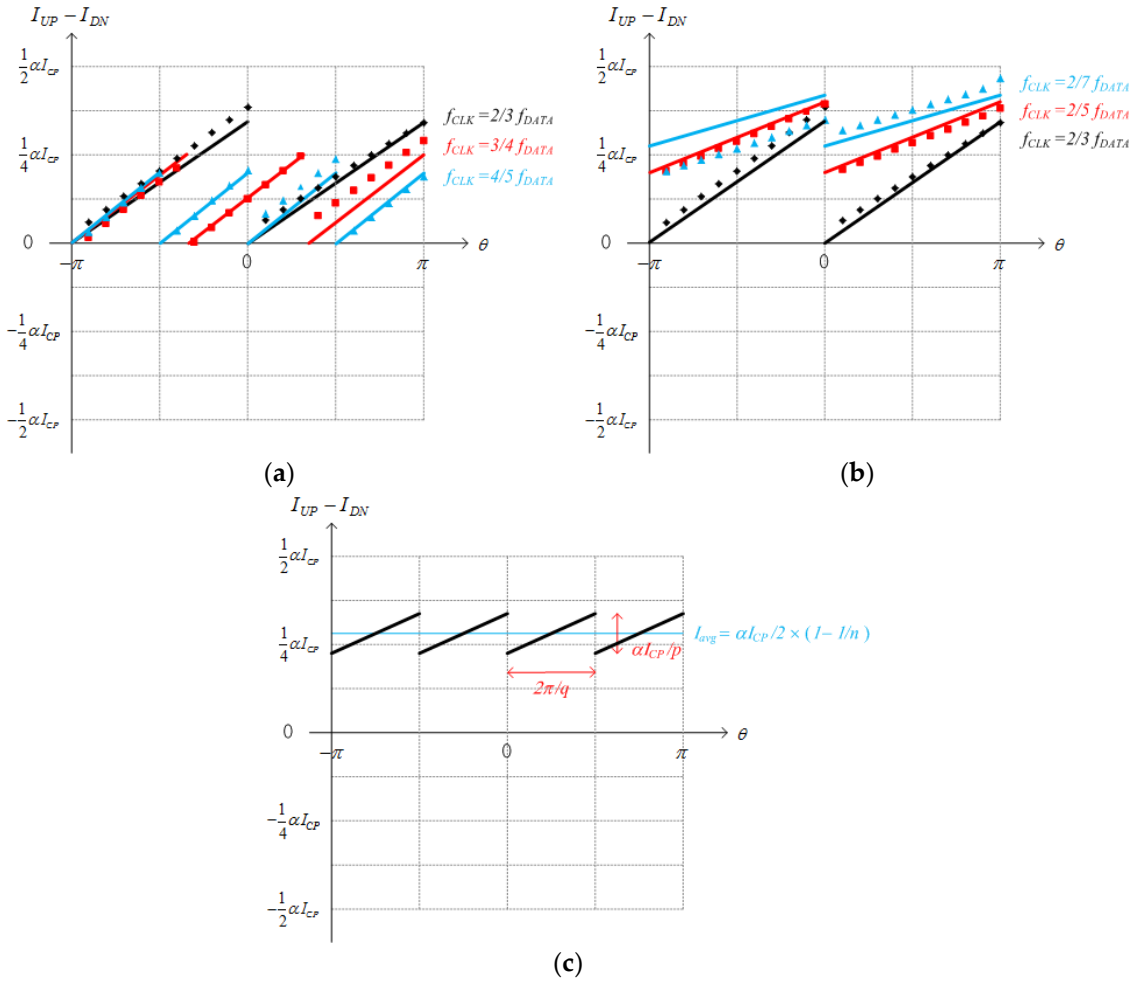

Figure 4. The phase characteristic of the combined full-rate linear PD and charge pump (CP) when $f_{CLK} = 1/n \times f_{DATA}$ and (**a**) $n = 3/2$, $n = 4/3$, and $n = 5/4$; (**b**) $n = 3/2$, $n = 5/2$, and $n = 7/2$; (**c**) $n = p/q$.

3. Lock Time of the Referenceless Single-Loop CDR Including the Full-Rate Linear PD

Figure 5 is the FLL model of the referenceless single-loop CDR including only the full-rate linear PD. The locking trajectory of the recovered clock frequency is represented by the exponential decay function with the single time constant (τ) if $f_{CLK}(0) < f_{DATA}$.

$$f_{CLK}(t) = f_{DATA} - (f_{DATA} - f_{CLK}(0)) \times e^{-\frac{t}{\tau}} \text{ where } \tau = RC_1 \times \left(1 + \frac{2\, f_{DATA}}{K_{VCO}\, R\, \alpha\, I_{CP}}\right) \quad (6)$$

Figure 6 shows both the ideal and actual locking trajectories of f_{CLK}(t). The difference between them is due to the high-frequency ripple voltage which is added onto the ideal VCO control voltage (V_{CONT}). This ripple voltage is mostly generated by R and C_2 of the loop filter and by the real-time CP output current which is depending on θ and the bit transition pattern of the received random data. Since the lock-in range is defined as the frequency range within which a phase-locked loop (PLL) locks fast without cycle slip between the reference frequency and the output frequency, the lock-in range of the referenceless single-loop CDR is equivalent to the peak frequency deviation of f_{CLK}(t) due to the ripple voltage [12]. Thus,

$$f_{CLK}(t_{lock}) + \Delta f_{lockin} = f_{DATA} \quad (7)$$

where Δf_{lockin} is the lock-in range and t_{lock} is the lock time as shown in Figure 6.

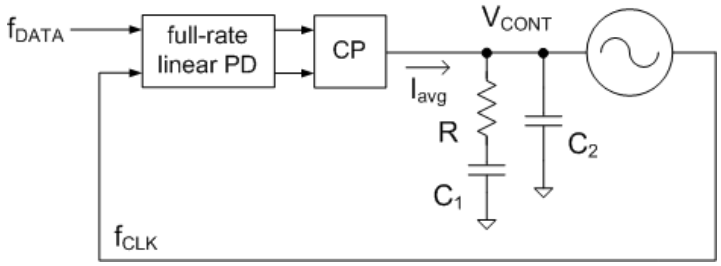

Figure 5. The frequency-locked loop model.

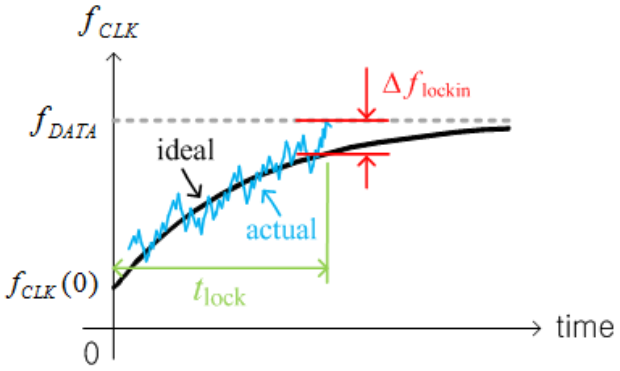

Figure 6. The locking trajectory of f_{CLK} and the lock-in range.

To derive the lock time of the referenceless single-loop CDR, we should obtain the peak frequency deviation of f_{CLK}(t). Figure 7 depicts the R and C_2 of the loop filter and the CP of the referenceless single-loop CDR. $\Delta v(t)$ is the ripple voltage and $i(t)$ is the real-time CP output current. The value of $\Delta v(t)$ will be maximum if $\theta = \pi$ and there comes consecutive bit transitions in the received data. Of course, keeping $\theta = \pi$ with long consecutive bit transitions is actually not possible and, thus, $\Delta v(t)$ may be a bit smaller than the maximum value. Figure 8a shows the ideal waveforms of the real-time CP output current after each bit transition assuming that $\theta = \pi$ and there comes consecutive bit transitions and Figure 8b shows that of the effective real-time CP output current. Since $i(t)$ flows into R and C_2, $\Delta v(t)$ increases asymptotically toward the maximum value ($\Delta v_{\max}$) as shown in Figure 8c and can be derived as

$$\Delta v(mT_b) = \Delta v((m-1)T_b)e^{-\frac{T_b}{RC_2}} + I_{\mathrm{CP}}R\left(1 - e^{-\frac{T_b}{2RC_2}}\right) \tag{8}$$

when $m \geq 2$. Figure 9 shows the MATLAB Simulink simulated waveforms of the UP and DN pulses and the V_{CONT} while frequency acquisition is being made. Since $\Delta v_{\max} = \Delta v(mT_b)$ when m is ∞ in Equation (8), the peak frequency deviation, or the lock-in range, is obtained from Equation (8) as

$$\Delta f_{\mathrm{lockin}} = K_{\mathrm{VCO}}\Delta v_{\max} = \frac{I_{\mathrm{CP}}R\,K_{\mathrm{VCO}}}{1 + e^{-\frac{T_b}{2RC_2}}} \tag{9}$$

By using Equations (6) and (7), the lock time can be also derived as follows.

$$t_{\mathrm{lock}} = \tau \ln \frac{f_{\mathrm{DATA}} - f_{\mathrm{CLK}}(0)}{\Delta f_{\mathrm{lockin}}} \tag{10}$$

For verification purpose, the MATLAB Simulink simulations were performed. The loop parameters of the referenceless single-loop CDR are set as f_{DATA} = 2 GHz, $f_{\mathrm{CLK}}(0)$ = 1 GHz, α = 0.5, K_{VCO} = 2 GHz/V, I_{CP} = 100 μA, R = 1 kΩ, C_1 = 159 pF and C_2 = 1.59 pF. The Bernoulli random binary sequence was used as the input data stream. Since V_{CONT} is linear with f_{CLK} in this simulation setup, we could measure the locking trajectory of V_{CONT} instead of f_{CLK} directly.

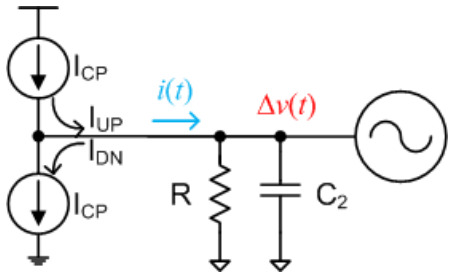

Figure 7. The calculation of the ripple voltage due to R and C_2.

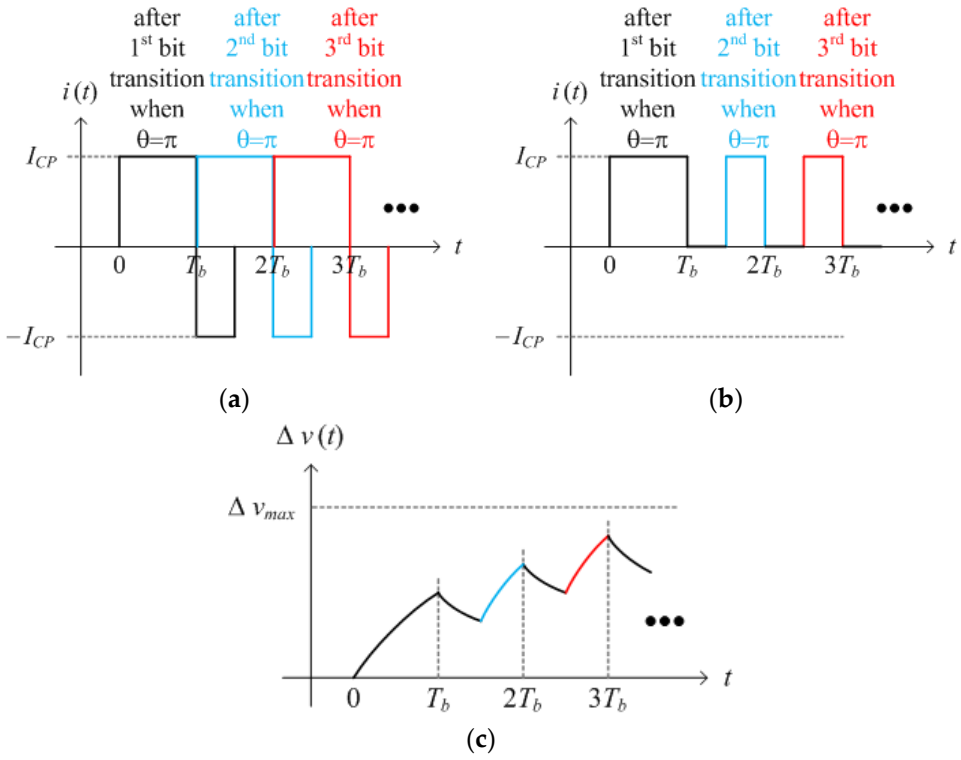

Figure 8. (**a**) Each and (**b**) the effective real-time charge pump current after consecutive bit transitions when $\theta = \pi$ and (**c**) the consequent ripple voltage.

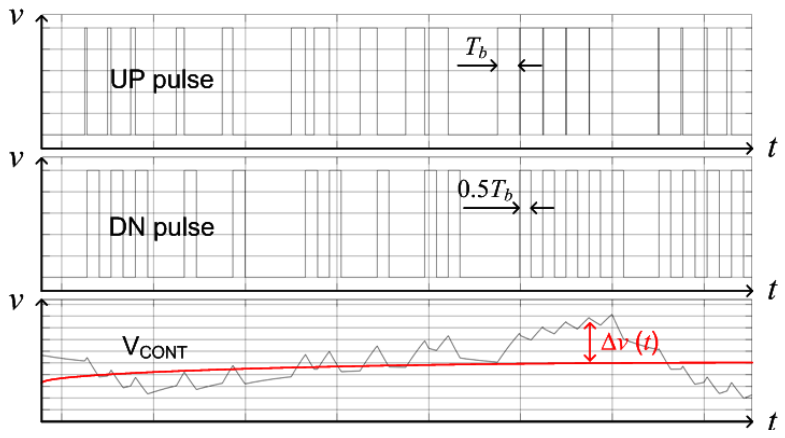

Figure 9. The simulated UP/DN pulses and V_{CONT} voltage.

Figure 10 shows the simulated locking trajectories of V_{CONT} when f_{DATA}, I_{CP}, C_1, and C_2 are varied, respectively. The measured lock times are summarized with the corresponding loop parameters in Table 1. As can be seen in Figure 10 and Table 1, the calculated lock times by Equation (10) agree well with the measured lock times from the MATLAB Simulink simulations.

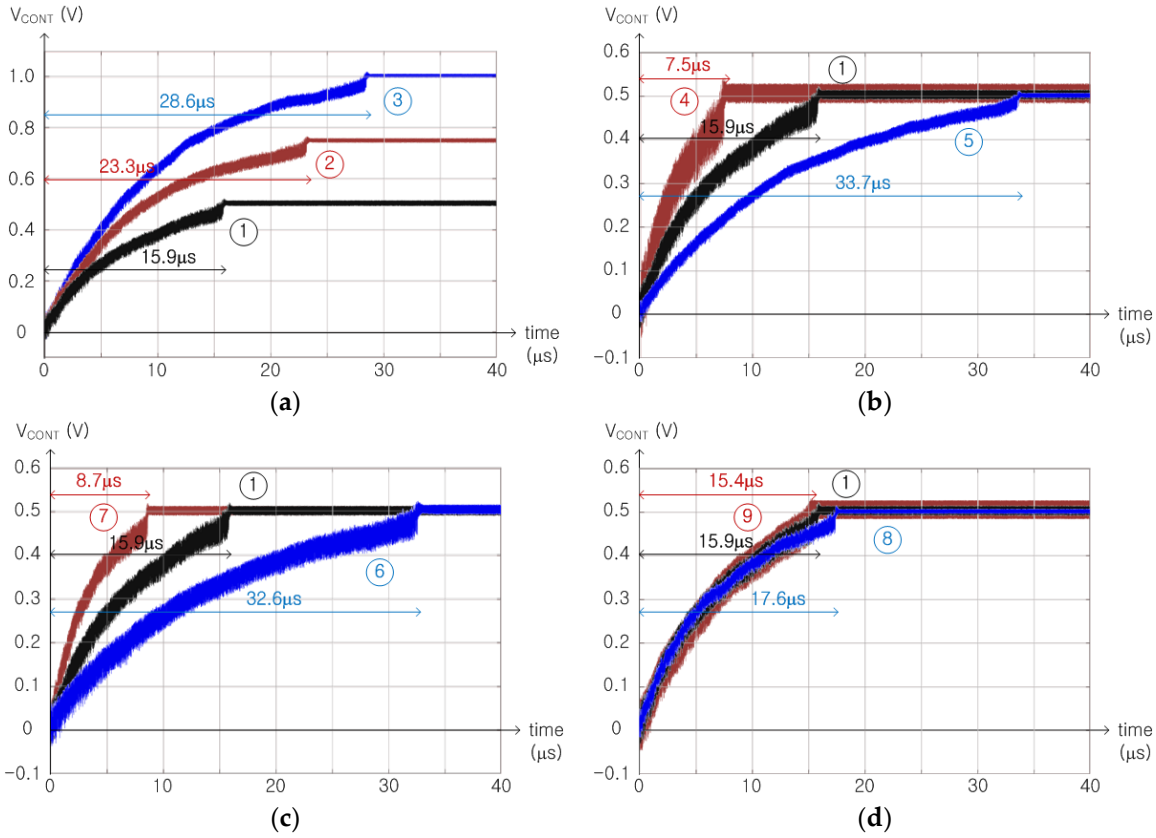

Figure 10. The simulated locking trajectories of V_{CONT} when (**a**) f_{DATA}, (**b**) I_{CP}, (**c**) C_1 and (**d**) C_2 are varied.

Table 1. The loop parameters and lock times.

	f_{DATA}	$f_{CLK}(0)$	α	K_{VCO}	I_{CP}	R	C_1	C_2	τ	Δf_{lockin}	calculated t_{lock} (A)	measured t_{lock} (B)	B/A
①	2 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	159 pF	1.59 pF	6.52 μs	108 MHz	14.5 μs	15.9 μs	1.10
②	2.5 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	159 pF	1.59 pF	8.11 μs	106 MHz	21.5 μs	23.3 μs	1.09
③	3 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	159 pF	1.59 pF	9.70 μs	105 MHz	28.6 μs	28.6 μs	1.00
④	2 GHz	1 GHz	0.5	2 GHz/V	200 μA	1 kΩ	159 pF	1.59 pF	3.34 μs	216 MHz	5.1 μs	7.5 μs	1.46
⑤	2 GHz	1 GHz	0.5	2 GHz/V	50 μA	1 kΩ	159 pF	1.59 pF	12.88 μs	54 MHz	37.6 μs	33.7 μs	0.90
⑥	2 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	318 pF	1.59 pF	13.04 μs	108 MHz	29.0 μs	32.6 μs	1.12
⑦	2 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	79.5 pF	1.59 pF	3.26 μs	108 MHz	7.3 μs	8.7 μs	1.20
⑧	2 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	159 pF	3.18 pF	6.52 μs	104 MHz	14.8 μs	17.6 μs	1.19
⑨	2 GHz	1 GHz	0.5	2 GHz/V	100 μA	1 kΩ	159 pF	0.795 pF	6.52 μs	116 MHz	14.1 μs	15.4 μs	1.09

4. Conclusions

In this paper, the phase and frequency characteristics of the combined full-rate linear PD and CP have been derived while the ratio of f_{DATA} to f_{CLK} is set as a general rational number. Additionally, the closed-form equations of the lock-in range and the lock time of the referenceless single-loop CDR including the full-rate linear PD have been derived theoretically. The calculated lock times by the derived equations agree well with the measured lock times from the MATLAB Simulink simulations.

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Conflicts of Interest: The author declares no conflict of interest.

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