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All-in-One Wafer-Level Solution for MMIC Automatic Testing

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Abstract: In this paper, we present an all-in-one wafer-level solution for MMIC (monolithic microwave integrated circuit) automatic testing. The OSL (open short load) two tier de-embedding, the calibration verification model, the accurate PAE (power added efficiency) testing, and the optimized vector cold source NF (noise figure) measurement techniques are integrated in this solution to improve the measurement accuracy. A dual-core topology formed by an IPC (industrial personal computer) and a VNA (vector network analyzer), and an automatic test software based on a three-level driver architecture, are applied to enhance the test efficiency. The benefit from this solution is that all the data of a MMIC can be achieved in only one contact, which shows state-of-the-art accuracy and efficiency.

Keywords: wafer-level; MMICs automatic test; OSL de-embedding; calibration verification model; dual-core topology

1. Introduction

MMICs (monolithic microwave integrated circuit) are the core components of sensors, radars, and wireless communication systems, the performance of which decides the capability of the whole system. Due to the imperfect yield of the former semiconductor process, after fabrication, wafer-level function testing for each chip is indispensable in order to eliminate the rejects. Hundreds of chips on one wafer may also have diverse application purposes. As a result, dozens of indicators are needed to be evaluated, like the DC (direct-current) characteristics, S-parameter (scatter parameter) and its derivatives, output power and PAE (power-added efficiency), spectrum and non-linearity, noise parameters, etc. [1]. These ask the system to have the abilities of automatic test item switching and high-speed measurement. Furthermore, with the development of semiconductor technology, the MMICs' performance, together with their highest operation frequencies and integration level, keep rising [2–8], which require the automatic system to have stronger abilities. Traditional test systems can either measure partial indicators of the MMICs or try to achieve the whole data by handling many instruments with a complex switch system. However, this leads to laborious operation, poor accuracy, and low speed. Traditional systems also ignore vector error correction, electromagnetic interference, temperature drift, and so on [9–15]. They cannot meet the precision and speed requirement of today's 5G communication, radars, safety inspection, and other mm-wave applications.

To solve the problems above, in this paper, we present an all-in-one wafer-level solution for MMIC automatic testing. To optimize the measurement accuracy, the OSL (open short load) two tier de-embedding [16–19], the calibration verification model, the accurate PAE testing, and the optimized vector cold source NF (noise figure) measurement techniques are integrated in the solution [20–22].

To improve the test efficiency, a dual-core topology formed by an IPC (industrial personal computer) and a VNA (vector network analyzer), and an automatic test software based on a three-level driver architecture are applied [23,24]. The benefit from this solution is that all the data of a MMIC can be acquired in only one contact, which is much more accurate and efficient than traditional systems.

This paper is organized as follows: Section 2 introduces the main problems of the current MMICs test. Section 3 demonstrates the improvements for measurement accuracy. Section 4 demonstrates the improvements for measurement efficiency. Section 5 shows the whole system and verifies its validity by measurement. In the final section, conclusions are drawn.

2. The Main Problems of the Current MMICs Test

Various MMICs are provided for different applications, like PA (power amplifiers), LNA (low noise amplifiers), MFC (multifunction chips), attenuators, filters, limiters, and other active or passive devices. According to different chip functions, the evaluation of dozens of indicators is commonly inevitable, like the DC characteristics, S-parameter and its derivatives, output power and PAE, spectrum and non-linearity, noise parameters, and so on. These indicators can be classified as four main types: DC characteristics, S-parameter, power and non-linearity, together with noise parameters. Typical MMIC test indicators and classification are shown in Table 1. These test indicators with weak correlation bring a significant challenge for MMIC measurement. Figure 1 shows the setup of the traditional test system. It is a mixture of scalar and vector measurements and a combination of wideband and narrowband testing. It has four subsystems roughly combined by a complex switch system. Table 2 shows different MMICs' test indicators. Table 3 shows the four subsystems and the corresponding instruments. It is certain that such a complicated system sacrifices accuracy and efficiency for covering the whole test. The situation becomes even worse for the wafer-level case.

Table 1. Typical MMICs' test indicators and classification.

	Test Indicators	Class
1	I_D (Drain current)	DC characteristics
2	I_G (Gate current)	DC characteristics
3	Pinch-off voltage	DC characteristics
4	Overshoot	DC characteristics
5	$VSWR_{In}$ (Input standing-wave ratio)	S-parameter
6	$VSWR_{Out}$ (Output standing-wave ratio)	S-parameter
7	Linear gain	S-parameter
8	Phase	S-parameter
9	P_{Out} (Output power)	Power and non-linearity
10	GC (Gain compression)	Power and non-linearity
11	PAE (Power added efficiency)	Power and non-linearity
12	Spectrum and non-linearity	Power and non-linearity
13	NF (Noise figure)	Noise parameters
14	NF_{Min} (Minimum noise figure)	Noise parameters
15	R_N (Noise resistance)	Noise parameters
16	Γ_{Opt} (Optimum source impendence)	Noise parameters
17	Magnitude consistency	Statistics
18	Phase consistency	Statistics

Table 2. Different MMICs' test indicators.

	DC	S-Parameter	Power and Non-Linearity	Noise
PA	√	√	√	×
LNA	√	√	×	√
MFC	√	√	√	×
Passive	×	√	×	×

Table 3. Subsystem and their instruments.

	Instruments
DC	1. DC power supply 2. DMM (digital multimeter) 3. Oscilloscope
S-parameter	4. VNA (vector network analyzer)
Power and non-linearity	5. SG (signal generator) 6. AWG (arbitrary waveform generator) 7. PM (power meter) and power sensor 8. SA (Spectrum analyzer)
Noise	9. Noise source 10. NFA (noise figure analyzer)
Number of instruments	**10**

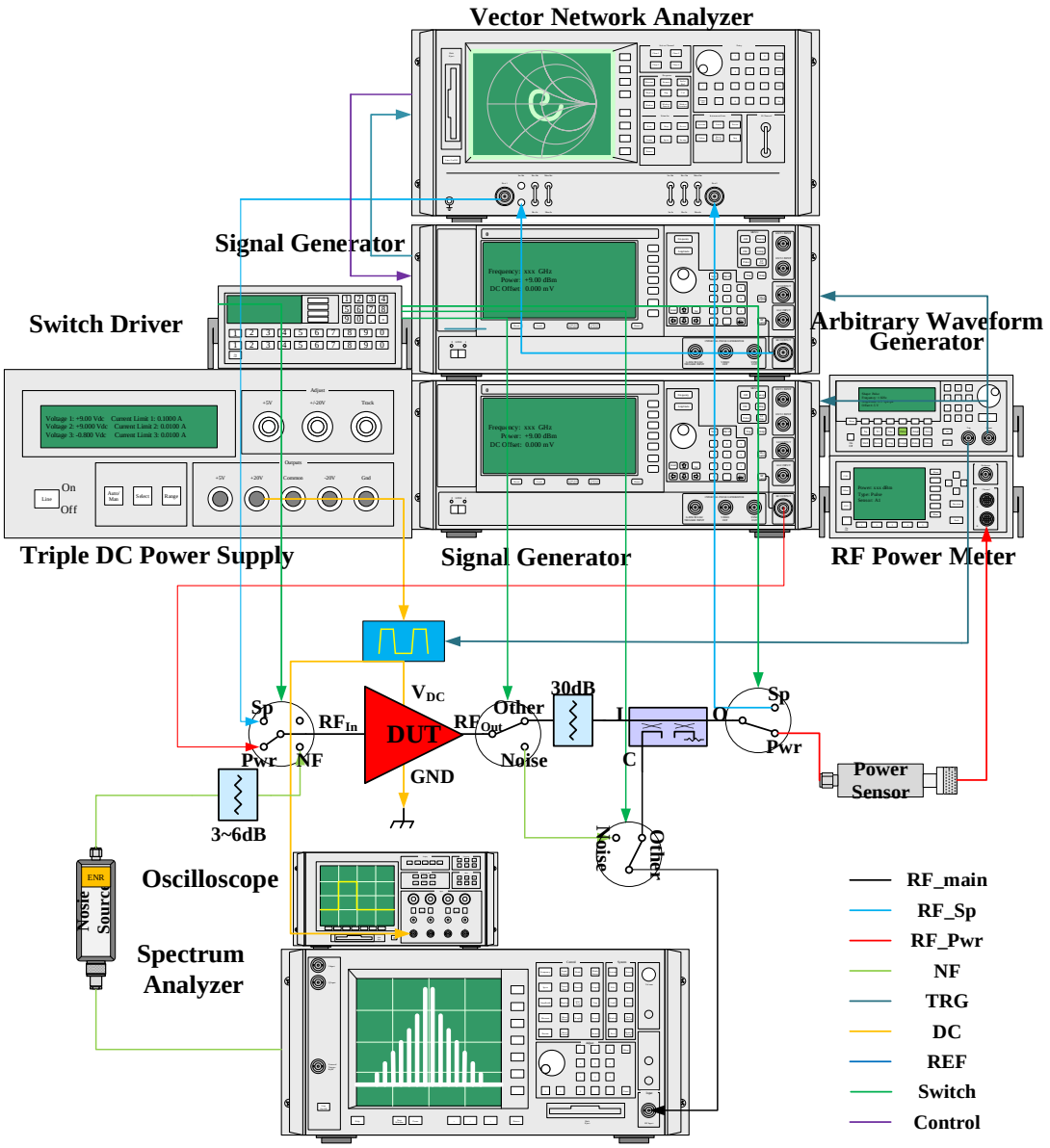

Figure 1. The traditional test system.

In terms of accuracy, such a complicated system leads to poor stability and arduous calibration. In the traditional system, only the S-parameter's reference plane can be extended to the probe tips, while others can only reach the coaxial plane. To correct this deviation, a simple scalar calculation may be performed by using the direct loss subtraction method. Meanwhile, because of the principle defects for power and noise testing, the system ignores the vector correction, switch repeatability, clutter, etc. Although after careful calibration, there is still a large remaining error [25,26]. In terms of speed, the system has to switch among each subsystem four times, the IPC needs to communicate with each instrument frequently, and the response for the power sensor and Y-factor (hot/cold source) noise measurement is always slow. All of these are time consuming, which can hardly be accepted for productive tests.

The complete MMIC test process can be summarized in three steps: calibration, verification, and measurement (Figure 2). The measurement errors come from three sources: system error, random error, and drift error [27]. However, only the system error can be removed by calibration, the other two can only be reduced by careful operation with a more accurate and compact system (shown in Table 4)

Table 4. Measurement errors and suppression means.

	System Error	Random Error	Drift Error
Calibration	√	×	×
Verification	√	√	√
Automation	×	√	√

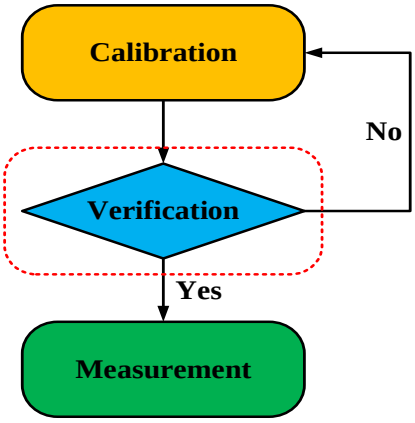

Figure 2. Test process generalizations.

Additionally, researchers commonly focus on better calibration methods [28–30], but overlook the verification step. They often verify the calibration by experience or even omit this step. An effective verification can judge the validity of the calibration, determine abnormalities of system operation, and guarantee the accuracy of the test data. Meanwhile, it must be conducted in a quantitative manner independent from human factors.

It is quite necessary to develop a more powerful system to solve the defects of the traditional ones and cover the complex measurement tasks. The system is aimed at supporting large-scale on-wafer testing. Therefore, it must have the ability of working in CW (continues wave), pulsed, or other modulation modes, and can perform precise testing of all the indicators in Table 1 in one contact. Additionally, it should support full vector correction precisely to the probe tips. Furthermore, it needs to be as simple as possible to reduce the complexity, improve the accuracy, and enhance the efficiency.

3. The Improvements in Measurement Accuracy

In this paper, in order to enhance the measurement accuracy, the proposed solution takes the commonly-neglected impacts, for instance, vector error correction, electromagnetic interference, and temperature drift, into account. Furthermore, light of the different subsystems' requirements, the measurement accuracy of our solution is markedly improved by integrating the OSL two-tier de-embedding, the calibration verification model, the accurate PAE testing, and the optimized vector cold source NF measurement, and other advanced test techniques. We discuss these in detail below.

3.1. S-parameter Test

Standard calkits are always in the same connector type. However, when meeting the heterotype connectors, calibration cannot be executed accurately. In an actual wafer-level test situation, only the S-parameter's reference plane is extended to the probe tips, and other indicators' reference planes can only reach the coaxial or waveguide plane. Traditional test systems either uses scalar correction.

$$\begin{bmatrix} S_{F11} \\ S_{F21}S_{F12} - S_{F11}S_{F22} \\ S_{F22} \end{bmatrix} = \begin{bmatrix} 1 & \Gamma_O & \Gamma_{MO} \\ 1 & \Gamma_S & \Gamma_{MS} \\ 1 & \Gamma_L & \Gamma_{ML} \end{bmatrix}^{-1} \begin{bmatrix} \Gamma_{MO} \\ \Gamma_{MS} \\ \Gamma_{ML} \end{bmatrix} \quad (1)$$

$$S_{F21} = \Gamma_{ML} \quad (2)$$

$$S_{F22} = \frac{\Gamma_S(\Gamma_{ML} - \Gamma_{MO}) + \Gamma_O(\Gamma_{MS} - \Gamma_{ML})}{\Gamma_S\Gamma_O(\Gamma_{MS} - \Gamma_{MO})} \quad (3)$$

$$S_{F21}S_{F12} = \frac{(\Gamma_S - \Gamma_O)(\Gamma_{MO} - \Gamma_{ML})(\Gamma_{MS} - \Gamma_{ML})}{\Gamma_S\Gamma_O(\Gamma_{MS} - \Gamma_{MO})} \quad (4)$$

$$\text{Delay}_{\text{Offset}} = \frac{l\sqrt{\varepsilon_r}}{c}, \varepsilon_r = 1.000649, c = 299792458 m/s \quad (5)$$

$$\text{Loss}_{\text{Offset}}|_{1GHz} = \frac{dB_{Loss}|_{1GHz} c\sqrt{\varepsilon_r} Z_0}{10log_{10}(e)l} = \frac{dB_{Loss} Z_0}{10log_{10}(e)\text{Delay}_{\text{Offset}}\sqrt{f}} \quad (6)$$

$$\alpha l = \frac{(\text{Loss}_{\text{Offset}})(\text{Delay}_{\text{Offset}})}{2(Z_{0,\text{Offset}})}\sqrt{\frac{f}{10^9}}, Z_{0,\text{Offset}} = 50\Omega \quad (7)$$

$$\beta l = 2\pi f(\text{Delay}_{\text{Offset}}) + \alpha l \quad (8)$$

$$\Gamma_i' = \Gamma_i \times e^{-2\gamma l}, \gamma = \alpha + j\beta, i = Open, Short, Load \quad (9)$$

which relies on direct loss subtraction method and ignores all vector factors, or even leaves this deviation alone. This can hardly be adopted by mm-wave applications (Ka band or above) or high-precision requirements. Therefore, we introduce the extended OSL de-embedding method (Figure 3) to extract the S-parameter of probes or other heterotype connectors. Firstly, we calibrate at the coaxial plane, then connect the probes and measure the on-wafer open, short, and load standards. $\mathbf{\Gamma_i}$ are the given reflection coefficients of on-wafer standards, and $\mathbf{\Gamma_{Mi}}$ are the measured data at the coaxial plane when the probes contact the standards. After acquiring these data, we use Equations (1) to (4) to calculate the probes' S-parameter. To solve the phase uncertainty in Equation (4), two external conditions, reciprocity and $\text{Phase}|_{0\text{Hz}} = 0^\circ$, are added. Then we can compensate the power vectorially and extend all reference planes to the probe tips. For the non-ideal calkits with $\text{Loss}_{\text{Offset}}$ (GΩ/s) and $\text{Delay}_{\text{Offset}}$ (ps), we use the correction algorithm from Equations (5) to (9) to obtain the correction factor $e^{-2\gamma l}$ and the new reflection coefficient $\mathbf{\Gamma_i}'$. In Figures 4 and 5, we use a 6 dB attenuator (Weinschel® 75A-06) as the DUT (device under test). We can see the calculated data are nearly the same with the measured one. In this way, the valid frequency range of the OSL method is remarkably extended.

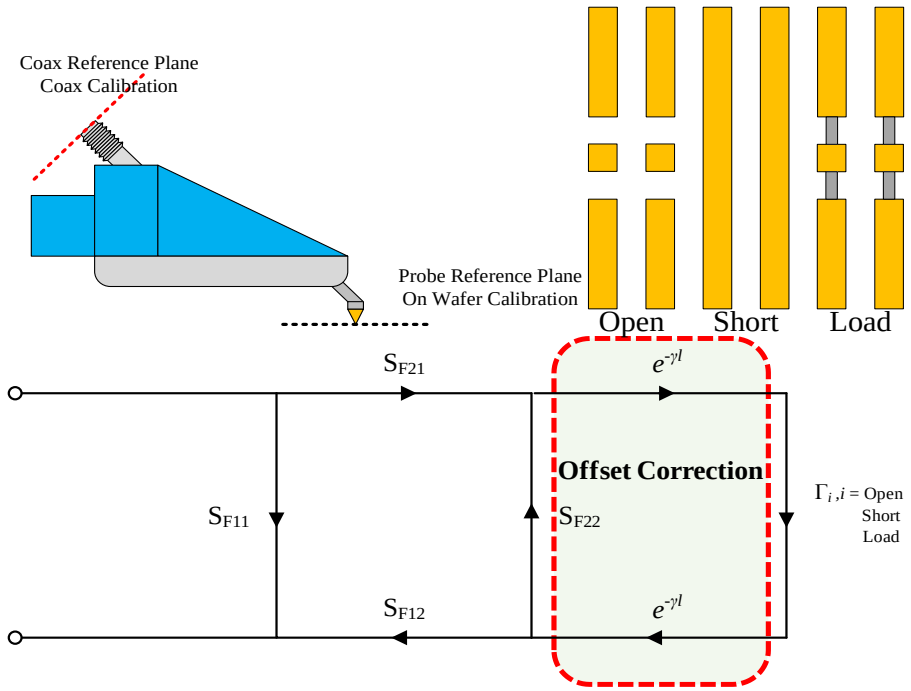

Figure 3. OSL de-embedding flow.

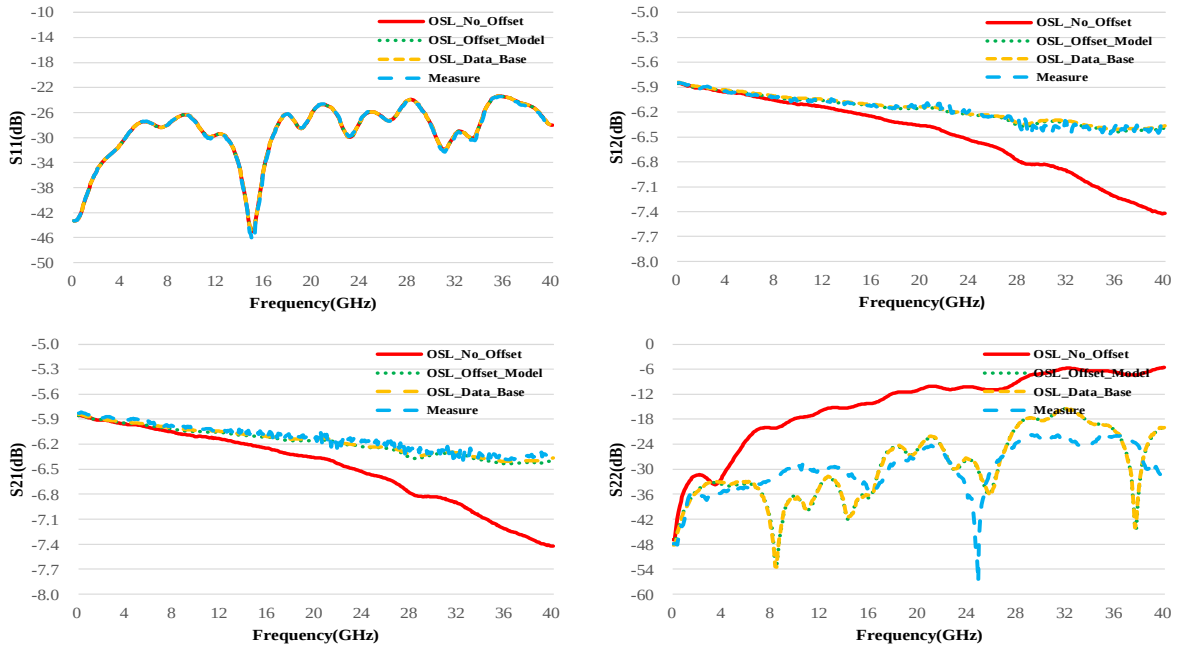

Figure 4. S-parameter magnitude of the 6 dB attenuator (Weinschel® 75A-06, Weinschel, Frederick, MD, USA).

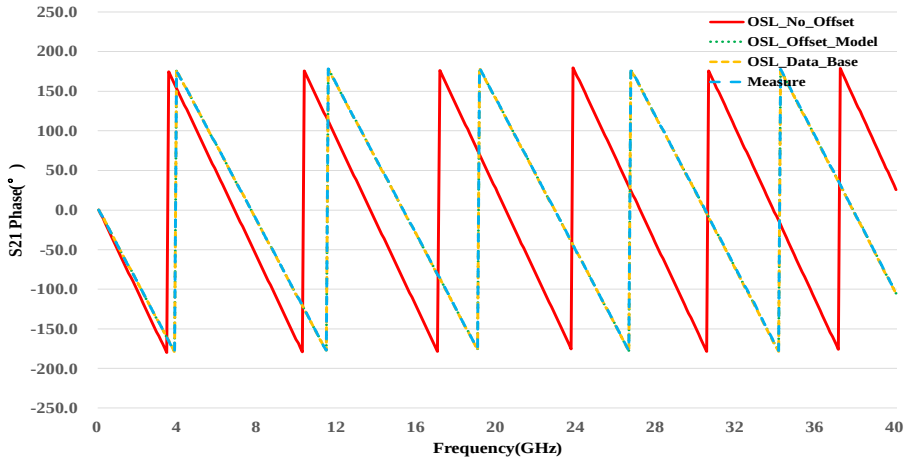

Figure 5. S-parameter phase of the 6 dB attenuator (Weinschel® 75A-06, Weinschel, Frederick, MD, USA).

It always perplexes the test operators whether the calibration is accurate enough and ready to use. In the coaxial condition, we can test a precisely-manufactured golden unit or the verification kit to validate its accuracy. However, it may not be suitable for on-wafer applications because of the process corner fluctuation and the destruction to the test kits by each contact. Sometimes they only test an open or a thru for simple verification. However, this method is not a quantitative way and closely related to the operator's experience. To overcome these defects, we introduce the delay line model to verify the calibration. The π-shaped equivalent circuit is shown in Figure 6, in which the delay line between two probes is indicated by the $\boldsymbol{L}$ and $\boldsymbol{R_{Series}}$ in series. The inductor $\boldsymbol{L}$ determines the characteristic time $\boldsymbol{\tau_D}$. The $\boldsymbol{R_{Series}}$ indicates the series resistor of the delay line resistor $\boldsymbol{R_{Line}}$ and the two probes' contact resistor $\boldsymbol{R_C}$, which should be small. The influence of the capacitors can be ignored. When the calibration is completed, we put the probes on another delay line (not used in calibration) with known $\boldsymbol{\tau_D}$ to perform the S-parameter measurement, and then calculate the real $\boldsymbol{\tau_D}$ and $\boldsymbol{R_{Series}}$ from the model (Equations (10) to (15)). Finally, after comparing the difference between the measured data and the nominal value, we can judge if the calibration is passed or not. Figure 7 shows an example. After a DC–110 GHz calibration, we use a new thru with a 1 ps delay for verification. We can see the characteristic time $\boldsymbol{\tau_D}$ is nearly 1 ps and the series resistor $\boldsymbol{R_{Series}}$ is no more than 300 mΩ. In this condition, we confirm that the calibration is effective. The verification model provides a quantitative manner to evaluate the calibration independent from experience.

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \frac{1}{Z_0 \Psi} \begin{bmatrix} (1-S_{11})(1+S_{22})+S_{12}S_{21} & -2S_{12} \\ -2S_{21} & (1+S_{11})(1-S_{22})-S_{12}S_{21} \end{bmatrix} \tag{10}$$

$$\Psi = (1+S_{11})(1+S_{22}) - S_{12}S_{21} \tag{11}$$

$$Z_A = \frac{1}{Y_{11}+Y_{12}},\ Z_B = -\frac{1}{Y_{12}},\ Z_C = \frac{1}{Y_{21}+Y_{22}} \tag{12}$$

$$Z_B = R_{Series} + j2\pi fL \tag{13}$$

$$R_{Series} = real(Z_B) \tag{14}$$

$$\tau_D = \frac{L}{Z_0} = \frac{imag(Z_B)}{2\pi f Z_0} \tag{15}$$

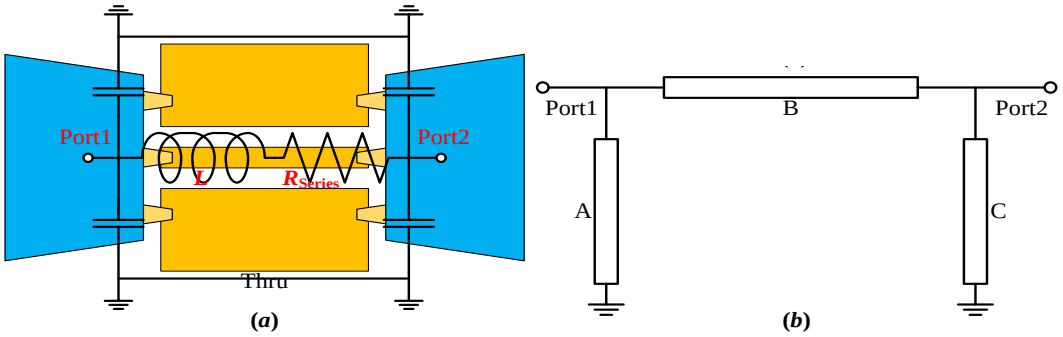

Figure 6. The equivalent circuit of delay line. (**a**) equivalent circuit, (**b**) π-shaped model.

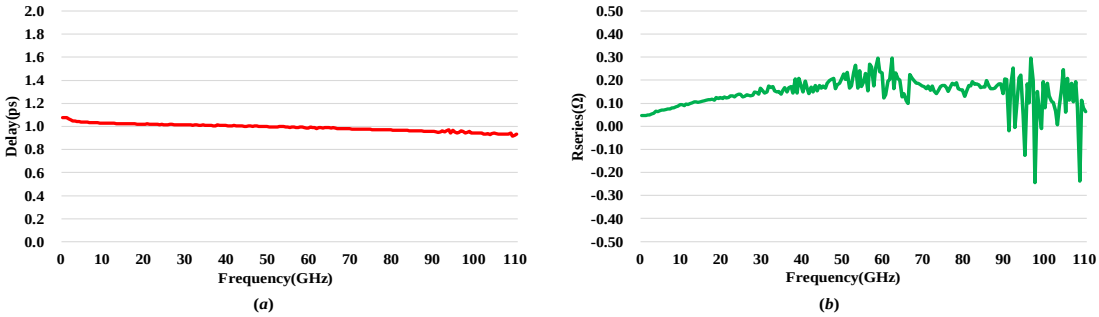

Figure 7. Calibration verification result. (**a**) delay in ps, (**b**) $R_{\mathbf{Series}}$ in Ω.

3.2. Power and Non-Linearity Test

PAE represents the key performance of PAs, and it is impacted by the output power and drain current jointly. Its measurement accuracy is influenced by many factors. The traditional method uses the SG and PM together with DMM to perform the scalar test (Table 3). Although this solution can obtain the accurate value of the current, it cannot make a fully vector correction. Meanwhile, PM only supports wideband power tests, which is easily interfered by the clutter near the test frequency. Additionally, limited by the testing principle of PM, the response of the power sensor is extremely slow when the power level is below –30 dBm, leading to communication timeout and system collapse. The VNA uses a superheterodyne receiver, which provides a narrowband method with a larger dynamic range and better accuracy. However, a sample resistor $\boldsymbol{R_{Sample}}$, shown in Figure 8, is introduced to obtain the drain current $\boldsymbol{I_D}$ [31,32] and PAE based on Equations (16) and (17), whose accuracy cannot be accepted. To settle these problems, we use a VNA to test the output power, and collect the DC data from the VNA's controller interface. The controller interface can control the DMM, read back the DC data, and then show it on the VNA's screen (Figure 9). After gathering all the data, the VNA sends them to the IPC to precisely calculate the PAE. This plan can remarkably improve the accuracy, speed, and stability. When a narrow-pulsed test is performed, or the current is larger than 3 A, the current probe is used instead of the DMM. Assisted by our unique calibration technique, the system can maintain the same accuracy.

$$I_D = \frac{\alpha(V_{In} - V_{Out})}{R_{Sample}}, \alpha = 2 \text{ or } 10 \tag{16}$$

$$PAE = \frac{P_{Out} - P_{In}}{I_D \times V_D} \times 100\% \tag{17}$$

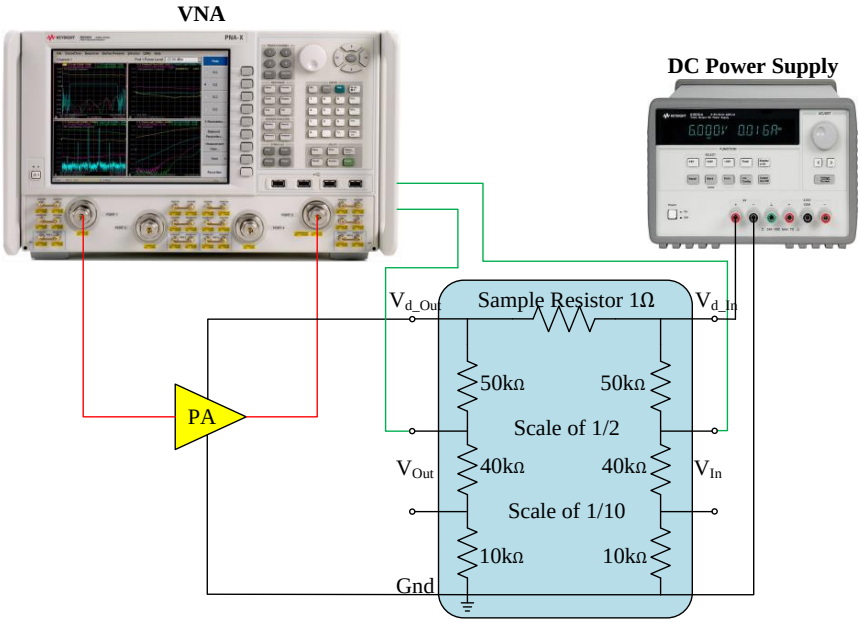

Figure 8. Traditional VNA PAE test plan.

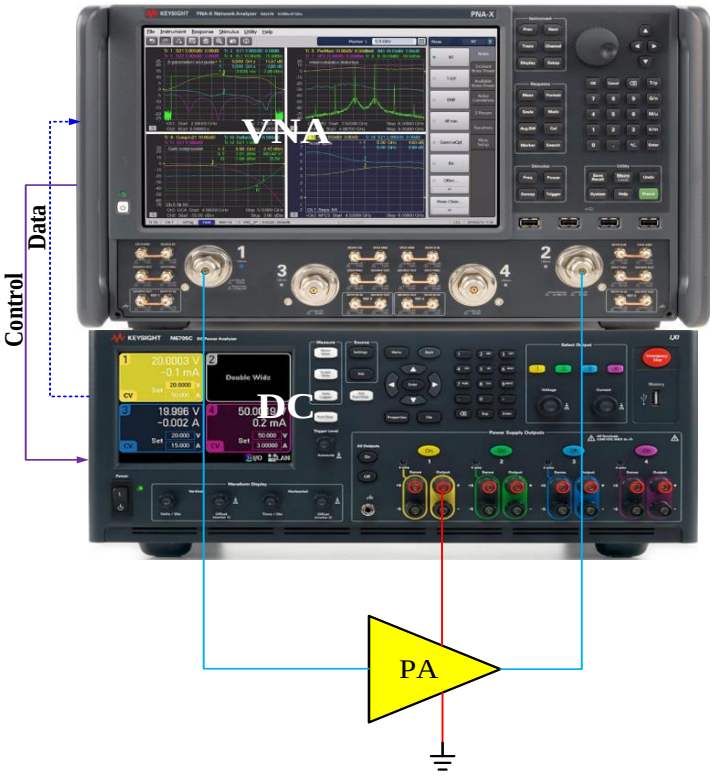

Figure 9. Accurate PAE test plan.

3.3. Noise Parameter Test

NF represents the key performance of LNAs. From Equations (18) and (19), we know NF is strongly related to source match. Both the former Y-factor method and the VNA scalar method assume the system $\boldsymbol{Z_0}$ is 50 Ω without considering the mismatch [33–35]. In reality, the result is mainly impacted by the mismatched source, the reflection coefficient difference between cold and hot states, and the uncertainty of ENR (excess noise ratio). Figure 10 gives the test result of an X-band LNA

(1.2 dB NF, 26 dB gain and 1.8 VSWR) under different mismatched source conditions. Furthermore, for its low speed, the Y-factor method is not suitable for production testing, and the scalar method is often limited by the DUT's gain. After careful comparison, we adopt the vector method for accurate NF testing. Meanwhile, the ambient temperature also needs to be concerned for precise testing. The NF test result impacted by ambient temperature is shown in Figure 11. We use the thermal control probe station to provide accurate temperature control. More than 0.1 dB NF deviations are obtained with 3 °C variations of the ambient temperature around 23 °C. For further optimization, we use a 3 dB or 6 dB attenuator before the probe to improve the source match. Calculated by Equation (20), the uncertainty reduces by about 25~40% (Figure 12). We choose the power sensor for noise calibration to avoid ENR uncertainty in mm-wave applications and integrate the thermal control probe station to suppress the effects of temperature fluctuation and electromagnetic interference. This solution thoroughly overcomes the shortcomings of low speed with large fluctuation and high sensitivity to the ambiance of the NF test. Table 5 shows the speed improvement of our method.

$$NF = 10\lg(F) = 10\lg(\frac{S_{In}/N_{In}}{S_{Out}/N_{Out}}), where\ S\ for\ signal,\ N\ for\ noise \tag{18}$$

$$F = F_{Min} + \frac{4R_N}{Z_0}\frac{\left|\Gamma_{Opt} - \Gamma_S\right|^2}{\left|1+\Gamma_{Opt}\right|^2(1-\left|\Gamma_S\right|^2)} \tag{19}$$

$$\Delta NF_{DUT} = \sqrt{\begin{array}{l}(\frac{F_{Sys}}{F_{DUT}} \cdot \Delta NF_{Sys})^2 \\ +(\frac{F_{Rcvr}}{F_{DUT}G_{DUT}} \cdot \Delta NF_{Rcvr})^2 \\ +(\frac{F_{Rcvr}-1}{F_{DUT}G_{A_{DUT}}} \cdot \Delta G_{A_{Sys\_dB}})^2 \\ +S((\frac{F_{Sys}}{F_{DUT}} - \frac{F_{Rcvr}}{F_{DUT}G_{A_{DUT}}})\Delta ENR_{dB})\end{array}} \tag{20}$$

- F is noise factor, as a ratio, F_{mim} is minimum noise factor, NF is the dB quantity;
- ENR_{dB} is the excess noise ratio of the noise source, in dB;
- The Δ terms are the associated uncertainties, always in dB; and
- S = 1 for a single-frequency measurement.

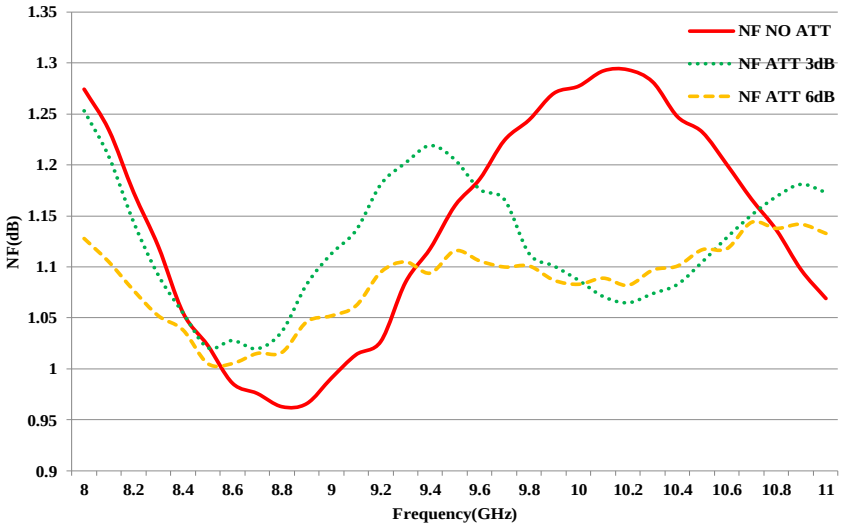

Figure 10. NF result influenced by source match.

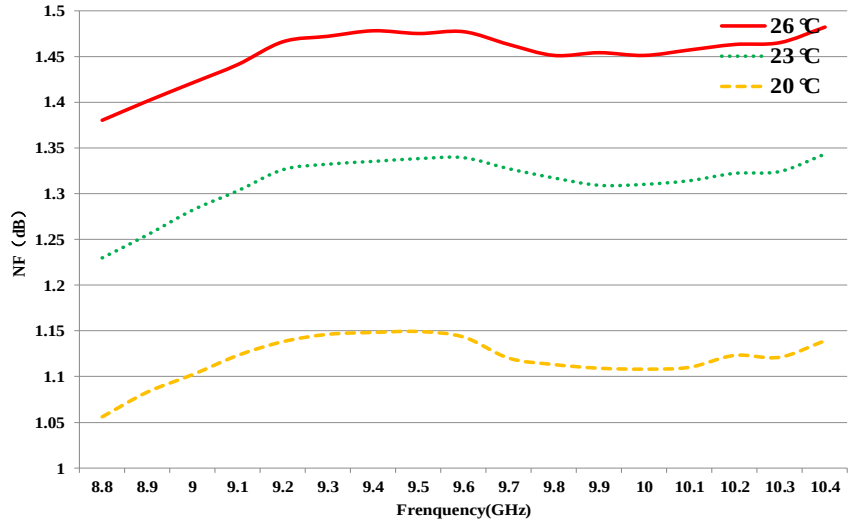

Figure 11. NF result influenced by ambient temperature.

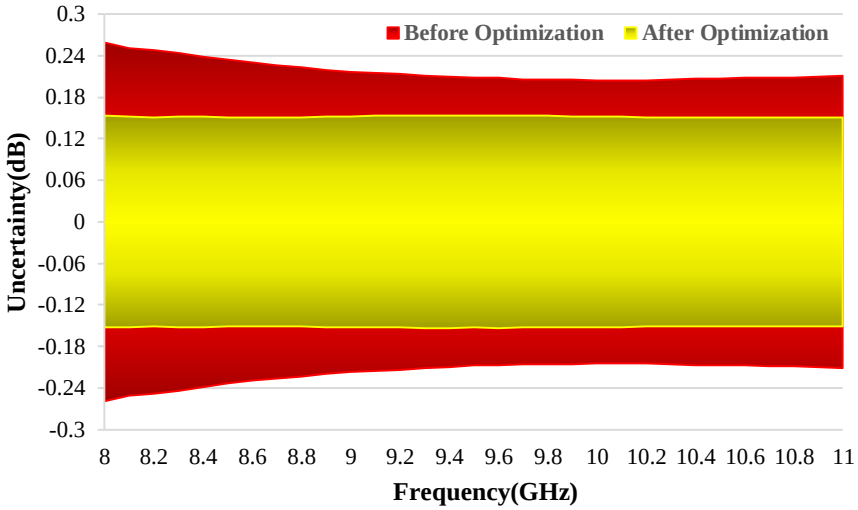

Figure 12. The test accuracy comparison.

Table 5. NF measurement speed (in second).

Points	NFA	PSA	EXA	This Work
11	2.8	2.2	2.1	2
51	11	9	9	2.6
101	21	18	18	3.1
201	42	35	36	4.2

4. The Improvements for Measurement Efficiency

Aimed at solving the low efficiency of the traditional test system and simplifying its laborious operation, we carefully compared different mm-wave instruments of many companies [36–39], then put forward a new all-in-one wafer-level solution for MMIC automatic testing. The solution adopts the dual-core hardware topology and a three-level software driver architecture. The solution uses the IPC as the control center, the VNA as the data center, the thermal control probe station with electromagnetic shielding as the on-wafer test platform, and the automatic test software is based on the three-level driver architecture of the HMI (human machine interface).

In terms of hardware, different from the former distribution mode (Figure 13), the dual-core topology uses the IPC to configure the whole system and the VNA to acquire all the data (Figure 14). Taking the architecture advantage of the modern VNA, the advanced calibration and measurement method can be easily integrated, and the test system is remarkably simplified. The number of instruments can be reduced from 10 (Figure 1) to, at most, four (Figure 15, the instruments surrounded with a dotted line can be omitted). The VNA communicates with other instruments directly at the hardware level, collects all the data together, and then sends them back to the IPC. Thus, we save much time wasted by the communication between the IPC and each instrument, which improves the efficiency and stability significantly.

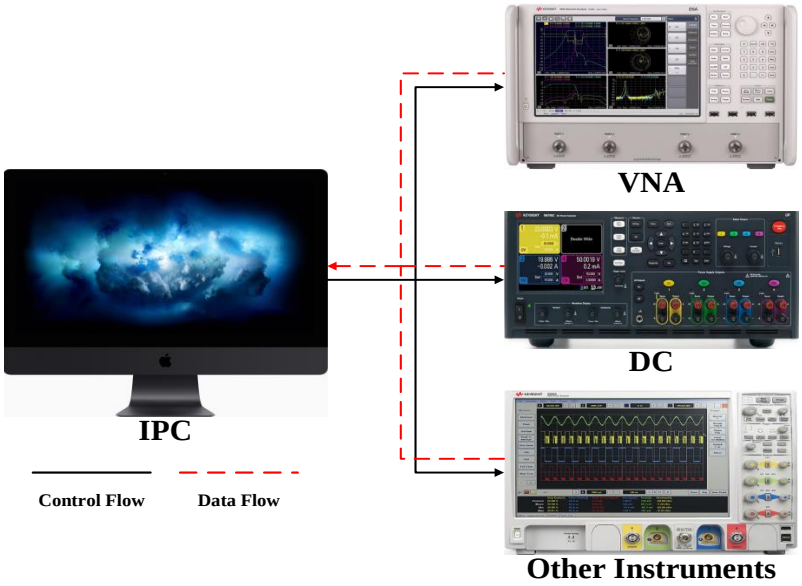

Figure 13. The former distribution mode.

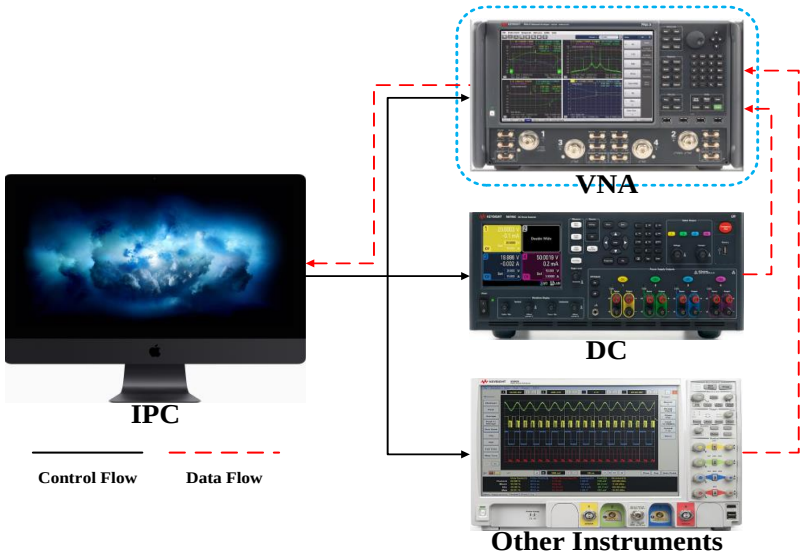

Figure 14. The dual-core topology.

In terms of software, the drivers are defined at three levels: the main window, the functional window, and the basic function driver. The benefit of this architecture is that the main program has the virtue of briefness. Each driver does a simple and clear job, which is very convenient for distributing

development and reduces the collapse probability significantly. The software combines the high efficiency and flexibility of the C# language and the strong data storage and processing abilities of the relational database. In this way, we can test different DUTs with high speed, and perform big data statistical analysis and processing conveniently.

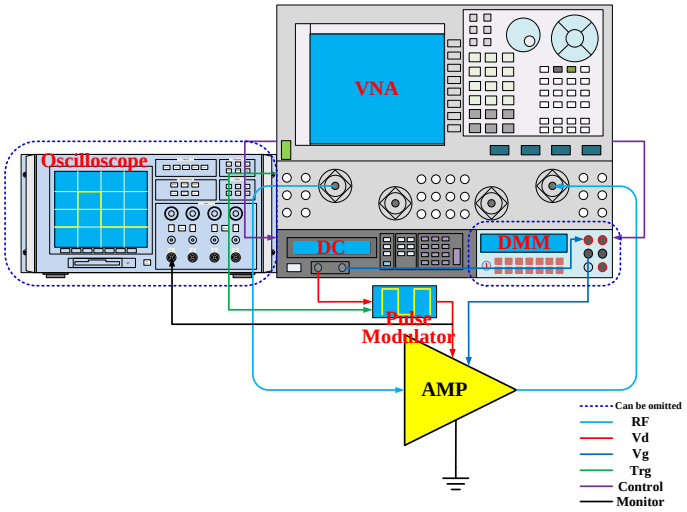

Figure 15. The new all-in-one solution.

5. All-in-One Solution and Measurement Results

Based on the improvement and optimization in Sections 3 and 4, we provide an all-in-one wafer-level solution for MMIC automatic testing. Figures 16 and 17 show the whole system setup and its software HMI. Figure 18 gives a photo of the system. Compared with the solution in Figure 1, the fully-upgraded system has a much simpler structure and a more friendly and intelligent HMI. After the accuracy and validity checking of the improved methods, we chose an X-band PA and LNA (their main indicators are shown in Table 6) fully evaluated before to inspect and verify the whole system. Figure 19 presents the screen of the VNA. Its six channels test the S-parameter, the gain compression, the intermodulation distortion, the noise parameters, and the spectrum, respectively. In Tables 7 and 8, we compare the test coverage, accuracy, and speed of our system with the traditional one. An efficiency improvement of 11 times is achieved. In Figure 20, we exhibit partial windows of the test result, and the windows of the auto screening and statistical analysis functions. Assisted by the HMI, we can clearly comprehend all the parameter tendencies of each DUT varying with the frequency or input power, and obtain the statistical distribution of each parameter in the test batch. Meanwhile, all the test results are sent to the database automatically, which ensures the safety and traceability of the results and provides great convenience for further deep analysis.

Table 6. DUTs' main indicators for verification.

DUT	Main Indicators	
PA	*Frequency range*	X-band
	P_{Out}	>34dBm
	Gain	>25dB
	PAE	>47%
LNA	*Frequency range*	X-band
	Gain	>26dB
	$VSWR_{In}/VSWR_{Out}$	<1.8
	NF	<1.2dB

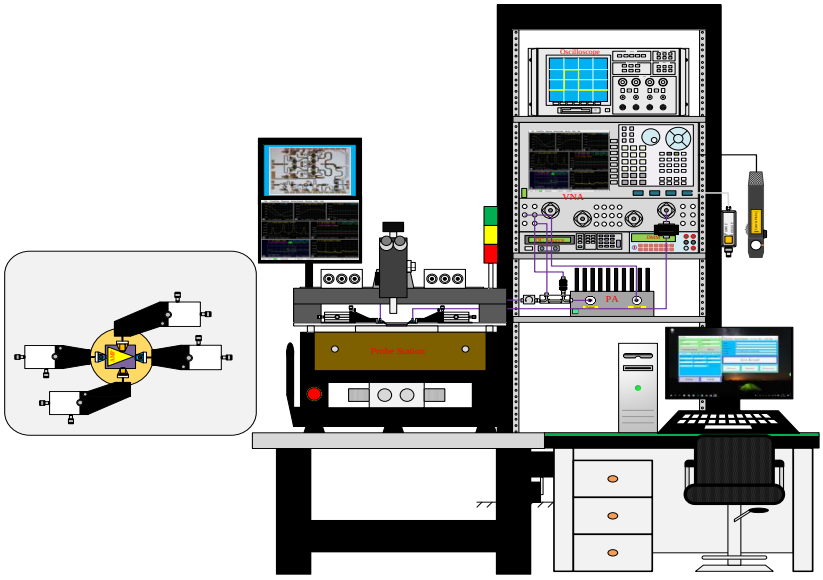

Figure 16. The whole system setup.

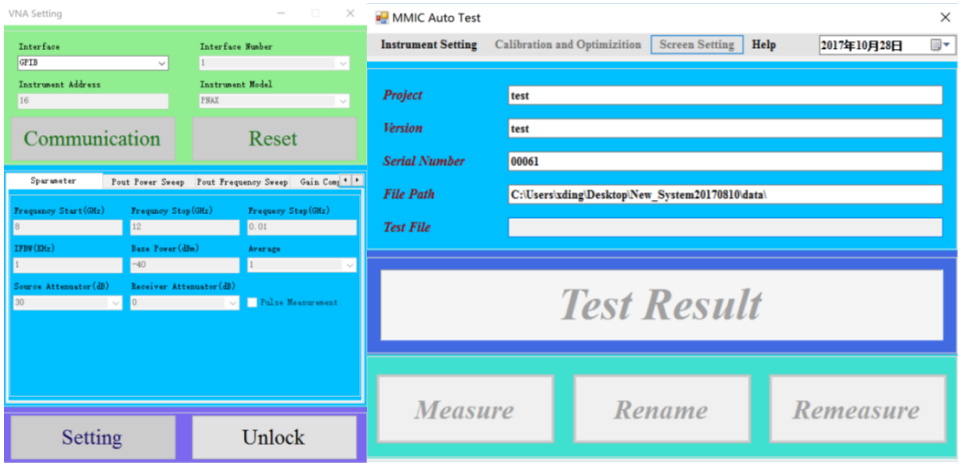

Figure 17. Automatic test control software HMI.

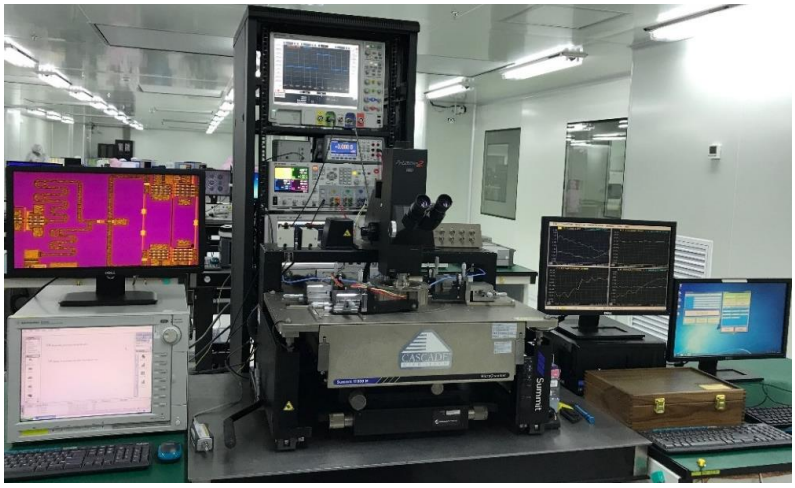

Figure 18. The photo of the all-in-one solution.

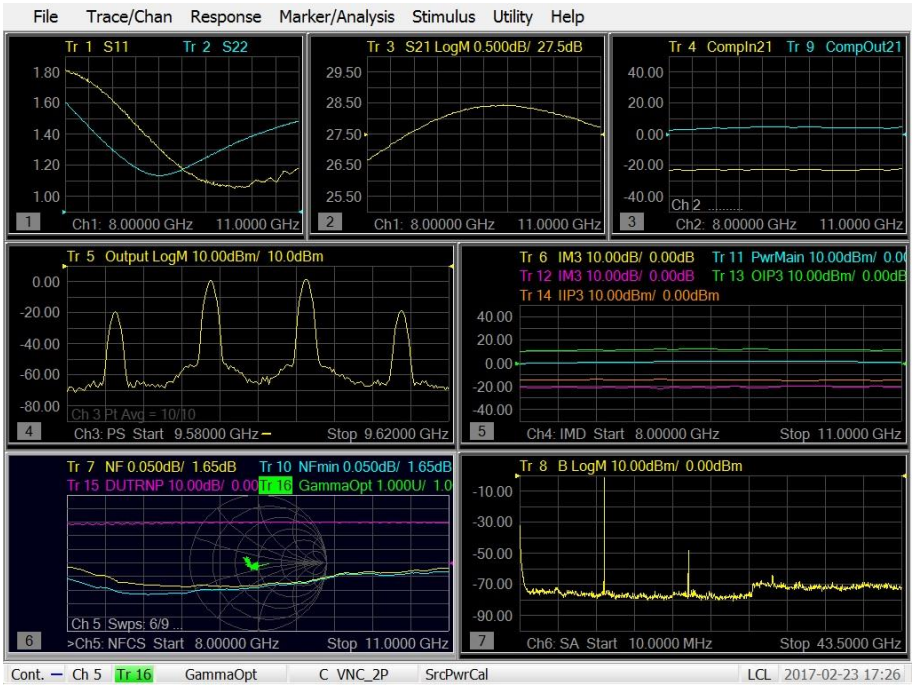

Figure 19. The screen of the VNA.

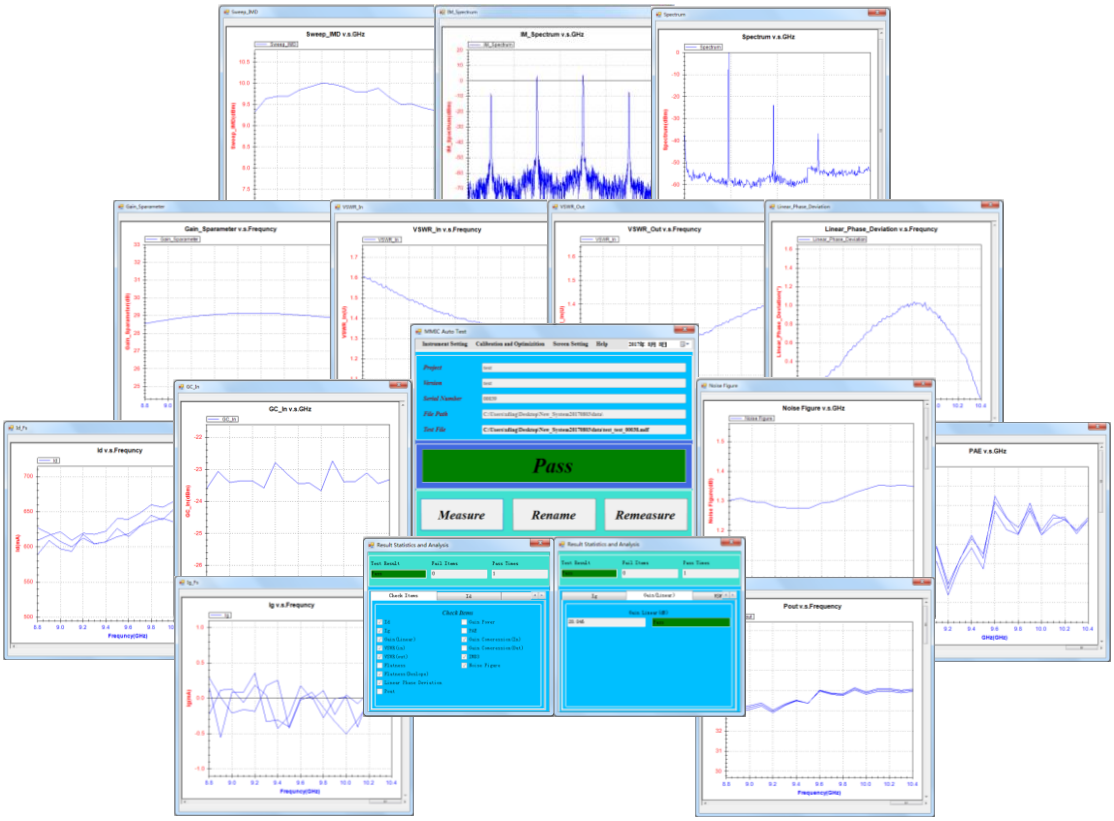

Figure 20. The windows of the measurement results.

Table 7. Test coverage and accuracy comparison.

Item	Traditional Systems	This Work
Test coverage	Poor, even assisted by complex switching, partial indicators cannot be measured	Good, all test in one contact
DC accuracy	Good	Good
S-parameter accuracy	Good	Better, without the influence of the switches
Power and non-linearity accuracy	Moderate, with scalar correction	Good, with full vector correction
Noise accuracy	Poor, without vector correction	Good, with full vector correction

Table 8. Measurement speed comparison (in seconds).

Item	Traditional Systems	This Work
I_D and I_G	22	<1
S-parameter	1	<1
P_{Out} and *PAE*	11	<1
2D GC List	×	2
IMD	×	2
NF	>55	3
Spectrum	>60	4
Switching	10	<1
Data Process	10	<2
Total	**>169**	**≈15**
Improvement	**-**	**>11X**

6. Conclusions

An all-in-one wafer-level solution for MMIC automatic testing has been presented and verified in this study, aimed at better evaluating the modern highly-integrated MMICs. The OSL two-tier de-embedding, the calibration verification model, an accurate PAE test method, and the optimized vector cold source NF measurement technique are combined in our system to improve the test accuracy. The system is designed based on a dual-core topology and three-level driver architecture. The automatic test software takes the advantage of C# and a relational database. Compared with the traditional test system, the new solution is much more simplified and efficient. By adopting these optimizations and corrections, the accuracy and efficiency of the system is significantly improved. Thanks to this method, we can obtain all the data of MMICs in only one contact and make the large-scale on-wafer testing much easier.

Author Contributions: X.D. conceived the solution; X.D and Z.W. designed the system; J.L., M.Z., and W.C. performed the experiments; H.C., J.M., and F.Y. analyzed the data; and X.D. and Z.W. wrote the paper.

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References

1. Adam, S.F. 50 years or more on RF and Microwave Measurements Microwave Symposium Digest. In Proceedings of the IEEE MTT-S International Conference on Microwave Symposium Digest, San Francisco, CA, USA, 11–16 June 2006; pp. 993–995.
2. Kim, D.; Lee, D.-H.; Sim, S.; Jeon, L.; Hong, S. An X-Band Switchless Bidirectional GaN MMIC Amplifier for Phased Array Systems. *IEEE Microw. Wirel. Compon. Lett.* **2014**, *24*, 878–880. [CrossRef]
3. Masuda, S.; Yamada, M.; Kamada, Y.; Ohki, T.; Makiyama, K.; Okamoto, N.; Imanishi, K.; Kikkawa, T.; Shigematsu, H. GaN single-chip transceiver frontend MMIC for X-band applications. In Proceedings of the IEEE/MTT-S International Conference on Microwave Symposium Digest, Montreal, QC, Canada, 17–22 June 2012.
4. Choi, P.; Goswami, S.; Radhakrishna, U.; Khanna, D.; Boon, C.-C.; Lee, H.-S.; Antoniadis, D.; Peh, L.-S. A 5.9-GHz Fully Integrated GaN Frontend Design With Physics-Based RF Compact Model. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 1163–1173. [CrossRef]
5. Liu, C.; Li, Q.; Li, Y.; Li, X.; Liu, H.; Xiong, Y.-Z. An 890 mW stacked power amplifier using SiGe HBTs for X-band multifunctional chips. In Proceedings of the 41st European Solid-State Circuits Conference (ESSCIRC), Graz, Austria, 14–18 September 2015.
6. Malta, D.; Vick, E.; Lueck, M.; Huffman, A.; Woodruff, S.; Ralston, P.; Hartman, J.; Bushyager, N.; Ebner, G.D.; Quade, S.; et al. TSV-Last, Heterogeneous 3D Integration of a SiGe BiCMOS Beamformer and Patch Antenna for a W-Band Phased Array Radar. In Proceedings of the 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 31 May–3 June 2016.
7. Meniconi, E.; Ziegler, V.; Sorrentino, R.; Chaloun, T. 3D integration technologies for a planar dual band active array in Ka-band. In Proceedings of the 2013 European Microwave Conference (EuMC), Nuremberg, Germany, 6–10 October 2013.
8. Pavlidis, S.; Alexopoulos, G.; Ulusoy, A.Ç.; Cho, M.K.; Papapolymerou, J. Encapsulated Organic Package Technology for Wideband Integration of Heterogeneous MMICs. *IEEE Trans. Microw. Theory Tech.* **2017**, *65*, 438–448. [CrossRef]
9. Boulanger, N.; Rumelhard, C.; Carnez, B.; Boulanger, L.; Sentubery, C. On Wafer Automatic Three Ports Measurement System for MMIC Circuits and Dual Gate FETs. In Proceedings of the 20th European Microwave Conference, Budapest, Hungary, 9–13 September 1990; Volume 1, pp. 220–225.
10. Lin, E.W.; Huang, T.W.; Lo, D.C.W.; Wang, H.; Yang, D.C.; Dow, G.S.; Allen, B.R. Versatile W-band On-wafer MMIC Test Set. In Proceedings of the 47th ARFTG Conference Digest-Spring, San Francisco, CA, USA, 20–21 June 1996; Volume 29, pp. 220–225.
11. Kamenopolsky, S.; Dankov, P. Automated measurement setup for Ku band MMIC characterization. In Proceedings of the 59th ARFTG Conference Digest, Spring 2002, Seattle, WA, USA, 7 June 2002. [CrossRef]
12. Vael, P.; Rolain, Y. Calibrated linear and nonlinear pulsed RF measurements on an amplifier. Microwave Symposium Digest. In Proceedings of the 2001 IEEE MTT-S International Conference on Microwave Symposium Digest, Phoenix, AZ, USA, 20–24 May 2001; Volume 3, pp. 2187–2190.
13. Yang, D.C.; Yang, J.M.; Wiang, H.; Huang, P. Characterization of W-band MMIC power amplifier using on-wafer pulsed power test. Microwave Symposium Digest. In Proceedings of the 1998 IEEE MTT-S International Conference on Microwave Symposium Digest, Baltimore, MD, USA, 7–12 June 1998; Volume 3, pp. 1483–1486.
14. Doo, S.J.; Roblin, P.; Lee, S.; Chaillot, D.; Bossche, M.V. Pulsed-IV pulsed-RF measurements using a large signal network analyzer. In Proceedings of the 65th ARFTG Conference Digest, Spring 2005, Long Beach, CA, USA, 17 June 2005.
15. Roblin, P.; Ko, Y.S.; Yang, C.K.; Suh, I.; Doo, S.J. NVNA Techniques for Pulsed RF Measurements. *Microw. Mag. IEEE* **2011**, *12*, 65–76. [CrossRef]
16. Zhu, N.H. Phase Uncertainty in Calibrating Microwave Test Fixtures. *IEEE Trans. Microw. Theory Tech.* **1999**, *41*, 1917–1922. [CrossRef]
17. Keysight. *Specifying Calibration Standards and Kits for Keysight Vector Network Analyzers*; Application Note 1287-11; Keysight: Palo Alto, CA, USA, 2011.
18. Crupi, G. *Dominique Schreurs, Microwave De-Embedding: From Theory to Applications*; Academic Press: Cambridge, MA, USA, 2013.

19. Lee, J. Modeling of SOL calibration standards for PCB channel probing. *IEEE Electromagn. Compat. Mag.* **2016**, *5*, 123–127. [CrossRef]
20. Joel, D.; Wood, S. Vector Corrected Noise Figure and Noise Parameter Measurements of Differential Amplifiers. In Proceedings of the 39th European Microwave Conference, Rome, Italy, 29 September–1 October 2009.
21. Nguyen, H.V.; Misljenovic, N.; Hosein, B. Efficient Noise Extraction Algorithm and Wideband Noise Measurement System from 0.3 GHz to 67 GHz. In Proceedings of the 2013 81st ARFTG Microwave Measurement Conference (ARFTG), Seattle, WA, USA, 7 June 2013. [CrossRef]
22. Keysight. *High-Accuracy Noise Figure Measurements Using the PNA-X Series Network Analyzer*; Keysight: Palo Alto, CA, USA, 2013.
23. Salnikov, A.S. Evgeny Karataev Software programs for storage and statistical analysis of MMIC measurement data. In Proceedings of the 21th International Crimean Conference on Microwave and Telecommunication Technology (CriMiCo), Sevastopol, Ukraine, 12–16 September 2011; pp. 212–213.
24. *Virtual Instrument Software Architecture*; Radoslav, L. (Ed.) Pon Press: New York, NY, USA, 2012; pp. 10–40.
25. Wartenberg, S.A. *RF Measurements of Die and Packages*; Artech House: Norwood, UK, 2002.
26. Dunsmore, J.P. *Handbook of Microwave Component Measurements: With Advanced VNA Techniques*; Wiley: Palo Alto, WA, USA, 2012.
27. Eppati. *Modern RF and Microwave Measurement Techniques*; Cambridge University Press: Cambridge, UK, 2013; pp. 30–50.
28. Benet, J.A. The Design and Calibration of a Universal MMIC Test Fixture. *Microw. Millim. Wave Monolithic Circuits* **1982**, *82*, 36–41.
29. Penn, J.E.; Moore, C. GaAs MMIC Probe Measurements and Calibration Techniques. In Proceedings of the 39th ARFTG Conference Digest-Spring, Albuquerque, NM, USA, 5 June 1992; Volume 21.
30. Shoaib. *The Calibration of 2-Port Vector Network Analyzer*; LAP Lambert Academic Publishing: Saarbrücken, Germany, 2012; pp. 60–80.
31. Keysight. *Measuring Power-Added Efficiency (PAE) with PNA Network Analyzers (1408-16)—Application Note*; Keysight: Palo Alto, CA, USA, 2007.
32. R&S. *Power Added Efficiency Measurement with R&S ZNB/R&S ZVA*; R&S: Muenchen, Germany, 2013.
33. Keysight. *Noise Figure Measurement Accuracy the Y-Factor Method*; Keysight: Palo Alto, CA, USA, 2013.
34. Keysight. *Fundamentals of RF and Microwave Noise Figure Measurements*; Keysight: Palo Alto, CA, USA, 2010.
35. R&S. *Noise Figure Measurement without a Noise Source on a Vector Network Analyzer*; R&S: Muenchen, Germany, 2010.
36. Morris, M.W.; Shaw, B.L.; Ziomek, C.D. Modular & benchtop instrument convergence decreases test costs and increases productivity. In Proceedings of the 2011 International Conference on Electric Information and Control Engineering, Baltimore, MD, USA, 17–20 September 2011.
37. Keysight. *PNA Series Network Analyzers Help (User Guide, Programming Guide)*; Keysight: Palo Alto, CA, USA, 2014.
38. R&S. *R&S ZVA, R&S ZVB, R&S ZVT Operating Manual*; R&S: Muenchen, Germany, 2014.
39. High Performance, Broadband Network Analysis Solutions, ME7838A/D/E Series Vector Network Analyzers Technical Data Sheet. Available online: http://gomeasure.dk/wp-content/uploads/2017/02/ME7838A.pdf (accessed on 1 April 2018).