## Article

# Soft Switching DC Converter for Medium Voltage Applications 

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#### Abstract

A dc-dc converter with asymmetric pulse-width modulation is presented for medium voltage applications, such as three-phase ac-dc converters, dc microgrid systems, or dc traction systems. To overcome high voltage stress on primary side and high current rating on secondary side, three dc-dc circuits with primary-series secondary-parallel structure are employed in the proposed converter. Current doubler rectifiers are used on the secondary side to achieve low ripple current on output side. Asymmetric pulse-width modulation is adopted to realize soft switching operation for power switches for wide load current operation and achieve high circuit efficiency. Current balancing cells with magnetic component are used on the primary side to achieve current balance in each circuit cell. The voltage balance capacitors are also adopted on primary side to realize voltage balance of input split capacitors. Finally, the circuit performance is confirmed and verified from the experiments with a 1.44 kW prototype.


Keywords: soft switching; asymmetric pulse-width modulation (APWM) converter; current doubler rectifier

## 1. Introduction

Medium voltage dc-dc converters have been proposed and implemented to achieve high power density and high efficiency advantages for dc light rail transportation systems [1,2], dc microgrid systems [3,4], or industry power converters [5,6]. In those applications, the high side dc bus voltage is normally at 750 V . The 1200 V SiC or Insulated Gate Bipolar Transistor (IGBT) power switches can be used to convert 750 V dc bus voltage to low voltage output through high-frequency link dc-dc converters. However, SiC devices are expensive, and the switching frequency of IGBT devices is less than 60 kHz . The series-connected switches $[7,8]$ and series-connected dc-dc converters $[9,10]$ can be used for medium voltage converters with 600V Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) power devices. These two approaches can reduce the voltage stress on power devices. However, the voltage stresses on each power switch are difficult and unbalanced. Therefore, power devices still have an unbalanced voltage stress problem. Three-level pulse-width modulation converters or resonant converters have been presented in [11-14] to lessen the voltage rating and switching loss on power devices. Modular converters with series or parallel connection have been developed in [15-17] for high voltage or current applications. However, the current balance in each circuit modular should be controlled well in order to distribute equal power in each modular. To solve the current balance issue in each circuit modular, the current balance control approaches have been discussed in $[18,19]$ by using the passive magnetic component.

This paper presents a high voltage dc-dc converter with three cascade half-bridge circuits on primary side to reduce the voltage and current ratings of power devices for high voltage and medium power applications, such as dc light trail transportation systems and three-phase ac-dc power converters. Voltage balance capacitors are also employed on the primary side in order to balance
input split voltages. To prevent current imbalance on each half bridge circuit, the magnetic coupling (MC) current balance components are employed between each half bridge circuit. If the primary-side currents are unbalanced, then the primary-side and secondary-side voltages of MC component will decreased, or increased, in order to compensate the imbalance in primary-side currents. Asymmetric pulse-width modulation approach is adopted to realize the soft switching turn-on characteristic for power switches. Therefore, the switching losses of power devices at high frequency operation can be reduced. Current doubler rectifiers are used on low voltage side in order to reduce the output ripple current. The paper is organized as follows. The circuit diagram and operating principle are presented in Section 2. The circuit characteristics of the proposed converter are discussed in Section 3. In Section 4, experiments are provided to demonstrate the effectiveness of the developed circuit. Then, the conclusion of the presented circuit is discussed in Section 5.

## 2. Circuit Diagram and Principles of Operation

The developed high-frequency link dc-dc converter is illustrated in Figure 1 to realize the main benefits of soft switching operation, low switching loss, low output ripple current and the balance primary-side and secondary-side currents. Three half-bridge circuits with primary-series secondary-parallel configuration are used in the proposed converter to realize low voltage stress $V_{i n} / 3$ on power switches $S_{1} \sim S_{6}$, and low current stress $I_{0} / 6$ on power diodes $D_{1} \sim D_{6}$. Therefore, 600 V power MOSFETs are used on the primary side to achieve high frequency operation and low conduction loss. Voltage balance capacitors $C_{f 1}$ and $C_{f 2}$ are employed on the primary side to achieve a split voltages balance at $V_{\text {in }} / 3$. Half-bridge circuits are operated under asymmetric pulse-width modulation. Therefore, the soft switching turn-on of power switches can be achieved, and the circuit efficiency is improved. The magnetic coupling current balance [19] cells, $M C_{1}$ and $M C_{2}$, are used on the primary side to achieve current balance for each half-bridge circuit. Therefore, the current unbalance issue of modular converters is overcome. The current doubler rectifiers are used on the secondary side to accomplish low ripple current on load side.


Figure 1. Circuit configuration of the developed modular converter for medium voltage applications.
Figure 2 provides the voltage and current waveforms of the studied converter in a switching cycle. Based on the pulse-width modulation waveforms shown in Figure 2, eight operating steps can be observed in each switching cycle under steady state. Power switches $S_{1}, S_{3}$, and $S_{5}$ have the same gating signals, and $S_{2}, S_{4}$, and $S_{6}$ have the same gating signals. The duty cycle of $S_{1}, S_{3}$, and $S_{5}$ denotes $d$ and the duty cycle of $S_{2}, S_{4}$, and $S_{6}$ is $1-d$. When $S_{1}, S_{3}$, and $S_{5}$ are active, then $S_{2}, S_{4}$, and $S_{6}$ are inactive. We can obtain that $v_{C f 1}=v_{C i n 1}$ and $v_{C f 2}=v_{C i n 2}$. If $S_{1}, S_{3}$, and $S_{5}$ are inactive, and $S_{2}, S_{4}$, and $S_{6}$ are active, then $v_{C f 1}=v_{C i n 2}$ and $v_{C f 2}=v_{C i n 3}$. For steady state operation, the capacitor voltages $v_{C i n 1}=v_{C i n 2}=v_{C i n 3}=v_{C f 1}=v_{C f 2}=V_{\text {in }} / 3$. Before the system analysis, the circuit parameters on
the proposed circuit are assumed as follows: (1) the same voltage balance capacitances $C_{f 1}=C_{f 2}=C_{f}$, (2) the same input split capacitances $C_{i n 1}=C_{i n 2}=C_{i n 3}=C_{i n}$, (3) the same output capacitances of power switches $C_{S 1}=\ldots=C_{S 6}=C_{o s s}$, (4) the same dc block capacitances $C_{1}=C_{2}=C_{3}=C_{c}$, (5) the same turns ratio $n_{1}=n_{2}=n_{3}=n$, (6) the identical magnetizing inductances $L_{m 1}=L_{m 2}=L_{m 3}=L_{m}$, (7) the same leakage inductances $L_{l k 1}=L_{l k 2}=L_{l k 3}=L_{l k} \ll L_{m}$, (8) the same output filter inductances $L_{1}=\ldots=L_{6}$ $=L_{0}$, and (9) the primary-side and secondary-side voltages of the magnetic coupling (MC) current balance transformers are zero under steady state. The equivalent circuits for eight operating steps are illustrated in Figure 3, and discussed as follows.


Figure 2. Pulse-width modulation waveforms of the proposed converter.
Step $1\left[t_{0} \sim t_{1}\right]$ : Before time $t_{0}$, all the secondary-side diodes are in the commutated interval, and the primary-side currents $i_{p 1} \sim i_{p 3}$ increase. After time $t_{0}$, the secondary-side diodes, $D_{1}, D_{3}$, and $D_{5}$, are off. In step 1 , the primary-side capacitor voltage $v_{C f 1}$ equals $v_{C i n 1}$, and $v_{C f 2}$ equals $v_{C i n 2}$. The ac-side input voltages of three half bridge circuits $v_{a b}, v_{c d}$, and $v_{e f}$ are clamped at $v_{\text {Cin } 1}, v_{\text {Cin } 2}$, and $v_{\text {Cin } 3}$, respectively. The magnetizing inductor voltages $v_{L m 1}, v_{L m 2}$, and $v_{L m 3}$ are equal to $V_{\text {in }} / 3-v_{C 1}, V_{\text {in }} / 3$ $-v_{C 2}$, and $V_{i n} / 3-v_{C 3}$, respectively. The secondary-side inductor voltages $v_{L 1}, v_{L 3}$, and $v_{L 5}$ are equal to $\left(V_{i n} / 3-v_{C 1}\right) / n-V_{o},\left(V_{i n} / 3-v_{C 2}\right) / n-V_{o}$ and $\left(V_{i n} / 3-v_{C 3}\right) / n-V_{o}$, respectively, and $v_{L 2}=v_{L 4}$ $=v_{L 6}=-V_{o}$. Therefore, the primary-side currents $i_{p 1} \sim i_{p 3}$ and the secondary-side currents $i_{L 1}, i_{L 3}$, and $i_{L 5}$ increase, and the output inductor currents $i_{L 2}, i_{L 4}$, and $i_{L 6}$ decrease, in step 1.

Step 2 [ $t_{1} \sim t_{2}$ ]: Switches $S_{1}, S_{3}$, and $S_{5}$ are turned off at time $t_{1}$. Due to the positive value of $i_{p 1} \sim i_{p 3}, v_{C S 1}, v_{C S 3}$, and $v_{C S 5}$ are increased and $v_{C S 2}, v_{C S 4}$, and $v_{C S 6}$ are decreased. The charged and discharged times of $C_{S 1} \sim C_{S 6}$ are very fast so that the primary-side and secondary-side currents are constant in step 2.

Step 3 [ $t_{2} \sim t_{3}$ ]: When $v_{C S 2}=v_{C 1}, v_{C S 4}=v_{C 2}$ and $v_{C S 6}=v_{C 3}$ at time $t_{2}$. The primary-side and secondary-side winding voltages of $T_{1} \sim T_{3}$ are zero voltage. Thus, the secondary-side diodes $D_{1} \sim D_{6}$ are forward biased to commutate the load current such that $i_{L 1} \sim i_{L 6}$ decrease, $i_{D 1}, i_{D 3}$, and $i_{D 5}$ increase, and $i_{D 2}, i_{D 4}$, and $i_{D 6}$ decrease in step 3. $C_{S 2}, C_{S 4}$, and $C_{S 6}$ can be discharged to zero voltage if the energy on the leakage inductors $L_{l k 1} \sim L_{l k 3}$ is large enough, and the dead time $t_{d}$ between the upper and lower switches on each half bridge leg is larger than the time interval in steps 2 and 3.

Step $4\left[t_{3} \sim t_{4}\right]$ : The capacitor voltages $v_{C S 2}=v_{C S 4}=v_{C S 6}=0$ at time $t_{3}$. Due to $i_{p 1}\left(t_{3}\right) \sim i_{p 3}\left(t_{3}\right)$ being positive, the body diodes of $S_{2}, S_{4}$, and $S_{6}$ are conducting so that $S_{2}, S_{4}$, and $S_{6}$ are turned on at zero voltage switching. The secondary-side diodes, $D_{1} \sim D_{6}$, are at the commutated interval, and the primary-side leakage inductor voltages are $v_{l k 1}=-v_{C 1}, v_{l k 2}=-v_{C 2}$, and $v_{l k 3}=-v_{C 3}$. Thus, the primary-side currents $i_{p 1} \sim i_{p 3}$ and the secondary-side inductor currents $i_{L 1} \sim i_{L 6}$ all decrease in step 4 .

In step 4 , the current variations on $i_{p 1} \sim i_{p 3}$ approximate $I_{o} /(3 n)$ in order to accomplish the commutation interval through diodes $D_{1} \sim D_{6}$.

Therefore, the duty loss in step 4 is calculated as

$$
\begin{equation*}
d_{l o s s, 4}=\frac{\Delta t_{34}}{T_{s w}} \approx \frac{L_{l k} I_{o} f_{s w}}{3 n v_{\mathrm{C} 1}} \tag{1}
\end{equation*}
$$

Step $5\left[t_{4} \sim t_{5}\right]$ : The secondary-side diode currents $i_{D 2}, i_{D 4}$, and $i_{D 6}$ are zero, and become reverse biased. In step 5, the capacitor voltages $v_{C f 1}=v_{C i n 2}$ and $v_{C f 2}=v_{C i n 3}$, and the ac side voltages $v_{a b}=v_{c d}$ $=v_{e f}=0$. Therefore, the magnetizing inductor voltages $v_{L m 1} \approx-v_{C 1}, v_{L m 2} \approx-v_{C 2}$ and $v_{L m 3} \approx-v_{C 3}$. The output inductor voltages $v_{L 1}=v_{L 3}=v_{L 5}=-V_{o}, v_{L 2} \approx v_{C 1} / n-V_{o}, v_{L 4} \approx v_{C 2} / n-V_{o}$ and $v_{L 6} \approx$ $v_{C 3} / n-V_{o}$. Thus, $i_{L 1}, i_{L 3}$, and $i_{L 5}$ decrease, and $i_{L 2}, i_{L 4}$, and $i_{L 6}$ increase, in step 5 .

(a)

(c)

(e)

(b)

(d)

(f)

Figure 3. Cont.


Figure 3. Operation steps in a switching period (a) step 1, (b) step 2, (c) step 3, (d) step 4, (e) step 5, (f) step 6, (g) step 7, and (h) step 8.

Step $6\left[t_{5} \sim t_{6}\right]$ : Power switches $S_{2}, S_{4}$, and $S_{6}$ are turned off at time $t_{5}$. Due to $i_{p 1}\left(t_{5}\right)<0$, $i_{p 2}\left(t_{5}\right)<0$ and $i_{p 3}\left(t_{5}\right)<0$, then $C_{S 1}, C_{S 3}$, and $C_{S 5}$ will be discharged in step 6 . Since the charged and discharged times of $C_{S 1} \sim C_{S 6}$ are very fast, the primary-side and secondary-side inductor currents are approximately constant in step 6.

Step $7\left[t_{6} \sim t_{7}\right]$ : The output capacitor voltages $v_{C S 1}, v_{C S 3}$, and $v_{C S 5}$ are discharged to $v_{C 1}, v_{C 2}$, and $v_{\mathrm{C} 3}$, respectively, at time $t_{6}$. Then, the primary-side and secondary-side winding voltages of $T_{1} \sim T_{3}$ are all zero voltage. In step 7 , the secondary-side diodes $D_{1} \sim D_{6}$ are all conducting to commutate the inductor currents $i_{L 1} \sim i_{L 6}$. At time $t_{7}, C_{S 1}, C_{S 3}$, and $C_{S 5}$ are discharged to zero voltage.

Step $8\left[t_{7} \sim t_{0}+T_{s w}\right]$ : The capacitor voltages $C_{S 1}, C_{S 3}$, and $C_{S 5}$ are discharged to zero voltage at time $t_{7}$. Due to $i_{p 1}\left(t_{7}\right) \sim i_{p 3}\left(t_{7}\right)$ being all negative, the body diodes of $S_{1}, S_{3}$, and $S_{5}$ conduct. Therefore, $S_{1}, S_{3}$, and $S_{5}$ can be turned on under zero voltage after time $t_{7}$. Since $D_{1} \sim D_{6}$ are still conducting, the primary-side currents increase. The diodes currents $i_{D 1}, i_{D 3}$, and $i_{D 5}$ decrease to zero at time $t_{0}+T_{s w}$. The duty loss in this step 8 is calculated as:

$$
\begin{equation*}
d_{l o s s, 8} \approx \frac{L_{l k} I_{o} f_{s w}}{3 n\left(V_{i n} / 3-v_{\mathrm{C} 1}\right)} \tag{2}
\end{equation*}
$$

## 3. Circuit Characteristics

Three half bridge circuits are used in the proposed converter with primary-series and secondary-parallel connection to distribute load power through three circuits. Therefore, the power rating of each half bridge circuit is one-third of load power, $P_{o} / 3$. In order to balance the modular currents, the magnetic coupling (MC) current balance cells are presented and discussed in [19]. Therefore, the magnetic coupling current balance components $M C_{1}$ and $M C_{2}$ are used in the proposed converter to achieve current balance issue between three half bridge circuits. If the primary-side currents are unbalanced, such as $\left|i_{p 2}\right|>\left|i_{p 3}\right|$, then the induced voltage $v_{M C 2, p}$ is lessened to decrease current $i_{p 2}$ and the secondary-side induced voltage $v_{M C 2, s}$ is increased to rise current $i_{p 3}$. If the primary currents are balanced $\left(\left|i_{p 1}\right|=\left|i_{p 2}\right|=\left|i_{p 3}\right|\right)$, then the induced primary-side and secondary-side voltages of $M C_{1}$ and $M C_{2}$ cells are zero voltage, $v_{M C 1, p}=v_{M C 1, s}=v_{M C 2, p}=v_{M C 2, s}=0$. Current doubler rectifiers are adopted on the secondary side to lessen the output ripple current. The average dc blocking voltages $V_{C 1} \sim V_{C 3}$ are related to the input voltage and duty cycle of $S_{1}, S_{3}$, and $S_{5}$. These three voltages can be calculated from the flux balance on the primary-side inductors.

$$
\begin{equation*}
V_{C 1}=V_{C 2}=V_{C 3}=d V_{i n} / 3 \tag{3}
\end{equation*}
$$

The output voltage is related to input voltage, duty cycle, and turns ratio, according to the flux balance on the output inductors.

$$
\begin{equation*}
V_{o}=\frac{d(1-d) V_{i n}}{3 n}-\frac{I_{o} L_{r} f_{s w}}{3 n^{2}}-V_{f} \tag{4}
\end{equation*}
$$

where $V_{f}$ is the voltage drop on $D_{1} \sim D_{6}$. Due to the MC, current balance components are used on the primary side of the proposed converter, and the output currents of three half bridge circuits are balanced in steady state. The average secondary-side winding currents of $T_{1} \sim T_{3}$ are zero. Therefore, the average output inductor currents are calculated as

$$
\begin{equation*}
I_{L 1}=I_{L 3}=I_{L 5}=(1-d) I_{o} / 3, I_{L 2}=I_{L 4}=I_{L 6}=d I_{o} / 3 \tag{5}
\end{equation*}
$$

If the duty cycle $d<0.5$, then the average inductor currents $I_{L 1}, I_{L 3}$, and $I_{L 5}$ are greater than $I_{L 2}$, $I_{L 4}$, and $I_{L 6}$. The ripple currents on $L_{1} \sim L_{6}$ are calculated as

$$
\begin{gather*}
\Delta i_{L 1}=\Delta i_{L 3}=\Delta i_{L 5}=\frac{V_{o}(1-d) T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n(1-d) V_{i n}}}{L_{o}}  \tag{6}\\
\Delta i_{L 2}=\Delta i_{L 4}=\Delta i_{L 6}=\frac{V_{o} d T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n d V_{i n}}}{L_{o}} \tag{7}
\end{gather*}
$$

From (5)~(7), the maximum and minimum output inductor currents are derived as

$$
\begin{align*}
i_{L 1, \max }= & i_{L 3, \max }=i_{L 5, \max }=\frac{(1-d) I_{o}}{3}+\frac{V_{o}(1-d) T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n(1-d) V_{i n}}}{2 L_{o}}  \tag{8}\\
i_{L 1, \min }= & i_{L 3, \min }=i_{L 5, \min }=\frac{(1-d) I_{o}}{3}-\frac{V_{o}(1-d) T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n(1-d) V_{i n}}}{2 L_{o}}  \tag{9}\\
& i_{L 2, \max }=i_{L 4, \max }=i_{L 6, \max }=\frac{d I_{o}}{3}+\frac{d V_{o} T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n d V_{i n}}}{2 L_{o}}  \tag{10}\\
& i_{L 2, \min }=i_{L 4, \min }=i_{L 6, \min }=\frac{d I_{o}}{3}-\frac{d V_{o} T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n d V_{i n}}}{2 L_{o}} \tag{11}
\end{align*}
$$

If the magnetizing inductances of $T_{1} \sim T_{3}$ are given, the ripple currents on $L_{m 1} \sim L_{m 3}$ are calculated as

$$
\begin{equation*}
\Delta i_{L m} \approx \frac{d(1-d) V_{i n} T_{s w}-\frac{L_{l k} I_{o}}{n}}{3 L_{m}} \tag{12}
\end{equation*}
$$

Due to the conducting time on $D_{1} \sim D_{6}$ being related to the duty cycle $d$, the secondary-side diode average currents and voltage ratings are calculated as

$$
\begin{gather*}
I_{D 1}=I_{D 3}=I_{D 5}=(1-d) I_{o} / 3, I_{D 2}=I_{D 4}=I_{D 6}=d I_{o} / 3  \tag{13}\\
V_{D 1, \text { stress }}=V_{D 3, \text { stress }}=V_{D 5, \text { stress }}=(1-d) V_{i n} /(3 n), V_{D 2, \text { stress }}=V_{D 4, \text { stress }}=V_{D 6, \text { stress }}=d V_{i n} /(3 n) \tag{14}
\end{gather*}
$$

Since the balance capacitors $C_{f 1}$ and $C_{f 2}$ are used on the primary side of three half bridge circuits, the input split voltages $V_{\operatorname{Cin} 1}, V_{\operatorname{Cin} 2}$, and $V_{\operatorname{Cin} 3}$ are balanced at $V_{i n} / 3$. Based on the half bridge circuit topology, the voltage rating of power switches $S_{1} \sim S_{6}$ is clamped at $V_{\text {in }} / 3$. If the ripple
currents on the output inductors and the magnetizing inductors are much less than the average output inductor currents at full load, then the root mean square ( rms ) currents of power devices are expressed in (15) and (16).

$$
\begin{gather*}
i_{S 1, r m s}=i_{S 3, r m s}=i_{S 5, r m s} \approx \frac{(1-d) I_{o}}{3 n} \sqrt{d}  \tag{15}\\
i_{S 2, r m s}=i_{S 4, r m s}=i_{S 6, r m s} \approx \frac{d I_{o}}{3 n} \sqrt{1-d} \tag{16}
\end{gather*}
$$

The zero voltage conditions of power switches $S_{1}, S_{3}$, and $S_{5}$ are related to the primary-side currents $i_{p 1}\left(t_{5}\right), i_{p 2}\left(t_{5}\right)$, and $i_{p 3}\left(t_{5}\right)$, respectively, and the input voltage. Similar, the zero voltage conditions of power switches $S_{2}, S_{4}$, and $S_{6}$ are related to the primary-side currents $i_{p 1}\left(t_{1}\right), i_{p 2}\left(t_{1}\right)$, and $i_{p 3}\left(t_{1}\right)$, respectively, and the input voltage. The primary-side currents $i_{p 1} \sim i_{p 3}$ at time $t_{1}$ and $t_{5}$ are related to the load current and the ripple currents on the magnetizing inductors $L_{m 1} \sim L_{m 3}$, and output inductors $L_{1} \sim L_{6}$.

$$
\begin{align*}
& i_{p 1}\left(t_{1}\right)=i_{p 2}\left(t_{1}\right)=i_{p 3}\left(t_{1}\right) \approx i_{L m 1, \max }+\frac{i_{L 1, \max }}{n} \approx \frac{d(1-d) V_{i n} T_{s w}-\frac{L_{l k} I_{o}}{n}}{6 L_{m}}+\frac{(1-d) I_{o}}{3 n}+\frac{(1-d) V_{o} T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n(1-d) V_{i n}}}{2 n L_{o}},  \tag{17}\\
& i_{p 1}\left(t_{5}\right)=i_{p 2}\left(t_{5}\right)=i_{p 3}\left(t_{5}\right) \approx i_{L m 2, \min }-\frac{i_{L 2, \max }}{n} \approx-\frac{d(1-d) V_{i n} T_{s w}-\frac{L_{l k} I_{o}}{n}}{6 L_{m}}-\frac{d I_{o}}{3 n}-\frac{d V_{o} T_{s w}+\frac{V_{o} L_{l k} I_{o}}{n d V_{i n}}}{2 n L_{0}} . \tag{18}
\end{align*}
$$

The necessary leakage inductance to achieve zero-voltage switching (ZVS) condition of $S_{1}, S_{3}$, and $S_{5}$ is expressed in (19).

$$
\begin{equation*}
L_{l k} \geq \frac{2 C_{o s s}\left(V_{i n} / 3\right)^{2}}{i_{p 1}^{2}\left(t_{5}\right)}=\frac{2 C_{o s s} V_{i n}^{2}}{9 i_{p 1}^{2}\left(t_{5}\right)} \tag{19}
\end{equation*}
$$

Similar, the necessary leakage inductance to achieve ZVS condition of $S_{2}, S_{4}$, and $S_{6}$ is expressed in (20).

$$
\begin{equation*}
L_{l k} \geq \frac{2 C_{o s s}\left(V_{i n} / 3\right)^{2}}{i_{p 1}^{2}\left(t_{1}\right)}=\frac{2 C_{o s s} V_{i n}^{2}}{9 i_{p 1}^{2}\left(t_{1}\right)} \tag{20}
\end{equation*}
$$

Based on the zero-voltage condition in (19) and (20), the necessary leakage inductance can be calculated in (21).

$$
\begin{equation*}
L_{l k} \geq \max \left\{\frac{2 C_{o s s} V_{i n}^{2}}{9 i_{p 1}^{2}\left(t_{1}\right)}, \frac{2 C_{o s s} V_{i n}^{2}}{9 i_{p 1}^{2}\left(t_{5}\right)}\right\} \tag{21}
\end{equation*}
$$

If the ripple voltage on dc blocking capacitors $C_{1} \sim C_{3}$ is less than $20 \%$ of the average voltage value, then the dc blocking capacitances $C_{1} \sim C_{3}$ are calculated as

$$
\begin{equation*}
C_{1}=C_{2}=C_{3}>\frac{5(1-d) I_{o} T_{s w}}{n V_{i n}} \tag{22}
\end{equation*}
$$

## 4. Experimental Results

Experiments based on a laboratory prototype are provided to verify the effectiveness of the developed circuit. The input dc voltage $V_{i n, \min }=750 \mathrm{~V}$ and $V_{i n, \max }=800 \mathrm{~V}$, the output voltage $V_{o}=24 \mathrm{~V}$ and the maximum load current $I_{o}=60 \mathrm{~A}$. The switching frequency $f_{s w}=100 \mathrm{kHz}$. The circuit components of the laboratory prototype are summary in Table 1. Figure 4 illustrates the picture of the laboratory prototype circuit. Figure 5 presents the test results of the gating signals of $S_{1}, S_{2}, S_{3}$, and $S_{5}$ under the rated power. The switches $S_{1}$ and $S_{2}$ have complementary gating signals, and $S_{1}$, $S_{3}$, and $S_{5}$ have identical pulse-width modulation signals. Figure 6 illustrates the test waveforms of the primary-side voltage $v_{a b}$ and currents $i_{p 1} \sim i_{p 3}$ at the rated power. It is clear that the three primary-side currents $i_{p 1} \sim i_{p 3}$ are well balanced. The input split voltages and balance capacitor voltage
at the rated power are measured and presented in Figure 7. The measured voltages are $V_{\text {Cin } 1}=251 \mathrm{~V}$, $V_{C i n 2}=249.3 \mathrm{~V}, V_{C i n 3}=249.7 \mathrm{~V}, V_{C f 1}=251 \mathrm{~V}$, and $V_{C f 2}=249 \mathrm{~V}$ under $V_{i n}=750 \mathrm{~V}$ input. It is clear that the input split voltages and balance capacitor voltages are well balanced. Figure 8 presents the test results of the gating voltage and drain current of power switch $S_{1}$ under $20 \%$ output load, and the rated output load for both 750 V and 800 V input cases. Before the power switch $S_{1}$ is turned on, the drain current is a negative value, to discharge the drain voltage. Therefore, the soft switching characteristic of $S_{1}$ can be realized from $20 \%$ output load to the rated output load, based on the test results in Figure 8. Similarly, the measured waveforms of $S_{2}$ are presented in Figure 9. It can be observed that the zero-voltage switching characteristic of $S_{2}$ is also achieved from $20 \%$ output load. Since power devices $S_{3}$ and $S_{5}$ are operated in the same circuit manner as power device $S_{1}$, and $S_{4}$ and $S_{6}$ are controlled in the same circuit manner as $S_{2}$, it can be expected that the zero-voltage switching of power switches $S_{3} \sim S_{6}$ are all achieved from $20 \%$ output load. The secondary-side inductor currents and diode currents of first half bridge circuit are measured and presented in Figure 10a under the rated power. The output currents of three half bridge circuits under the full output power are illustrated in Figure 10b. The test results show the three output currents are well balanced. Figure 11 illustrates the measured efficiencies of the proposed circuit under different load conditions and input voltages. The measured circuit efficiencies of the developed converter are $91.5 \%$ at $20 \%$ rated power, $93.2 \%$ at $50 \%$ rated power, and $92.7 \%$ at the rated power under 750 V input. At 750 V input and the rated power, the duty ratio is close to 0.5 , and the current rating on power devices and inductors are almost balanced. Therefore, the power losses are nearly distributed into each power devices and the circuit efficiency is improved, compared to the low load condition and higher voltage input.

Table 1. Prototype Circuit Parameters.

| Items | Symbol | Parameter |
| :---: | :---: | :---: |
| Input voltage | $V_{i n}$ | $750 \mathrm{~V} \sim 800 \mathrm{~V}$ |
| Output voltage | $V_{o}$ | 24 V |
| Rated output current | $I_{o}$ | 60 A |
| Switching frequency | $f_{s w}$ | 100 kHz |
| Input capacitors | $C_{i n 1}, C_{i n 2}, C_{i n 3}$ | $180 \mu \mathrm{~F} / 450 \mathrm{~V}$ |
| Voltage balance capacitors | $C_{f 1}, C_{f 2}$ | $2.2 \mu \mathrm{~F} / 630 \mathrm{~V}$ |
| Power switches | $S_{1 \sim} \sim S_{6}$ | 2 SK 4124 |
| Rectifier diodes | $D_{1 \sim D_{6}}$ | MBR 40100 PT |
| dc block capacitors | $C_{1} \sim C_{3}$ | $0.2 \mu \mathrm{~F}$ |
| Turns ratio of $T_{1} \sim T_{3}$ | $n_{1} \sim n_{3}$ | $1.5(33 \mathrm{turns} / 22 \mathrm{turns})$ |
| Leakage inductances | $L_{l k 1} \sim L_{r 3}$ | $15 \mu \mathrm{H}$ |
| Magnetizing inductances | $L_{m 1} \sim L_{m 3}$ | 0.6 mH |
| Output inductances | $L_{1 \sim L_{6}}$ | $66 \mu \mathrm{H}$ |
| Output capacitance | $C_{o}$ | $4700 \mu \mathrm{~F} / 50 \mathrm{~V}$ |



Figure 4. Picture of the prototype circuit.


Figure 5. Measured waveforms of the gating voltages of $S_{1}, S_{2}, S_{3}$, and $S_{5}$ at the rated power (a) with $V_{\text {in }}=750 \mathrm{~V}$ and (b) with $V_{\text {in }}=800 \mathrm{~V}$.

(a)

Figure 6. Cont.

(b)

Figure 6. Measured three primary-side currents $i_{p 1} \sim i_{p 3}$ at rated power (a) with $V_{i n}=750 \mathrm{~V}$ and (b) with $V_{\text {in }}=800 \mathrm{~V}$.


Figure 7. Measured results of the input split voltages and balance capacitor voltage at the rated power (a) with $V_{\text {in }}=750 \mathrm{~V}$ and (b) with $V_{\text {in }}=800 \mathrm{~V}$.


Figure 8. Measured results of the gating voltage and current of $S_{1}$ under (a) $V_{i n}=750 \mathrm{~V}$ and $20 \%$ output load, (b) $V_{\text {in }}=750 \mathrm{~V}$ and the rated output load, (c) $V_{i n}=800 \mathrm{~V}$ and $20 \%$ output load, and (d) $V_{\text {in }}=800 \mathrm{~V}$ and the rated output load.


Figure 9. Cont.


Figure 9. Measured results of the gating voltage and current of $S_{2}$ under (a) $V_{i n}=750 \mathrm{~V}$ and $20 \%$ output load, (b) $V_{\text {in }}=750 \mathrm{~V}$ and the rated output load, (c) $V_{i n}=800 \mathrm{~V}$ and $20 \%$ output load, and (d) $V_{\text {in }}=800 \mathrm{~V}$ and the rated output load.


Figure 10. Measured waveforms of the secondary-side currents at the rated output power (a) $i_{L 1}, i_{L 2}$, $i_{D 1}$, and $i_{D 2}$ in first half bridge circuit and (b) output currents of three half bridge circuits.


Figure 11. Measured efficiencies of the proposed converter.

## 5. Conclusions

A modular dc-dc converter with magnetic coupling current balance is presented for high power industry power units, dc light rail transportation, or dc microgrid system applications. Three half bridge circuits are employed in the proposed converter with primary-series secondary-parallel connection to lessen the voltage stress of power devices on high voltage side and current stress of passive components on low voltage side. Balance capacitors are used on high voltage side to achieve voltage balance on input split capacitors. In order to achieve current balance of three half bridge circuits, magnetic coupling current balance components are employed on the primary-side. The current doubler rectifiers are used on low voltage side to achieve partial ripple current reduction. Asymmetric pulse-width modulation approach is used to control power switches and regulate load voltage. From the experimental results, all power switches can be turned on at zero voltage from $20 \%$ output power. The other dc-dc converter topologies, such as full-bridge converter with phase-shift pulse-width modulation and resonant converter with frequency control, can also be applied in the proposed modular dc-dc converter with series-parallel connection with currents sharing and split voltages balance. Full-bridge circuit has two times of switch counts compared to the half-bridge circuits in the proposed converter. That will increase the cost and converter size. The resonant converter with frequency modulation cannot be designed at the optimal condition due to the switching frequency being related to the load condition and input voltage. Based on the analysis of circuit characteristics in Section 3 and the test results, it can be observed that the main drawbacks of the proposed converter, with asymmetric pulse-width modulation scheme, are unbalanced current rating on power devices $S_{1} \sim S_{6}$ and $D_{1} \sim D_{6}$, and inductors $L_{1} \sim L_{6}$, due to the duty cycle being related to the load current and input voltage. Similar, the average voltages on dc blocking capacitors $C_{1} \sim C_{3}$ are also related to duty cycle. If the proposed converter is operated under duty cycle equals 0.5 , then the current rating of all power devices and inductors are balanced.

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