electronics

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A Radiation-Hardened Instrumentation Amplifier for Sensor Readout Integrated Circuits in Nuclear Fusion Applications

Kyungsoo Jeong [1], Duckhoon Ro [1], Gwanho Lee [2], Myounggon Kang [2,*] and Hyung-Min Lee [1,*]

[1] School of Electrical Engineering, Korea University, Seoul 02841, Korea; jksoo2002@korea.ac.kr (K.J.); roduckhoon@korea.ac.kr (D.R.)

[2] Department of Electronics Engineering, Korea National University of Transportation, Chungju 27469, Korea; ghlee@ut.ac.kr

* Correspondence: mgkang@ut.ac.kr (M.K.); hyungmin@korea.ac.kr (H.-M.L.); Tel.: +82-43-841-5164 (M.K.); +82-2-3290-3219 (H.-M.L.)

Received: 22 November 2018; Accepted: 9 December 2018; Published: 12 December 2018

Abstract: A nuclear fusion reactor requires a radiation-hardened sensor readout integrated circuit (IC), whose operation should be tolerant against harsh radiation effects up to MGy or higher. This paper proposes radiation-hardening circuit design techniques for an instrumentation amplifier (IA), which is one of the most sensitive circuits in the sensor readout IC. The paper studied design considerations for choosing the IA topology for radiation environments and proposes a radiation-hardened IA structure with total-ionizing-dose (TID) effect monitoring and adaptive reference control functions. The radiation-hardened performance of the proposed IA was verified through model-based circuit simulations by using compact transistor models that reflected the TID effects into complementary metal–oxide–semiconductor (CMOS) parameters. The proposed IA was designed with the 65 nm standard CMOS process and provides adjustable voltage gain between 3 and 15, bandwidth up to 400 kHz, and power consumption of 34.6 μW, while maintaining a stable performance over TID effects up to 1 MGy.

Keywords: radiation-hardened; instrumentation amplifier; sensor readout IC; total ionizing dose; nuclear fusion

1. Introduction

Radiation effects on electronic components are critical issues in various fields, such as space, medical imaging, and nuclear applications. Among them, nuclear fusion has been considered a safe and effective solution to generate massive energy, while requiring accurate sensing systems to precisely control environmental parameters in the nuclear fusion reactor, such as temperature, pressure, electromagnetic field, etc. [1–3]. Thus, a sensor readout system, which amplifies sensor signals and provides digitized codes to the back-end control system, plays an important role to guarantee reliability and safety of the nuclear fusion system.

The sensor readout integrated circuit (IC) typically consists of four circuit blocks as shown in Figure 1: instrumentation amplifier (IA), filter, analog-to-digital converter (ADC), and multiplexer (MUX). The IA amplifies the small sensor signals, and the filter passes the signals in the frequency band of interest. Then, the ADC converts the analog signals to digital codes, which are serialized through the MUX and provided to the back-end control system. The IA is one of the most critical circuits that needs to amplify the sensor signal accurately at the first stage of the sensor readout IC.

However, the IA typically consists of variation-sensitive analog circuits, and its performance easily suffers from parameter variations under radiation effects.

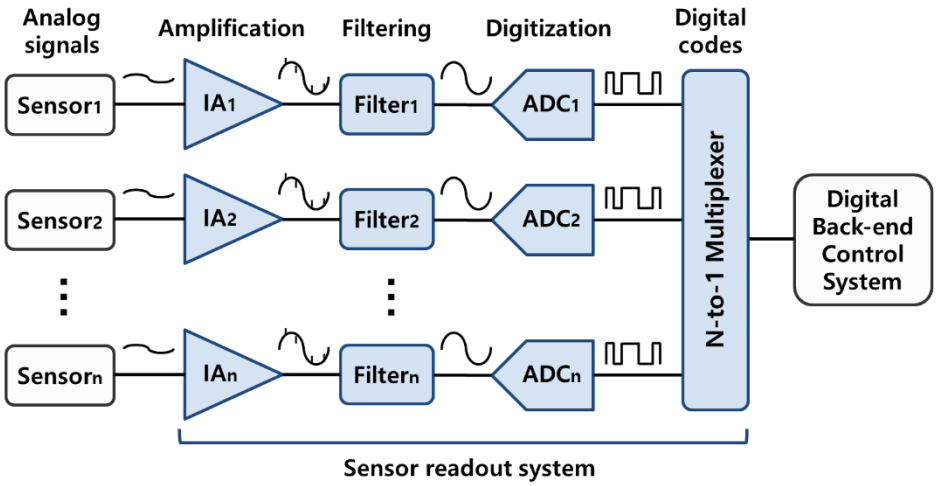


Figure 1. Block diagram of the sensor readout integrated circuit (IC) system. IA: instrumentation amplifier; ADC: analog-to-digital converter.

To reduce the radiation effects on the electronic components, three radiation-hardening methods have been widely considered: radiation hardening by process (RHBP), radiation hardening by shielding (RHBS), and radiation hardening by design (RHBD) [4–6]. While RHBP and RHBS, which improve the radiation tolerance by enhancing the process parameters and using shielded packages, respectively, have been effective ways for space and medical imaging applications, the nuclear fusion reactor suffers from more harsh radiation environments with high integral dose of MGy or higher [2,3]. Therefore, RHBD, which utilizes the optimized circuit structure against radiation effects, should also be considered for the sensor readout IC, especially, sensitive analog circuits, in nuclear fusion systems [6–12].

Silicon-based transistors in ICs, such as CMOS and bipolar junction transistor (BJT), can be affected by electrons, protons, and neutrons in radiation environments, which change the transistor parameters and degrade the circuit performance. These radiation effects on transistors can be categorized into three effects, i.e., total ionizing dose (TID), single event effect (SEE), and displacement damage (DD), as summarized in Table 1 [11–15]. The analog circuits with CMOS transistors mainly suffer from TID effects, which change the transistor parameters over time and are less vulnerable to SEE and DD effects. Thus, the proposed IA focuses on improving the radiation tolerance against the TID effects.

Table 1. Radiation effects to silicon-based transistors in ICs.

Radiation Effects	Cause	Effects to Analog Circuits
Total ionizing dose (TID)	- High-energy particles get through devices and produce electron–hole pair - The holes are trapped in gate oxide	- Changes threshold voltages - Increases leakage currents - Changes transconductance - Increases 1/f noise
Single event effect (SEE)	- High-energy particles impact a device in a moment and change the voltage in a device	- Changes voltages in capacitors - Upsets data in memory or flip-flop
Displacement damage (DD)	- Silicon ions are deviated from crystal lattice by high-energy particles.	- Critical in BJTs and Diodes - Increases leakage current - Less effects to CMOS

In addition, it is important to estimate the IA performance against TID effects during the design stage. To accurately reproduce radiation effects on CMOS transistors, we utilized the compact transistor models, whose parameters were degraded by TID and applied those compact models to SPICE circuit

simulations. This compact model-based simulation methodology enables the precise estimation of the IA performance before conducting experiments in actual radiation environments.

The rest of this paper focuses on detailed techniques for the radiation-hardened IA design and performance verification through the compact model-based circuit simulation. Section 2 explains design considerations for choosing the IA topology for radiation environments. Section 3 proposes circuit techniques to improve the radiation tolerance in IAs. Section 4 describes how to use the compact transistor models for SPICE circuit simulations with radiation effects. Section 5 shows model-based simulation results, followed by concluding remarks in Section 6.

2. Radiation-Hardened IA Design

2.1. IA Topology Comparison

There is a variety of topologies of instrumentation amplifiers (IA) for sensor readout front-end ICs, such as capacitive-feedback IA, current-feedback IA, and three-op-amp IA, depending on users' requirements [16]. To design a radiation-hardened IA, it is essential to compare the performances in radiation environments and choose the optimum IA topology that is robust against TID and SEE effects.

The capacitive-feedback IA uses a couple of capacitors in the feedback loop, and the voltage gain is determined by the ratio between the capacitors. However, the voltage values across the capacitors can vary because of unwanted charge injection by SEE, which results in inaccurate output voltages. The current-feedback IA utilizes transconductance amplifiers at input and feedback paths to define its voltage gain with the ratio of transconductance (G_m). The current-feedback IA has the advantages of high common-mode rejection ratio (CMRR) and large input range, but the gain accuracy suffers from TID effects, which change the transconductance values.

Compared to those IAs, the three-op-amp IA enables relatively stable voltage gain against TID effects, since the gain is determined by the ratio between feedback resistors. While the three-op-amp IA has the advantages of high-input impedance and good linearity over wide input–output ranges, it is also less affected by SEE because the DC bias current flowing through the feedback loop keeps the voltage values across resistors from instantaneous charge injection by SEE. Therefore, the three-op-amp IA can be used as the radiation-hardened IA topology, which is less affected by both TID and SEE, compared to other IAs. Table 2 compares the performance of various IA topologies against TID and SEE.

Table 2. Performance comparison of IA topologies against total ionizing dose (TID) and single event effect (SEE). G_m: transconductance.

IA Topologies	Capacitive-Feedback IA	Current-Feedback IA	Three-op-amp IA
TID tolerance	O (Gain ∝ capacitor ratio)	X (Gain ∝ CMOS G_m ratio)	O (Gain ∝ resistor ratio)
SEE tolerance	X (Capacitor voltage changes)	O (DC bias on feedback)	O (DC bias on feedback)

2.2. Radiation-Hardened IA Structure

For the radiation-hardened IA, the op-amp circuits in the three-op-amp IA topology should also operate properly against radiation effects. For accurate readout of sensor signals, the two-stage op-amp with p-type metal–oxide–semiconductor (PMOS) input stages has been widely used thanks to its low noise, high gain, and wide output range [16]. However, the op-amp performance, such as voltage gain, bandwidth, and power consumption, can be degraded due to TID effects as follows: (1) threshold voltage (V_{th}) variation due to TID effects leads the transistors to operate in improper triode regions instead of saturation regions, especially, a tail current transistor in the input stage, and (2) bias currents flowing through the op-amp vary by TID effects, affecting the amplifier performance.

To overcome these limitations, we propose a radiation-hardened IA structure, which adopts the three-op-amp topology and fully-differential structure, while employing TID effect monitoring, V_{th}-insensitive current generator, and adaptive reference control. Figure 2 shows the conceptual block diagram of the proposed radiation-hardened IA. The TID effect monitoring circuit, which is reliably biased by the V_{th}-insensitive current generator, senses the V_{th} variation due to TID effects. Then, the adaptive reference control circuit automatically adjusts the sensor reference voltage, V_{REF}, keeping the tail current transistors in op-amps, A_1 and A_2, to operate in saturation regions regardless of V_{th} variation in the transistors. The voltage gain, which is defined as $A_V = [(R_1 + R_{sel} + R_1)/R_{sel}] \times [R_3/R_2]$, can be adjusted by digitally tuning the R_{sel} value, and the op-amp, A_3, provides fully differential output voltages, V_{OUTP} and V_{OUTN}, to the following ADC for accurate signal digitization. The V_{th}-insensitive current generator also supplies the bias currents not only to the op-amps, A_1–A_3, but also to the ADC for robust DC biasing against TID effects.

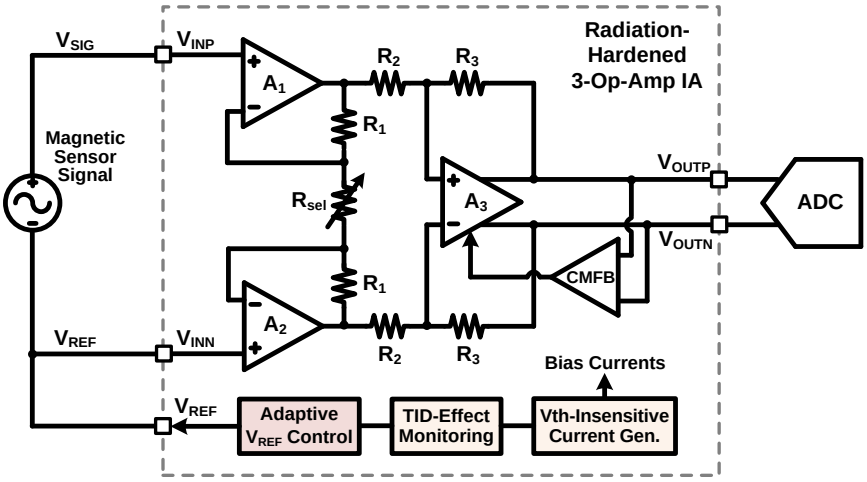


Figure 2. Conceptual block diagram of the proposed radiation-hardened IA.

3. Circuit Details for Radiation-Hardened IA

3.1. TID Effect Monitoring

Figure 3 shows the conceptual and schematic diagrams of the TID effect monitoring circuit, which can monitor the V_{th} variation of the CMOS transistor depending on the integral amount of TID effects. In Figure 3a, the TID effect monitoring consists of the PMOS monitoring transistor, M_M, and the current source, I_{REF}. Then, the monitoring voltage, V_M, can be expressed as follows:

$$V_M = V_{DD} - V_{SG,MM} = V_{DD} - V_{ov,MM} - V_{th,MM} \quad (1)$$

where V_{DD} is the supply voltage, and $V_{ov,MM}$ and $V_{th,MM}$ are the overdrive and threshold voltages of M_M, respectively. If I_{REF} has little variation against TID, then $V_{ov,MM}$ can be relatively constant, and $V_{th,MM}$ variation can be observed by monitoring V_M, which changes as TID increases.

To generate a constant I_{REF} against V_{th} variation by TID, we adopted a beta multiplier structure to implement the TID effect monitoring circuit, as shown in Figure 3b. The n-type metal–oxide–semiconductor (NMOS) transistors, M_6 and M_7, have different size ratio of 1:K, and the amplifier, which consists of M_1–M_4, ensures that drain and gate voltages of M_6 and M_7 are the same. M_M and M_5 have the same size ratio, flowing the same bias current of I_{REF} to M_6 and M_7, respectively. Then, I_{REF}, which flows through M_M, can be defined relatively constant, regardless of V_{th} variation as follows:

$$V_{GS6} = V_{GS7} + I_{REF}R_2 = \sqrt{\frac{2I_{REF}}{\beta_N}} + V_{th,M6} = \sqrt{\frac{2I_{REF}}{K\beta_N}} + V_{th,M7} + I_{REF}R_2 \quad (2)$$

$$I_{REF} = \frac{1}{\beta_N}\left(\frac{2}{R_2{}^2}\right)\left(1-\frac{1}{\sqrt{K}}\right)^2 \quad (3)$$

where β_N is $\mu_n C_{ox}(W/L)$, which are the NMOS transistor parameters, and assuming NMOS threshold voltages, $V_{th,M6}$ and $V_{th,M7}$, are affected by TID in the same way. Therefore, V_{th} variation of the monitoring transistor, M_M, which depends on TID over time, can be monitored by observing V_M. The bias current, I_{BIAS}, which supplies the op-amps in the IA, can be generated through M_{10}.

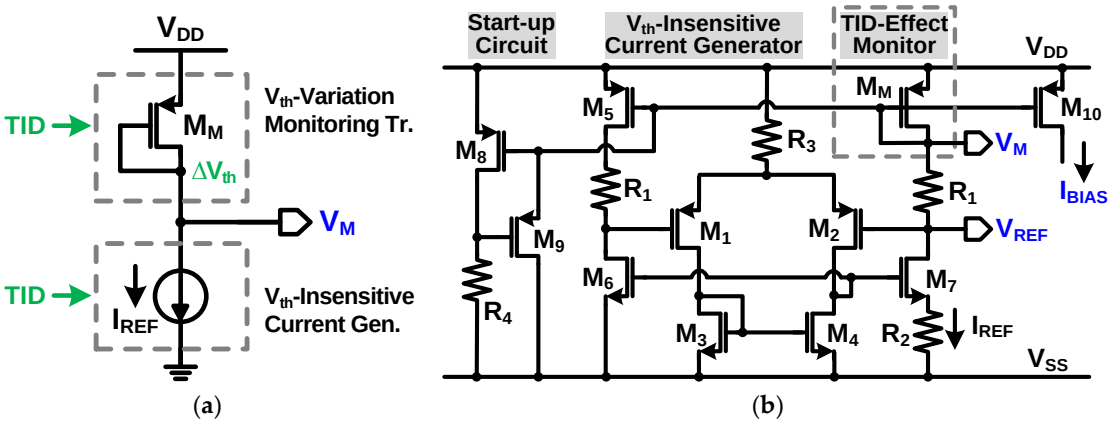


Figure 3. (**a**) Conceptual diagram and (**b**) schematic diagram of the TID effect monitoring circuit with the V_{th}-insensitive current generator.

3.2. Adaptive Reference Control

The maximum input voltage level of the op-amps with PMOS input transistors, such as A_1 and A_2 in Figure 2, is limited as $V_{DD} - V_{SG,in} - V_{ov,tail}$, where $V_{SG,in}$ is the source-gate voltage of the PMOS input transistor, and $V_{ov,tail}$ is the overdrive voltage of the tail current source transistor. However, the TID effects can change V_{th} of the transistors (typically increase V_{th} of PMOS transistors), decreasing the maximum input levels, leading the tail current transistor to operate in the triode region and finally degrading the op-amp performance.

To circumvent this situation, the adaptive reference control was utilized to automatically adjust the sensor reference voltage, V_{REF}, which is the common-mode input level of A_1 and A_2, as shown in Figure 4. The adaptive reference control utilizes the TID effect monitoring and the additional resistor R_1 to generate V_{REF} as $V_{DD} - V_{SG,MM} - I_{REF}R_1$. For example, if V_{th} of PMOS transistors increases due to TID, which decreases the maximum input level of the op-amps, V_{REF} (i.e., op-amp input levels) also adaptively decrease to ensure that op-amp input stages are operating properly in saturation regions. The detailed circuit to generate V_{REF} is shown in Figure 3b, and the buffer amplifier, A_4, drives the sensor reference node with V_{REF}.

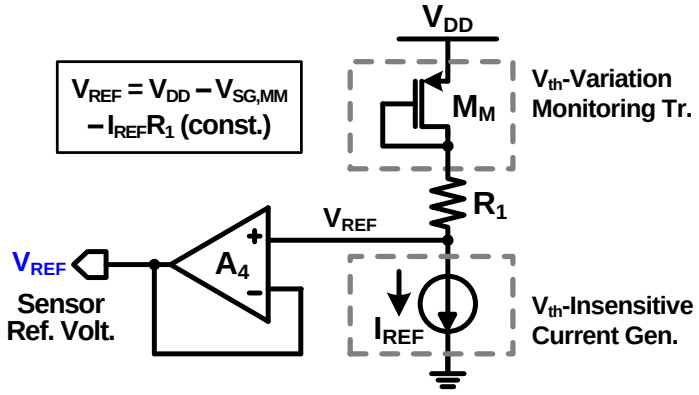
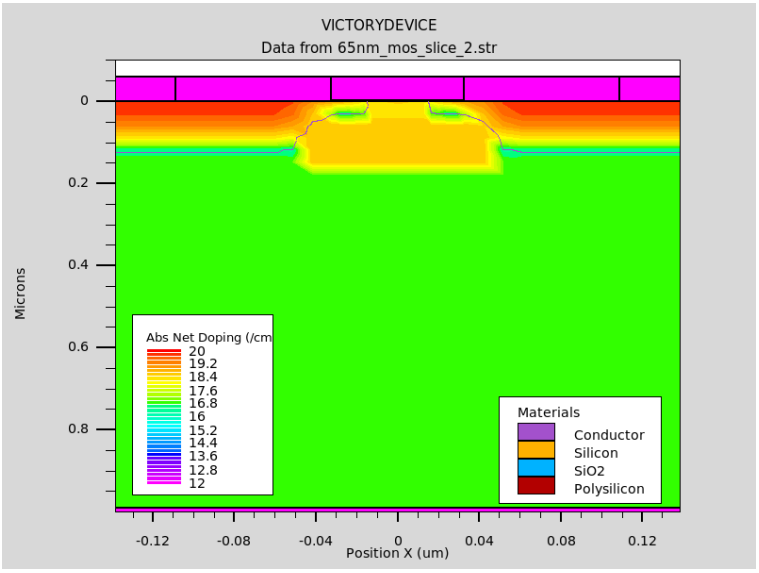


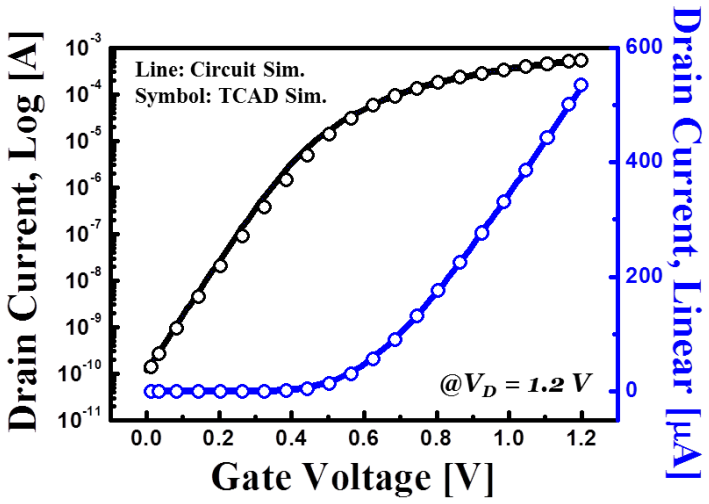
Figure 4. Conceptual diagram of the adaptive reference control.

4. Compact Transistor Modeling with Radiation Effects

In order to observe the circuit performance with the TID effects, the Berkeley short-channel IGFET Model (BSIM) 4 SPICE model was used in this work. The BSIM4 model is widely used as a standard compact model in the industry and has been developed for silicon-based MOS transistors [17,18]. Figure 5a shows a 65 nm device structure using a 3D technology computer-aided design (TCAD) simulation with the Silvaco Victory Device software. We evaluated the electrical characteristics considering various channel widths (W) and channel lengths (L) of the device structure. Figure 5b shows V_{GS} versus I_D characteristics with W = 1 µm and L = 65 nm. The TCAD simulation (circle symbols) showed excellent agreement with the circuit simulation (lines). This indicates that our TCAD simulation exactly reflected the devices used in the 65 nm CMOS process.



(**a**)



(**b**)

Figure 5. The 65 nm CMOS (**a**) structure and (**b**) comparison of V_{GS} vs. I_D between technology computer-aided design (TCAD) and circuit simulation.

Figure 6 shows the electrical characteristics of the device with TID effects for each Gy level. Figure 6a shows V_{GS} versus I_D, and Figure 6b shows V_{DS} versus I_D. To obtain compact models for each TID quantity, several levels of TID effects were applied to CMOS transistors through the TCAD

simulation with the Silvaco Victory Device software, which generated corresponding *I-V* curves. Then, BSIM parameters, such as *VTH*0 (long channel threshold voltage), *VFB* (flatband voltage), *VSAT* (saturation velocity), *CIT* (interface trap capacitance), etc., which affect the threshold voltage, subthreshold swing, and leakage current, were extracted from those *I-V* curves and utilized to develop the compact models for each TID. The V_{th} shift phenomenon and the off-current increase, which were caused by the TID effects, were confirmed. The *I-V* curve in Figure 6 was used for compact modeling in the BSIM4 parameter extraction process for each cumulative dose. The BSIM4 parameters were extracted by using Silvaco Utmost IV software. The flow chart of BSIM4 model parameter extraction was detailed in a previous work [18]. In order to extract the BSIM4 parameters, the V_{GS} versus I_D curve in linear and log scales and the V_{DS} versus I_D curve in linear scale were simultaneously considered. The BSIM4 parameters were extracted by matching the linear and saturation regions of the *I-V* curve by adjusting parameters such as V_{th0}, V_{sat}. [19,20].

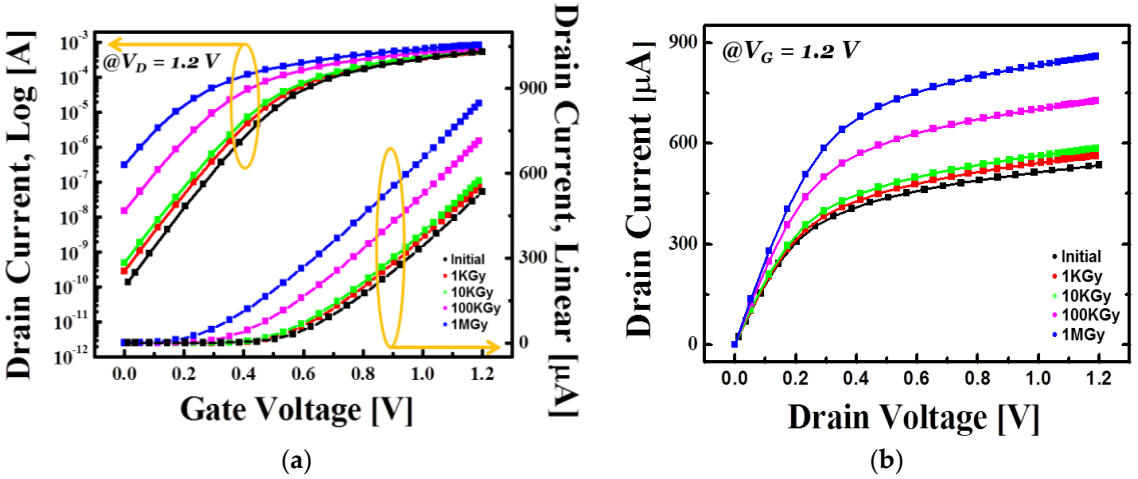


Figure 6. CMOS transistor characteristics depending on TID effects: (**a**) V_{GS} vs. I_D and (**b**) V_{DS} vs. I_D.

5. Simulation Results with Compact Transistor Models

The radiation-hardened IA in Figure 2 was designed in a 65 nm standard CMOS process with a supply voltage, V_{DD}, of 1.2 V and verified through the SPICE simulation. To emulate the TID effects on circuit simulation, we also utilized the compact transistor models described in Section 4. Each compact model included the TID effects of 1 kGy, 10 kGy, 100 kGy, and 1 MGy.

Figure 7 shows the reference current (I_{REF}), monitoring voltage (V_M), and sensor reference voltage (V_{REF}) of Figure 3 against the TID effects. While I_{REF} was relatively constant at higher TID, V_M showed the V_{th} variation of the TID-monitoring PMOS transistor (M_M in Figure 3). Then, V_{REF}, which also decreased at higher TID, could adaptively control the sensor reference level, ensuring TID-tolerant IA operation. Figure 8 shows the voltage gain of the radiation-hardened IA against the TID effects. In Figure 8a, the voltage gain of the radiation-hardened IA was set to 5 and showed a little variation as TID increased. However, the conventional IA, which also had the three-op-amp structure but its sensor reference level (V_{REF}) was fixed to half V_{DD}, had a significant drop of the voltage gain with TID above 10 kGy, because some transistors in the op-amps could operate in triode regions, and their bias currents significantly changed. On the contrary, the radiation-hardened IA could provide an adjustable voltage gain between 3 and 15 over high TID effects, as shown in Figure 8b.

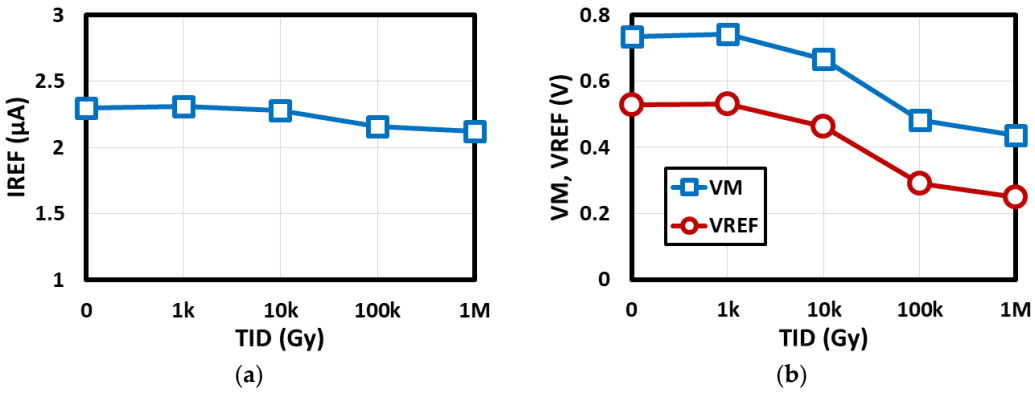


Figure 7. Model-simulation results showing (**a**) reference current (I_{REF}) vs. TID and (**b**) monitoring voltage (V_M) and sensor reference voltage (V_{REF}) vs. TID.

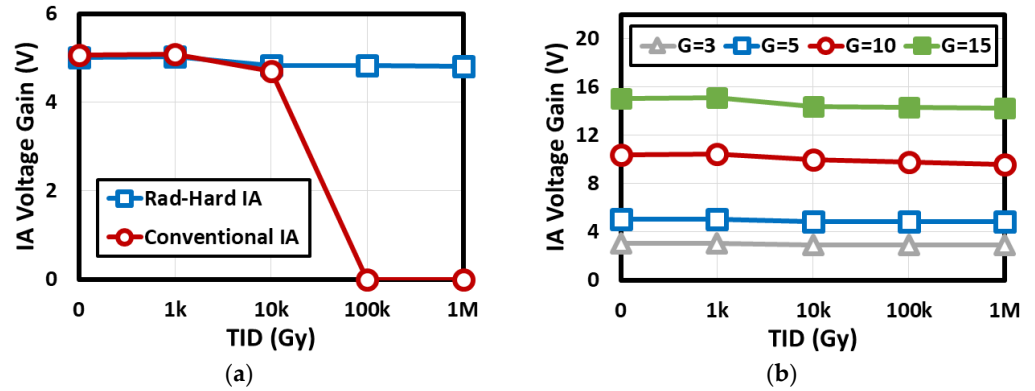


Figure 8. Model simulation results showing (**a**) voltage gain comparison between proposed and conventional IAs by TID and (**b**) adjustable voltage gain (3, 5, 10, and 15) of the proposed IA by TID.

The proposed IA aims for magnetic sensor signals in nuclear fusion reactors, in which the amplitude can be up to 100 mV, so that the IA adopts the adjustable voltage gain range between 3 and 15. Table 3 summarizes the overall performance of the radiation-hardened IA when the voltage gain was set to 5 and TID was 0 and 1 MGy. While the proposed IA maintained similar levels of voltage gains at the high TID of 1 MGy, the power consumption of the IA increased mainly as a consequence of V_{th} variations and leakage currents of the transistors. The bandwidth of the IA decreased to 80 kHz at TID of 1 MGy, but the proposed IA could still operate properly with sensor signals, whose frequencies were typically of the kHz order or lower. Also, the proposed IA provides fully differential output voltages, i.e., V_{OUTP} and V_{OUTN}, as in Figure 2, which enables a high power supply rejection ratio (PSRR). When intended offsets of 5 mV were applied to the amplifiers in experimental practical cases, the proposed IA achieved the PSRR of 81 dB, which could be maintained to 77.7 dB at TID up to 1 MGy.

Table 3. Overall performance of the radiation-hardened IA.

Specification	TID = 0 Gy	TID = 1 MGy
Process	65-nm standard CMOS	
Supply voltage (V)	1.2	
Voltage gain (V/V) *	5.008	4.812
Bandwidth (kHz) **	240	80
Power consumption (μW) **	34.6	98.3
Input referred noise (μV/$\sqrt{}$Hz) **	0.94	1.12
Power supply rejection ratio (dB) ***	81	77.7

* Adjustable between 3 and 15, ** model-simulated when the voltage gain was set to 5. *** Intended offsets of 5 mV were applied to the amplifiers in experimental practical cases.

While there have been few previous studies about radiation-hardened IAs, the radiation-hardening performance can be roughly compared with that of other analog circuits in sensor front-end systems, such as ADCs and voltage references. The radiation-hardened delta-sigma ADC in reference [11] showed 2.8% degradation (from 109 to 106 dB) in signal-to-noise-distortion ratio (SNDR) at TID up to 1.36 MGy. In radiation-hardened voltage references, the bandgap reference as reported [7] showed ±0.8% variation (±1.5 mV) in reference voltages at TID up to 0.44 MGy, and the bandgap reference reported in another study [12] achieved about ±3% variation (±18 mV) in reference voltages at TID up to 4.5 MGy. Compared to those performances, the proposed radiation-hardened IA achieved 3.9% degradation (from 5.008 to 4.812) in voltage gain at TID up to 1 MGy, showing competitive performance of the circuit design techniques for radiation hardening. Also, it should be noted that the proposed radiation hardening by design (RHBD) can be used along with RHBP and RHBS to further improve the radiation tolerance of the electronic components.

6. Conclusions

A radiation-hardened instrumentation amplifier (IA), which needs to ensure a robust operation against radiation effects such as TID and SEE, is an essential component of sensor readout systems in harsh radiation environments such as nuclear fusion reactors. This paper studied design considerations for choosing the IA topology for radiation environments and proposed the radiation-hardened IA circuit with TID effect monitoring and adaptive reference control functions. The radiation tolerance of the proposed IA was verified through the SPICE circuit simulations by adopting compact transistor models that reflected the TID effects into CMOS parameters.

Author Contributions: Methodology, Validation, Paper Writing, K.J., D.R. and G.L.; Conceptualization, Funding Acquisition, Investigation, Supervision, Writing-Review & Editing, M.K. and H.-M.L.

Funding: This research was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science & ICT (NRF-2017M1A7A1A01016260). This research was also supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science & ICT (NRF-2017M1A7A1A01016265).

Acknowledgments: The EDA tool was supported by the IC Design Education Center (IDEC), Korea. The authors would like to thank Suk-Ho Hong and Heung Su Kim of the National Fusion Research Institute (NFRI), Daejeon, Korea, for technical discussion.

Conflicts of Interest: The authors declare no conflict of interest.

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