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Design of an Highly Efficient AC-DC-AC Three-Phase Converter Using SiC for UPS Applications

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Abstract: With the constant increase of energy consumption in the world, the efficiency of systems and equipment is becoming more important. Uninterruptible Power Supply (UPS) is an equipment that provides safe and reliable supply for critical load systems, that is, systems where a supply interruption can lead to economical or even human losses. The Double Conversion UPS is the most complete UPS class in terms of load protection, regulation, performance, and reliability, however, it has lower efficiency and higher cost because of its high number of power converters. Silicon Carbide devices are emerging as an opportunity to construct power converters with higher efficiency and higher power density. The main purpose of this work is to design a three-phase AC-DC-AC converter using Silicon Carbide for Double Conversion UPS applications. The aim is to maximize efficiency and minimize volume and mass. The methodologies to size and choose the main hardware components are described in detail. Experimental results obtained with the prototype prove the high efficiency and high power density achievable with Silicon Carbide Metal Oxide Semiconductor Field Effect Transistor (MOSFETs).

Keywords: UPS; Silicon Carbide; power converters; design; high efficiency

1. Introduction

Currently, final energy consumption in the form of electricity accounts for a large share of the world's energy consumption, and may reach more than 50% in some countries [1]. In developing countries, the consumption of electric energy presents accelerated growth, for example, it has increased about 56% in Brazil and 455% in China between 2000 and 2014 [1]. Against this scenario, rational use of electricity and energy efficiency of the generation-storage-distribution-consumption cycle become very important for engineers and researchers that aim the sustainable development.

Among the various types of loads present in the electrical system, we can highlight the critical loads, that is, loads that cannot have the supply of electricity interrupted regardless of the environmental conditions and failures in the electrical system. Examples of critical loads are: Telecommunications and information technology systems, hospital equipment, and banking systems. In order to supply such loads, Uninterruptible Power Supplies (UPS) are often used.

According to the topology or configuration, UPS can be classified as double conversion, passive standby, and line interactive types [2,3]. Double conversion UPS is generally preferred because of the wide tolerance to input voltage variation, output voltage regulation and high system reliability [2,3]. A conventional three-phase double conversion UPS usually contains a rectifier, battery charger, battery pack, inverter, and by-pass switches.

Three-phase UPSs found commercially and in scientific work are based, with slight variations, on a classical topology employing two-level PWM converters [4–7]. Despite being able to maintain power quality on both the mains side and the load side, its efficiency is limited due to the large switching losses in the electronic switches.

For the sake of improving UPS system's performance, the use of three-level topologies in the rectifier and in the inverter [8,9] has been proposed. The proposed converters can achieve high efficiency, however the complexity and number of electronic switches increases considerably. In order to find a compromise between performance, cost and complexity, hybrid converters can be used, combining different topologies on the inverter side and on the rectifier side [10].

Despite being a mature technology, silicon power transistors have limitations in terms of switching performance due to reverse recovery from diodes and IGBT tail current which significantly increase switching losses [11]. One approach to overcome these limitations and to improve the performance of electronic converters is the use of transistors made of materials with wide bandgap (WBG), such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Several studies have demonstrated the possibility of applying SiC and GaN transistors in converters operating at high switching frequencies, high voltages, and high working temperature [11–14], including in the UPS sector for single-phase converters [15,16]. The characteristics of such materials allow the construction of equipment with smaller passive elements, smaller heat sinks, and at the same time improve the efficiency of the system [17].

In the cited circumstances, this work intents to design a more compact three-phase AC-DC-AC converter for UPS applications using silicon carbide and advanced topologies. The resulting converter should have higher efficiency and higher power density in relation to commercially available equipment, thus becoming more competitive in the market. The focus of this work is the AC-DC-AC conversion chain, so the investigation of auxiliary circuits such as by-pass switches, battery charger, and DC-link balance leg will not be made.

2. UPS Specifications

Table 1 summarizes the main specifications and design criteria for this AC-DC-AC conversion chain. An extensive topology and components comparison was done in [18] for two case scenarios, from the analyses carried out, it was decided to design the optimal converter that fits the specifications declared. The schematic diagram of the chosen topology is shown in Figure 1, it employs a Vienna Rectifier at the input and a 2-level inverter at the output. Silicon Carbide devices SCT3030AL (Q_1 to Q_{12}) and STPSC40065C (D_1 to D_6) will be used operating with switching frequencies up to 102 kHz in order to improve power density and achieve high efficiency. It was also verified in [18] that a Silicon IGBT-based converter would be unpractical due to very high switching losses when operating at 100 kHz. The converter will operate with slightly different switching frequencies for the rectifier and for the inverter to avoid resonances and oscillations.

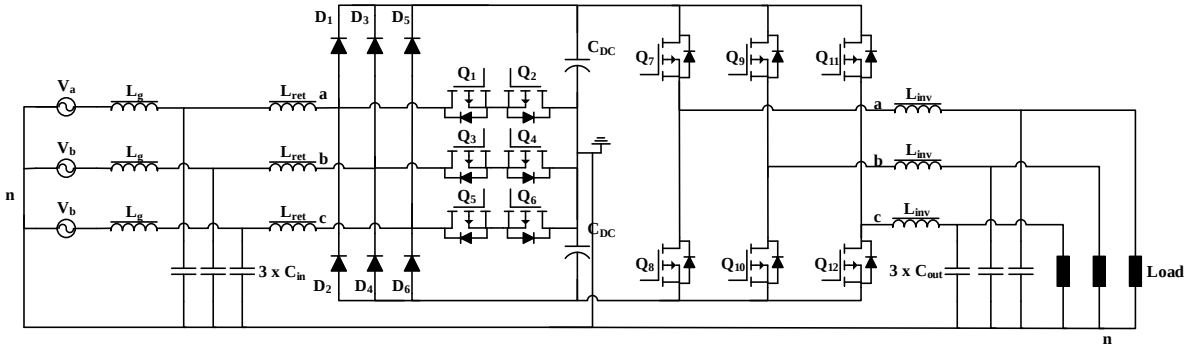

Figure 1. Proposed AC-DC-AC converter.

Table 1. Main specifications and design criteria.

Especification	Value
Output Power (P_{inv})	10 kW
Output voltage phase-neutral (V_{a-inv})	127 V
Output current (I_{a-inv})	26.25 A
Input Power (P_{ret})	11 kW
Input voltage phase-neutral (V_{a-ret})	127 V +/− 10%
Input current (I_{a-ret})	32 A (worst case)
DC link voltage (V_{dc})	400 V
Grid frequency (f_g)	60 Hz
Inverter's switching frequency (f_{sw-inv})	101.34 kHz
Rectifier's switching frequency (f_{sw-inv})	102 kHz
Ambient temperature (T_a)	40 °C
Max. junction temperature (T_j)	150 °C
Max. inverter current ripple($\Delta I_{max-inv}$)	40% of peak current
Max. rectifier current ripple ($\Delta I_{max-ret}$)	30% of peak current
Max. DC link ripple (ΔV_c)	5% of V_{dc}
Efficiency (η)	95%

3. Hardware Design

This section is focused on the design of the main hardware components. The following topics are addressed: Thermal design (loss estimation and heat sink sizing), inductor design (L_{ret} and L_{inv}), and capacitors sizing (DC link and filter capacitors).

3.1. Thermal Design

Despite being a good first step for comparison and topology choice, the estimation of switch losses through the use of datasheet's switching energy curves, as done in [18], is not accurate. The manufacturer does not clearly state the conditions under which the double pulse test was performed, the measuring equipment used, and the inductance of the switching loop are not reported. Some researchers have published recent works reporting big differences between the energy curves available in the datasheet and experimental curves verified in real prototypes [19–21].

The cited works used experimental setups to measure the switching energies to, then, be able to use this data in the converter loss estimation. However, most of the time it is necessary that the designer can estimate the losses of a converter without the need to perform an experimental procedure.

Thus, this work will use a simulation approach to estimate the energy curves of the SiC MOSFET and, afterward, estimate the losses. The simulation will be done in Spice via SImetrix software using the Spice model of the SCT3030AL transistor provided by the manufacturer. However, the simulation must be done in order to model a more realistic condition of operation considering the inductances of the power loop and transistors leads. These inductances exert great influence on the transistor's switching and can make it slower. Thus, a more realistic simulation was performed including the parasitic inductances of decoupling capacitors, transistors, and PCB tracks. The simulation diagram can be seen in Figure 2.

The simulation was performed for current values between 0 and 75 A, and the energy curves obtained were plotted in Figure 3 with the curves provided by the manufacturer.

By analyzing the graph, it is possible to notice that the inclusion of the parasite inductances greatly affects the switching losses, which reaffirms the need to minimize these inductances. The difference reaches about 70% to the maximum current point. In addition, it is noted that when the current is close to zero, the switching energy is not zero, this is due to insufficient energy to discharge and charge the parasitic capacitances of the transistors. In this way, the switching will only occur after the end of the dead time, when the complementary key will be closed, realizing the abrupt charge and discharge of the MOSFETs output capacitances. Therefore, when the current is close to zero, the energy lost in the switching corresponds to the energy stored in the parasitic capacitances.

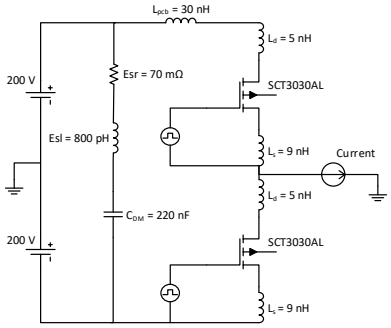

Figure 2. Diagram of the simulation performed in Spice to extract the switching energy curves, with addition of parasite inductances.

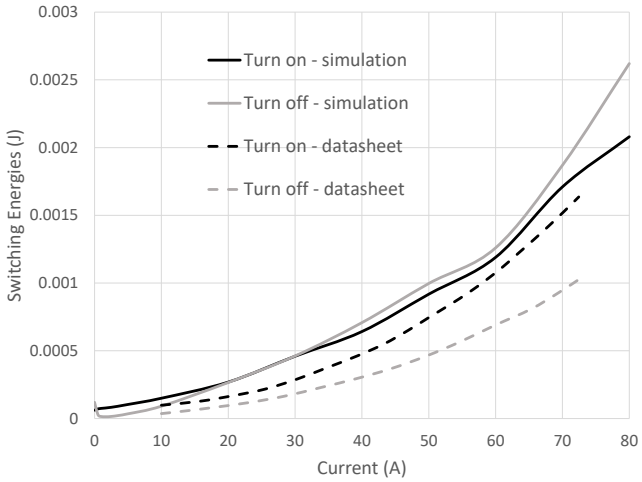

Figure 3. Comparison of the energy curves obtained by simulation and the curves disclosed in the datasheet of the device SCT3030AL. Conditions: V_{gs} = 18 V/0 V, V_{ds} = 400 V, R_G = 0 Ω.

The total losses were calculated, using the method of loss estimation described in [22] and the curves obtained by simulation, and are shown in Table 2 for the rectifier and in Table 3 for the inverter. Since the SiC Schottky diode has negligible reverse recovery, its switching losses were considered zero.

Table 2. Losses calculated for the rectifier operating at 102 kHz switching frequency.

	Per Diode STPSC40065C			**Per MOSFET SCT3030AL**			**Total Losses**
Load	P_{cond}	P_{sw}	P_{diode}	P_{cond}	P_{sw}	P_{MOSFET}	$P_{losses-ret}$
25%	2.10 W	0	2.10 W	0.36 W	3.70 W	4.06 W	36.96 W
50%	4.70 W	0	4.70 W	1.40 W	7.10 W	8.50 W	79.20 W
75%	7.70 W	0	7.70 W	3.40 W	11.30 W	14.70 W	134.40 W
100%	11.50 W	0	11.50 W	5.70 W	16.60 W	22.30 W	202.80 W

Table 3. Losses calculated for the inverter operating at 101.34 kHz switching frequency.

	Per MOSFET SCT3030AL			**Total Losses**
Load	P_{cond}	P_{sw}	P_{MOSFET}	$P_{losses-inv}$
25%	0.83 W	9.2 W	10.03 W	60.2 W
50%	3.09 W	16.91 W	20 W	120 W
75%	6.7 W	26.4 W	33.1 W	198.6 W
100%	12.55 W	37.55 W	50.1 W	300.6 W

From the estimation of losses it is possible to size the heatsink for cooling the converter. Two identical heatsinks have been chosen for use, one for the rectifier switches and one for cooling the inverter switches, the part number is P 16 from Semikron with standard length of 100 mm.

The thermal resistance (R_{th_s-a}) of this heatsink, when subjected to an air flow of 6 m/s in its fins, is 0.175 °C/W. A Sil-Pad 2000 thermal interface was used whose thermal resistance (R_{th_c-s}) is 0.23 °C/W. As the junction-case (R_{th_j-c}) thermal resistance of the diode and the MOSFET are respectively 0.6 °C/W and 0.44 °C/W, the temperatures at the junctions of the transistors can be calculated through the thermal models of the Figures 4 and 5.

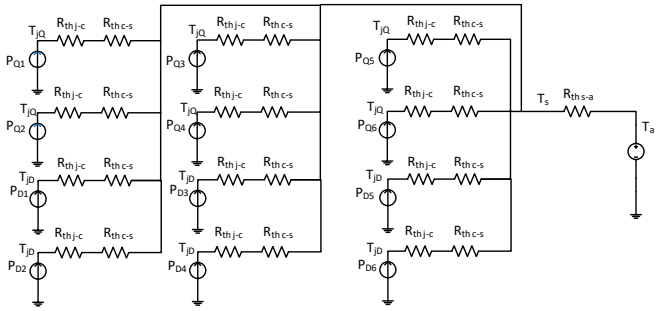

Figure 4. Equivalent thermal model for dissipation of the heat generated by the rectifier switches.

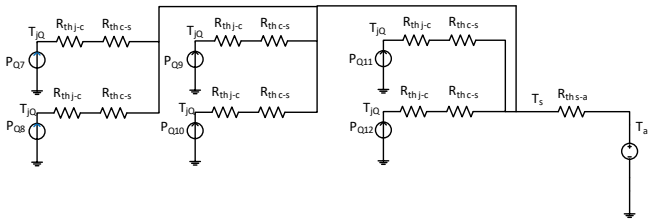

Figure 5. Equivalent thermal model for dissipation of the heat generated by the inverter switches.

The temperatures were calculated and are shown in Table 4, it was considered an ambient temperature of 40 °C. As can be seen, the none of the junction temperatures of the semiconductor devices exceeded the maximum operating limit of 175 °C. Thus, the thermal design developed is considered adequate.

Table 4. Temperatures calculated using the thermal models from the Figures 4 and 5.

	Rectifier			
	T_a	T_{jQ}	T_{jD}	T_s
Temperature	40 °C	90.4 °C	85.0 °C	75.5 °C
	Inverter			
	T_a	T_{jQ}	T_{jD}	T_s
Temperature	40 °C	126.2 °C	NA	104.1 °C

3.2. Inductor Design

The input and output inductors are responsible for filtering the harmonic components at the switching frequency. The inductor design involves calculating the inductance required to obtain a particular ripple, choice of magnetic core material, and winding design.

The required inductance value can be calculated by the following generic equation [23]:

$$L = \frac{1}{n} \times \frac{V_{dc}}{\Delta I_{max} \times f_{sw}} \quad (1)$$

where n is a variable that depends on the number of levels, for 2-level converters $n = 4$ and for 3-level converters $n = 8$. Thus, it is possible to calculate the value for input and output inductances. Firstly for the rectifier:

$$L_{ret} = \frac{1}{8} \times \frac{400}{32\sqrt{2} \times 0.3 \times 102,000} = 36\,\mu\text{H} \tag{2}$$

Then, a similar calculation is made for the inverter:

$$L_{inv} = \frac{1}{4} \times \frac{400}{26.24\sqrt{2} \times 0.4 \times 101,340} = 66\,\mu\text{H} \tag{3}$$

It was decided to use relatively high ripple values to reduce the inductance required and improve system dynamics.

For the choice of magnetic material, only alloy powder cores were considered because they are often more suitable for operation at high currents and mid switching frequency range. It was decided to fix the core size and choose the material based on its losses and its cost. Table 5 shows the main characteristics of the evaluated cores.

Table 5. Characteristics of the magnetic cores considered.

Material	High Flux	XFlux	MPP	Kool Mμ
Composition	FeNi	FeSi	FeNiMo	FeSiAl
Part Number	C058090A2	0078090A7	C055090A2	0077090A7
μ_r	60	60	60	60
A_L (nH/Turn)	86 ± 8%	86 ± 8%	86 ± 8%	86 ± 8%
B_{sat} (T)	1.5	1.6	0.8	1.0
T_{max} (°C)	200	200	200	200
OD (mm)	47.63	47.63	47.63	47.63
ID (mm)	27.88	27.88	27.88	27.88
HT (mm)	16.2	16.2	16.2	16.2
l_e (mm)	116	116	116	116
A_e (mm^2)	134	134	134	134
A_W (mm^2)	610	610	610	610
V_e (cm^3)	15.6	15.6	15.6	15.6
MTL (mm)	66.4	66.4	66.4	66.4
k_c (mW/cm^3)	0.055	0.034	0.155	0.026
α	1.32	1.332	1.12	1.29
β	2.22	1.825	2.05	2.01
Cost (USD)	6.60	2.21	32.42	5.19

Core losses can be calculated using the formula proposed by Steinmetz, which is an empirical expression that is adjusted to the loss data by choosing 3 coefficients supplied by the manufacturers or obtained from curves that can also be supplied by the manufacturers. The equation can be written as:

$$P_{core} = k_c f^{\alpha} \hat{B}^{\beta} V_e, \tag{4}$$

where k_c, α, and β are the Steinmetz coefficients which depend on the characteristics of the material, f is the operating frequency, $\hat{B}$ is the peak value of the flux density, and V_e is the volume of the magnetic core.

However, this empirical equation is obtained from the application of sinusoidal flux densities. The flux density imposed on magnetic materials of static converters usually has non-sinusoidal waveforms. For this reason, many researchers have proposed improvements to the Steinmetz equation to take into account the application of non-sinusoidal waveforms. Some of these proposals are Modified Steinmetz Equation-MSE [24], Generalized Steinmetz Equation-GSE [25], improved Generalized Steinmetz Equation-iGSE [26], and improved-improved Generalized Steinmetz Equation-i^{2}GSE [27].

Some papers have presented accurate results when iGSE or i^{2}GSE are used to estimate core losses, with errors between the experimental and theoretical results lower than 10% [26–29]. The difference

between iGSE and i^{2}GSE is the fact that i^{2}GSE includes the relaxation effects due to DC levels of the flux density. However, the flux-density waveforms of the converters in this work do not show DC levels, so the use of iGSE is sufficient for calculating core losses. The formula for using the iGSE method is given below:

$$P_{core} = \frac{V_e}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{5}$$

with k_i being determined by:

$$k_i = \frac{k_c}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^{\alpha} 2^{\beta-\alpha} d\theta}, \tag{6}$$

Although the iGSE has been demonstrated to be accurate, the computational routine proposed by its authors has two drawbacks: the first is the computational complexity of the algorithm that must scan the flux density data vector to perform a loops separation, the second is the generation of the flux density data vector which, if done by simulation, can spend considerable time.

For this reason, a method to accelerate the process of using iGSE has been proposed in [30]. The method consists of the deduction of the closed-form solution of the excitation waveform. In this way, it is possible to perform the iGSE calculations only with the converter input data (RMS voltage, RMS current, switching frequency, magnetic core data), i.e., without the need for simulation or complex algorithms, making it ideal for use in design optimization softwares for inductors. The authors in [30] made the deductions in the case of a single-phase Bridgeless PFC converter, and can also be applied to 3-level Vienna rectifiers. An extension was made to cover a 2-level inverter and was used in this work to calculate core losses.

Then, the losses were calculated for the four cores evaluated as a function of the number of turns for $18 \leq N \leq 36$. Figure 6 shows the results of calculating the core losses. First, it can be seen that the core with the highest losses is the XFlux, so it is discarded from selection. Then, the higher the number of turns the lower the difference between the losses of the High Flux core and the high-cost MPP core. Moreover, MPP and Kool Mμ cores have the disadvantage of low saturation flux density, Figure 6 shows that, even with few turns, these cores saturate due to the high current of the inverter. Therefore, the core High Flux will be chosen for the rectifier and inverter inductors.

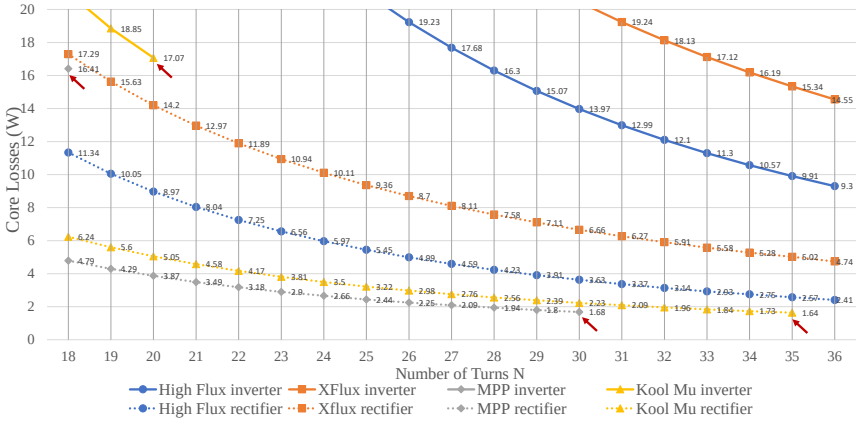

Figure 6. Core losses comparison of the inductors of the rectifier and inverter for four materials as a function of number of turns. The arrows indicate an occurrence of core saturation.

The number of turns used in the rectifier and inverter inductors will be 26 and 33, respectively. With this amount of turns it is possible to achieve the required inductance. To compose the windings, 38 AWG25 gauge copper wires will be used in parallel. Considering that the copper resistivity at 100 °C is 2.19×10^{-8} [31], the dc winding resistance will be 6.1 mΩ and 7.8 mΩ for the rectifier and inverter inductors, respectively. The estimated copper losses and core losses are shown in Table 6,

only the fundamental component was considered to calculate copper losses, core losses were considered constant and independent of the load.

Table 6. Losses calculated for inductors.

	Per Rectifier's Inductor		Per Inverter's Inductor		Total
Load	P_{core}	P_{copper}	P_{core}	P_{copper}	$P_{inductors}$
25%	4.99 W	0.29 W	11.3 W	0.33 W	50.7 W
50%	4.99 W	1.16 W	11.3 W	1.33 W	56.3 W
75%	4.99 W	2.62 W	11.3 W	3.00 W	65.7 W
100%	4.99 W	4.66 W	11.3 W	5.34 W	78.9 W

3.3. Capacitor Sizing

The sizing of the DC link capacitor takes into account the ripple criteria. For the DC link capacitor, the worst case occurs when the inverter feeds an unbalanced load, the higher the unbalance the greater the ripple. Thus, it is possible to calculate the needed capacitance when the neutral current and the ripple are given [4]:

$$C_{dc} = \frac{V_{a-peak} \cdot I_{n-peak}}{4\pi \cdot f_g \cdot V_{dc} \cdot \Delta V_c} = \frac{127\sqrt{2} \times 78.75}{4\pi \times 60 \times 400 \times 20} = 2344\ \mu\text{F} \quad (7)$$

where V_{a-peak} is the output voltage peak value and I_{n-peak} is the neutral current peak value.

It was decided to use 4 electrolytic capacitors of 560 µF/400 V, manufactured by EPCOS part number B43644B9567M000, in parallel, totaling a capacitance of 2240 µF for each C_{dc} group.

Then, the output LC filter capacitor will be sized based on the attenuation criteria, this filter is required to attenuate harmonic components close to the switching frequency. It is a second order and has attenuation of 40 dB per decade from the cutoff frequency, so the cutoff frequency, fc, will be defined as less than one-tenth of the switching frequency, which will guarantee a 100-fold attenuation in the amplitude of the harmonics. Therefore, the capacitor value can be determined by:

$$C_{out} = \frac{1}{(2\pi f_c)^2 L_{inv}} = \frac{1}{(2\pi \frac{f_{sw}}{12})^2 L_{inv}} = \frac{1}{(2\pi 8.44e3)^2 66e-6} = 5.38\ \mu\text{F} \quad (8)$$

Thus, it was decided to use three capacitors of 2.2 µF/400 V in parallel, totaling a capacitance of 6.6 µF, the capacitors are manufactured by Panasonic part number ECQ-E4225KF.

The input LCL filter is formed by the grid inductance (L_g), rectifier inductance (L_{ret}) and input capacitance (C_{in}). Several researchers have published works where the central subject is the design and modeling of LCL filters using different methodologies and criteria [32–35]. However, the grid inductance changes depending on the electrical network, the equipment is expected to operate in facilities where the grid inductance varies from 64.19 µH to 1.28 mH, which allows a short circuit power from 10 to 200 times the power of the equipment. As the rectifier inductance and the grid inductance were already defined, it remains only to size the input capacitor.

One of the criteria defined in [32] recommends to allocate the resonance frequency between ten times the grid frequency (600 Hz) and half the switching frequency (51 kHz). The resonant frequency of an LCL filter can be calculated by the equation:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_{ret}}{L_g L_{ret} C_{in}}} \quad (9)$$

By rearranging the terms of the Equation (9) and allocating the resonance frequency at 15 kHz, it is possible to obtain a range of values for the capacitor.

$$C_{in} = \frac{L_g + L_{ret}}{(2\pi)^2 f_{res}^2 L_g L_{ret}} \Rightarrow 4.21\ \mu F \leq C_{in} \leq 5.8\ \mu F \quad (10)$$

In this way, it was decided to use two 2.2 µF/400 V capacitors in parallel, totalizing a capacitance of 4.4 µF, the capacitors are manufactured by Panasonic part number ECQ-E4225KF.

4. Converter Control

This section addresses the subject of converter control. Although the control strategy is not the main focus of this paper, a closed loop control system is needed for proper converter operation. The goals of the control are:

- Power factor correction;
- Keep the input current and output voltage at low THD (<15%);
- Regulate output voltage;
- Rejection of load disturbances;
- Synchronize input and output voltages;
- Regulate DC link voltage at 400 V.

The control strategy was implemented with the micro-controller TMS320F28379D which has two processing cores, one core was used to control the rectifier and the second was used to control the inverter.

Figure 7 shows the rectifier's control system. The first three loops, more internal, control the currents in the inductors of each phase, the control action is composed by the response of a proportional controller (P) together with the feed-forward of the input voltage. The outermost and slower loop is responsible for maintaining constant voltage on the DC link, the use of a proportional-integral compensator (PI) is sufficient to guarantee zero error in a steady state, the output of this loop multiplied by three-phase sine-wave voltages generates the reference for the internal current loops. The PLL (Phase Locked Loop) is used to generate these three-phase voltages, this decouples the reference of possible distortions present in the input voltages, improving the quality of the synthesized current [36].

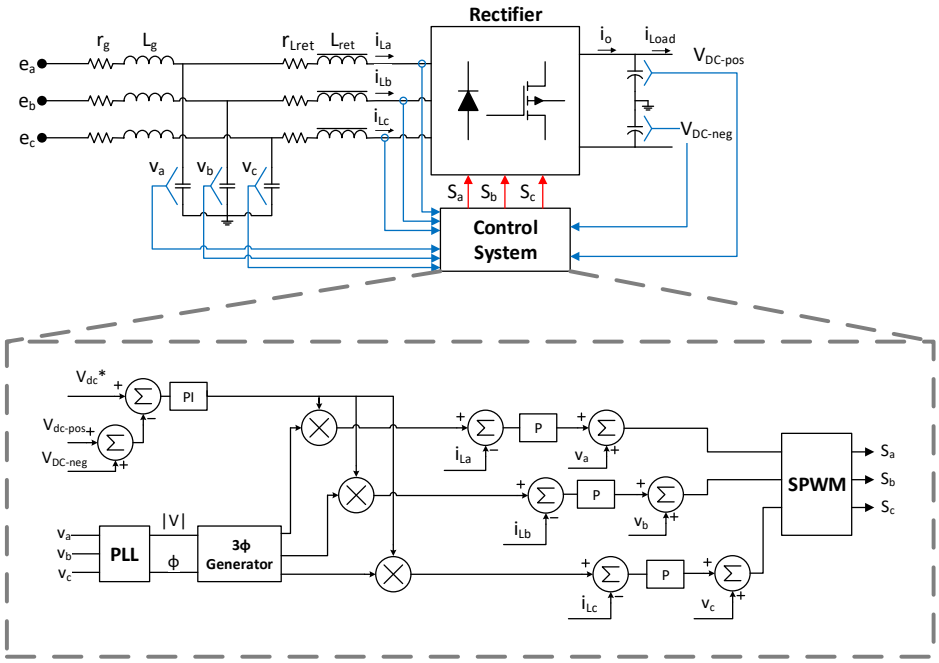

Figure 7. Control strategy applied for the rectifier.

Figure 8 shows the inverter's control system. It is composed by three voltage loops, one for each phase, the control action is composed by the response of a proportional-integral controller (PI) together with the feed-forward of the reference voltage. The PLL is used to generate reference voltages that are synchronized with the input voltages.

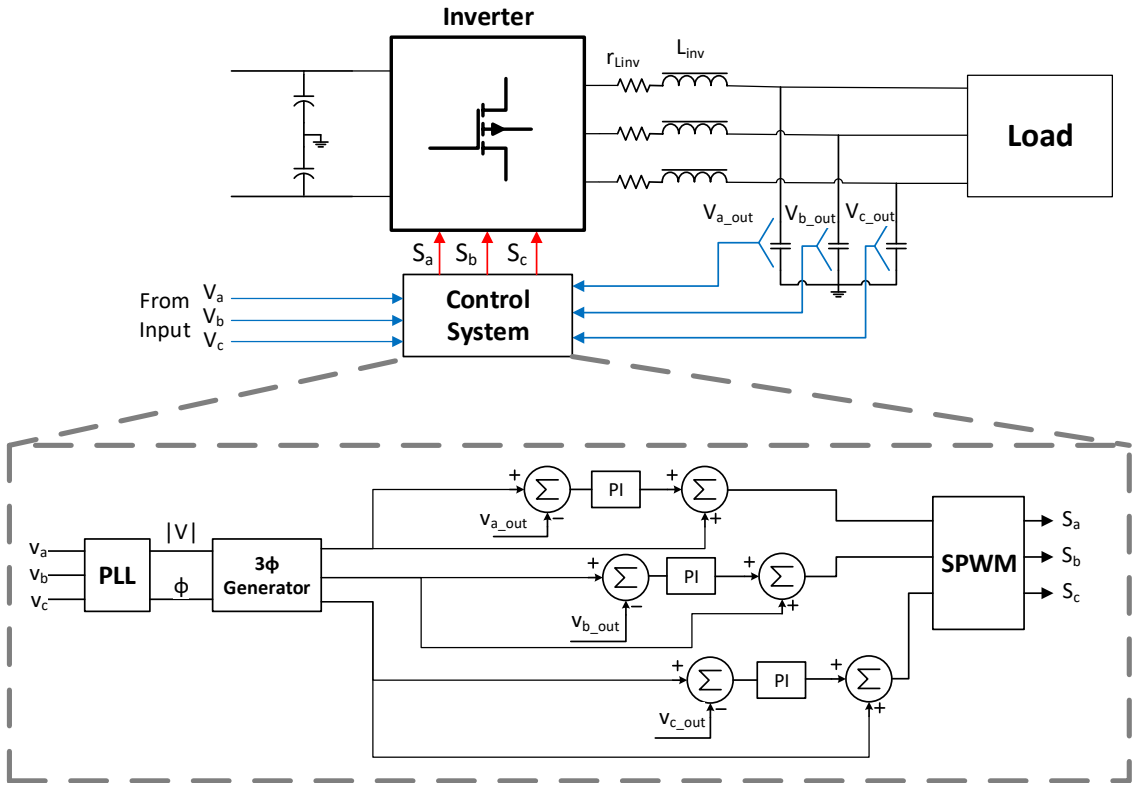

Figure 8. Control strategy applied for the inverter.

5. Prototype Analysis and Experimental Results

In this section, the developed AC-DC-AC converter will be analyzed in terms of power density and the experimental results will be presented. The efficiency and compliance with norms in terms of power factor and THD will be validated.

5.1. Prototype

Figure 9 shows a photo of the designed prototype, it employs a Vienna Rectifier at the input and a 2-level inverter at the output and uses Silicon Carbide devices operating with switching frequencies up to 102 kHz. This converter is intended for use in highly efficient three-phase double conversion UPS applications and is rated at 10 kW.

The currents of the inductors, the input voltages, the output voltages, and the DC link voltages were measured and fed into a LaunchPad Development Kit TMS320F28379D to implement the closed loop PWM control.

To highlight the benefits of using Silicon Carbide devices, the developed SiC-based prototype was compared to a commercial Silicon IGBT-based UPS with the same specifications. Figure 10 shows a size comparison between the two pieces of equipment, it is possible to observe that the SiC-based prototype is much smaller than the IGBT-based UPS. However, the prototype is not a complete product and does not have batteries, protections, nor enclosure, hence one can say that the comparison is not equitable. To establish a fair comparison, this work will focus on the hardware components designed and performance.

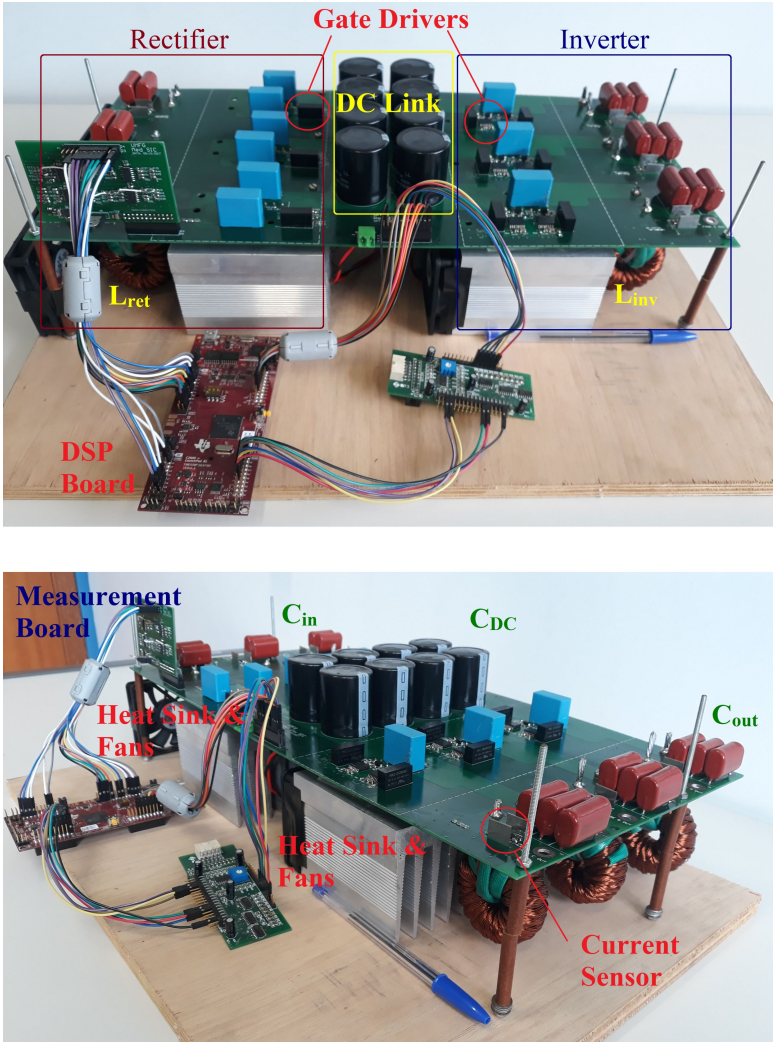

Figure 9. Designed prototype.

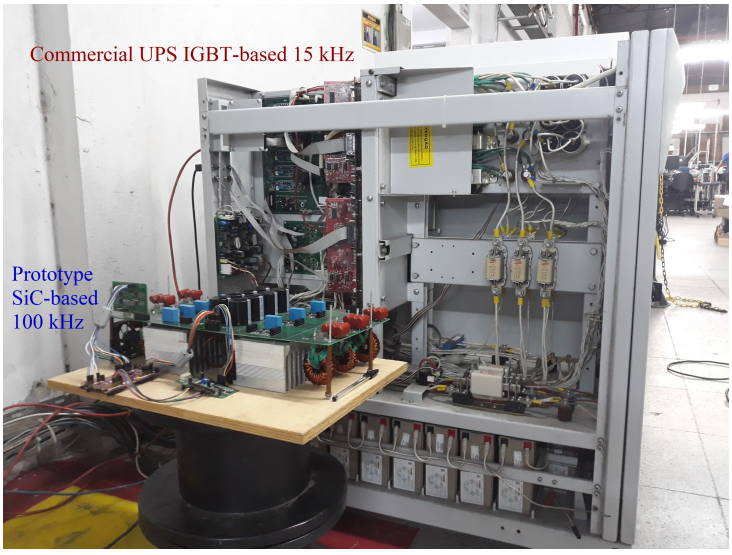

Figure 10. Size comparison between the developed SiC-based prototype and a commercial IGBT-based Uninterruptible Power Supply (UPS) with the same specifications.

Table 7 shows a performance and power density comparison with regard to the converter as a whole and to individual components.

Table 7. Performance and power density comparison between the developed SiC-based prototype and a commercial IGBT-based Uninterruptible Power Supply (UPS) with the same specifications.

Parameter	Commercial UPS IGBT-Based 15 kHz	Prototype SiC-Based 100 kHz	Difference
Nominal point losses	950 W	500 W	−47.3%
Hardware * mass	21.36 kg	6.88 kg	−67.8%
Hardware * volume	11.9 L	4.38 L	−63.2%
Filter capacitance (C_{out})	90 µF	6.6 µF	−92.7%
Filter capacitor mass (C_{out})	226 g	23 g	−89.8%
Filter capacitor volume (C_{out})	200 cm³	22 cm³	−89%
Filter inductance (L_{inv})	290 µH	66 µH	−77.2%
Filter inductor mass (L_{inv})	1588 g	255 g	−83.9%
Filter inductor volume (L_{inv})	464.8 cm³	35.3 cm³	−92.4%
Heat sink mass	9400 g	4700 g	−50%
Fan mass	1090 g	300 g	−72.5%

* Hardware considers the sum of all components sized in the paper, that is, all capacitors, all inductors, fans and heat sinks. It does not account for batteries, protections, auxiliary circuits, PCB nor steel case.

Silicon Carbide switches enabled the construction of an highly efficient prototype, the 450 W reduction on losses allows a saving of about 1380 USD, considering that the prototype would operate continuously during one year in Germany. Less losses also means lighter cooling systems, the mass of heat sink and fans were reduced by 50% and 72.5%, respectively.

Additionally, the high switching frequency operation capability of SiC devices allows the size reduction of passive components such as inductors and capacitors, Figures 11 and 12, these components had a reduction of about 90% in mass and volume. The prototype measures 17 L and 7.13 kg, which means a power density of 0.588 kW/L and a power-to-mass ratio of 1.4 kW/kg.

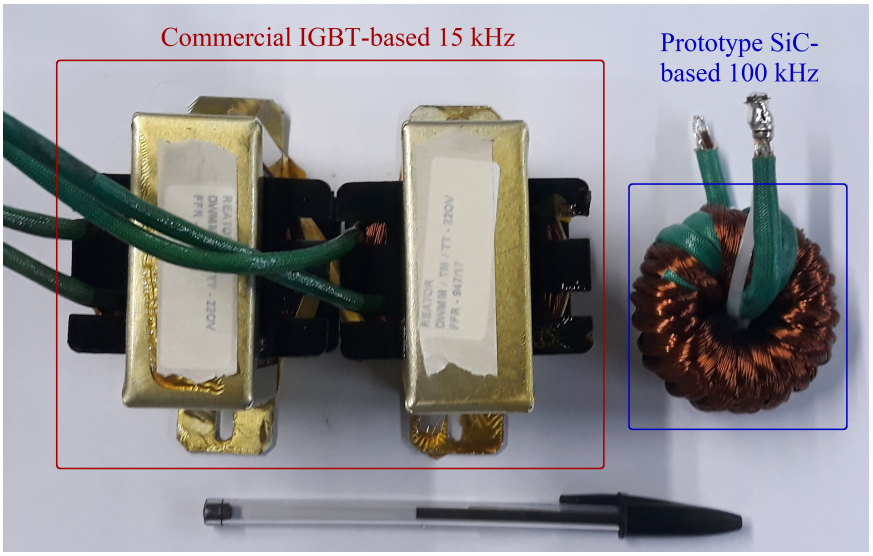

Figure 11. Size comparison between filter inductors for the developed SiC-based prototype and for a commercial IGBT-based UPS with the same specifications.

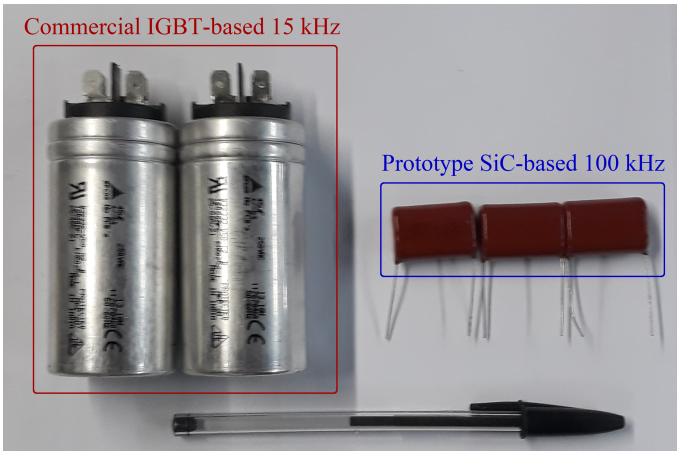

Figure 12. Size comparison between filter capacitors for the developed SiC-based prototype and for a commercial IGBT-based UPS with the same specifications.

5.2. Experimental Results

The first result is the steady state behavior of the converter. Figure 13 shows the main input and output electrical variables at nominal load measured with the power analyzer YOKOGAWA WT1800. It is possible to note that these waveforms respect a sinusoidal shape that will lead to high power quality, that affirmation is confirmed by measuring the THD of the input current and the output voltage whose values are 3.8% and 3.2%, respectively. The measured rectifier power factor was 0.997 at rated load. The input current THD is kept low, even for cases of light load, as shown in Figure 14 and Table 8. The steady state performance under nonlinear was also evaluated, a nonlinear load rated at 3.3 kVA, Power factor 0.62, and Crest factor 3.4 was connected on phase A, Figure 15 demonstrates the obtained result, the output voltage was kept at low distortion yielding a THD of 5.3%. The obtained results validate the steady state operation and complies with the IEC-62040-3 and the IEC-61000-3-12.

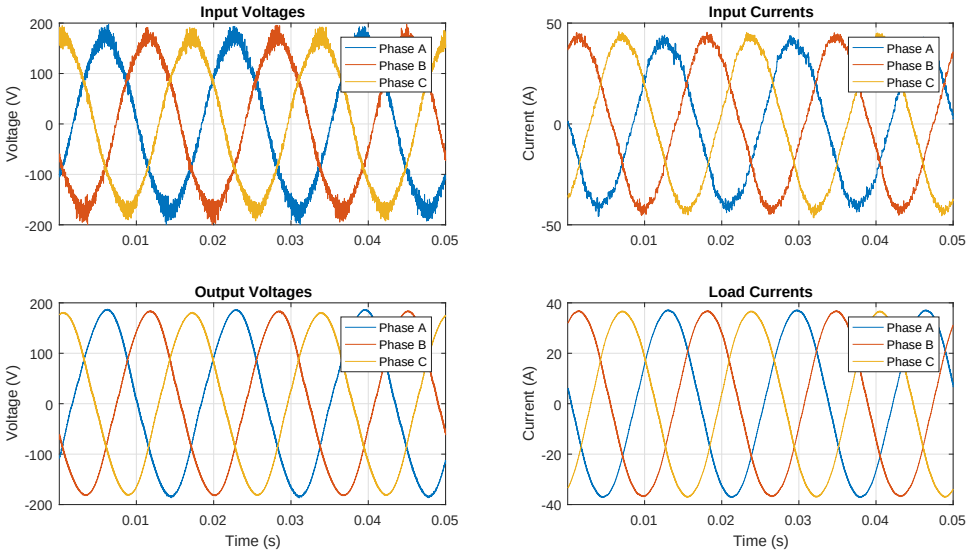

Figure 13. Measured input and output waveforms in steady state at nominal power, the input voltage is 120 V (phase-neutral).

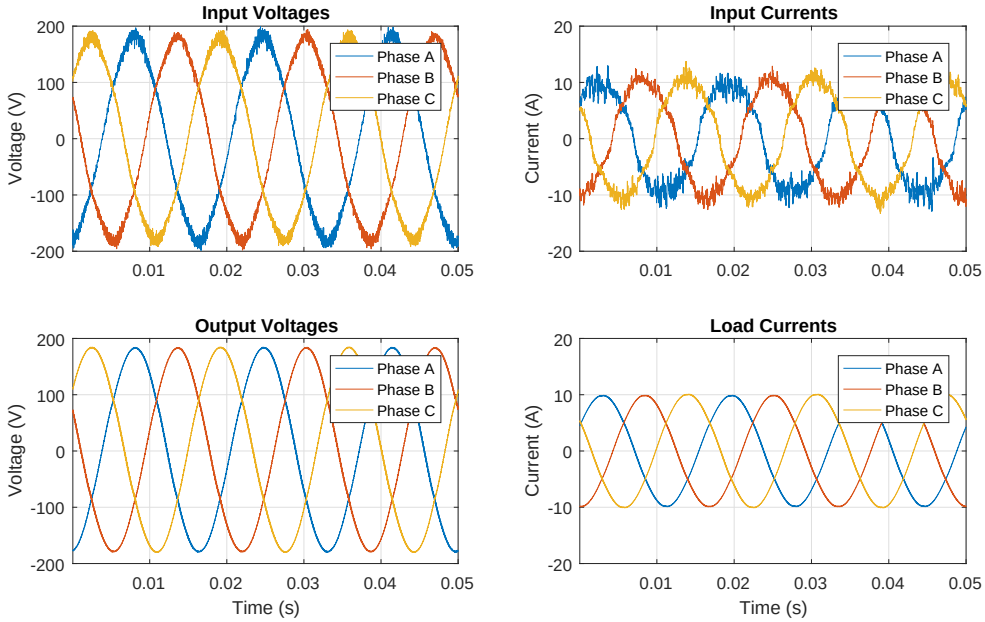

Figure 14. Measured input and output waveforms in steady state at 25% load, the input voltage is 127 V (phase-neutral).

Table 8. Input and output power quality measurements under linear load condition.

Load	Rectifier Power Factor	Input Current THD (%)	Output Voltage THD (%)
25%	0.98	11.2	1.4
50%	0.994	5.7	1.8
75%	0.996	4.5	2.7
100%	0.997	3.8	3.2

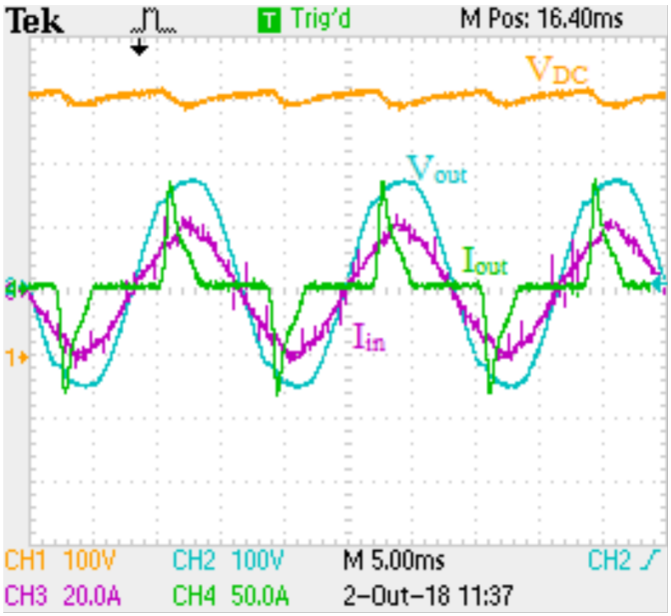

Figure 15. Experimental results supplying a nonlinear load. CH1: DC Link voltage, CH2: Output voltage, CH3: Input current, CH4: Output current.

Next, the converter dynamic behavior under load changes was evaluated. Figure 16 shows the DC link voltage, output voltage, input current and output current under two load variations, one negative

25% load step, and a positive 25% load step. For both cases, the control loop responds rapidly and the overvoltage/voltage dip has an absolute value lower than 20 V.

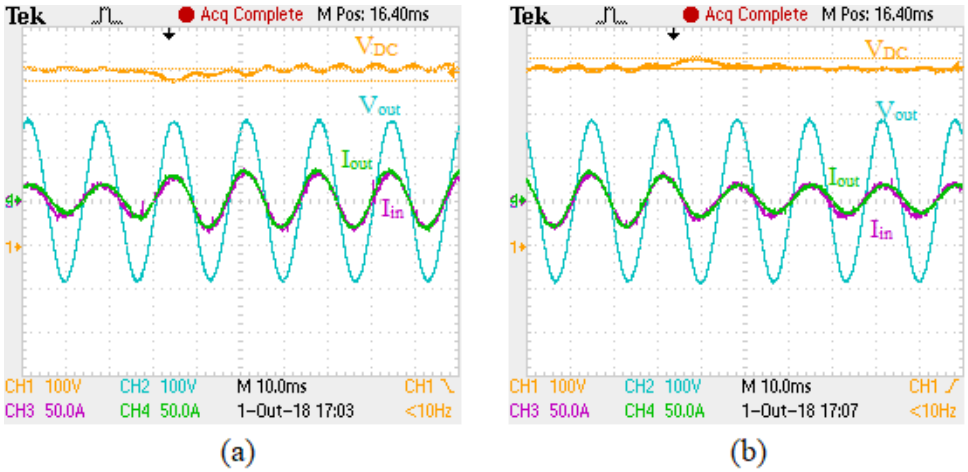

Figure 16. Dynamic behavior of the converter under load changes (**a**) −25% load step (**b**) 25% load step. CH1: DC Link voltage, CH2: Output voltage, CH3: Input current, CH4: Output current.

Then, Figure 17 shows an efficiency evaluation as a function of the output power and the input voltage. The experimental efficiency is over 95% for most operating points, meeting the design requirements, and reach a peak of 95.6% when the input voltage is 140 V (phase-neutral) and the load is 75% of the nominal power. The difference between experimental and theoretical efficiency is lower than 1% when the input voltage is 120 V. Although the converter is rated at 10 kW, it was experimentally verified that it can operate continuously with 10% overload.

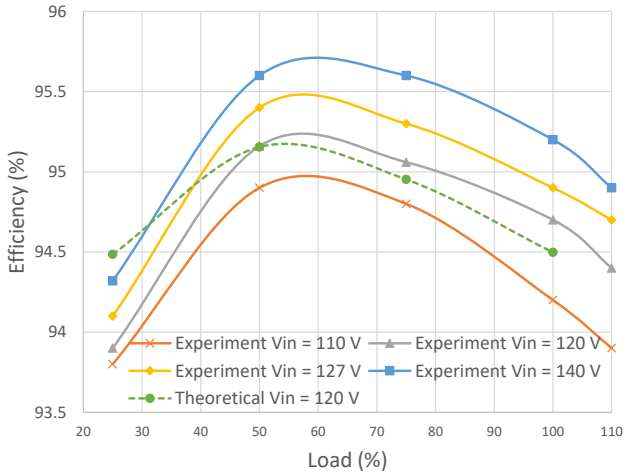

Figure 17. Efficiency measured with the power analyzer YOKOGAWA WT1800 for different input voltages and load conditions.

Figure 18 shows the temperature distribution for both inverter and rectifier inductors operating at rated load. The temperature of the rectifier inductors is lower for two reasons: The rectifier 3-level configuration that lowers the excursion of magnetic flux density and consequently reduces core losses, the second reason is the positioning of the fans, which generates an air flow that passes first through the rectifier and exits at the inverter. The observed maximum temperatures are 54.8 °C and 85.8 °C for the rectifier and inverter inductors, respectively. In this way, the inductors operate with a good safety margin, since the maximum operating temperature of the material High Flux is 200 °C.

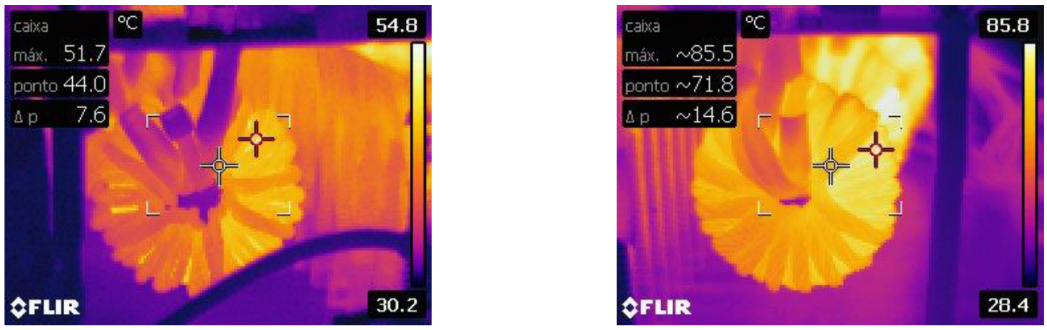

Figure 18. Thermal images for inductors operating at nominal power (**a**) Rectifier (**b**) Inverter.

Due to the positioning of the electronic switches under the PCB, it is difficult to capture a thermal image that clearly shows the temperature distribution over all components. Since the inverter has less components, a lateral view was captured and is shown in Figure 19. It is possible to see that the maximum temperature is about 126 °C , which validates the thermal model and the loss model for the inverter.

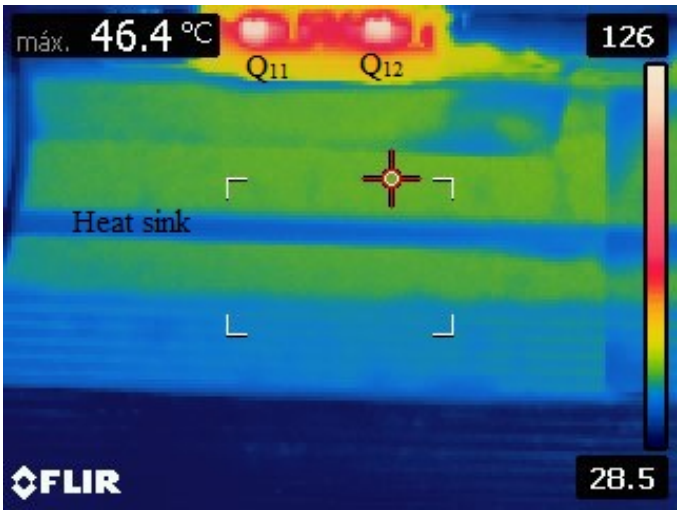

Figure 19. Thermal image for the inverter operating at nominal power, this lateral view shows only Q_{11} and Q_{12} on phase C.

6. Conclusions

This work has made an extensive coverage on the design of a three phase AC-DC-AC converter for UPS applications using Silicon Carbide. The focus was the hardware design which includes thermal design, inductor design, and filter capacitors sizing.

Since the manufacturer's datasheet does not completely characterize the SiC MOSFET for real operating conditions, a simulation method to estimate switching energy curves was proposed to incorporate parasitic inductance into switching behavior, allowing for more accurate losses prediction. An accurate losses prediction avoids oversizing or undersizing of the heatsink.

Also, it was shown that the inductors have a great impact on the UPS efficiency and cost. The inductor design method achieved inductors with a moderate compromise between losses, cost, and size.

The design procedure described in this work has achieved an highly efficient electronic converter for double conversion UPS that complies with the IEC-62040-3. If higher efficiency is required, the designer can reduce the switching frequency and/or improve the inductor by changing its core material, although this can increase cost.

Experimental results and comparisons have shown that Silicon Carbide devices can offer the possibility of higher frequency operation while enhances the system efficiency, thus, the obtained converters have smaller passive components and smaller heatsinks. UPS that employs these wide

bandgap devices will offer energy savings and reduce costs with cooling systems and equipment accommodation.

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Abbreviations

The following abbreviations are used in this manuscript:

UPS	Uninterruptible Power Supplies
SiC	Silicon Carbide
GaN	Gallium Nitride
WBG	Wide Bandgap
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
THD	Total Harmonic Distortion
PLL	Phase Locked Loop

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