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# Optimized Digital Controllers for Switching-Mode DC-DC Step-Down Converter

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**Abstract:** In this paper, a nonlinear least squares optimization method is employed to optimize the performance of pole-zero-cancellation (PZC)-based digital controllers applied to a switching converter. An extensively used step-down converter operating at 1000 kHz is considered as a plant. In the PZC technique, the adverse effect of the (unwanted) poles of the buck converter power stage is diminished by the complex or real zeros of the compensator. Various combinations of the placement of the compensator zeros and poles can be considered. The compensator zeros and poles are nominally/roughly placed while attempting to cancel the converter poles. Although PZC techniques exhibit satisfactory performance to some extent, there is still room for improvement of the controller performance by readjusting its poles and zeros. The (nominal) digital controller coefficients thus obtained through PZC techniques are retuned intelligently through a nonlinear least squares (NLS) method using the Levenberg-Marquardt (LM) algorithm to ameliorate the static and dynamic performance while minimizing the sum of squares of the error in a quicker way. Effects of nonlinear components such as delay, ADC/DAC quantization error, and so forth contained in the digital control loop on performance and loop stability are also investigated. In order to validate the effectiveness of the optimized PZC techniques and show their supremacy over the traditional PZC techniques and the ones optimized by genetic algorithms (GAs), simulation results based on a MATLAB/Simulink environment are provided. For experimental validation, rapid hardware-in-the-loop (HiL) implementation of the compensated buck converter system is also performed.

**Keywords:** Levenberg-Marquardt (LM) algorithm; nonlinear least squares (NLS) method; optimized digital controllers; pole-zero-cancellation technique; switching converter

## 1. Introduction

Modern-day digital devices such as cellular phones, camcorders, calculators, digital cameras, portable electronic devices, microprocessors, DSP core, handheld computers and PDAs, MP3 personal players, and so on utilize switch-mode power supplies (SMPSSs). The devices need to have regulated output voltages irrespective of the perturbation in the input voltage or load current. For this purpose, traditionally, analog controllers have been applied to SMPSSs to ensure regulated voltages for the digital devices. Analog controllers, however, show limitations in the form of poor design portability, large

size, low reliability, and low flexibility. Digital controllers, on the other hand, offer advantages in the form of high flexibility and programmability, competency to implement complex control strategies, no need to alter hardware upon changing algorithms, high performance/cost ratio, and excellent dynamic performance, among others [1]. Consequently, SMPS designers are more interested in developing efficient and optimized digital controllers as compared to the predominately used analog controllers. In this paper, well-recognized PZC techniques-based optimized digital controllers are designed for buck converters to display much-improved performance. One of the optimization techniques, named the nonlinear least squares technique, is employed to optimize the performance of PZC-based digital controllers.

As far as the literature review is concerned, in [2], a pole-zero-cancellation technique-based digital controller for a buck converter was suggested by Abe et al. to improve the performance characteristics. The effect of the resonance peak and ESR-zero is nullified by completely cancelling the poles and the zero of the buck converter with the help of the complex zeros and the pole of the compensator, respectively. An additional pole representing a simple low-pass filter is introduced to gain control of the characteristics of the composite buck converter system. A two-pole two-zero analog controller is mapped into the digital controller using bilinear transformation. In [3], the same authors (Abe et al.) applied successfully the two-pole two-zero analog compensator to the buck and boost converters to ensure superior performance, yet without cancelling the RHP-zero in the case of the boost converter. The effect of change in the capacitance of the output capacitor in a PZC-based digitally controlled buck converter on the stability margin, and thus the performance, was investigated in [4]. Reference [5] also suggested the application of a three-pole two-zero (analog) compensator with complex as well as real zeros to a switching converter exhibiting nonminimum phase characteristics. Such a converter possesses RHP-zero in its transfer function, which limits the bandwidth, thus causing the response to be slow and sluggish. Reference [6] suggested a slightly different approach for designing a PZC-based digital controller for the step-down converter. Rather than using the real or complex zeros by the compensator close to the resonant frequency of the converter's power stage, the compensator zeros are selected on the basis of the quality factor and output impedance of the plant. The effect of the quality factor on compensator design is also investigated efficiently. In [7], the task of providing feedback compensation to the relatively complicated switching converters (as they involve RHP-zero), namely boost and flyback working in continuous conduction mode, was efficiently performed through various combinations of PZC-based controllers. The PZC-based digital controllers mentioned in the aforementioned references show somewhat satisfactory performance. Their performance may even be improved by retuning their coefficients through some optimization techniques.

Many researchers successfully applied advanced numerically based or metaheuristic optimization techniques to tune the compensator parameters to ameliorate performance. Reference [8] suggested the tuning of the parameters of the digital controller designed on the basis of a Chebyshev polynomial approach for the fifth-order boost converter through a genetic algorithm (GA). The problem with the GA is that it has to employ its three operators, namely selection, crossover, and mutation, at each iteration, thus resulting in slower responses. In addition, it shows enhanced sensitivity to the initial population and does not use gradients. In [9], although metaheuristic techniques such as particle swarm optimization (PSO) and the gravitational search algorithm (GSA) were successfully employed for the fine-tuning of parameters of Type II and Type III compensators applied to a step-up converter, but they may converge prematurely. Mercader et al. in [10] tried to overcome the problem of convergence to the local minimum of convex optimization and proposed a convex-concave procedure (CCP) for the fine-tuning of PID controller coefficients that controlled the loop shape efficiently to ensure better dynamic performance. On the other hand, the NLS method capitalizes on the structure of the Hessian, which can be attained through the computation of Jacobian (first-order derivatives only) and minimizes the errors (residuals) quickly, and thus ensures better set-point tracking.

In addition, many instances in the literature have been reported where the nonlinear least squares (NLS) method has been successfully employed to optimize the performance of various types of

compensators used for various applications. In [11], optimization of the discrete root locus-based discrete-time controller applied to a buck converter was accomplished through the NLS method. In [12], tuning of the PID-based track-keeping controllers of a remotely controlled autonomous in-scale fast-ferry model was carried out through the NLS method and a genetic algorithm (GA), where the former showed superiority over the latter one while doing sea trials. Reference [13] suggested the use of the NLS method for the optimization of offline pulse patterns for arbitrary modulation indices and arbitrary numbers of modules per branch, while minimizing the harmonic content of the load current (specifically measured in the total demand distortion (TDD)), instead of using selective harmonic elimination, in the case of the indirect modular multilevel converter (MMC). In [14], a Levenberg-Marquardt (LM) and quasi-Newton (QN)-based NLS hybrid method was used efficiently to improve the performance of the designed linear-phase quadrature mirror filter (QFM) bank in the form of mean squares error in passband and stopband regions, as well as peak reconstruction error (PRE) and error in the transition band at quadrature frequency. This was accomplished by optimizing the quadratic measure of the ideal characteristics of the prototype filter and filter bank at quadrature frequency. In [15], a predictive current controller with an extended-state observer (ESO), suggested for the grid integration of wind energy systems, utilized the NLS method to minimize a cost function, defined as a sum of the squared values of d-axis and q-axis current errors, while computing the optimal converter switching time. In [16], calibration of the roadside camera employed in traffic surveillance systems was accomplished on the basis of the least squares optimization method, which involved camera-intrinsic parameters and rotation angles. In [17], for anticipating the epileptic seizure via EEG signals in epileptic individuals suffering from unexpected and momentary electrical deterioration in the brain, fitting of the EEG signals filtered through singular spectrum analysis into the exponential curve was carried out using the NLS method. Statistical examination of the features extracted from exponential curves assists in diagnosis. In [18], nonlinear rational systems were identified using an NLS-based, globally consistent two-step estimator. In [19], a high face recognition rate was achieved by performing NLS computations, while taking into account the ‘holistic’ and ‘detailed’ features of the face.

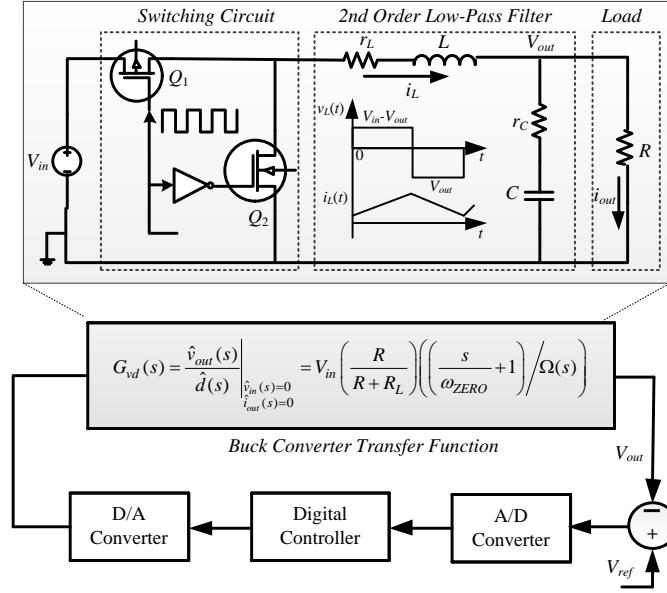
Although enormous numbers of examples of the application of the NLS method to control plants of various types are found in the literature, to the best knowledge of the authors, very limited instances are found in the literature where pole-zero-cancellation-based digital controllers have been optimized through the NLS method. In this paper, PZC-based optimized digital controllers are, thus, suggested for the buck converter to achieve much-improved performance.

The paper is formulated in the following way. Section 2 describes the dynamics of the buck converter, which is considered to be the plant in the paper. Three types of pole-zero-cancellation (with complex and real zeros)-based digital controllers are designed in Section 3. The digital controller design techniques are essentially of the types digital redesign or emulation. The NLS method involving the LM algorithm to optimize the digital controllers is detailed in Section 4. Nonlinearities involved in the digital control loop are modelled in Section 5. Section 6 involves the redesigning and reoptimizing of the digital controllers when the nonlinear effects in the digital control loop are considered. Section 7 is dedicated to additional simulation results. HiL implementation is described in Section 8. Concluding remarks are given in Section 9.

## 2. Buck Converter Modelling

For the sake of reducing higher unregulated DC input voltage,  $V_{in}$ , to lower regulated DC output voltage,  $V_{out}$ , a realistic buck converter circuit (see Figure 1) is used, as it takes into consideration the parasitic resistances, i.e., capacitor equivalent series resistance (ESR) and inductor direct current resistance (DCR), denoted explicitly by  $r_C$  and  $r_L$ , respectively. Owing to capacitor ESR, a zero is introduced into the buck converter transfer function [20]. The component values to be considered for the converter throughout the paper are the following:  $V_{in} = 3.6$  V,  $V_{out} = 2.0$  V,  $L = 4.7 \mu\text{H}$ ,  $C = 4.7 \mu\text{F}$ ,  $r_L = 505 \text{ m}\Omega$ ,  $r_C = 5 \text{ m}\Omega$ ,  $f_s = 1000 \text{ kHz}$ , and  $T_s = 1/f_s = 1 \mu\text{s}$ . The block diagram of the closed-loop

(digital) control system containing the buck converter power stage, ADC and DAC converters, and the digital controller is shown in Figure 1.



**Figure 1.** Closed-loop (digital) control system block diagram.

The buck converter's dynamics (transfer function) imperative for the controller design can be derived through its small-signal AC-equivalent circuit model (see Figure 2), where the nonlinear power switches  $Q_1$  and  $Q_2$  are replaced by their equivalent linear small-signal models [21]. By applying the averaging and linearization technique adopted in [22] to the small-signal model, the small-signal transfer functions, such as duty cycle-to-output voltage  $G_{vd}(s)$ , input voltage-to-output voltage  $G_{vg}(s)$ , and load current-to-output voltage (loaded power converter output impedance  $Z_o(s)$ ), can be computed and are described by Equations (1)–(3), respectively [22,23].

$$G_{vd}(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} \Big|_{\begin{array}{l} \hat{v}_{in}(s) = 0 \\ \hat{i}_{out}(s) = 0 \end{array}} = V_{in} \left( \frac{R}{R + r_L} \right) \left( \frac{\frac{s}{\omega_{ZERO}} + 1}{\Omega(s)} \right) \quad (1)$$

$$G_{vg}(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)} \Big|_{\begin{array}{l} \hat{d}(s) = 0 \\ \hat{i}_{out}(s) = 0 \end{array}} = D \left( \frac{R}{R + r_L} \right) \left( \frac{\frac{s}{\omega_{ZERO}} + 1}{\Omega(s)} \right) \quad (2)$$

$$Z_o(s) = - \frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)} \Big|_{\begin{array}{l} \hat{d}(s) = 0 \\ \hat{v}_{in}(s) = 0 \end{array}} = r_L \left( \frac{R}{R + r_L} \right) \left( \frac{\left( \frac{s}{\omega_L} + 1 \right) \left( \frac{s}{\omega_{ZERO}} + 1 \right)}{\Omega(s)} \right) \quad (3)$$

where

$$\Omega(s) = \left( \frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1 \right)$$

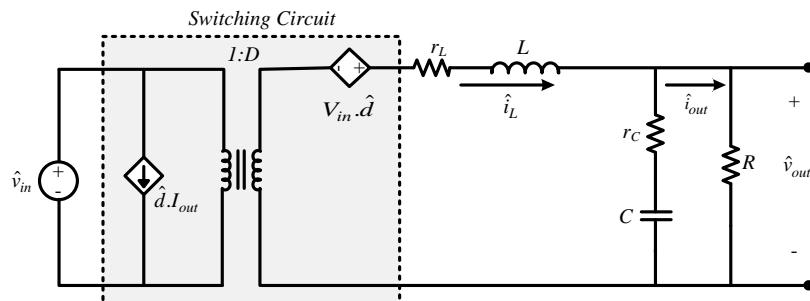
$$\omega_0 = \frac{1}{\sqrt{LC \frac{R+r_C}{R+r_L}}} \approx \frac{1}{\sqrt{LC}}, \quad \text{if } \begin{cases} r_C \ll R \\ r_L \ll R \end{cases} \quad (4)$$

$$Q = Q_{LOSS} \parallel Q_{LOAD} = \frac{1}{2\xi} = \frac{1}{\omega_0 \left( \frac{L}{R+r_L} + \frac{Rr_L}{R+r_L} + r_C C \right)} \approx \frac{1}{\omega_0 \left( \frac{L}{R} + r_L C + r_C C \right)}, \quad \text{if } \begin{cases} r_C \ll R \\ r_L \ll R \end{cases} \quad (5)$$

$$\omega_{ZERO} = \frac{1}{r_C C} \quad (6)$$

and

$$\omega_L = r_L / L \quad (7)$$



**Figure 2.** AC small-signal equivalent circuit for the buck converter power stage.

Here  $\omega_0$ ,  $\omega_{ZERO}$ , and  $Q$  represent the filter resonance frequency, capacitor zero frequency, and the quality factor of the filter, respectively.

Among the transfer functions, the one described in Equation (1), i.e., duty cycle-to-output voltage, is controlled through the controller for output voltage regulation. To achieve the closed-loop characteristics, and thus required performance, a controller is applied to it as it behaves as a plant. The  $G_{vd}(s)$  contains a complex conjugate pair whose effect can be nullified by the complex or real zeros of the compensator.

In order to design the digital controller, the continuous-time converter transfer function  $G_{vd}(s)$  is discretized using zero-order-hold (ZOH) with a sampling period  $T_s$ , as follows:

$$G_p(z) = Z \left\{ \frac{1 - e^{-sT_s}}{s} \cdot G_{vd}(s) \right\} = (1 - z^{-1}) \cdot Z \left\{ \frac{G_{vd}(s)}{s} \right\} \quad (8)$$

For the component values mentioned above, the transfer function in the analog and digital form of the buck converter with a short description is presented in Table 1.

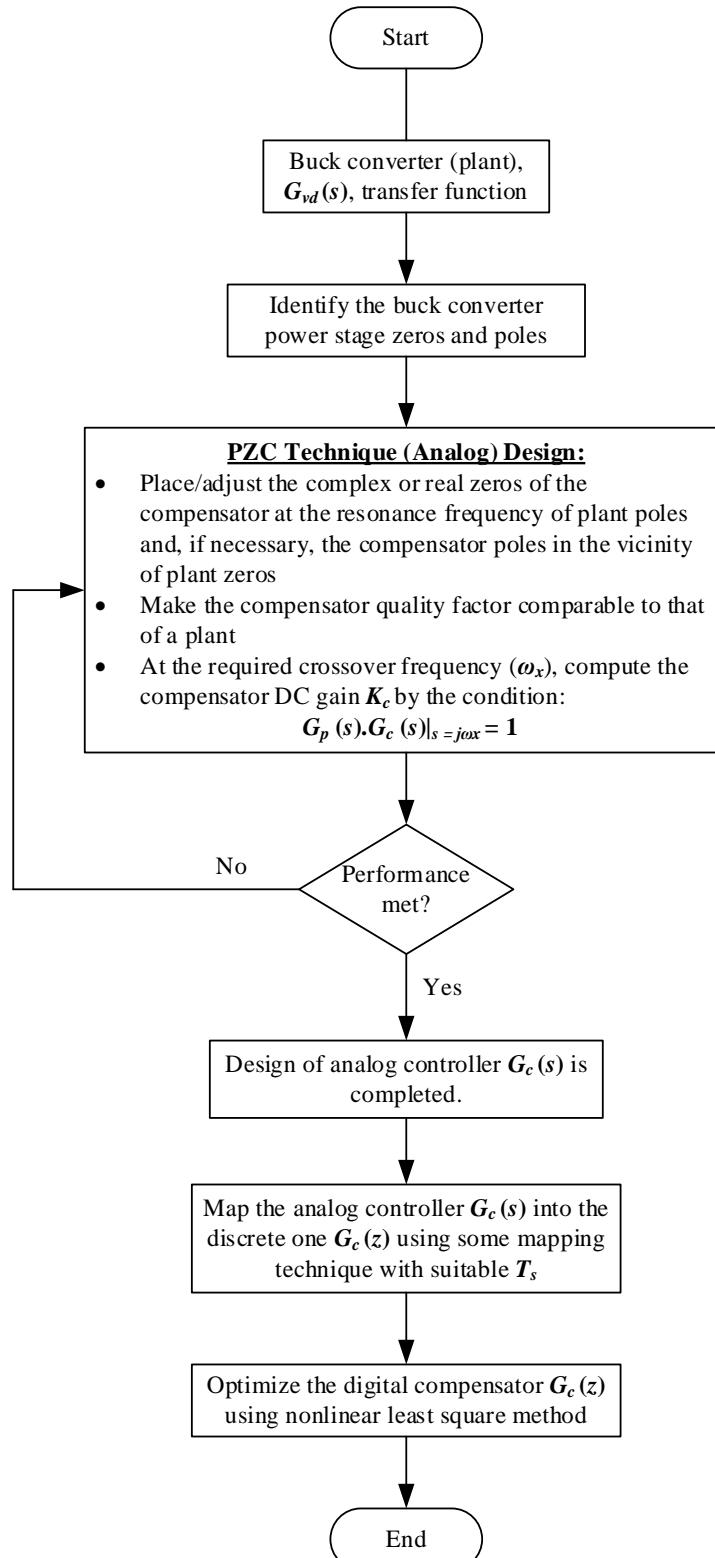
**Table 1.** Buck converter transfer function.

Converter	Transfer Function	Description
Analog	$\frac{7.606 \times 10^{-8}s + 3.237}{1.988 \times 10^{-11}s^2 + 3.097 \times 10^{-6}s + 1}$	A two-pole, one-zero converter, having complex conjugate poles at $10^5 \times (-0.7787 \pm j2.1031)$ with $Q = 1.44$
Digital	$\frac{0.07288z + 0.06332}{z^2 - 1.827z + 0.8692}$	Discretized form obtained using ZOH with $T_s = 1 \mu s$

### 3. PZC-Based Digital Controllers

The buck converter power stage contains two complex conjugate poles occurring at the LC filter's resonant frequency, which results in phase reduction, thus making the system unstable. In order to meet the required specifications, such as bandwidth, steady-state accuracy (ensured through static-error constant/DC gain of the system), robust relative stability, reduced sensitivity to parameter changes, superior transient response, and so on, appropriate gain and phase margins at a specific 0-dB crossover frequency and loop gain should be ensured. This can be accomplished by placing the compensation zeros, real or complex, near the LC filter's resonant frequency. Such a pole-zero-cancellation (PZC) technique in analog form is employed in the paper for designing the digital controllers (emulation technique), which are then optimized using the NLS method. Three types of PZC techniques, designed for a 100 kHz, 0-dB crossover frequency (10 times below the switching frequency, to satisfy the Nyquist criterion), unless otherwise stated, distinguished on the basis of placement of compensator's zeros

and poles, are designed to ensure better static and transient responses. All the cases involve the same method of computing the compensator gain. For the design of PZC techniques, the same procedure is adopted, which is outlined in the flow chart shown in Figure 3.



**Figure 3.** Flow chart explaining the design procedure adopted for the various cases. PZC: pole-zero-cancellation.

### 3.1. A Three-Pole Two-Zero Compensator—Case 1

#### 3.1.1. Using Complex Zeros

In this type of PZC technique, the effect of a pair of complex poles of the converter is nullified by placing the two complex zeros of the compensator at the LC resonant frequency ( $\omega_0$ ). This actually adds to the phase to boost the phase margin. One of the compensator poles is placed at the ESR zero ( $\omega_{ZERO}$ ) to keep the gain of the open-loop transfer function at a slope of  $-1$ . For the rejection of high-frequency noises, the second high-frequency pole is moved from approximately 0.2 to 0.7 of the switching frequency. This additionally incorporated high-frequency pole not only makes the compensator less sensitive to high-frequency noise phenomena, but also assists in smoothing the quantization error in the compensator output. To achieve zero steady-state error, an integrator (a pole at origin) is also introduced.

With the mentioned placement of the compensator poles and zeros, the compensator transfer function takes the form

$$G_c(s) = K_c \frac{\left(\frac{s^2}{\omega_z^2} + \frac{s}{Q_C \omega_z} + 1\right)}{s \left(\frac{s}{k \cdot \omega_s} + 1\right) \left(\frac{s}{\omega_{ZERO}} + 1\right)} \quad (9)$$

where parameter  $k$ , ranging from 0.2 to 0.7, controls the location of the high-frequency pole;  $\omega_z = \omega_0$  designates the compensator complex zero frequencies, numerically equivalent to the plant poles' resonance frequencies; the dimensionless  $Q$ -factor,  $Q_C$ , of the compensator is selected close to the power stage,  $Q$ ; and the DC gain,  $K_c$ , of the compensator is adjusted to meet the required 0-dB crossover frequency (100 kHz) denoted by  $\omega_x$ . Then,  $s_x = j\omega_x = j2\pi f_x$ .

Assuming the condition that the compensated system's gain plot crosses 0-dB at a  $-1$  slope, i.e.,  $G_p(s)|_{s=s_x} \cdot G_c(s)|_{s=s_x} = 1$ ,  $K_c$  is then calculated by

$$K_c = \left. \frac{s \left( \frac{s}{k \cdot \omega_s} + 1 \right) \left( \frac{s}{\omega_{ZERO}} + 1 \right)}{\left( \frac{s^2}{\omega_z^2} + \frac{s}{Q_C \omega_z} + 1 \right)} \right|_{s=s_x} \cdot \frac{1}{G_p(s)|_{s=s_x}} \quad (10)$$

With the placement of poles and zeros and calculation of the DC gain, the analog controller transfer function is given, numerically, by:

$$G_c(s) = \frac{4.309 \times 10^{-6}s^2 + 0.6041s + 1.951 \times 10^5}{3.74 \times 10^{-15}s^3 + 1.827 \times 10^{-7}s^2 + s} \quad (11)$$

The continuous-time compensator can be mapped into its discrete-time counterpart using one of the transformation techniques, such as 'Tustin' (in our case), expressed mathematically by  $s = \frac{2}{T_s} \left( \frac{1-z^{-1}}{1+z^{-1}} \right)$ , with the sampling time equivalent  $T_s = 1 \mu\text{s}$ . The corresponding discrete-time compensator is given by:

$$\begin{aligned} G_c(z) &= \frac{6.753z^3 - 5.595z^2 - 6.47z + 5.877}{z^3 + 0.4273z^2 - 0.9566z - 0.4707} \\ &= \frac{6.753 - 5.595z^{-1} - 6.47z^{-2} + 5.877z^{-3}}{1 + 0.4273z^{-1} - 0.9566z^{-2} - 0.4707z^{-3}} \end{aligned} \quad (12)$$

With the help of an inverse z-transform, the compensator discrete-time transfer function can be translated into the difference equation given by

$$\begin{aligned} u[n] &= -0.4273u[n-1] + 0.9566u[n-2] + 0.4707u[n-3] \\ &+ 6.753e[n] - 5.595e[n-1] - 6.47e[n-2] + 5.877e[n-3] \end{aligned} \quad (13)$$

where  $e[n]$ ,  $e[n-1]$ ,  $e[n-2]$ , and  $e[n-3]$  designate the current, one sample period, two sample period, and three sample period delayed values of the error signals, respectively, whereas  $u[n]$ ,  $u[n-1]$ ,  $u[n-2]$ ,

and  $u[n - 3]$  represent the present, one sample period, two sample period, and three sample period delayed values of the duty ratio, respectively.

### 3.1.2. Using Real Zeros

A compensator with three poles and two real zeros can also be realized and is expressed by

$$G_c(s) = K_c \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s\left(\frac{s}{k\omega_s} + 1\right)\left(\frac{s}{\omega_{ZERO}} + 1\right)} \quad (14)$$

Usually, the real zeros  $\omega_{z1}$  and  $\omega_{z2}$  are placed close to the resonant frequency,  $\omega_0$ . Their positions can be controlled using the relationships:  $\omega_{z1} = m_1\omega_0$  and  $\omega_{z2} = m_2\omega_0$ , where the coefficients  $m_1$  and  $m_2$  describe the deviation of the zeros from  $\omega_0$ . Here, in our case, it is observed that placement of one of the zeros at  $\omega_0$ , i.e.,  $m_1 = 1$ , and the other slightly below  $\omega_0$ , i.e.,  $m_2 = 0.8$ , ensures the increase in phase margin, thus the better performance. The compensator's three poles are placed in the same way as described in the complex zeros case.

With such an arrangement of poles and real zeros, the analog controller, numerically, takes the form

$$G_c(s) = \frac{3.597 \times 10^{-6}s^2 + 1.378s + 1.303 \times 10^5}{3.74 \times 10^{-15}s^3 + 1.827 \times 10^{-7}s^2 + s} \quad (15)$$

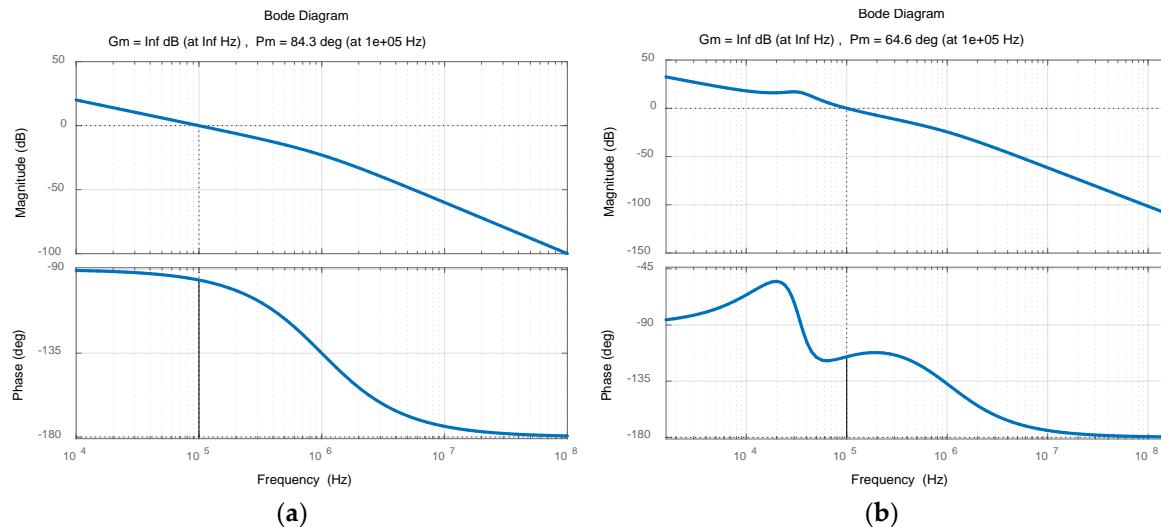
The digital controller obtained from the analog controller using the bilinear mapping technique is then described by

$$G_c(z) = \frac{6.257z^3 - 4.072z^2 - 6.069z + 4.261}{z^3 + 0.4273z^2 - 0.9566z - 0.4707} \quad (16)$$

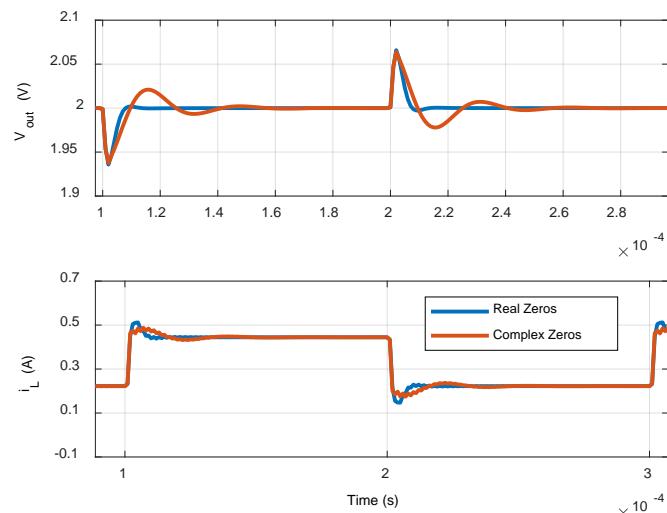
When comparing the analog compensators with real and complex zeros and the digital compensators, the following corollaries can be deduced.

- It is revealed from the inspection of the Bode plots (see Figure 4) of the open-loop compensated buck converter system that the compensator using the complex zeros at the resonance frequency achieves a phase margin of  $84.3^\circ$ , as compared to the one with real zeros, which attains a phase margin of  $64.6^\circ$ . Both the compensators are designed for 100-kHz bandwidth (0-dB crossover frequency). This suggests that complex-zero compensation offers larger stability margins and reduced amplitude of the resonance peak, in comparison to that of the real-zero compensation. Consequently, complex-zero compensation displays excellent static properties.
- Unlike the excellent static properties, complex-zero compensation shows poor dynamic properties. In order to check the dynamicity, the load is changed from  $4.5\ \Omega$  to  $9\ \Omega$  and then from  $9\ \Omega$  to  $4.5\ \Omega$ . Although the output voltage settles to its steady-state value of 2 V for both compensators, the compensator with complex zeros shows more recovery time and spike voltage peak at the load transient as compared to that of the one with real zeros. This is due to the fact that a change in load displaces the converter poles from their original positions. Thus, the predetermined compensator zeros are not able to perfectly annul the effects of the converter's complex poles. If the compensator zeros are made adaptive according to the perturbation in the load current, then the complete cancellation effect can be ensured. MATLAB/Simulink-based simulation results shown in Figure 5 highlight this fact.

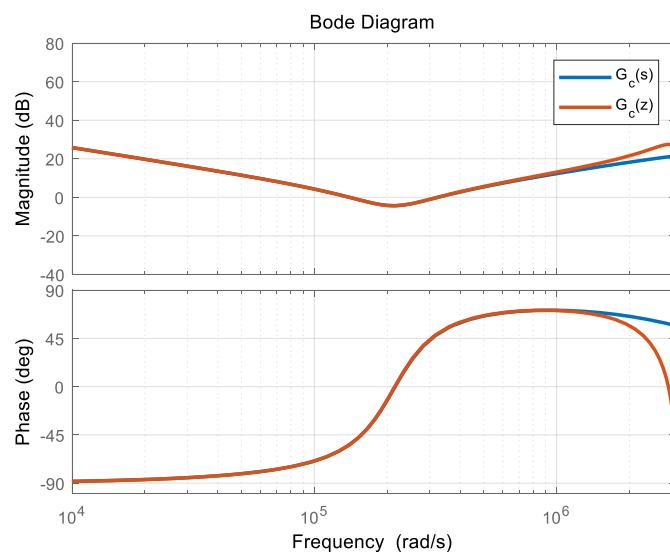
Transformation of the continuous-time controller into the discrete-time controller results in frequency distortions. Consequently, the discrete-time controller shows a slightly deviated behavior from its analog counterpart at frequencies close to the Nyquist frequency. The Bode plot of the analog and digital compensators (see Figure 6) pinpoints the phenomenon of frequency distortions.



**Figure 4.** Bode plot of the open-loop compensated system using (a) the complex zeros and (b) the real zeros.



**Figure 5.** Load regulation by real and complex zeros-based compensators.



**Figure 6.** Bode diagram of the compensators.

### 3.2. A Two-Pole (with One Pole at the Origin) Two-Zero Compensator—Case 2

#### 3.2.1. Using Complex Zeros

Reasonable compensation can also be achieved using two poles (with two complex zeros), rather than using three poles. The poles and the (complex) zeros are placed in the same way as described in case 1. For example, in a two-pole two-zero compensator, a pair of matching complex zeros is placed exactly at the resonance frequency to nullify the effects of a pair of complex conjugate poles introduced by the converter power stage. In order to avoid undesirable ripples in the output voltage introduced by the output capacitor ESR, one of the compensator poles is placed at the ESR zero frequency to compensate for the capacitor ESR zero. For the sake of ensuring high low-frequency gain to achieve low static error and good input rejection, a pole (an integrator) is placed at the origin. Such a two-pole two-zero compensator, in transfer function form, is described by [24] as follows:

$$G_c(s) = K_c \frac{\left(\frac{s^2}{\omega_z^2} + \frac{s}{Q_C \omega_z} + 1\right)}{s \left(\frac{s}{\omega_{ZERO}} + 1\right)} \quad (17)$$

With  $K_c$  computed from the condition  $G_p(s)|_{s=s_x} \cdot G_c(s)|_{s=s_x} = 1$ , the compensator's transfer function in the s-domain, numerically, takes the form as follows:

$$G_c(s) = \frac{4.288 \times 10^{-6}s^2 + 0.6011s + 1.941 \times 10^5}{2.35 \times 10^{-8}s^2 + s} \quad (18)$$

The analog controller is mapped into the digital one with the help of the Tustin mapping technique using a sampling time of 1  $\mu$ s, as follows:

$$G_c(z) = \frac{8.858z^2 - 16.2z + 7.71}{z^2 - 0.08978z - 0.9102} \quad (19)$$

#### 3.2.2. Using Real Zeros

With the real zeros replacing the complex zeros, the transfer function of a two-pole two-zero compensator is then described by

$$G_c(s) = K_c \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s \left(\frac{s}{\omega_{ZERO}} + 1\right)} \quad (20)$$

Regarding the placement of the zeros, one of the real zeros is placed at  $\omega_0$ , i.e.,  $m_1 = 1$ , and the other slightly below  $\omega_0$ , i.e.,  $m_2 = 0.8$ . This combination ensures the increase in phase margin, thus better response characteristics. With the placement of compensator poles and zeros and the adjustment of gain  $K_c$  to achieve the desired crossover frequency, the analog controller reduces to

$$G_c(s) = \frac{3.512 \times 10^{-6}s^2 + 1.495s + 1.59 \times 10^5}{2.35 \times 10^{-8}s^2 + s} \quad (21)$$

Using the bilinear transformation with 1  $\mu$ s, the discrete controller, equivalently, is expressed by

$$G_c(z) = \frac{8.213z^2 - 13.27z + 5.358}{z^2 - 0.08978z - 0.9102} \quad (22)$$

### 3.3. A Two-Pole Two-Zero Compensator—Case 3

#### 3.3.1. Using Complex Zeros

Another type of a two-pole two-zero compensator can be achieved by placing a pole at the origin with a low-frequency pole. In such a compensator, the buck converter transfer function is completely cancelled with the complex zeros (occurring at resonance frequency) and a pole (placed at the ESR zero frequency) of the compensator. Thus, the phase shift introduced by an LC filter complex double pole and output capacitor ESR zero is annulled by making the converter characteristics ineffective. Through the remaining part of the compensator (gain and a low-frequency pole), which is essentially a low-pass filter, the composite system's response is thus controlled. Mathematically, the transfer function of the compensator is given by

$$G_c(s) = \frac{K_c}{\left(\frac{s}{\omega_p} + 1\right)} \left( \frac{\frac{s^2}{\omega_z^2} + \frac{s}{Q_C \omega_z} + 1}{\frac{s}{\omega_{ZERO}} + 1} \right) \quad (23)$$

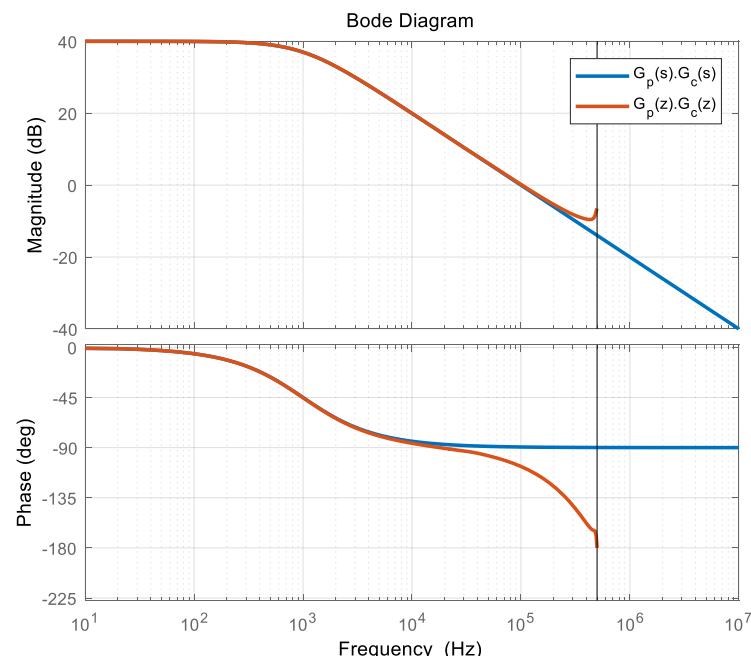
With the low-frequency pole placed far below (approximately  $10^3$  times)  $f_s$ , the compensator is described, numerically, by

$$G_c(s) = \frac{6.825 \times 10^{-10}s^2 + 9.567 \times 10^{-5}s + 30.9}{3.74 \times 10^{-12}s^2 + 1.592 \times 10^{-4}s + 1} \quad (24)$$

Using the Tustin mapping technique, the analog controller is mapped in to the digital controller as follows:

$$G_c(z) = \frac{8.831z^2 - 16.15z + 7.686}{z^2 - 0.08352z - 0.9045} \quad (25)$$

For the controllers designed for the 100-kHz crossover frequency, the analog control system offers a phase margin of about  $90.6^\circ$ , whereas the digital control system provides a phase margin of  $72.7^\circ$  (see Figure 7). Frequency distortion due to the mapping from the s-plane to z-plane deteriorates the performance of the digital controller. This requires the retuning of the coefficients of the digital controller.



**Figure 7.** Bode plot of the open-loop compensated buck converter system.

### 3.3.2. Using Real Zeros

A two-pole two-zero compensator with one of the poles lying at low frequency and real zeros lying in the vicinity of the resonance frequency is characterized by the transfer function as follows:

$$G_c(s) = K_c \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_p} + 1\right)\left(\frac{s}{\omega_{ZERO}} + 1\right)} \quad (26)$$

Numerically, the analog controller is given by

$$G_c(s) = \frac{3.512 \times 10^{-6}s^2 + 1.495s + 1.59 \times 10^5}{2.35 \times 10^{-8}s^2 + s} \quad (27)$$

The equivalent discrete-time controller using the bilinear transformation is expressed by

$$G_c(z) = \frac{8.213z^2 - 13.27z + 5.358}{z^2 - 0.08978z - 0.9102} \quad (28)$$

## 4. NLS Method-Based Optimized Digital Controllers

In the context of optimization, the nonlinear least squares (NLS) method bears a tempting structure that can be exploited with great effectiveness in algorithm design. Regarding the compensated buck converter system, minimization of the voltage error signal essentially constitutes the NLS problem. Specifically, the NLS technique can be employed to retune the discrete-time controller coefficients for fast setpoint tracking. This is accomplished by adjusting the controller coefficients to speedily reduce the error  $e(t) = V_{out} - V_{ref}$  at all steps of the simulation time. As the minimization of the sum of squares of the error functions is carried out by the algorithm at each step, this constitutes the multiobjective optimization problem.

In the paper, for calculating the sum of error squares, among the different large-scale algorithms [25], such as the trust-region-reflective (TRR), variable projection (VP), and Levenberg–Marquardt (LM) algorithms, LM is employed. Linear algebra is exploited in large-scale algorithms which do not require or store full matrices for its operation. It is a well-established fact that the LM algorithm performs better when bound constraints are not considered in the problem.

The algorithm starts with the initial design vector,  $x_0$ , indicating the initial design variables in the form of coefficients of the digital controller computed through the pole-zero-cancellation techniques. For the considered cases, no restriction has been imposed on the lower and upper bounds of the design variables.

Mathematically speaking, the NLS method using the LM algorithm involves minimizing the sum of squares of the error signal, i.e.,

$$\begin{aligned} \min_{x \in \Re^n} f(x) &= \min_{x \in \Re^n} \|e(x)\|_2^2 \\ &= \min_{x \in \Re^n} (e_1^2(x) + e_2^2(x) + \dots + e_m^2(x)) \\ &= \min_{x \in \Re^n} \sum_{i=1}^m e_i^2(x) \end{aligned} \quad (29)$$

subject to the constraints:

$$\begin{cases} A_{eq} \cdot x = b_{eq} & \text{linear equality} \\ A \cdot x \leq b & \text{linear inequality} \\ l \leq x \leq u & \text{bounds} \\ C(x) = 0 & \text{nonlinear equality} \\ C_{eq}(x) \leq 0 & \text{nonlinear inequality} \end{cases} \quad (30)$$

where  $x = (x_1, x_2, \dots, x_n) \subset \Re^n$ ,  $l \subset (\Re \cup (-\infty))^n$ , and  $u \subset (\Re \cup (\infty))^n$ . Here,  $A$  and  $A_{eq}$ , and  $C$  and  $C_{eq}$  are the matrices of doubles for linear inequalities and equalities, and nonlinear inequalities and equalities, respectively. Similarly,  $b$  and  $b_{eq}$  are the vectors of doubles for linear inequalities and equalities, respectively, and  $l$  and  $u$  represent the lower and upper bounds, respectively, on each  $x$  component. In our case, since no restriction is imposed on the bounds of design variables for the unconstrained multiobjective optimization problem, all matrices and vectors are empty sets. Here, the function to be minimized,  $f(x) = \|e(x)\|_2^2$ , representing the  $l_2$ -norm of error, is assumed to be continuously differentiable at point  $x_0$ . It is assumed that  $m \geq n$ . As remarked, the vector  $x$  represents the number of design/decision variables, which are specifically the coefficients of the digital controllers.

In the compensated control systems, in order to achieve the targeted trajectories realistically, the residual  $\|e(x)\|$ , being a function from  $\Re^n$  to  $\Re^m$ , described in Equation (31)

$$\begin{aligned} \|e(x)\| &= e_i(x) \\ &= \begin{bmatrix} e_1(x) \\ e_2(x) \\ \vdots \\ e_m(x) \end{bmatrix} = \begin{bmatrix} v_o(x, t_1) - v_{ref}(t_1) \\ v_o(x, t_2) - v_{ref}(t_2) \\ \vdots \\ v_o(x, t_m) - v_{ref}(t_m) \end{bmatrix} \end{aligned} \quad (31)$$

is made small optimally and converged speedily. Rapidly converged minimum residuals result in better set-point tracking. A unique solution is guaranteed due to the convex nature of the minimizer.

In order to get deep mathematical insight, the algorithm forces the output  $v_o(x, t)$  to track the continuous required trajectory  $v_{ref}(t)$  for the decision vector  $x$  and scalar  $t$ . That is to say,

$$\min_{x \in \Re^n} \int_{t_1}^{t_2} (v_o(x, t) - v_{ref}(t))^2 dt \quad (32)$$

Discretization of the integral through an appropriate quadrature formula reduces Equation (32) to the least squares problem:

$$\min_{x \in \Re^n} \|e(x)\|_2^2 = \min_{x \in \Re^n} \sum_{i=1}^m (v_o(x, t_i) - v_{ref}(t_i))^2 \quad (33)$$

A  $m$ -by- $n$ -sized Jacobian matrix  $J(x)$  of the residual  $\|e(x)\|$  of  $n$  variables is computed by

$$J(x) = \frac{\delta e_i(x)}{\delta x_k}, \quad 1 \leq i \leq m, \quad 1 \leq k \leq n \quad (34)$$

On the basis of  $J(x)$ , the specially structured gradient vector  $G(x)$  and Hessian matrix  $H(x)$  of the NLS method are calculated by Equations (35) and (36), respectively.

$$\begin{aligned} G(x) &= \nabla \|e(x)\|_2^2 \\ &= \sum_{i=1}^m e_i(x) \nabla e_i(x) = 2(J(x)^T e(x)) \end{aligned} \quad (35)$$

$$\begin{aligned} H(x) &= \nabla^2 \|e(x)\|_2^2 \\ &= 2 \left( J(x)^T J(x) + \sum_{i=1}^m e_i(x) \nabla^2 e_i(x) \right) \\ &= 2 \left( J(x)^T J(x) + Q(x) \right) \end{aligned} \quad (36)$$

where

$$Q(x) = \sum_{i=1}^m (e_i(x) \times H_i(x)) \quad (37)$$

The matrix  $Q(x)$  comes with the property that it tends to approach zero as the residual  $\|e(x)\|$  approaches zero on the occasion the decision variables  $x_k$ , finally settling to optimal values. In other words, the matrix  $Q(x)$  gives an indication of how fast the minimization of the error is accomplished.

By amalgamating the salient characteristics of the Gauss–Newton (GN) and steepest descent (SD) algorithms, the LM method computes the search direction on the basis of a solution of the linear set of equations [26], i.e.,

$$(J(x_k)^T J(x_k) + \lambda_k I) d_k = -J(x_k)^T e(x_k) \quad (38)$$

More precisely, the LM method modifies the GN search direction by altering  $J(x_k)^T J(x_k)$  with  $J(x_k)^T J(x_k) + \lambda_k I$ . By replacing the identity matrix with the diagonal of the Hessian, Equation (38) can be expressed alternatively as

$$\begin{aligned} & (J(x_k)^T J(x_k) + \lambda_k \text{diag}(J(x_k)^T J(x_k))) d_k \\ &= -J(x_k)^T e(x_k) \end{aligned} \quad (39)$$

Or, equivalently, in terms of the least squares problem, Equation (39) takes the form

$$\min_{d_k} \| \begin{pmatrix} J(x_k) \\ \sqrt{\lambda_k} \text{diag}(J(x_k)^T J(x_k)) \end{pmatrix} - \begin{pmatrix} -e(x_k) \\ 0 \end{pmatrix} \|_2^2 \quad (40)$$

The magnitude and direction of  $d_k$  is controlled through the scalar  $\lambda_k$ , whose initial value  $\lambda_0$  is set empirically, perhaps, as 100. The LM method therefore uses a search direction that falls within the directions calculated by the GN and SD methods. The LM algorithm, thus, essentially is an aggregation of the SD and GN algorithms. For example, when  $\lambda_k$  is zero, the direction  $d_k$  refers to the direction of the GN method, whereas when  $\lambda_k$  tends to infinity,  $d_k$  assumes the direction of SD, with its magnitude tending to zero. This comes with the observation that the term  $e(x_k + d_k) < e(x_k)$  holds true for some adequately large values of  $\lambda_k$ . Through the control of the term  $\lambda_k$ , descent can be ensured even when second-order terms, which limit the GN method's efficiency, are experienced. The algorithm adjusts the value of  $\lambda_k$  during each of the step as follows:

$$\lambda_{k+1} = \begin{cases} \frac{\lambda_k}{10}, & \text{when the move passes} \\ \lambda_k \times 10, & \text{when the move fails} \end{cases} \quad (41)$$

In a nutshell, the LM algorithm works in the following way:

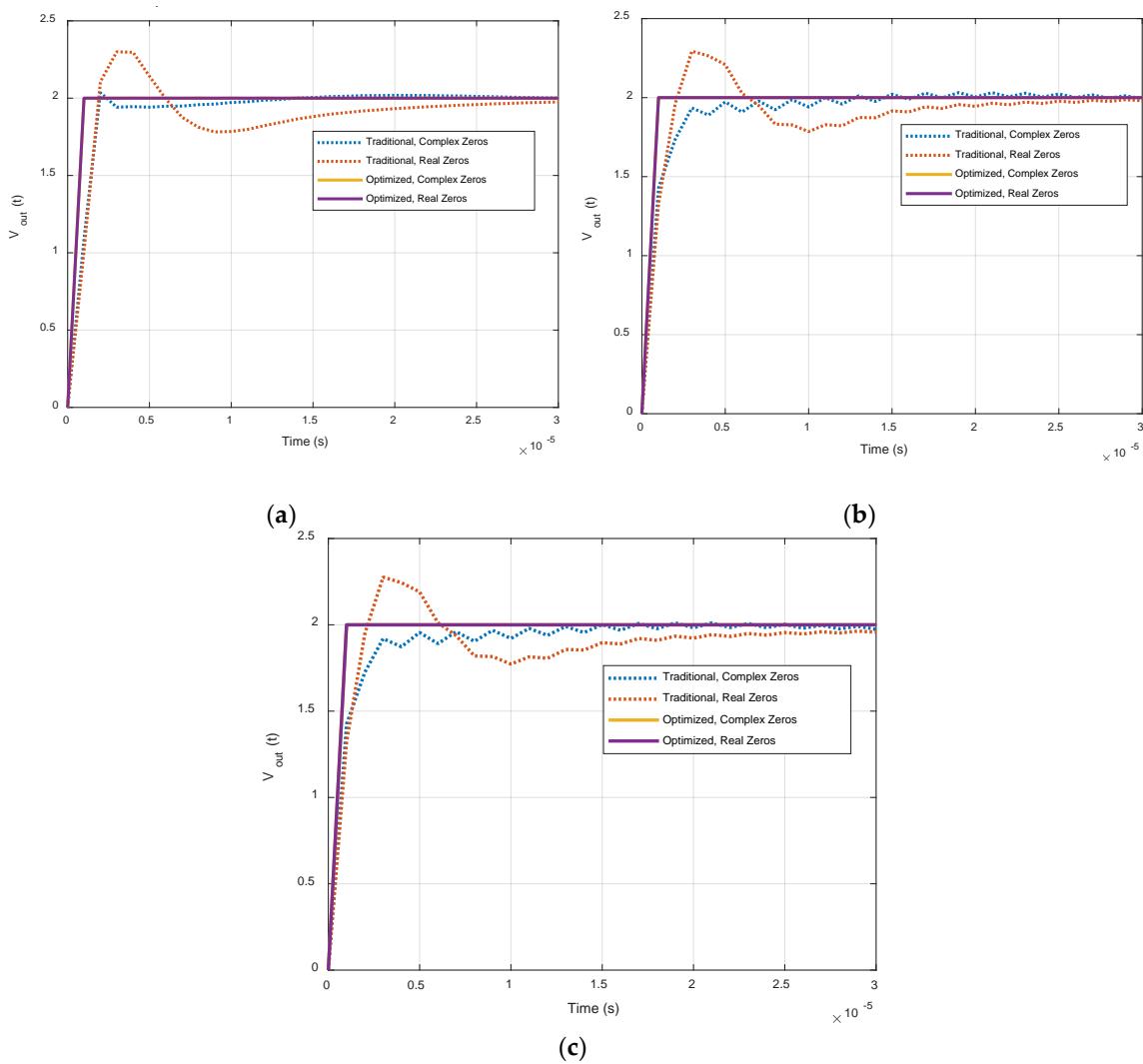
- It starts with an initial guess  $x_0$  and iterates for  $k = 1, 2, \dots, n$ .
- The Lagrange multiplier  $\lambda_k$  is then selected for each step  $k$ .
- Equation (39) or (40) is solved for determining  $d_k$ .
- For the next iteration,  $k + 1$ ,  $d_{k+1} = d_k + \Delta d_k$  is calculated.
- At the end, the solution is checked for convergence.

Although several stopping criteria, such as absolute function criterion, sequence convergence criterion, maximum iteration count criterion, and so on, can be adopted, here, the algorithm stops when the final change in the sum of squares relative to its initial value is less than the default value of the function tolerance. One must remember that although the algorithm ensures optimal performance, convergence to the global minimum of the objective function cannot be guaranteed. To realize the LM algorithm based on the NLS method, a MATLAB/Simulink environment is used. Termination tolerance for both the objective function and the parameter estimation is appropriately selected.

When the NLS method is applied to retune the coefficients of the digital controllers, tremendous improvement in performance is observed. All the controllers, traditional and optimized, in transfer function form, are summarized in Table 2. Correspondingly, step response characteristics displayed by all the controllers, traditional and optimized, are shown in Figure 8. The performance parameters in the form of maximum overshoot, settling time, and rise time, computed from the step response characteristics, are summarized and compared in Table 3. From Table 3, it is inferred that the optimized digital controllers offer much-improved performance as compared to their traditional counterparts. This validates the applicability and workability of the NLS method.

**Table 2.** Controllers' transfer functions.

Case No.	Compensator Zeros	Analog Controller $G_c(s)$	Digital Controller $G_c(z)$	Optimized Digital Controller $G_c(z)$
1	Complex	$\frac{4.309 \times 10^{-6}s^2 + 0.6041s + 1.951 \times 10^5}{3.74 \times 10^{-15}s^3 + 1.827 \times 10^{-7}s^2 + s}$	$\frac{6.753z^3 - 5.595z^2 - 6.47z + 5.877}{z^3 + 0.4273z^2 - 0.9566z - 0.4707}$	$\frac{6.8515z^3 - 5.5501z^2 - 6.625z + 5.8584}{0.5529z^3 + 0.4746z^2 - 0.5528z - 0.4707}$
	Real	$\frac{3.597 \times 10^{-6}s^2 + 1.378s + 1.303 \times 10^5}{3.74 \times 10^{-15}s^3 + 1.827 \times 10^{-7}s^2 + s}$	$\frac{6.257z^3 - 4.072z^2 - 6.069z + 4.261}{z^3 + 0.4273z^2 - 0.9566z - 0.4707}$	$\frac{5.7210z^3 - 4.3870z^2 - 5.8969z + 5.1035}{0.4617z^3 + 0.4163z^2 - 0.4644z - 0.4135}$
2	Complex	$\frac{4.288 \times 10^{-6}s^2 + 0.6011s + 1.941 \times 10^5}{2.35 \times 10^{-6}s^2 + s}$	$\frac{8.858z^2 - 16.2z + 7.71}{z^2 - 0.08978z - 0.9102}$	$\frac{8.9562z^2 - 16.2048z + 7.6637}{0.7227z^2 - 0.1018z - 0.6209}$
	Real	$\frac{3.512 \times 10^{-6}s^2 + 1.495s + 1.59 \times 10^5}{2.35 \times 10^{-6}s^2 + s}$	$\frac{8.213z^2 - 13.27z + 5.358}{z^2 - 0.08978z - 0.9102}$	$\frac{7.4178z^2 - 13.4213z + 6.3473}{0.5986z^2 - 0.0843z - 0.5143}$
3	Complex	$\frac{6.825 \times 10^{-10}s^2 + 9.567 \times 10^{-5}s + 30.9}{3.74 \times 10^{-12}s^2 + 1.592 \times 10^{-4}s + 1}$	$\frac{8.831z^2 - 16.15z + 7.686}{z^2 - 0.08352z - 0.9045}$	$\frac{8.9287z^2 - 16.155z + 7.6401}{0.7205z^2 - 0.1015z - 0.6190}$
	Real	$\frac{5.59 \times 10^{-10}s^2 + 23.79 \times 10^{-5}s + 25.31}{3.74 \times 10^{-12}s^2 + 1.592 \times 10^{-4}s + 1}$	$\frac{8.187z^2 - 13.23z + 5.341}{z^2 - 0.08352z - 0.9045}$	$\frac{7.3954z^2 - 13.3807z + 6.3281}{0.5968z^2 - 0.0841z - 0.5127}$

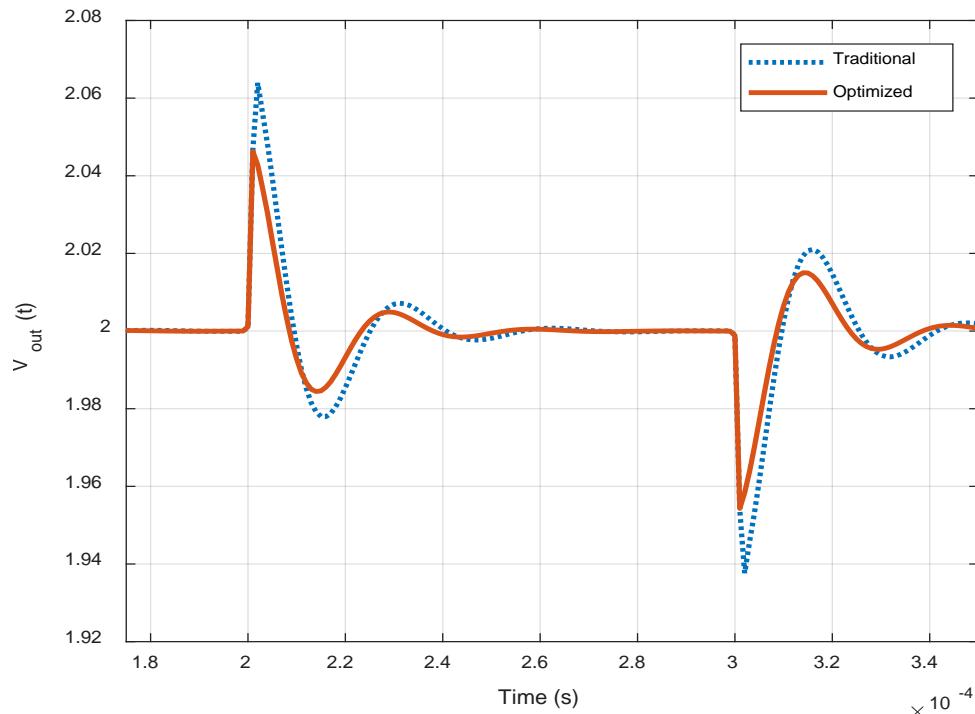


**Figure 8.** Step response offered by (a) case 1, (b) case 2, and (c) case 3 controllers.

**Table 3.** Comparative analysis of controllers' performance characteristics.

Case No.	Controller	Performance Parameters		
		Max. Overshoot (%)	Rise Time ( $\mu$ s)	Settling Time ( $\mu$ s)
1	Traditional, Complex Zeros	1.7789	1.5674	8.5697
	Traditional, Real Zeros	14.9854	1.5228	25.322
	Optimized, Complex Zeros	0.0536	0.80	0.98
	Optimized, Real Zeros	0.000004	0.80	0.98
2	Traditional, Complex Zeros	1.5949	2.1813	12.02
	Traditional, Real Zeros	14.7028	1.5953	22.31
	Optimized, Complex Zeros	0.0055	0.79	0.97
	Optimized, Real Zeros	0.00005	0.80	0.98
3	Traditional, Complex Zeros	0.5560	2.2435	14.103
	Traditional, Real Zeros	13.8212	1.6108	24.22
	Optimized, Complex Zeros	0.0029	0.799	0.979
	Optimized, Real Zeros	$4.1280 \times 10^{-10}$	0.80	0.98

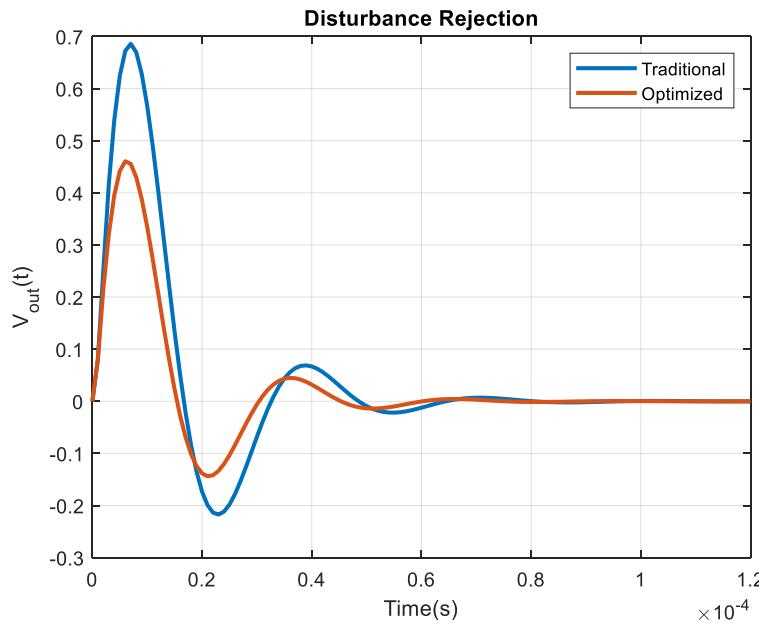
Like the step response characteristics, the optimized controllers also offer superior transient behavior. A three-pole two-zero (complex)-based optimized digital controller offers reduced recovery time and peak-to-peak spike voltage at the time of load transient as compared to its traditional form (see Figure 9). In the same way, other optimized controllers also show fast transient response with regard to their unoptimized counterparts.

**Figure 9.** Load transient response.

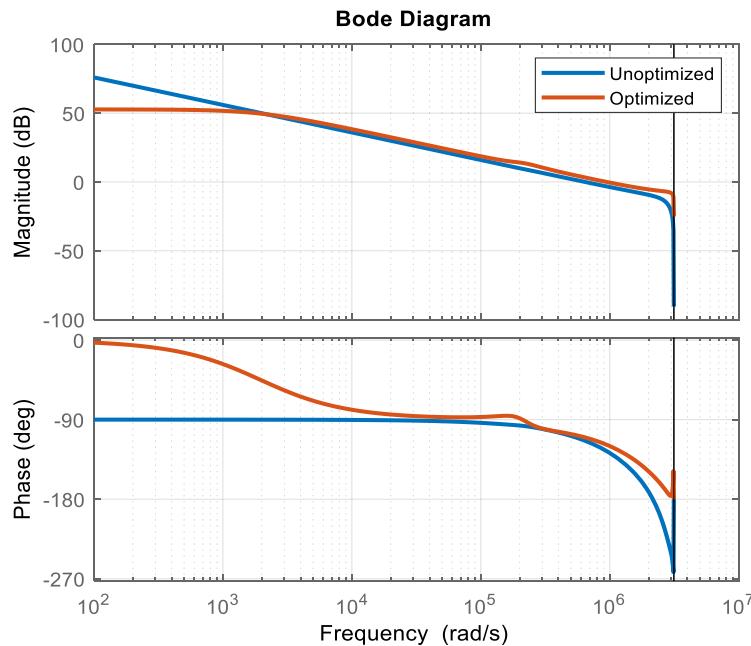
The optimized controller not only offers excellent set-point tracking and load regulation characteristics, but also exhibits improved disturbance rejection abilities against the disturbance (due to variations in the converter power-stage parameters because of aging or model uncertainties) injected at the converter input (see Figure 10).

To gain more insight into the performance in terms of frequency-domain characteristics, the Bode plot of the unoptimized and optimized  $G_p(z) \cdot G_c(z)$  of case 1 shown in Figure 11 clearly depicts that

the optimized digital controller assists in ensuring more phase margin (and thus system stability) for all the frequencies, as compared to the unoptimized digital controller.

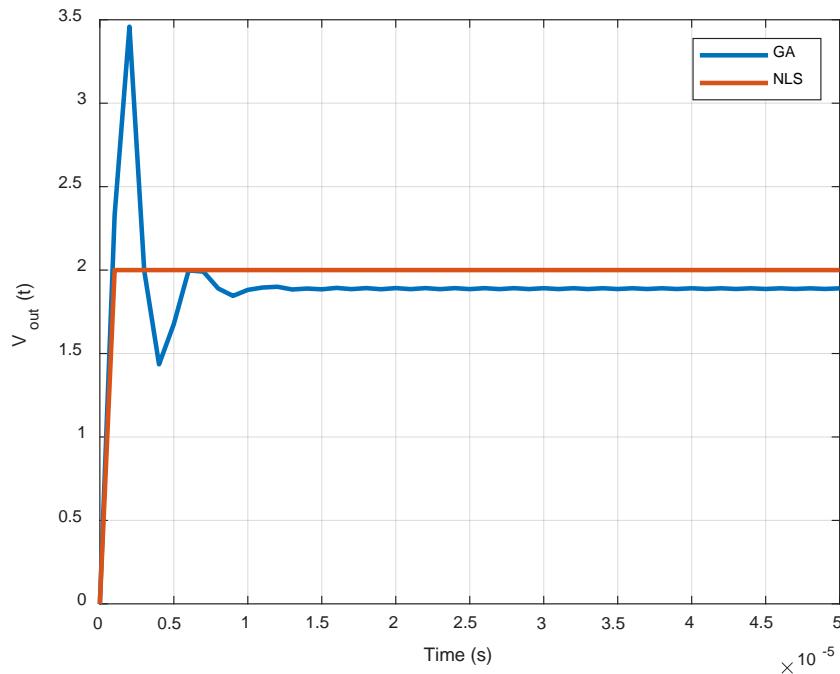


**Figure 10.** Disturbance rejection comparison.



**Figure 11.** Bode plot of the unoptimized and optimized  $G_p(z) \cdot G_c(z)$ .

In order to validate the superiority of the proposed NLS method over the other optimization techniques, such as a genetic algorithm (GA), a comparison of the voltage response of the two-pole two-zero (complex)-based optimized digital controllers obtained through NLS and GA is presented in Figure 12. For the typical design example, the NLS method completely outshines GA performance-wise (overshoots, steady-state error, etc.). The GA parameters considered are the following: objective function = Integral Time Absolute Error (ITAE), population size = 200, generations = 25, crossover fraction = 0.65, and function tolerance =  $1 \times 10^{-6}$ .



**Figure 12.** Output voltage response of the optimized digital controllers.

## 5. Digital Control Loop Elements Modelling

A digital control loop involves mixed signals. A continuous-time error signal digitized through the ADC is processed by the digital controller. The discrete-time controller output signal is then converted into the analog one through the DAC/DPWM to apply on-off pulses to the switching circuit. For the more realistic digitally compensated buck converter system, inherently existing nonlinearities occurring in the digital control loop should be modelled and considered.

### 5.1. Loop Delay

The digital control loop suffers from the delay introduced by various elements in the loop. The delay due to the ADC conversion time  $t_{ADC}$ , the digital controller processing time  $t_p$ , the DAC conversion time  $t_{DAC}$ , the gate-driver propagation delay  $t_{GD}$ , and so forth constitutes the total loop delay  $t_d$ , which adversely limits the loop bandwidth, thus resulting in deteriorated performance. However, the effect becomes less prominent if the loop delay remains within the one sampling period  $T_s$ . With the availability of high-speed ADCs, DACs, processors, and FPGAs, the total loop delay can be reduced. A delay of half the period, i.e.,  $t_d = 0.5 \mu s$ , is considered in the design examples. The delay can be modelled mathematically by  $e^{-st_d} \approx 1 + (1 + st_d)$ , where the first-order lag approximation has been used to make the calculations simpler.

### 5.2. ADC and DAC Resolutions

In order to avoid unwanted oscillations, called limit cycle oscillations (LCOs), and thus to ensure steady-state behavior, ADC and DAC resolutions should be selected with care. Regarding the ADC resolution, LCOs can be avoided if the output error voltage is restricted within the allowed output voltage variation  $\Delta V_{out}$ . Alternatively, the ADC quantization step calculated by  $q_{v,ADC} = V_{max}/2^{n_{ADC}}$  should be lesser in value than  $\Delta V_{out}$ , i.e.,

$$\begin{aligned} \left(\frac{1}{H}\right) \cdot \left(\frac{V_{max}}{2^{n_{ADC}}}\right) &\leq \Delta V_{out} \\ \Rightarrow \left(\frac{V_{max}}{2^{n_{ADC}}} \cdot \frac{1}{V_{out}}\right) &\leq \left(\frac{\Delta V_{out}}{V_{out}} \cdot \frac{V_{ref}}{V_{out}}\right), \text{ with } H = \frac{V_{ref}}{V_{out}} \end{aligned} \quad (42)$$

Manipulation of Equation (42) gives the formula for ADC resolution  $n_{ADC}$  as follows [27]:

$$n_{ADC} \geq \text{int}[\log_2 \left( \frac{V_{max}}{V_{ref}} \cdot \frac{V_{out}}{\Delta V_{out}} \right)] \quad (43)$$

where  $V_{max}$ ,  $V_{out}$ , and  $V_{ref}$  represent the maximum output, output, and reference voltages, respectively;  $H$  signifies the scaling factor for the sensed output voltage and is set to one for concerned design examples; the function  $\text{int}[]$  refers to the upper rounded integer value of the argument.

Without going into the mathematical detail, it has been observed experimentally that the DPWM resolution,  $n_{DPWM}$ , should be finer than that of the ADC,  $n_{ADC}$ . Mathematically,

$$n_{DPWM} \geq \text{int}[n_{ADC} + \log_2 \left( \frac{V_{ref}}{V_{max} \cdot D} \right)] \quad (44)$$

In Equation (44), addition of the term  $\log_2(V_{ref}/V_{max} \cdot D)$  to  $n_{ADC}$  indicates that  $n_{DPWM}$  should at least be set one bit larger than  $n_{ADC}$  in the steady state. This corresponds two DPWM levels to one ADC level.

Numerically, assuming the maximum ripples do not exceed 1% of the output voltage (the design specification considered for the design example) and  $V_{ref}$  to be 80% of  $V_{max}$ , the minimum resolution required by the ADC is 7 bits. The quantization step  $q_{v,ADC}$  for the error signal ranging from  $-1$  to  $+1$  (ADC's dynamic range), thus, is calculated to be  $2/2^7 = 0.0156$ . The  $n_{DPWM}$  is, then, 8 bits. ADC and DPWM gains, being dependent on their resolutions, computed through  $K_{ADC} = 2^{n_{ADC}}$  and  $K_{DPWM} = 1/(2^{n_{DPWM}} - 1)$  respectively, are calculated to be 128 and 1/255, respectively.

## 6. Redesigning and Optimizing the Digital Controller

In order to compensate all the additionally incorporated effects in the digital control loop due to the inclusion of delay and ADC and DAC gains, the digital controller has to be resigned. More specifically, the controller has to be redesigned for the modified plant described by

$$G_p(s) = e^{-st_d} \cdot G_{vd}(s) \cdot K_{ADC} \cdot K_{DPWM} \quad (45)$$

Following the same procedure as described above, a three-pole two-zero (complex)-based digital controller (instead of using all the controllers for saving space) for the modified plant  $G_p(s)$  is given by

$$G_c(z) = \frac{14.1z^3 - 11.68z^2 - 13.51z + 12.27}{z^3 + 0.4273z^2 - 0.9566z - 0.4707} \quad (46)$$

On the optimization of this digital controller through the nonlinear least squares method, somewhat deviated coefficients are observed this time. The optimized digital controller for the modified plant comes out to be

$$G_c(z) = \frac{16.7824z^3 - 25.6728z^2 + 9.2157z - 0.0464}{0.3731z^3 + 0.0796z^2 - 0.4081z - 0.0446} \quad (47)$$

Once the algorithm is run, as can be seen from Figure 13, with the progression of iterations, the residual decreases monotonically, thus ensuring the better set-point tracking. This certifies the fine-tuning of the digital controller coefficients by the NLS method. The algorithm stops when the final change in the sum of squares relative to its initial value is less than the default value of the function tolerance.

Iteration	Func-count	Residual	First-Order optimality	Lambda	Norm of step
0	9	2.70497	1.36	0.01	
1	18	2.64974	1.77	0.001	1.13346
2	27	2.15315	0.62	0.0001	2.02207
Objective function returned Inf; trying a new point...					
3	40	2.05369	0.119	1	0.125325
4	49	2.04254	0.0346	0.1	0.0593508
5	58	2.0164	0.0543	0.01	0.35283
6	68	1.99511	0.0211	0.1	0.287836
7	77	1.98067	0.0255	0.01	0.254616
8	87	1.96967	0.0163	0.1	0.22126
9	96	1.96163	0.0141	0.01	0.191628
10	105	1.9481	0.237	0.001	0.776357
11	114	1.94266	0.0707	0.0001	0.303732
12	123	1.94106	0.0513	1e-05	2.26269
13	132	1.93611	0.0903	1e-06	9.5579
14	141	1.93189	0.0659	1e-07	15.879
15	150	1.93123	0.00263	1e-08	0.379977
16	159	1.93123	1.13e-05	1e-09	0.0874944

Figure 13. Iterative process offered by the nonlinear least squares (NLS) method.

## 7. Additional Numerical Simulations

For the sake of investigating the effectiveness of the proposed optimized digital controllers, some additional simulation results for the digital control loop incorporating the delay and ADC and DAC gains using the MATLAB/Simulink environment are presented. A solver of the fixed-step type is used. The loop delay is considered to be half the switching period. ADC and DPWM gains are set to 128 and 0.0039, respectively. The step response offered by the three-pole two-zero (complex)-based unoptimized and optimized digital controllers described in Equations (46) and (47), respectively, for the modified plant described in Equation (45) is shown in Figure 14.

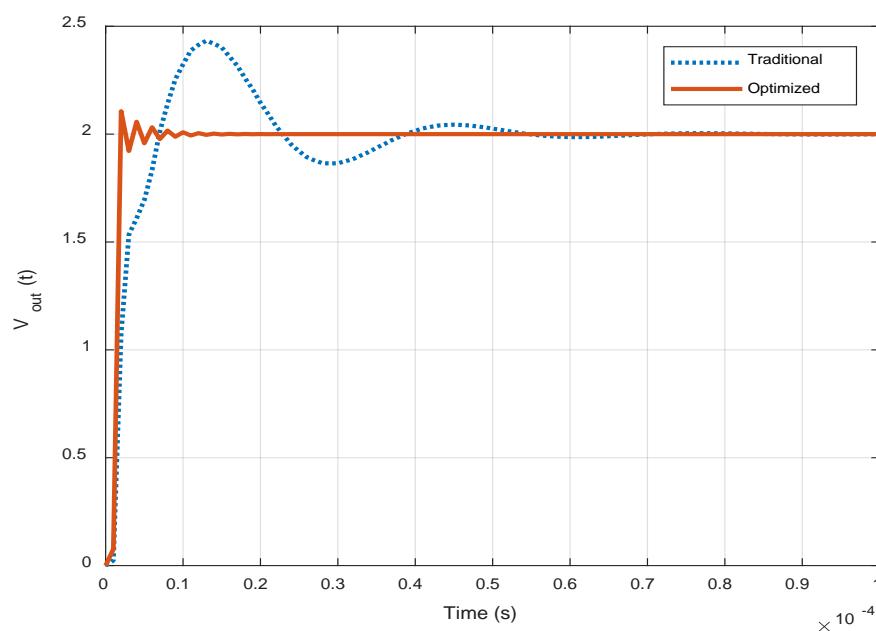


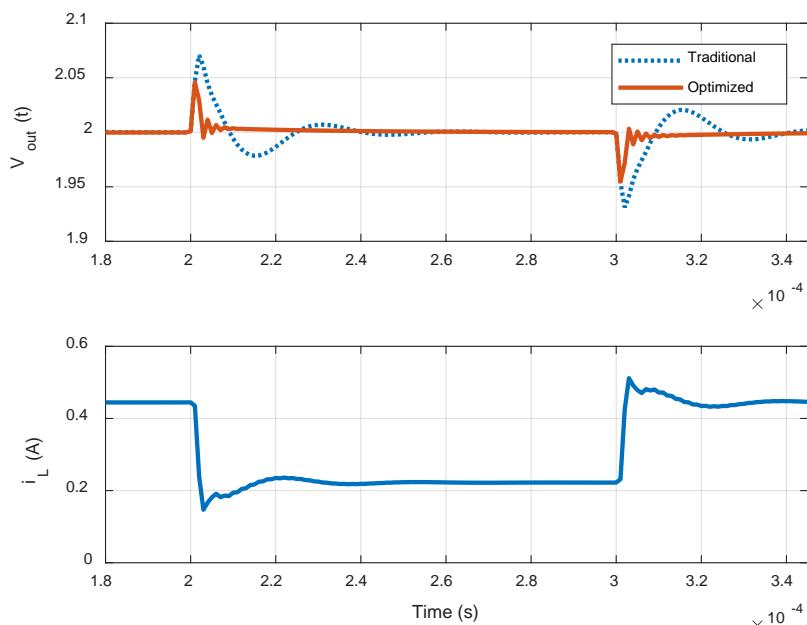
Figure 14. Controllers' output voltage response.

From the step response offered by the controllers, it is depicted that the optimized controller offers better static performance characteristics as compared to its unoptimized form (see Table 4).

**Table 4.** Comparison of performance characteristics.

Performance Characteristics	Digital Controller	Optimized Digital Controller
Rise Time (s)	$4.5888 \times 10^{-6}$	$7.8825 \times 10^{-7}$
Settling Time (s)	$4.7043 \times 10^{-5}$	$5.0295 \times 10^{-6}$
Overshoot (%)	21.6457	5.3088
(First) Peak (V)	2.4329	2.1062
Peak Time (s)	$1.30 \times 10^{-5}$	$2.00 \times 10^{-6}$

In addition, at the time of transient, the response takes much less time to recover to its steady-state value with a controlled peak spike. For example, for a load current change of 0.44 A to 0.22 A and then from 0.22 A to 0.44 A, the optimized controller shows less recovery time as well as reduced voltage peak-to-peak spike with regard to its traditional form (see Figure 15). Simulation results reveal that the digital controllers are well-retuned by the NLS method and offer superior static and dynamic performance.

**Figure 15.** Response of the controllers against the changes in load current.

## 8. Rapid Hardware-in-the-Loop (HiL) Implementation

The Simulink plugged-in architecture-level design tool named Xilinx System Generator (XSG), for DSP from Xilinx, is employed for the implementation of a digital control algorithm on a high-speed, high-end, and high-density Basys 3 Artix-7 FPGA board after automatically generating portable, synthesizable, and vendor-neutral VHDL code. XSG automatically invokes both the Core Generator and ChipScope generator to construct the netlist and cores, and thus the configuration bitstream, once the target device/FPGA XC7A35T-1CPG236C from Xilinx, Inc. (an American technology company) and the compilation target (Hardware Co-Simulation JTAG) are set in its settings. High-level abstractions produced by a control design engineer in the Simulink model are translated into the low-level and executable VHDL code through the bitstream. FPGAs can be easily interfaced with Simulink through the XSG environment. This enables control design engineers to build sophisticated digital control algorithms quickly, with respect to the traditional Resistor-Transistor Logic (RTL) development times without having the knowledge of VHDL language, and then implement it on an FPGA, thus shortening the design and testing time.

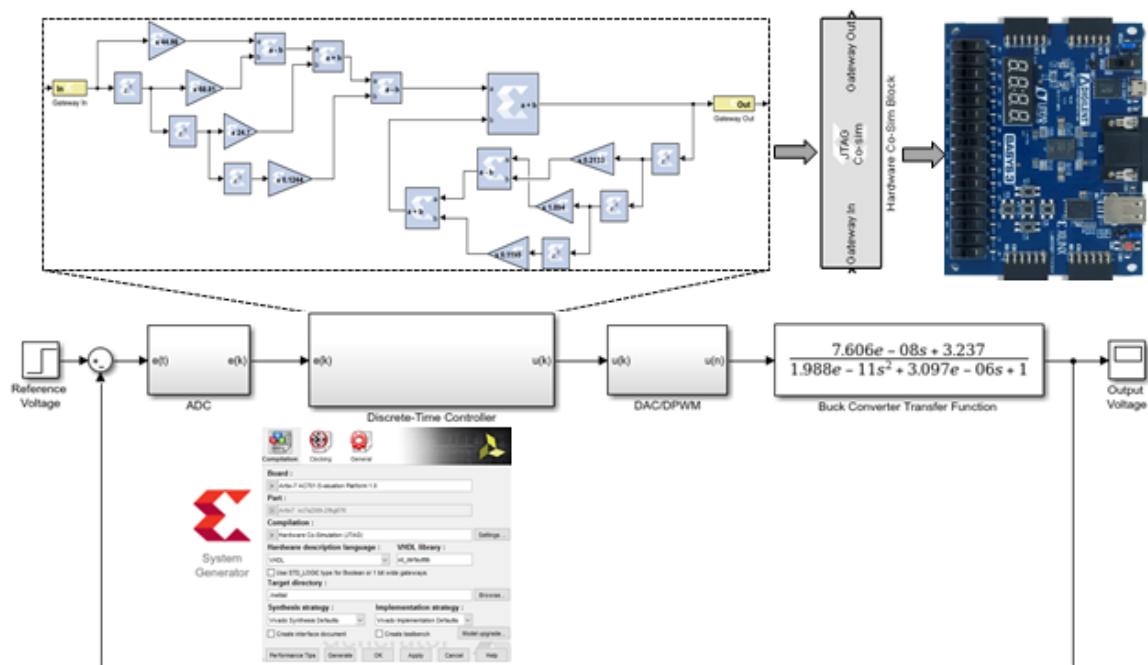
The optimized digital controller described in Equation (47) can be expressed equivalently in the standard form as follows:

$$G_c(z) = \frac{44.9810 - 68.8094z^{-1} + 24.7003z^{-2} - 0.1244z^{-3}}{1 + 0.2133z^{-1} - 1.0938z^{-2} - 0.1195z^{-3}} \quad (48)$$

Equation (48) can be translated into the difference equation through the inverse Z-transform as follows:

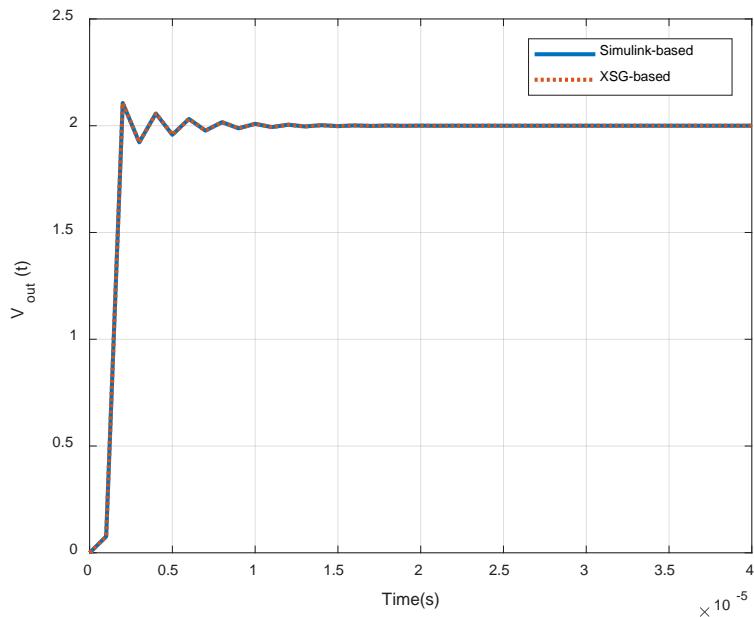
$$\begin{aligned} u(k) = & 44.9810e(k) - 68.8094e(k-1) + 24.7003e(k-2) - 0.1244e(k-3) - 0.2133u(k-1) \\ & + 1.0938u(k-2) + 0.1195u(k-3) \end{aligned} \quad (49)$$

The above controller difference equation realized using hardware-realizable blocks from the XSG library is shown in Figure 16. The controller coefficients are realized using a single precision floating-point data type characterized by the word lengths of 32 bits. A new hardware cosimulation library and thus a synthesizable block (which is to be downloaded into the Artix-7 board) are automatically generated (see Figure 16) on the successful generation of VHDL code. The JTAG cosimulation block is the equivalent representation of the previously used XSG simulation blocks, including the gateway-in and gateway-out blocks used for the realization of digital control algorithms. JTAG communication between a hardware platform (Artix-7 FPGA board) and Simulink (on PC) for a supported board is carried out for downloading the bitstream. In this way, a JTAG-based hardware cosimulation is performed by downloading the Vivado program-based generated bit file into the FPGA, thereby closing the loop.



**Figure 16.** Hardware-in-the-loop (HiL) implementation of the compensated buck converter system.

Careful analysis of the step response shown in Figure 17 depicts that the XSG-based compensated system displays almost the same performance as the Simulink-based compensated system. This is due to the fact that XSG uses the floating-point data format for the realization of controller coefficients, just like Simulink, which utilizes 'double' type data. Set time-steps for the hardware implementation, rounding and truncation errors, and the sampling issues associated with the digital systems may cause slight performance deterioration in the XSG-based system. The bit-true and cycle-true characteristic of the XSG makes the numerical simulations such as if they were attained through the real hardware implementation.



**Figure 17.** Output voltage response obtained through the Simulink and Xilinx System Generator (XSG)-based compensated system.

## 9. Conclusions

In this paper, optimization of the PZC technique-based digital controllers through the NLS method is performed to enhance the static and dynamic performance. In the proposed control methodology, which is essentially a digital redesign or emulation technique, the analog compensators with complex and real zeros designed on the basis of the PZC technique are mapped into the digital compensators by using a bilinear transformation technique with an appropriate sampling period. Discrete-time approximation of continuous-time controllers, even when accomplished through using the ‘best’ Tustin transformation, introduces frequency distortion. Although low analog frequencies are relatively well-mapped into the same digital frequencies, high frequencies result in highly nonlinear mapping. As a result, the performance of the digital controllers deteriorates. The coefficients of the digital controllers are retuned through the NLS optimization method to enhance their performance. There occur also opportunities for improvement in compensator performance, as the placing of the compensator’s real or complex zeros in the vicinity of the plant’s poles ensures only nominal performance. Numerical results reveal that NLS-based optimized digital controllers exhibit superior static and dynamic performance as compared to the conventional (unoptimized) digital controllers, thus validating the effectiveness of the NLS optimization method. When comparing their performance, the NLS method outshines metaheuristic techniques such as GA. Rapid HiL implementation of the compensated buck converter system is also successfully performed.

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