A Fixed-Frequency Sliding-Mode Controller for Fourth-Order Class-D Amplifier

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Abstract: Since the parasitic voltage ringing and switching power losses limit the operation of active devices at elevated frequencies; therefore, a higher-order inductor-capacitor (LC) filter is commonly used, which offers extended attenuation above the cutoff frequency and thus, improves the total harmonic distortion (THD) of the amplifier. This paper applies the concept of integral sliding-mode control to a fourth-order class-D amplifier. Two fixed-frequency double integral sliding-mode (FFDISM) controllers are proposed, where one uses the inductor current while the other involves the capacitor current feedback. Their equivalent control equations are derived, but from the realization viewpoint, the controller using the capacitor current feedback is advantageous and, therefore, is selected for final implementation. The performance of the proposed FFDISM controller for fourth-order GaN class-D amplifier is confirmed using simulation and experimental results.

1. Introduction

For decades, silicon transistors have dominated the power amplifiers industry due to the low-cost and well-established fabrication technology. Since the transistors in a linear power amplifier operate in the active region where power dissipation is significant, thereby they experience poor efficiency. In addition to advanced fabrication techniques like laterally diffused metal oxide semiconductor (LDMOS) [1,2], different control strategies such as Doherty's architecture and load-modulation were adopted to improve the efficiency of a linear amplifier [3]. Due to a narrow margin for improvement left in Si, the demand for high operating voltage, temperature and efficiency has enabled the trend towards wide band-gap (WBG) materials. The attractive features such as a high electric breakdown field, low thermal impedance, and saturated electron drift velocity, motivated their rapid substitution for Si counterparts [4]. Particularly, GaN high electron mobility transistor (HEMT) has become a potential candidate for large bandwidth and low-noise power amplifiers [5].

The earlier release of high-power GaN HEMT was a depletion-mode device also referred to as normally-on FET [6]. Since it requires additional control and protection circuitry for a safe power-up of power converters built with normally-on FETs, therefore, enhancement-mode FETs are preferred over depletion-type devices. There were several attempts made to fabricate a normally-off GaN HEMT, including a recessed gate structure [7], Si substrate with p-type GaN [8], and fluorine plasma treatment [9]. However, due to a low threshold and gate breakdown voltages, the proposed HEMTs are vulnerable to spurious turn-on and gate failure. Alternatively, to achieve a normally-off GaN HEMT, a cascode configuration has been proposed by combining the GaN HEMT with a low-voltage Si metal oxide semiconductor field effect transistor (MOSFET) [10]. Due to the low-cost leaded packages and superior characteristics, GaN cascode is a dominating power device and is preferred over the

enhancement-mode HEMTs [11]. They are commonly available in TO-220 package, which enables easy assembling of the heat-sink and does not need special equipment for soldering to printed circuit board (PCB).

The class-D amplifier motivated by its high-efficiency (ideally 100%) encodes the reference signal into a pulse-width modulation output using a switching power circuit, with pulse-width proportional to the amplitude of the reference signal [12]. Since the operation of active devices in either the cutoff or saturation region significantly reduces the power dissipation, therefore, the heat sink requirement relaxes. In the case of battery-powered devices, high efficiency means longer battery life. Thus, class-D amplifier is the ideal choice for miniaturized high-power amplification as compared to the class-A, class-B and class-AB. Today, in addition to the stereo system, class-D amplifiers are also used in a high-precision control application, including the wafer positioning system, magnetic resonance imaging (MRI), and power hardware-in-loop simulation (PHIL) [13,14].

An LC filter demodulates the output pulse-train by attenuating high-frequency content and produces the amplified output with minimum distortion. More LC stages are commonly added at the output of a class-D amplifier to meet the desired level of THD at a given switching frequency [15]. Low THD amplifier with high-power capability has applications in AC power sources and is used for the emulation of certain characteristics of an electrical system. However, the higher-order class-D amplifier causes an irregular-shaped frequency response due to multiple resonant frequencies in the uncompensated architecture [16]. Furthermore, the peaking at resonant frequency increases with an increase in load resistance and approaches zero-damping under the no-load condition. Therefore, it is required to have well-damped characteristics of a higher-order class-D amplifier, almost independent of load variations.

The feedback compensation of a class-D amplifier with a single LC stage is extensively investigated in the literature [17,18]. However, for the fourth-order system, the reported passive damping uses a low-valued resistor in series with filter capacitors to flatten the frequency response, at the cost of reduced efficiency [19]. Feedback controller supplemented with passive damping was adopted in Reference [20], which results in relatively lower power losses. In addition to an RL-branch between the capacitive filter of the first and inductive filter of the second LC stage, authors in Reference [21] proposed a multi-loop controller. Employment of such networks degrades the efficiency, which is the sole advantage of the class-D amplifier. Since passive damping negatively affects the efficiency of the amplifier, the application of high-cost GaN cascode becomes vestigial.

A purely feedback-controlled fourth-order class-D amplifier presented in Reference [22], achieved a peak efficiency of 87%. However, the controller was extremely complex as it requires feedback from all four state-variables. Feedback compensation using an integral sliding-mode (ISM) controller of the fourth-order class-D amplifier has been recently reported in Reference [23]. Nevertheless, it is inhibited for use due to the variable switching frequency nature of hysteretic modulation (HM) [24,25]. Therefore, a promising feedback controller with pulse-width modulation (PWM) is required, which ensures fixed switching frequency, flatter frequency response, reduced tracking error and a high-efficiency.

Since the equivalent control of a fixed-frequency sliding-mode controller is extracted from the sliding-surface by a differentiation operation [26]. Therefore, it is obvious to add a double integral term in the sliding-surface essential for ensuring reduced steady-state error [27,28]. However, the design of the sliding-surface becomes more challenging and would require tedious manipulations while deriving the equivalent control [29,30]. Moreover, due to a number of feedback signals, the resulting controller may not be practical. Thus, the FFDISM is proposed here, with two different control structures based on sliding-surfaces: One uses the inductor current while the other utilizes the capacitor current feedback to flatten the frequency response. The controller that offers high efficiency and realization using reduced opamp count is implemented for experimental verification.

The rest of this paper is organized as follows: Section 2 presents the mathematical model of the fourth-order class-D amplifier, which is an essential step for filter and controller design. Section 3 focuses on the derivation of the equivalent control for the two controllers where one uses the inductor

current while the other involves the capacitor current feedback. In Section 4, the circuit realization of the proposed controllers is discussed. Simulation and experimental results are given in Section 5, followed by conclusion in Section 6.

2. Modeling of Fourth-Order Class-D Amplifier

The role of the second LC stage is to improve the THD by reducing the residuals of switching harmonics [31]. It is important to investigate the effect of the additional LC stage on frequency response using average modeling, in order to ease the controller design process. Modeling of the power stage presented here neglects the non-idealities such as the forward voltage drop in the diode, conduction resistance of MOSFET and dead-time delay. Figure 1a,b shows the equivalent circuits during the two class-D operation modes determined by the control signals, i.e., u_H and u_L. These switching signals can attain the binary values; 1 and 0 for the on and off state of MOSFET respectively. For $u_H = 1$, the low-side GaN cascode S_L is in the off-state while the high-side S_H is in the conduction state, and the voltage v_s clamps to $V_{IN}/2$ as shown in Figure 1a. Similarly, for $u_H = 0$, voltage v_s clamps to $-V_{IN}/2$ as shown in Figure 1b. The dynamic equations of the converter for each switching state are expressed as

$$\begin{cases} L_A d\frac{di_{LA}}{dt} = d\frac{V_{IN}}{2} - v_A & \text{when} \quad u_H = 1 \\ L_A d\frac{di_{LA}}{dt} = -d\frac{V_{IN}}{2} - v_A & \text{when} \quad u_H = 0 \end{cases} \tag{1}$$

The subscript "A" and "B" depict parameters of the first and second LC stage. Thus, L_A, i_{LA}, and v_A are the inductance of the first LC stage, the current through L_A, and the voltage across C_A respectively. V_{IN} is the source, and v_o is the output voltage. The average-model of the class-D amplifier, by combining (1) using duty cycle $d_H = \text{avg}(u_H)$ is expressed as

$$\begin{aligned} L_A \frac{di_{LA}}{dt} &= \frac{V_{IN}}{2}(2d_H - 1) - v_A \\ C_A \frac{dv_A}{dt} &= i_{LA} - i_{LB} \\ L_B \frac{di_{LB}}{dt} &= v_A - v_B \\ C_B \frac{dv_B}{dt} &= i_{LB} - \frac{v_B}{R} \end{aligned} \tag{2}$$

where L_B, i_{LB}, and v_B are the inductance of the second LC stage, the current through L_B, and the voltage across C_B, respectively, and the load resistance is denoted by R. The dynamics of the class-D amplifier may also be written in state-space form as

$$\dot{x} = f(x,t) + g(x,u,t) \tag{3}$$

where x is the state vector, and f and g are functions of the state vector explicitly given in (4).

$$\begin{cases} x = \begin{bmatrix} i_{LA} & v_A & i_{LB} & v_B \end{bmatrix}^T \\ f(.) = \begin{bmatrix} 0 & \frac{-1}{L_A} & 0 & 0 \\ \frac{1}{C_A} & 0 & \frac{-1}{C_A} & 0 \\ 0 & \frac{1}{L_B} & 0 & \frac{-1}{L_B} \\ 0 & 0 & \frac{1}{C_B} & \frac{1}{RC_B} \end{bmatrix}, g(.) = \begin{bmatrix} \frac{V_{IN}}{2L}(2d_H - 1) & 0 & 0 & 0 \end{bmatrix}^T \end{cases} \tag{4}$$

The open-loop transfer function from v_S to output voltage v_o can be deduced from (4) as:

$$\frac{v_o(s)}{v_S(s)} = \frac{R}{s^4 L_A L_B C_A C_B R + s^3 L_A L_B C_A + s^2(L_A C_A + L_B C_B + L_A C_B)R + s(L_A + L_B) + R} \tag{5}$$
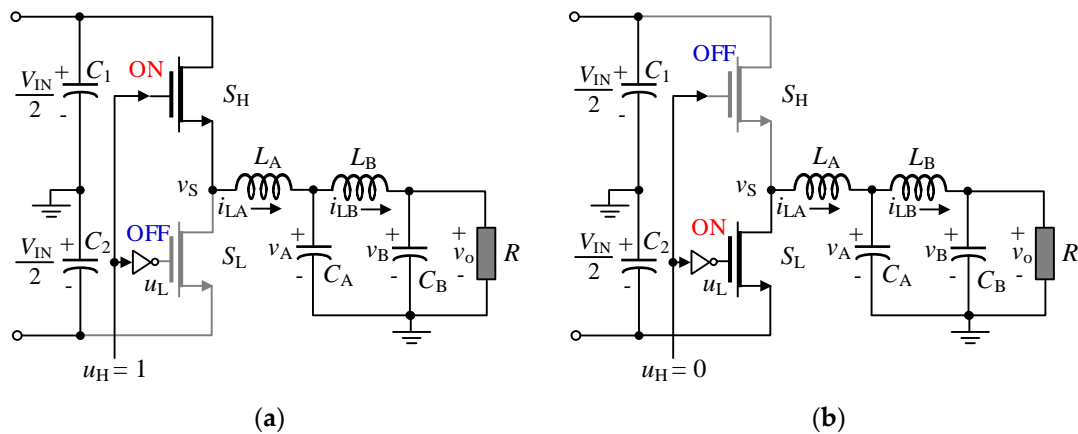
Figure 1. Equivalent circuits of fourth-order GaN class-D amplifier when (**a**) $u_H = 1$ (**b**) $u_H = 0$.

Figure 2 shows the frequency response of the fourth-order class-D amplifier in an open-loop configuration. Using the filter values set (i) in Table 1 results in resonant frequencies at 14 kHz and 51 kHz, as shown in Figure 2a. The two frequencies are somewhat close to each other as the relations between the inductances and capacitances of the two stages are $L_A = 2L_B$ and $C_B = 2C_A$ respectively. The frequency response is repeated in Figure 2b using the filter values from the set (ii) in Table 1, resulting in resonant frequencies at 14 kHz and 114 kHz. It indicates that the first resonant frequency is independent of L_B and merely depends on L_A, C_A, and C_B. Moreover, the separation between the two frequencies determines the damping of the second resonance. The second frequency can be displaced adequately by using an appropriate integer multiplier $n \geq 2$ such that $L_A = nL_B$ [9]. It is also noted that the resonant peaking increases with the load resistance and approaches zero-damping under a no-load condition.
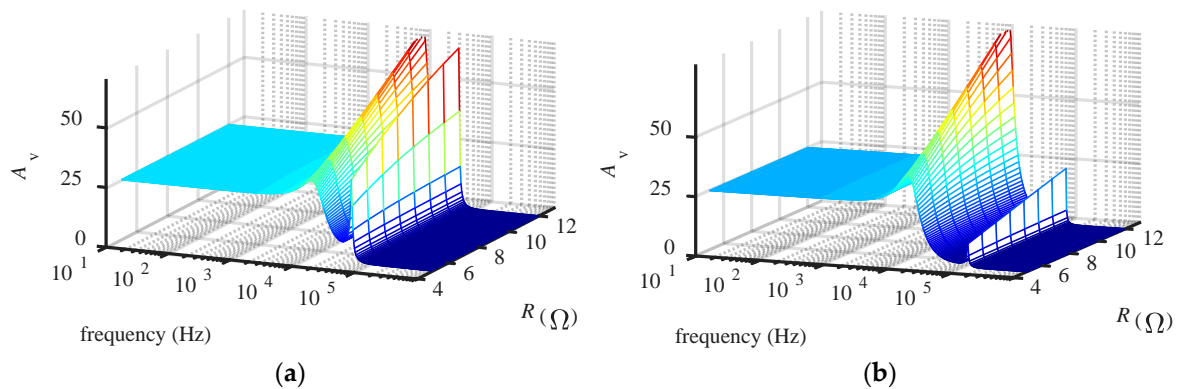

Figure 2. Open-loop frequency response of GaN class-D amplifier with fourth-order filter using (**a**) value set-i in Table 1 and (**b**) value set-ii in Table 1.

Table 1. Parameters of GaN class-D amplifier with fourth-order filter.

Parameter	Symbol	Value Set	
		i	**ii**
source voltage	V_{IN}	100 V	100 V
first stage filter	L_A, C_A	36 µH, 1 µF	36 µH, 1µF
second stage filter	L_B, C_B	18 µH, 2 µF	3 µH, 2 µF

To improve the frequency response of fourth-order GaN class-D amplifier, the FFDISM controller is proposed. Two different sliding-surfaces are proposed; each includes an extra current term (either inductor or capacitor current of the first LC stage) in addition to voltage error in the state variables.

The coefficients of the sliding-surfaces are determined using the stability condition. The controller using capacitor current is compared to the controller with an inductor current in terms of high-efficiency and ease of implementation. The simulation and experimental results are presented to verify the performance of the FFDISM controller using capacitor current feedback.

3. FFDISM Controller of Fourth-Order GaN Amplifier

The design starts by proposing a sliding-surface as a function of state-variables followed by the derivation of the equivalent control, and finally choosing the coefficients of the sliding-surfaces using stability condition [32,33]. Two different sliding-surfaces are proposed here; the first includes the inductor current feedback while the later employs capacitor current feedback.

3.1. Inductor Current Feedback

The state-variables for FFDISM controller are denoted by δ_1 and δ_2 and expressed as

$$\begin{cases} \delta_1 = \int e \, dt - \rho L_A i_{LA} \\ \delta_2 = \int \left\{ \left(\int e \, dt \right) - \rho L_A i_{LA} \right\} dt \end{cases} \tag{6}$$

where e is the voltage error between reference signal v_{ref} and scaled down output voltage βv_o, i_{LA} is inductor current feedback, ρ and β are scaling factors. Differentiating the set of equations in (6), substituting from (4) gives:

$$\begin{cases} \dot{\delta}_1 = (v_{\text{ref}} - \beta v_o) - \rho \left(\frac{V_{\text{IN}}}{2} m - v_A \right) \\ \dot{\delta}_2 = \int \left(v_{ref} - \beta v_o \right) dt - \rho L_A i_{LA} \end{cases} \tag{7}$$

where $m = 2d_{\text{H}} - 1$ is the modulation signal.

The sliding-surface is proposed as the weighted sum of δ_1 and δ_2 and expressed as

$$S_1 = \gamma_1 \delta_1 + \gamma_2 \delta_2 \tag{8}$$

where the weights γ_1 and γ_2 are sliding coefficients. By differentiating the sliding-surface in (8), using (4), and finally solving $\dot{S}_1 = 0$ for m_{equ} gives the equivalent control [34] as

$$m_{\text{equ}} \left(\frac{\beta V_{\text{IN}}}{2} \right) = -\left(L_A \frac{\gamma_2 \beta}{\gamma_1} \right) i_{LA} + \beta v_A + \left(\frac{\beta}{\rho} \right)(v_{\text{ref}} - \beta v_o) + \left(\frac{\gamma_2 \beta}{\gamma_1 \rho} \right) \int \left(v_{ref} - \beta v_o \right) dt \tag{9}$$

where the equivalent control is bounded as $|m_{\text{equ}}| \leq 1$. By further manipulation, the equivalent control signal as a function of controller gains can be expressed as

$$m_{\text{equ}} \left(\frac{\beta V_{\text{IN}}}{2} \right) = v_m = -\alpha_1 i_{LA} + \beta v_A + \alpha_2 (v_{\text{ref}} - \beta v_o) + \alpha_3 \int \left(v_{ref} - \beta v_o \right) dt \tag{10}$$

where

$$\alpha_1 = \left(L_A \frac{\gamma_2 \beta}{\gamma_1} \right), \alpha_2 = \left(\frac{\beta}{\rho} \right), \alpha_3 = \left(\frac{\gamma_2 \beta}{\gamma_1 \rho} \right) \tag{11}$$

The gains α_1, α_2, and α_3 derived using the necessary existence and stability condition determines the controller performance. The selected range of gains using existence condition determines the region where state trajectory will always be directed to the sliding-surface. By satisfying the Lyapunov condition $\dot{S}_1 \times S_1 < 0$, gives the existence condition:

$$\begin{cases} \beta \left(\frac{V_{\text{IN}} - 2v_A}{2} \right) > -\alpha_1 i_{LA} + \alpha_2 (v_{\text{ref}} - \beta v_o) + \alpha_3 \int \left(v_{ref} - \beta v_o \right) dt \\ \beta \left(\frac{V_{\text{IN}} + 2v_A}{2} \right) > \alpha_1 i_{LA} - \alpha_2 (v_{\text{ref}} - \beta v_o) - \alpha_3 \int \left(v_{ref} - \beta v_o \right) dt \end{cases} \tag{12}$$

The stability condition can be derived by substituting $\dot{S}_1 = 0$, which results in the following characteristic equation

$$\gamma_1 \dot{e}_1 + \gamma_2 \dot{e}_2 = 0$$
$$\Rightarrow \gamma_1 \dot{\delta}_1 + \gamma_2 \delta_1 = 0 \tag{13}$$

where the straightforward criterion $\gamma_2 / \gamma_1 > 0$ ensures the asymptotic stability. Therefore, the ratio of sliding coefficients is chosen as $\gamma_2 / \gamma_1 = 1.5\pi f_b$ where f_b is the natural frequency of the closed-loop system. Using $L_A = 33 \ \mu H$, $f_b = 10 \ kHz$ and $\beta = \rho$ in (11) gives the controller gains as:

$$\alpha_1 = \left(L_A \frac{\gamma_2 \beta}{\gamma_1} \right) = 0.067, \alpha_2 = \left(\frac{\beta}{\rho} \right) = 1, \alpha_3 = \left(\frac{\gamma_2 \beta}{\gamma_1 \rho} \right) = 47124 \tag{14}$$

3.2. Capacitor Current Feedback

The controller design procedure is repeated using a different sliding-surface which involves capacitor current i_{CA}. The state-variables for FFDISM controller are redefined as Δ_1 and Δ_2

$$\begin{cases} \Delta_1 = \int e \ dt - \sigma L_A i_{CA} \\ \Delta_2 = \int \left\{ (\int e \ dt) - \sigma L_A i_{CA} \right\} dt \end{cases} \tag{15}$$

where e is the voltage error between reference signal v_{ref} and scaled down output voltage βv_o, β and σ are scaling factors. Differentiating Equation (15) and substituting (4) gives

$$\begin{cases} \frac{d\Delta_1}{dt} = (v_{ref} - \beta v_o) - \sigma L_A \frac{d}{dt} (i_{LA} - i_{LB}) \\ \frac{d\Delta_2}{dt} = \int \left(v_{ref} - \beta v_o \right) dt - \sigma L_A i_{CA} \end{cases} \tag{16}$$

The sliding-surface for the FFDISM controller is defined as

$$S_2 = \varsigma_1 \Delta_1 + \varsigma_2 \Delta_2 \tag{17}$$

where ς_1 and ς_2 are sliding coefficients. The equivalent control [34] is obtained by differentiating the sliding-surface S_2, using (4) and finally solving $\dot{S}_2 = 0$ for equivalent control m_{equ}

$$m_{equ} \left(\frac{\beta V_{IN}}{2} \right) = -\left(L_A \frac{\varsigma_2 \beta}{\varsigma_1} \right) i_{CA} + \beta v_o + \frac{\beta L_A}{L_B} (\beta v_A - \beta v_o) + \left(\frac{\beta}{\sigma} \right) (v_{ref} - \beta v_o) + \left(\frac{\varsigma_2 \beta}{\varsigma_1 \sigma} \right) \int \left(v_{ref} - \beta v_o \right) dt \tag{18}$$

By further manipulation, the equivalent control signal as a function of controller gains can be expressed as

$$m_{equ} \left(\frac{\beta V_{IN}}{2} \right) = v_m = -\lambda_1 i_{CA} + \beta v_o + \lambda_2 (v_{ref} - \beta v_o) + \lambda_4 (\beta v_A - \beta v_o) + \lambda_3 \int \left(v_{ref} - \beta v_o \right) dt \tag{19}$$

where

$$\lambda_1 = \left(L_A \frac{\varsigma_2 \beta}{\varsigma_1} \right), \lambda_2 = \left(\frac{\beta}{\sigma} \right), \lambda_3 = \left(\frac{\varsigma_2 \beta}{\varsigma_1 \sigma} \right), \lambda_4 = \left(\frac{\beta L_A}{L_B} \right) \tag{20}$$

The controller gains λ_1, λ_2, λ_3, and λ_4 are derived using existence and stability conditions. Satisfying the Lyapunov condition $\dot{S}_2 \times S_2 < 0$, ensures the existence condition:

$$\begin{cases} \beta \left(\frac{V_{IN} - 2v_o}{2} \right) > -\lambda_1 i_{CA} + \lambda_2 (v_{ref} - \beta v_o) + \lambda_4 (\beta v_A - \beta v_o) + \lambda_3 \int \left(v_{ref} - \beta v_o \right) dt \\ \beta \left(\frac{V_{IN} + 2v_o}{2} \right) > \lambda_1 i_{LA} - \lambda_2 (v_{ref} - \beta v_o) - \lambda_4 (\beta v_A - \beta v_o) - \lambda_3 \int \left(v_{ref} - \beta v_o \right) dt \end{cases} \tag{21}$$

The stability condition can be derived using $\dot{S} = 0$, which gives the characteristic equation as

$$\varsigma_1 \frac{d\Delta_1}{dt} + \varsigma_2 \frac{d\Delta_2}{dt} = 0$$
$$\Rightarrow \varsigma_1 \frac{d\Delta_1}{dt} + \varsigma_2 \Delta_1 = 0 \tag{22}$$

The criterion $\varsigma_2/\varsigma_1 > 0$ ensures stability. Therefore, the ratio of sliding coefficients is chosen as ς_2/ς_1 = πf_b where f_b is the natural frequency of the closed-loop system. The controller parameters, using f_b = 10 kHz and $\beta = \sigma$ in (20), are given as:

$$\lambda_1 = \left(L_A \frac{\varsigma_2\beta}{\varsigma_1} \right) = 0.045, \lambda_2 = \left(\frac{\beta}{\sigma} \right) = 1, \lambda_3 = \left(\frac{\varsigma_2\beta}{\varsigma_1\sigma} \right) = 31416, \lambda_4 = \left(\frac{\beta L_A}{L_B} \right) = 0.08 \tag{23}$$

The two FFDISM configurations corresponding to sliding-surfaces S_1 and S_2 are implemented by translating their respective equivalent control equations to analog systems. The FFDISM controller implemented using (10) is shown in Figure 3a, where the difference between the scaled output voltage βv_o and reference signal v_{ref}, is applied to the proportional integral (PI-type) controller. In addition to v_o, it also requires feedback voltage v_A and current i_{LA} from the first LC stage. The closed-loop response is determined by the gains $\alpha_2 - \alpha_3$ and plays the important role of the error signal e processing. Similarly, Figure 3b shows the FFDISM controller involving the capacitor current i_{CA} feedback implemented using (19) where the gains $\lambda_1 - \lambda_4$ determine the response of the closed-loop system. It is observed that the FFDISM controller for fourth-order class-D amplifier requires more feedback variables, i.e., beside i_{LA} and i_{CA} the controller in Figure 3a,b respectively requires βv_A and $\beta(v_A - v_B)$. These additional variables make the circuit implementation more challenging. Therefore, it is important to select the controller that in addition to shaping the frequency response also offers ease of circuit implementation.
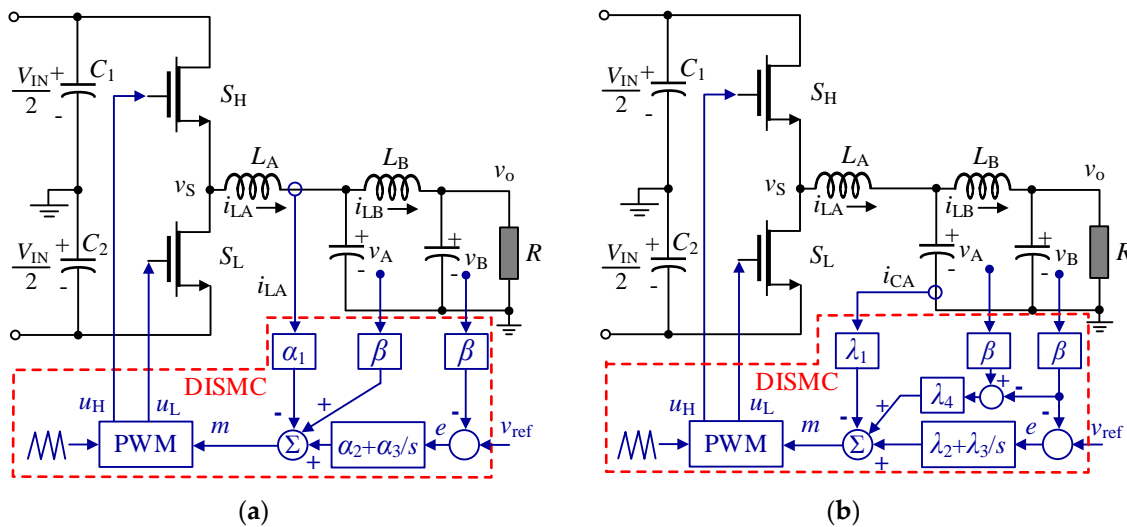

Figure 3. FFDISM controller of fourth-order class-D amplifier using (**a**) i_{LA} feedback (CNRL1) (**b**) i_{CA} feedback (CNRL2).

4. Realization of FFDISM Controller

High switching frequency necessitates the analog implementation of the controller using low-cost, single-supply opamps. Figures 4 and 5 show the circuit realization of FFDISM controllers for fourth-order GaN class-D amplifier, with additional i_{LA} and i_{CA} feedback respectively. For ease of reference, the controller involving inductor current and capacitor current is pointed as CNRL1 and CNRL2 respectively. Single-supply opamps are used due to its rail-to-rail input and low power consumption as compared to the dual-supply counterparts. The V_{cc} and V_b are opamps dc supply and mid-point bias voltage respectively. Here, both FFDISM designs are evaluated to find the one that offers ease of implementation, determined by the required number of opamps. The additional voltage feedback signals, i.e., v_A in CNRL1 and $\beta(v_A - v_B)$ in CNRL2 unanimously increases the opamp count.

However, dc-biasing of i_{LA} is required, which increases the opamp count in CNRL1 as compared to CNRL2.
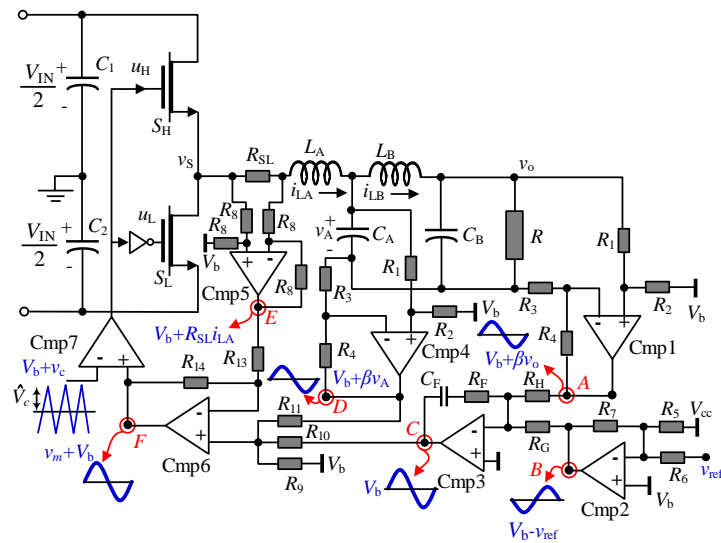

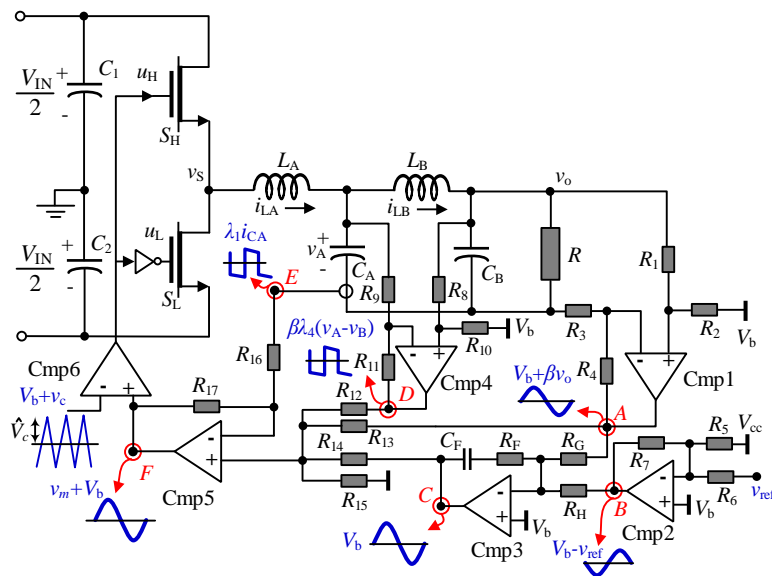**Figure 4.** Circuit realization of FFDISM controller with i_{LA} feedback (CNRL1).

Figure 5. Circuit realization of FFDISM controller with i_{CA} feedback (CNRL2).

Furthermore, the capacitor current i_{CA} in CNRL2 is bidirectional and therefore, can be sensed using a low-cost current transformer as there is no saturation problem. A sense resistor R_{SC} across the secondary of the current transformer converts the current signal into the voltage signal and adequately scales, i.e., $\lambda_1 = 0.01 R_{SC}$. This R_{SC} carries low-current and thus, does not affect the efficiency. On the other hand, the sense resistor for the inductor current i_{LA} feedback in CNRL1 can cause a significant reduction in overall efficiency. It is concluded that CNRL2 offers improvement in efficiency and requires fewer numbers of opamps as compared to CNRL1. Therefore, FFDISM controller using the capacitor current i_{CA} is finally implemented for experimental testing.

In Figure 5, the voltage at node *A* is the scaled and biased output voltage, with the scaling factor determined by the ratio $\beta = R_2/R_1 = R_4/R_3 = 4\ \text{k}\Omega/100\ \text{k}\Omega$. Meanwhile, Cmp2 inverts and adds bias V_b to v_{ref} as the waveform shows at node *B*, with the resistors $R_5 = R_6 = R_7 = 200\ \text{k}\Omega$. The opamp Cmp3 serves as a proportional integral (PI-type) controller, where capacitor C_F and resistors R_F, R_G,

and R_H together determine the proportional and integral gains as $\lambda_2 = R_F R_G$ and $\lambda_3 = 1/C_F R_G$. Since modulating signal is referenced to $V_b = +2.5$ V, the carrier signal is also biased to the same dc-level, where its peak, denoted as hat$\{V_c\}$ is given by $\beta V_{IN}/2 = 2$ V.

A prototype of the fourth-order GaN class-D amplifier has been built using the GaN cascode transistor, with the top and bottom sides shown in Figure 6a,b respectively. GaN cascode is realized by combining a low-voltage Si MOSFET with a high-voltage GaN HEMT to exhibit low-conduction and switching power losses. The TPH3006PD (Transphorm Inc., San Jose, CA, USA) available in TO-220 package is used to realize the power circuit. A conventional totem-pole gate driver with a low-valued gate resistance of 3 Ω is used to enable fast switching. The parasitic inductances of the package are high, which is responsible for drain voltage overshoot followed during turn-off transient. Therefore, an resistor-capacitor (RC) snubber across the low-side GaN cascode is used to suppress undesired oscillations. Three 150 μF electrolytic capacitors are connected in parallel to achieve high bus capacitance and reduce the effect of interconnection inductances.
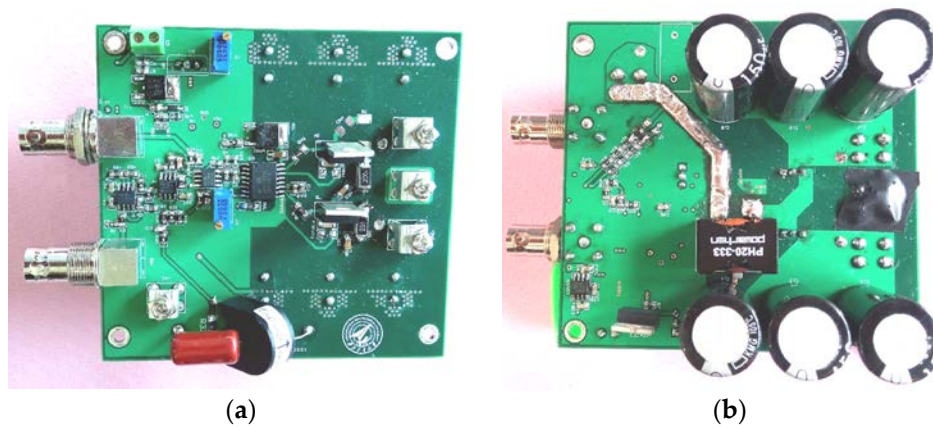

Figure 6. Prototype of GaN class-D amplifier (**a**) top-side (**b**) bottom side.

5. Results and Discussion

In this section, the performance of the proposed FFDISM controller is evaluated using simulation and experimental results. First, the frequency response and step response of the closed-loop system based on control diagram reduction are presented. This fundamental technique is useful to investigate the effect of the inner-loop on the compensation of resonance. Furthermore, computer–based circuit simulator i.e., Plexim Plecs is used to analyze the transient behavior of class-D amplifier using different resistive loads. Finally, experimental results are presented for validation of FFDISM controller.

5.1. Simulation Results

Figure 7a shows the multi-loop control diagram of the class-D amplifier, while the equivalent reduced form is shown in Figure 7b with the open-loop transfer functions H_o and G_o given in (24) and (25) respectively:

$$H_o = \frac{v_o(s)}{v_A(s)} = \frac{R}{s^2 L_B C_B R + s L_B + R} \tag{24}$$

$$\frac{v_A(s)}{v_S(s)} = \frac{v_A(s)}{v_o(s)} \times \frac{v_o(s)}{v_S(s)} = \frac{s^2 L_B C_B R + s L_B + R}{s^4 L_A L_B C_A C_B R + s^3 L_A L_B C_A + s^2 (L_A C_A + L_B C_B + L_A C_B) + s(L_A + L_B) + R} \tag{25}$$

where the parameters of the amplifier are given in Table 1 (value set i), selected using second-order Butterworth approximation. The feedback gains employed are $\lambda_4 = 0.08$ and $\beta = 0.04$. Figure 8a shows the frequency response of the closed-loop class-D amplifier using frequency sweep ranging from 10 Hz to 300 kHz. The frequency response of the FFDISM-controlled amplifier is presented to investigate the significance of the inner-loop for different values of the capacitor current gain λ_1. It is observed that the controller effectively mitigates the resonant peaks and promises a flatter frequency response,

almost independent of the load. Further, the proposed control strategy is verified by analyzing the step response in Figure 8b. The voltage overshoot and oscillations decrease with an increase in the capacitor current gain λ_1.
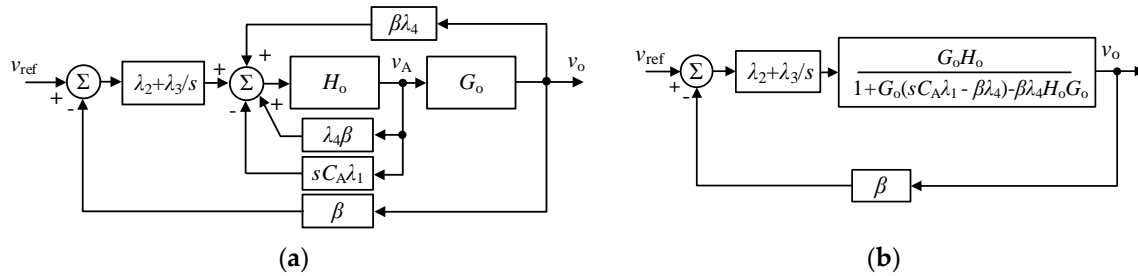

(a)　　　　　　　　　　　　　　　　　　　　　　　　　　(b)

Figure 7. Closed-loop schematic of the class-D amplifier: (**a**) multi-loop form (**b**) reduced form.

(a)　　　　　　　　　　　　　　　　　　　　　　　　　　(b)
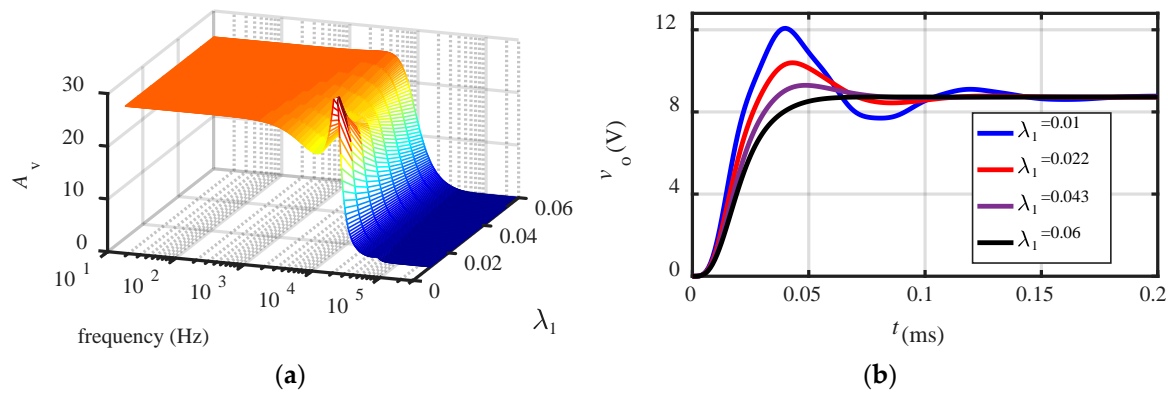
Figure 8. Effect of capacitor current i_C feedback on damping of fourth-order class-D amplifier (**a**) closed-loop frequency response for different λ_1 and (**b**) step response for different λ_1.

The transient response of fourth-order GaN class-D amplifier is analyzed using a circuit simulator, which offers a chance to evaluate the correctness of the proposed design. A close match to the experimental results can be obtained by adding the nonidealities to the simulation. Therefore, parasitic resistances of 500 mΩ and 200 mΩ are added to the filter inductors and capacitors, respectively. A sampling time of 1ns is used to capture the simulation results with adequate accuracy at a switching frequency of 100 kHz. Furthermore, a dead-time of 50 ns is introduced before every switching transition. Other factors such as delay in gate driver stage, jitters in PWM, finite rise and fall time of the gate signal are ignored; otherwise, the model takes a long time for solving.

The reference signal is a square wave of 1 kHz frequency, 50% duty cycle and 2 V peak-to-peak amplitude. Such a reference acts as a series of periodic step changes where the slew rate of the rising edge indicates the amplifier's bandwidth. Simulations are performed using the resistive load of 7 Ω and 14 Ω to observe the change in the voltage overshoot and the settling time with the load. Figure 9a indicates that the response of the open-loop GaN class-D amplifier is strongly dependent on the load, and the observed voltage overshoot and settling time are 9.34 V and 0.15 ms, respectively, for $R = 7\ \Omega$. By increasing the load resistance to 14 Ω, voltage overshoot and settling time rises to 13.25 V and 0.21 ms respectively. The FFDISM controller using inductor current is also simulated, and results are shown in Figure 9b. The improvement in response is observed using the controller gains derived in (11). Finally, the simulation results for GaN class-D amplifier with FFDISM using the capacitor current obtained under different loads are presented in Figure 9c. The proposed FFDISM controller reduces the voltage overshoot and steady-state error to 0.41 V and 0.3 V, respectively, thereby proving its superiority.
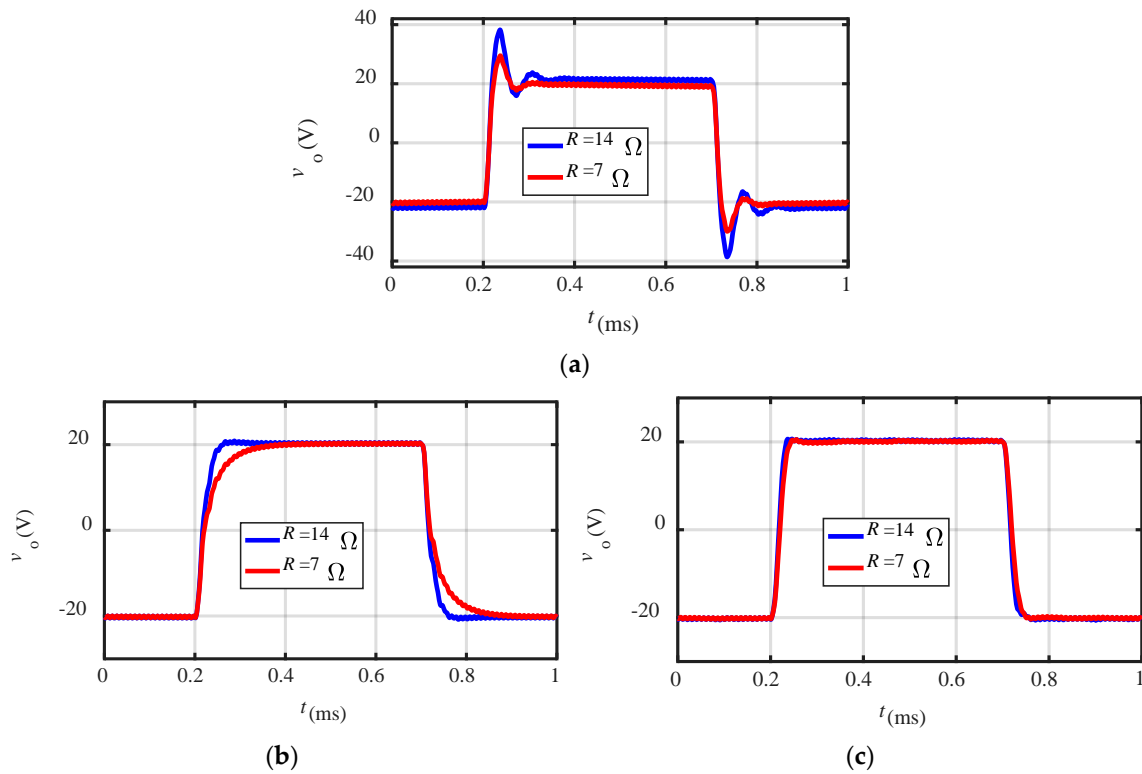
Figure 9. Simulation-based transient response of (**a**) open-loop GaN class-D amplifier; (**b**) FFDISM controller using inductor current; (**c**) FFDISM controller using capacitor current.

5.2. Experimental Results

For experimental validation, a prototype of fourth-order class-D amplifier was implemented on PCB using GaN, available in TO-220 package. Single-supply opamps were used to translate the equivalent control equation in (19) into the analog controller.

For measurement of the frequency response, sinusoidal reference signals (v_ref) of different frequencies ranging from 10 Hz to 50 kHz were applied using a signal generator, and the corresponding outputs were listed. The voltage gain (A_v) was computed for open and closed-loop configurations, as the ratio of the reference v_ref to output voltage v_o. Figure 10a shows the voltage gain plotted against the frequency of the reference signal when there is a 10 Ω resistive load. It is noted in open-loop (shown in blue), that the voltage gain at the 33 kHz resonant frequency is 29.3 which is successfully compensated by FFDISM controller as depicted in red.
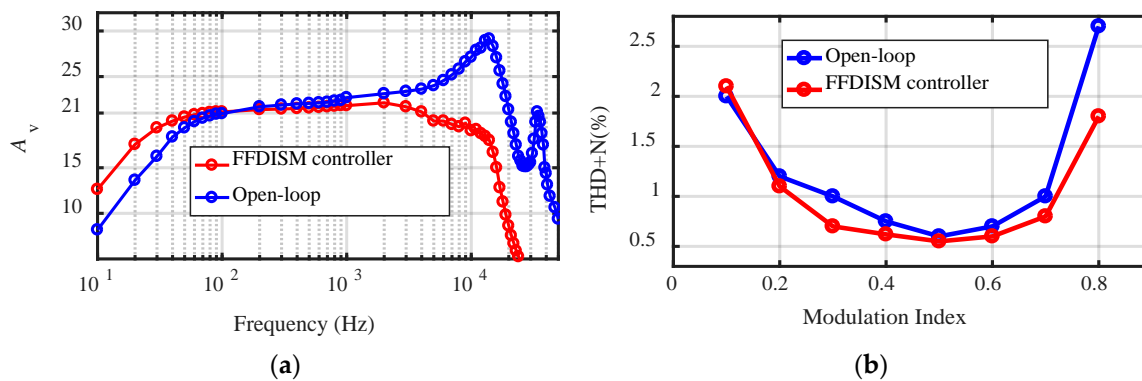

Figure 10. (**a**) Frequency response of the open-loop GaN class-D amplifier and with FFDISMC (**b**) THD+N the of open-loop GaN class-D amplifier and with FFDISMC.

Figure 10b shows the THD+N of GaN amplifier against the modulation index, defined as the ratio of the carrier to reference voltage and can range from 0 to 1. The output voltage v_o was recorded using the data-acquisition card at 5 MSa/s sampling frequency, and the fast Fourier transform (FFT) was used to extract THD+N. It was observed that FFDISM controlled fourth-order class-D amplifier achieved improved THD+N as compared to open-loop architecture.

Figure 11a shows the experimental transient response of open-loop GaN class-D amplifier to a reference square wave of 1 kHz frequency. It is found that with a load resistance of 10 Ω, the resonant frequencies result in voltage overshoot of 5.2 V. Similarly, the transient response with FFDISM controller to 1 kHz reference square wave is shown in Figure 11b, with a recorded overshoot of 1.3 V. Thus it is validated, that the proposed controller improves the transient response of the fourth-order class-D amplifier.
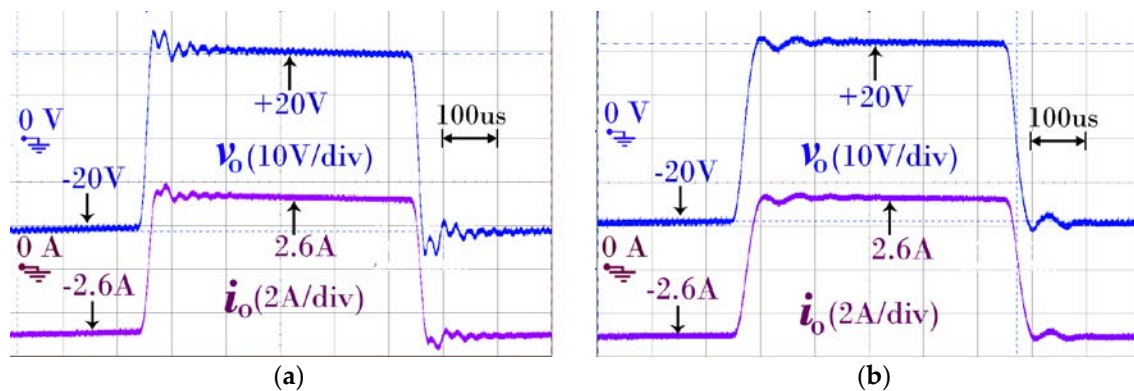

(**a**)   (**b**)

Figure 11. Experimental results transient response of: (**a**) open-loop GaN class-D amplifier; (**b**) GaN class-D amplifier with FFDISMC.

Furthermore, the scalogram analysis was performed, which illustrated a combined time and frequency-domain response of the amplifier. The wavelet transform was applied to represent the output voltage v_o as a weighted sum of the limited duration wavelet functions. Figure 12a shows the scalogram of the transient response in Figure 11a. A horizontal line in the figure represents a particular harmonic in the output waveform with its frequency on the y-axis and magnitude given on the color-bar. Since the square wave is a weighted sum of odd harmonics, the parallel lines below 16 kHz can synthesize it with adequate accuracy. Similarly, the line at 100 kHz is due to residual switching noise. There is a noticeable activity in the time interval 2–4 ms and 7–9 ms due to voltage ringing, corresponding to the resonant frequencies at 12.7 kHz and 33 kHz. Figure 12b shows the scalogram of the transient response in Figure 11b. The shrunken oval-shaped region and the reduction in magnitude noted on the color-bar verify the effectiveness of the FFDISM controller.

Finally, sinusoidal and triangular signals were generated using the FFDISM controlled GaN class-D amplifier. Figure 13a shows the 1 kHz sinusoidal output voltage v_o and the corresponding current i_o of the fourth-order amplifier. Similarly, for a 1 kHz triangular reference, output voltage v_o and current i_o are shown in Figure 13b. Thus, the effectiveness of the FFDISM controller, proposed for fourth-order class-D amplifier has been validated. Figure 14 illustrates the efficiency of GaN class-D amplifier at different operating powers. It is observed that at 150 W power, the amplifier achieves 93% efficiency. Moreover, the efficiency and bandwidth of the proposed class-D amplifier are compared in Table 2, against the hysteretic modulation-based implementation. It indicates that the class-D amplifier with PWM not only gets rid of the variable switching frequency but also improves the efficiency by reducing switching losses.
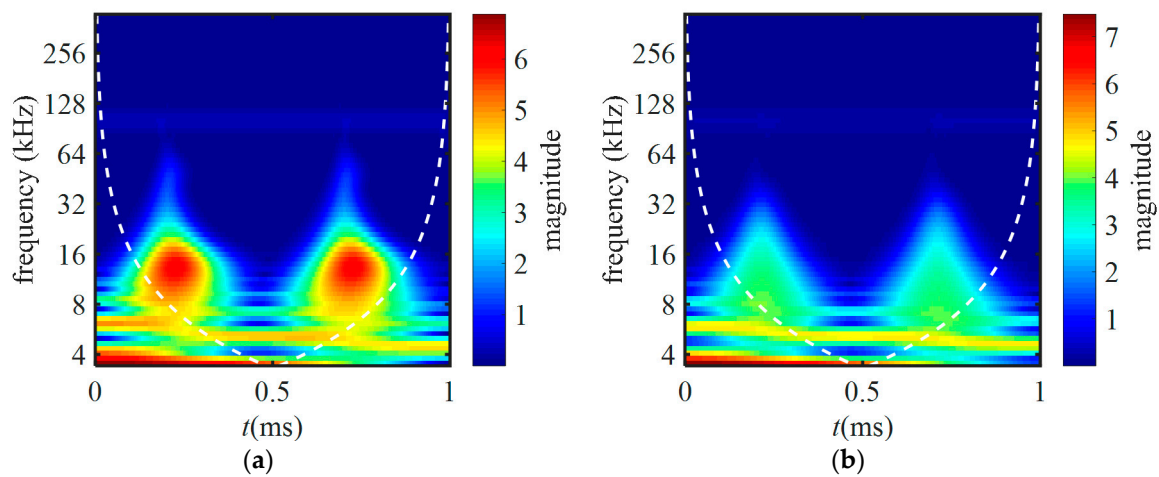
Figure 12. Experimental magnitude scalogram of GaN class-D amplifier: (**a**) open-loop; (**b**) with FFDISM controller.

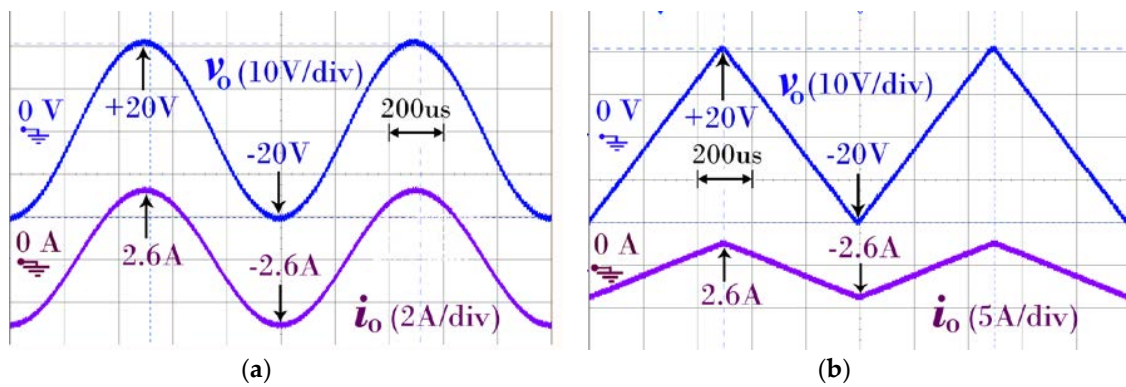**Figure 13.** (**a**) Experimental result of GaN class-D amplifier with FFDISM controller output voltage v_o and load current i_o and (**b**) output voltage v_o for reference sine wave v_{ref}.
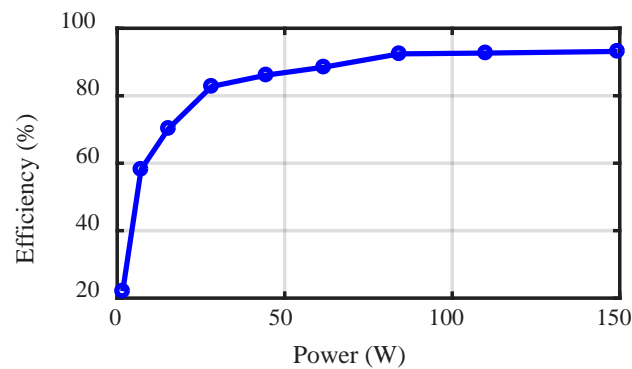

Figure 14. The efficiency of GaN class-D amplifier at different power.

Table 2. Comparative analysis of PWM and Hysteretic modulation based class-D amplifier.

Design	Modulation	Efficiency (%)	Bandwidth (kHz)
[20]	Hysteretic	81	4.6
[22]	Hysteretic	87	3.5
[35]	Hysteretic	84	5
This work	PWM	93.2	10

6. Conclusions

The FFDISM controller has been successfully applied to the GaN-based fourth-order class-D amplifier. The fourth-order filter has been used to improve the THD of class-D amplifiers, operating at a relatively lower switching frequency. Two different FFDISM structures were proposed using the inductor and capacitor current. The advantages offered by the FFDISM controller using the capacitor current over the counterpart using inductor current feedback are listed as: The bidirectional nature of the capacitor current demands a low-cost current-transformer for feedback; the current sense circuit does not affect the overall efficiency; and reduced opamp are required for circuit realization. A prototype of the amplifier was implemented on a PCB. The experimental results revealed that the proposed FFDISM controller effectively flattens the frequency response of the fourth-order amplifier, and results in THD and voltage overshoot of 0.6% and 1 V respectively.

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