Article

Comprehensive Sensing Current Analysis and Its Guideline for the Worst-Case Scenario of RRAM Read Operation

Zhensen Tang ¹ , Yao Wang ², Yaqing Chi ² and Liang Fang ^{1,*}

¹ Institute of Quantum Information and State Key Laboratory of High Performance Computing, College of Computer, National University of Defense Technology, Changsha 410073, China; zhensentang@nudt.edu.cn

² Institute of Microelectronics, College of Computer, National University of Defense Technology, Changsha 410073, China; wangyaobsz@nudt.edu.cn (Y.W.); yqchi@nudt.edu.cn (Y.C.)

* Correspondence: lfang@nudt.edu.cn; Tel.: +86-731-8457-3637

Received: 2 September 2018; Accepted: 28 September 2018; Published: 30 September 2018

Abstract: In this paper, the dependence of sensing currents on various device parameters is comprehensively studied by simulating the complete crossbar array rather than its equivalent analytical model. The worst-case scenario for read operation is strictly analyzed and defined in terms of selected location and data pattern, respectively, based on the effect of parasitic sneak paths and interconnection resistance. It is shown that the worst-case data pattern depends on the trade-off between the shunting effect of the parasitic sneak paths and the current injection effect of the parasitic sneak leakage, thus requiring specific analysis in practical simulations. In dealing with that, we propose a concept of the threshold array size incorporating the trade-off to define the parameter-dependent worst-case data pattern. This figure-of-merit provides guidelines for the worst-case scenario analysis of the crossbar array read operations.

Keywords: RRAM; crossbar array; read operation; sensing current; worst-case scenario

1. Introduction

Resistive switching random-access memory (RRAM) is considered one of the most promising candidates in developing next generation non-volatile memory technologies, in which memresistive devices with reproducible resistance switching between low resistance state (LRS) and high resistance state (HRS) serve as the memory cells [1–4]. For their simple metal-insulator-metal (MIM) sandwiched structure, compatible with CMOS technology, low-cost fabrication and ultra-high density can be accessible with crossbar array configurations [5–8].

Motivated by practical applications, the quantitative evaluation of the RRAM array write and read operations has been conducted extensively based on analytical models [9–11]. Since the RRAM array has inherent drawbacks, arising from parasitic sneak leakages [12] and interconnection resistances [13], the consequent numerous parasitic components make the situation extremely complicated for analytical models. Nevertheless, an extreme-case analysis method considering both the worst-case selected location and data patterns is usually employed in those studies. For write operation, the worst-case scenario is that the selected cell sees the smallest voltage across the memory cell when accessed. Thus, the selected cell is located at the furthest corner from the word-line (WL) and bit-line (BL) voltage sources and all of the unselected cells are in its LRS, as shown in Figure 1a. In this case, the voltage degradation caused by the interconnection resistances and parasitic sneak paths is the largest. However, for read operation, the worst-case scenario is much more controversial and has not been strictly defined. Although in most previous studies [9,11,14–16], the cell located at the furthest

corner from power lines is usually defined as the worst-case selected cell, a detailed and comprehensive analysis from the circuit's point of view is seldom given. On the other hand, the worst-case data pattern for read operation has been oversimplified in previous studies, or, if not, they mostly rely on instinctive assumption, irrespective of devices parameters, which relatively lack insightful description of circuits and mechanisms behind it. Leqi et al. assumed the leakage current on the bit-complement cells has a dominant impact on the sense amplifier, which senses the current on the selected BL [17]. In their analysis, the worst-case data pattern for reading LRS or HRS corresponds to the bit-complement cells being in HRS and LRS, respectively. This is based on the assumption that a certain portion of the sensing current is injected from the unselected WLs, ignoring the possibility of a reverse flow of sensing current into the unselected WLs (Figure 1b). Moreover, several previous studies simply took all memory cells in LRS except for the selected cell as the worst-case data pattern for reading LRS and HRS, which may underestimate the complication of the actual resistance status of the crossbar array. Therefore, a comprehensive analysis of the read operation considering the device and circuit interaction is essential for clarifying the discrepancy and inconsistency among all these studies.

Figure 1. (a) Schematic diagram of an $N \times N$ RRAM crossbar array; and (b) the two possible sneak current directions at bit-complement cells.

With a similar Gauss–Seidel numerical iteration method to that used in Ref. [18] to investigate the read scheme in crossbar array, in this work, we investigated a parameter-dependent sensing current analysis for passive RRAM array under the given bias condition. Without the aid of using a complex analytical approach or SPICE-based simulation, the dependence of the sensing current on various device parameters such as array size, memory resistance, interconnection resistance, and data patterns is comprehensively revealed by simulating the complete crossbar array.

The rest of this manuscript is organized as follows: Section 2 describes the details of the simulation setup. In Section 3, the experimental results are presented and analyzed. Finally, a conclusion follows in Section 4.

2. Experimental Details: Simulation Setup

The RRAM crossbar architecture is shown in Figure 1a. In this architecture, the resistance state of a selected cell is detected by applying a read voltage (V_{read}) to the selected WL, while the selected BL is grounded through a current-to-voltage converter, which acts as a current sense amplifier (SA). For simplicity, the SA and peripheral circuit are not covered in our consideration. A current-based definition of read margin is defined as: $RM = \frac{\Delta I}{I_{ref}} = \frac{I_{LRS,min} - I_{HRS,max}}{I_{LRS,min}} \times 100\% = (1 - \frac{I_{HRS,max}}{I_{LRS,min}}) \times 100\%$, which is a worst-case measure of the difference between the sensed LRS and HRS current levels. Due to the non-zero interconnection resistances and parasitic sneak leakages, the sensing current level is significantly affected by the combination effect of the selected location and data patterns. Thus, the worst-case scenario for read operation is the following: when reading a LRS memory cell,

the parasitic sneak paths and interconnection resistances degrade the output as much as possible; when reading a HRS memory cell, the parasitic components lower the output as little as possible.

To simulate the complete RRAM crossbar array, the current continuity at every memory junction is defined based on Kirchhoff's law as in Equations, as shown in Figure 2a, which can be derived by a set of node voltages for a given array data pattern and interconnection resistance, as in Equations (1) and (2). For each memory junction, there are two current continuity equations corresponding to WLs and BLs, respectively. Initially, the node voltage of all memory junctions is assumed to be $V_{read}/2$. Based on these initial values, voltage distribution along the WLs is calculated using Equation (3). Then, the voltage distribution along the BLs is calculated based on the updated junction voltages using Equation (4). This Gauss-Seidel iteration process is continued until the current continuity is verified by calculating the net current at every junction within the error range, i.e., the iteration converges. In this way, all node voltages can be solved based on these $2 \times N \times N$ voltage equations.

Figure 2. (a) Kirchhoff’s law at every memory junction in the crossbar array; and (b) parameters for simulation.

In this work, a variability-free approach is employed, i.e., all cells ($R_{(i,j)}$), either in LRS (R_{on}) or HRS (R_{off}), are identical from device to device. The default interconnection resistance (R_L) between two adjacent memory cells is fixed at $2.5\ \Omega$ for a $4F^2$ crossbar structure assuming a 22-nm technology node [9]. For simplicity, both LRS and HRS are assumed to be Ohmic, where R_{on} is defined to be $k \times R_L$, and R_{off} is defined to be $r \times R_{on}$. The k and r are the on-line resistance ratio and the on-off resistance ratio, respectively. Among the various voltage schemes suggested to perform the read operation, the GND read scheme with one-bit per cell operation was chosen as the model system for elucidating the concerns arising from the parasitic components because it has the most complex sneak paths. In this scheme, the selected WL is biased with the read voltage, while the selected BL is connected to the ground potential. In addition, all of the unselected WL and BLs are grounded. The simulation parameters, listed in Figure 2b, are comparable with the parameters adopted in Ref. [9,18]. These parameters are not intended to represent any particular devices, but instead are chosen to represent desired yet still reasonable RRAM crossbar arrays. Especially, our intent is to investigate how various device parameters affect the sensing current, and provide valuable insights into the worst-case scenario of the RRAM read operation.

$$\frac{V_{WL}(i,j) - V_{BL}(i,j)}{R_{(i,j)}} = \frac{V_{WL}(i,j-1) - V_{WL}(i,j)}{R_L} + \frac{V_{WL}(i,j+1) - V_{WL}(i,j)}{R_L} \quad (1)$$

$$\frac{V_{WL}(i,j) - V_{BL}(i,j)}{R_{(i,i)}} = \frac{V_{BL}(i,j-1) - V_{BL}(i,j)}{R_L} + \frac{V_{BL}(i,j+1) - V_{BL}(i,j)}{R_L} \quad (2)$$

$$V_{WL(i,j)} = \frac{R_{(i,j)} \cdot (V_{WL(i,j-1)} + V_{WL(i,j+1)})}{2R_{(i,j)} + R_L} + \frac{R_L \cdot V_{BL(i,j)}}{2R_{(i,j)} + R_L} \quad (3)$$

$$V_{BL(i,j)} = \frac{R_{(i,j)} \cdot (V_{BL(i,j-1)} + V_{BL(i,j+1)})}{2R_{(i,j)} + R_L} + \frac{R_L \cdot V_{WL(i,j)}}{2R_{(i,j)} + R_L} \quad (4)$$

3. Experimental Results and Discussion

3.1. Worst-Case Selected Location

As reported in previous studies, with finite interconnection resistance, the voltage and current delivered to the selected cell would differ depending on the location [19,20]. To evaluate the impact of the selected location on the readout current, the LRS/HRS read operations are performed across the whole crossbar array. For each cell operation, the selected device is in LRS or HRS, whereas the rest of the array is initialized with a random data pattern with an equal distribution for the LRS and HRS. The sensing current of reading LRS or HRS is calculated and illustrated in Figure 3a,b, respectively. One can clearly observe that the LRS sensing current (I_{LRS} , normalized by I_{on} , $I_{on} = V_{read}/R_{on}$) and HRS sensing current (I_{HRS} , normalized by I_{off} , $I_{off} = V_{read}/R_{off}$) are degraded in approaching the top-right corner, which is the furthest corner from the WL and BL voltage sources. During read operations, both the interconnection resistances and parasitic sneak paths would degrade the current delivered to cells further away from voltage sources. Since the array is uniformly distributed with the LRS and HRS, it is reasonable to consider that the data pattern has an equivalent impact on each cell across the whole crossbar array. Therefore, the sensing current variations are predominantly influenced by the interconnection resistances instead of parasitic sneak paths. The worst affected cell is that the selected cell located at the furthest corner from the WL and BL voltage sources. In this case, the current decay caused by the interconnection resistances is the largest, and all current between the selected WL and grounded WLs/BLs would effectively bypass the selected cell and choose shorter pathways throughout the array instead of injecting into the selected BL. In addition, to some extent, the interconnection resistances could help to make the very corner near the WL and BL voltage sources isolated from parasitic sneak paths in the rest of the array, while also making the worst affected corner less accessible.

On the other hand, the sensing margin ($(I_{LRS} - I_{HRS})$ normalized by I_{on}) of each bit is also degraded toward the furthest corner, as shown in Figure 3c. For the purpose of illustration, the average sensing current evolution along the topmost WL is simulated over 50 samples of random data pattern initializations, as shown in Figure 3d. Both I_{LRS} and I_{HRS} decrease with respect to the bit position. Compared to I_{HRS} , I_{LRS} decreases more rapidly, causing the sensing margin of each bit also degrading with respect to the bit position. This is because that the I_{LRS} is more sensitive to the current damping effect of the interconnection resistance. For a simple explanation, as shown in Figure 4, one may consider a series circuit consisting of one fixed resistor, the selected memory cell, whose resistance equals to LRS or HRS, and another variable resistor, the equivalent parasitic resistance connected in series with the selected memory cell in this case. These two serially connected resistors form a voltage divider. When a fixed voltage (V_{read}) is biased to the serially connected resistors, the current flowing through the circuit can be derived from the voltage drop across the memory cell. Assuming that the memory cell is in the HRS, almost all the bias is transferred to the memory cell due to the much higher resistance of the HRS compared with the series parasitic resistance. Even though the serially connected parasitic resistance increases as the selected cell locates further away from voltage sources, the decrease in the voltage drop across the selected cell is almost negligible, thus causing the current flowing through the circuit to decrease more slowly compared with that when the selected cell is in the LRS.

Figure 3. Bitmap of sensing current in 64×64 crossbar array with a uniform random data pattern (probability of 0.5 for LRS and HRS) showing: (a) I_{LRS} ; (b) I_{HRS} ; and (c) sensing margin varying with the location of the selected cell; and (d) the degradation of sensing margin along the topmost WL. Inset: The degradation of sensing currents along the topmost WL. The k and r are assumed to be 10^3 and 10, respectively.

Figure 4. The equivalent circuit for accessing $R_{1,j}$. $R_{sneak,eq}$ and $R_{L,eq}$ represent the equivalent parasitic resistances connected in parallel with $R_{1,j}$ and in series with $R_{1,j}$, respectively. $R_{1,j}$ and $R_{L,eq}$ form a voltage divider.

From the simulation results above, it can be concluded that the worst-case selected locations corresponding to the minimum I_{LRS} and maximum I_{HRS} occur at the furthest and closest corner from the WL and BL voltage sources, respectively. However, this would make the evaluation of the worst-case data patterns too complicated for the worst-selected cell of reading LRS and HRS occurring at two different locations. Particularly, a novel self-adjusting reference circuit utilizing the locality principle has been proposed for the passive RRAM crossbar array read operation, which can help to

relieve the requirement of a constant reference scheme [20]. In this case, the cell with a worst-degraded read margin will be a limiting factor for the peripheral sensing circuit design. Therefore, it is reasonable for us to define the cell located at the furthest corner from the power lines as the worst-case selected cell for read operation. This is also consistent with the practice in previous studies. In the following, the selected location is fixed to this bit cell.

3.2. Worst-Case Data Pattern

To evaluate the impact of data patterns on the sensing current, the whole crossbar array is divided into three regions, i.e., word-complement cells (R_I), bit-complement cells (R_{II}), and the rest of the array (R_{III}), as shown in different colors in Figure 1a. In most previous studies, cells in the same region are assumed to share the same resistance state, but they can be different from those in other regions. With this assumption, it is conceivable that eight extreme data patterns can be acquired, as shown in Figure 5. In this section, a data-dependent sensing current evaluation is performed with respect to the probability of LRS within the R_I (p_I), R_{II} (p_{II}), and R_{III} (p_{III}), respectively. The data probability of these three regions are individually controlled. According to the eight-extreme-data-pattern categories, each region (i.e., p_I) is investigated with the other two regions either in HRS or LRS (i.e., $p_{II} = p_{III} = 0$ or 1), as shown in Figure 5b. For each individual region, the data pattern is randomly generated for a given probability with an uniform distribution throughout the whole region. In this case, the LRS and HRS are randomly assigned and uniformly distributed in the individual region. Therefore, it is reasonable for us to assume that this statistical approximation can approximately reflect the average trend of the effect of data patterns on the sensing current. It is noted that such a statistical approximation approach has also been employed to estimate the array performance in the previous studies [14,21].

(a)	R_I	R_{II}	R_{III}	(b)	R_I	R_{II}	R_{III}
	HRS	HRS	HRS		HRS	HRS	LRS %
	HRS	HRS	LRS		HRS	LRS %	HRS
	HRS	LRS	HRS		LRS %	HRS	HRS
	LRS	HRS	HRS		LRS %	LRS	LRS
	HRS	LRS	LRS		LRS	LRS %	LRS
	LRS	HRS	LRS		LRS	LRS	LRS %
	LRS	LRS	HRS				
	LRS	LRS	LRS				

Figure 5. (a) The eight possible extreme data patterns based on the four-region division; and (b) the six data-dependent evaluations performed in this study.

First, we investigated the dependence of I_{LRS} and I_{HRS} on the data probability of each region (i.e., p_I) while keeping the remaining two regions in HRS (i.e., $p_{II} = p_{III} = 0$), as shown in Figure 6. With p_I and p_{II} increasing, the sensing current is significantly degraded, while p_{III} has almost negligible effects, slightly enhancing the sensing current. This result can be explained by the sneak paths involved during the read operation. The sneak paths are significantly affected by data patterns [21]. Figure 7 is the approximate model of the crossbar array to elucidate the roles of different regions in shaping the sneak paths. As shown in Figure 7a, a large number ($N - 1$) of complement cells are connected in parallel with the selected cell at the selected WL and BL, respectively; thus, the parasitic sneak paths are predominantly determined by R_I and R_{II} . Since all the unselected lines are grounded, as p_I and p_{II} increase, the current flowing along the selected WL and BL would be effectively shunted.

Figure 6. The I_{LRS} (a–c) and I_{HRS} (d–f) associated with data probabilities of three different crossbar array regions for different array sizes. The k and r are assumed to be 10^4 and 100, respectively.

Figure 7. Simple circuit model for elaborating the roles of different regions in shaping the reading current: (a) the shunting effect of R_I and R_{II} ; and (b) two sneak paths involved with the cells in R_{III} .

Ideally, the current flowing through the cells in R_{III} is supposed to be zero due to the symmetric bias on their WL and BL terminals. However, due to the non-zero interconnection resistance, the unselected WLs and BLs cannot be assumed to be sufficiently well grounded throughout their entire lengths, thus resulting in above ground voltages at the terminals of the unselected cells where the voltages are supposed to be zero. In this case, the cells in R_{III} that are not supposed to conduct sneak currents actually conduct a slight sneak current, and they can be treated as resistors connected with the unselected lines in series. For example, as shown in Figure 7b, two sneak paths serially

connected with the cell of R_3 in R_{III} , marked as (i) and (ii), respectively, can be conceivable. For the sneak path (i), we can get the Equation (5):

$$V_A = \frac{r_2}{R_1 + R_3 + r_1 + r_2} \cdot V_{word}. \quad (5)$$

As the resistance of R_3 decreases from HRS to LRS, the node voltage of V_A will increase, as a result of which the sneak current of $I_{(ii)}$ will be suppressed. For the sneak path (ii), we can get the Equation (6):

$$V_B = \frac{r_4}{R_2 + R_3 + r_3 + r_4} \cdot V_{bit}. \quad (6)$$

Similarly, as the resistance of R_3 decreases from HRS to LRS, the node voltage of V_B will increase, which will also hinder the sneak current of $I_{(i)}$ in return. Therefore, as p_{III} increases, the equivalent resistance of R_{III} with $(N-1)(N-1)$ cells connected in parallel would decrease rapidly, thus facilitating the rising of the node voltages at the WL terminals of the bit-complement cells (R_{II}) and the BL terminals of the word-complement cells (R_I), respectively, hindering the shunting effect of the complement cells. Moreover, when the node voltages at the WL terminals of the bit-complement cells are above those of their BL terminals, extra sneak currents would be injected into the selected BL.

Figure 8 shows the simulated I_{LRS} associated with different array sizes, data probabilities, k , and r for the three different crossbar array regions (the data for I_{HRS} exhibit the same trends and are not shown here). The sensed current decreases as the crossbar array size increases because this change leads to a larger current degradation along the selected WL and BL. As k and r decrease, the current degradation is more obvious. This effect can be explained from the fact that decreasing the value of LRS and on-off resistance ratio decreases the memory cell resistance, which is detrimental for mitigating the parasitic sneak leakage and lowering the current decay caused by the interconnection resistances. It is also worth noting that the sensing current decreases as p_I and p_{II} increase but slightly increases as p_{III} increases.

Figure 8. The I_{LRS} associated with different array sizes, data probabilities, k , and r for three different crossbar array regions: (a) R_I ; (b) R_{II} ; and (c) R_{III} .

To verify the validity of the above analysis, we also investigated the dependence of the sensed I_{LRS} and I_{HRS} on the data probability of each group (i.e., p_I) while keeping the other two groups in

LRS (i.e., $p_{II} = p_{III} = 1$) for various array sizes, as shown in Figure 9. For I_{LRS} , the data-dependence exhibits a similar trend as shown in the previous simulation. However, for I_{HRS} , the data-dependence shows much more complicated behavior. When the crossbar array size is small, the sensing current degrades as p_I and p_{II} increase, but slightly increases as p_{III} increases. On the other hand, when the array size is larger, the sensing current would be enhanced as p_I , p_{II} , and p_{III} increase. The simulated I_{HRS} associated with different array sizes, k , r , and data probabilities of R_I is shown in Figure 10 (the data associated with the data probabilities of R_{II} and R_{III} exhibit the same trends and are not shown here).

Figure 9. The I_{LRS} (a–c) and I_{HRS} (d–f) associated with data probabilities of three different crossbar array regions for different array sizes. The k and r are assumed to be 10^5 and 10, respectively.

The existence of two different data-dependences of I_{HRS} on p_I and p_{II} with respect to the array size is the result of two competing mechanisms arising from the memory cell resistance. On the one hand, a higher HRS can help to suppress parasitic sneak leakages. When the dependence of I_{HRS} on the data probability of R_I or R_{II} is investigated with the other two groups in HRS, the sneak currents injection into the selected BL is dominantly prohibited by the large value of HRS. The shunting effect of the unselected WLs/BLs prevails over the parasitic sneak currents injection. Hence, with the data probability increasing, the current would bypass the selected BL and choose shorter pathways throughout the crossbar array, as is previously shown in Figure 8. On the other hand, the small value of LRS is detrimental for suppressing parasitic sneak currents. When we investigate the dependence of I_{HRS} on the data probability of R_I or R_{II} with the rest two groups in LRS, the sneak currents injection into the selected BL could be prohibited by the interconnection resistances reluctantly within a small array size. In this case, as the data probability increases, the shunting effect of the corresponding complement cells would be enhanced, causing the sensing current degradation as well (Figure 10a, marked (i)). However, as the array size increases, the total resistance of the array decreases rapidly, which will make the current throughout the whole crossbar array significantly

improved. Large amounts of parasitic sneak currents would be injected into the selected BL inevitably as the data probability increases (Figure 10a, marked (ii)). As the array size continues to increase, the sneak currents injection would be damped and shunted by the interconnection resistances and shorter pathways (Figure 10a, marked (iii)).

Figure 10. The I_{HRS} associated with different array sizes, k , r , and data probabilities of R_I : (a) $r = 10$; (b) $r = 10^2$; (c) $r = 10^3$; (d) $k = 10^3$; (e) $k = 10^4$; (f) $k = 10^5$.

In addition, there are two other trends worth mentioning. Firstly, as k increases, the sneak currents injection into I_{HRS} tends to occur at a larger array size (Figure 10a–c). This is probably because, with a larger value of k at a specific value of r , the memory cell resistance is much larger as well. Thus, the total resistance of the crossbar array could only decrease at a larger size. Secondly, the effect of sneak currents injection is also dependent on r . The larger the value of r is, the smaller array size the sneak currents injection occurs at, and the more significantly the sneak currents would inject (Figure 10d–f). This is because that with a larger on–off ratio at a specific LRS, I_{HRS} is much more sensitive to the sneak currents injection. A threshold array size (N_{th}) for sneak currents tending to inject into I_{HRS} is roughly presented in Figure 11, which could be more accurately depicted with more detailed simulation parameters.

From the analysis above, we can conclude that I_{HRS} is dominantly determined by the trade-off between the shunting effect of sneak paths and the current injection effect of parasitic leakages. When the crossbar array size is small (e.g., $<N_{th}$), the shunting effect prevails. Thus, as the probability of HRS in R_I and R_{II} increases, large amounts of the current bypassing the selected BL and choosing the shorter pathways throughout the crossbar array would be prohibited. Due to the non-zero interconnection resistance, as the probability of LRS in R_{III} increases, the shunting effect would be slightly suppressed further. Therefore, the worst-case data pattern for HRS reading corresponds to all complement cells (R_I and R_{II}) being in HRS, and the remaining unselected cells (R_{III}) being in LRS. When the array size increases (e.g., $>N_{th}$), sneak currents would significantly inject into the selected BL, interfering with the shunting effect of parasitic sneak paths. As the probability of LRS increases in the whole crossbar array, the sensing current would be enhanced. Thus, the worst-case data pattern occurs when all unselected cells are in LRS.

For I_{LRS} , we notice that a similar trade-off occurs in our simulation as well, but manifests at a much larger threshold array size, which could be simply deduced by setting $r = 1$ in Figure 11, with the sensing current significantly degraded. Therefore, the current injection effect of the parasitic

leakage is almost negligible. It is reasonable for us to simply consider that I_{LRS} is dominantly interfered by the shunting effect of the parasitic sneak paths. In this case, the worst-case data pattern for LRS reading occurs when the complement cells (R_I and R_{II}) are in LRS, and the remaining unselected cells (R_{III}) are in HRS.

Figure 11. Threshold array size (N_{th}) associated with different k and r for the sneak current tending to inject into the sensed HRS current.

The overall discussion in this paper is based on the GND read scheme for its complicated parasitic sneak paths. However, the analysis method can also be employed to the other two read bias schemes, known as the V/2 and V/3 read schemes. In the V/2 scheme, all unselected WLs and BLs are biased at $V_{read}/2$. In the V/3 scheme, all unselected WLs are biased at $V_{read}/3$, while all unselected BLs are biased at $2V_{read}/3$. Since all of the unselected WLs and BLs are biased with voltage sources, the current throughout the whole crossbar array is eventually injected into the selected BL. Thus, all the unselected cells can be regarded as part of the parasitic sneak paths in parallel with the selected cell. Therefore, the worst-case data pattern for V/2 and V/3 read schemes occurs in the following case: (i) when reading LRS, all unselected cells are in HRS; and (ii) when reading HRS, all unselected cells are in LRS.

4. Conclusions

In this paper, a comprehensive numerical analysis of the sensing current depending on various device parameters such as array size, memory resistance, interconnection resistance, and data probability in the passive RRAM crossbar array with the GND read scheme is presented. The worst-case scenario for read operation, including the worst-case selected location and worst-case data pattern was strictly analyzed based on a comprehensive evaluation of the effect of parasitic sneak paths and interconnection resistances. The worst-case selected location is the one that locates at the furthest corner from the WL and BL voltage source. As at this location, the read margin suffers the most degradation caused by the parasitic interconnection resistances. On the other hand, the worst-case data pattern is much more complicated and depends on the trade-off between the shunting effect of the parasitic sneak paths and the current injection effect of the parasitic leakage, which is associated with different array sizes, memory resistance, and interconnection resistance. A concept of threshold array size is suggested to define the parameter-dependent worst-case data pattern. The importance of the present work is that the analysis method presented in this paper provides guidelines and references for the accurate circuit analysis of the RRAM crossbar array in the future.

Author Contributions: Methodology, Z.T. and Y.C.; Formal Analysis, Z.T. and Y.W.; Investigation, Z.T. and Y.W.; Resources, Y.C. and L.F.; Data Curation, Z.T.; and Supervision, L.F.

Funding: This work was supported by the National Natural Science Foundation of China (Grant No. 61332003) and the National Core Electronic Device, High-end Generic Chips and Basic Software Project (Grant No. 2018ZX01029-103).

Acknowledgments: The authors would like to thank Zhiwei Li and Nuo Xu for helpful discussions.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

SPICE Simulation Program with Integrated Circuit Emphasis

References

1. Waser, R.; Aono, M. Nanoionics-based resistive switching memories. *Nat. Mater.* **2007**, *6*, 833–840. [[CrossRef](#)] [[PubMed](#)]
2. Strukov, D.B.; Snider, G.S.; Stewart, D.R.; Williams, R.S. The missing memristor found. *Nature* **2008**, *453*, 80–83. [[CrossRef](#)] [[PubMed](#)]
3. Lee, M.J.; Lee, C.B.; Lee, D.; Lee, S.R.; Chang, M.; Hur, J.H.; Kim, Y.B.; Kim, C.J.; Seo, D.H.; Seo, S. A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta₂O_(5-x)/TaO_(2-x) bilayer structures. *Nat. Mater.* **2011**, *10*, 625–630. [[CrossRef](#)] [[PubMed](#)]
4. Tang, Z.S.; Chi, Y.Q.; Fang, L.; Liu, R.L.; Yi, X. Resistive Switching Effect in Titanium Oxides. *J. Nanosci. Nanotechnol.* **2014**, *14*, 1494–1507. [[CrossRef](#)] [[PubMed](#)]
5. Strukov, D.B.; Williams, R.S. Four-dimensional address topology for circuits with stacked multilayer crossbar arrays. *Proc. Natl. Acad. Sci. USA* **2009**, *106*, 20155–20158. [[CrossRef](#)] [[PubMed](#)]
6. Kùgeler, C.; Meier, M.; Rosezin, R.; Gilles, S.; Waser, R. High density 3D memory architecture based on the resistive switching effect. *Solid-State Electron.* **2009**, *53*, 1287–1292. [[CrossRef](#)]
7. Yu, S.; Chen, H.Y.; Gao, B.; Kang, J.; Wong, H.S.P. HfOx-Based Vertical Resistive Switching Random Access Memory Suitable for Bit-Cost-Effective Three-Dimensional Cross-Point Architecture. *ACS Nano* **2013**, *7*, 2320–2325. [[CrossRef](#)] [[PubMed](#)]
8. Chen, H.Y.; Yu, S.; Gao, B.; Liu, R.; Jiang, Z.; Deng, Y.; Chen, B.; Kang, J.; Wong, H.S.P. Experimental study of plane electrode thickness scaling for 3D vertical resistive random access memory. *Nanotechnology* **2013**, *24*, 465201. [[CrossRef](#)] [[PubMed](#)]
9. Jiale, L.; Wong, H.S.P. Cross-Point Memory Array Without Cell Selectors—Device Characteristics and Data Storage Pattern Dependencies. *IEEE Trans. Electron Devices* **2010**, *57*, 2531–2538. [[CrossRef](#)]
10. Sungho, K.; Jiantao, Z.; Lu, W.D. Crossbar RRAM Arrays: Selector Device Requirements during Write Operation. *IEEE Trans. Electron Devices* **2014**, *61*, 2820–2826. [[CrossRef](#)]
11. Zhou, J.; Kim, K.H.; Lu, W. Crossbar RRAM Arrays: Selector Device Requirements During Read Operation. *IEEE Trans. Electron Devices* **2014**, *61*, 1369–1376. [[CrossRef](#)]
12. Flocke, A.; Noll, T.G. Fundamental analysis of resistive nano-crossbars for the use in hybrid Nano/CMOS-memory. In Proceedings of the 33rd European Solid State Circuits Conference, San Francisco, CA, USA, 11–15 February 2007; pp. 328–331. [[CrossRef](#)]
13. Liang, J.; Yeh, S.; Wong, S.S.; Wong, H.S.P. Effect of Wordline/Bitline Scaling on the Performance, Energy Consumption, and Reliability of Cross-Point Memory Array. *J. Emerg. Technol. Comput. Syst.* **2013**, *9*, 1–14. [[CrossRef](#)]
14. Vourkas, I.; Stathis, D.; Sirakoulis, G.C.; Hamdioui, S. Alternative Architectures Toward Reliable Memristive Crossbar Memories. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2016**, *24*, 206–217. [[CrossRef](#)]
15. Song, L.; Zhang, J.; Chen, A.; Wu, H.; Qian, H.; Yu, Z. An efficient method for evaluating RRAM crossbar array performance. *Solid-State Electron.* **2016**, *120*, 32–40. [[CrossRef](#)]
16. Gao, Y.; Kavehei, O.; Al-Sarawi, S.F.; Ranasinghe, D.C.; Abbott, D. Read operation performance of large selectorless cross-point array with self-rectifying memristive device. *Integr. VLSI J.* **2016**, *54*, 56–64. [[CrossRef](#)]

17. Zhang, L.; Cosemans, S.; Wouters, D.J.; Groeseneken, G.; Jurczak, M.; Govoreanu, B. One-Selector One-Resistor Cross-Point Array With Threshold Switching Selector. *IEEE Trans. Electron Devices* **2015**, *62*, 3250–3257. [[CrossRef](#)]
18. Kim, S.; Kim, H.D.; Choi, S.J. Numerical study of read scheme in one-selector one-resistor crossbar array. *Solid-State Electron.* **2015**, *114*, 80–86. [[CrossRef](#)]
19. Chen, A. A Comprehensive Crossbar Array Model With Solutions for Line Resistance and Nonlinear Device Characteristics. *IEEE Trans. Electron Devices* **2013**, *60*, 1318–1326. [[CrossRef](#)]
20. Mustafa, J.; Waser, R. A Novel Reference Scheme for Reading Passive Resistive Crossbar Memories. *IEEE Trans. Nanotechnol.* **2006**, *5*, 687–691. [[CrossRef](#)]
21. Sangho, S.; Kyungmin, K.; Kang, S.M.S. Data-Dependent Statistical Memory Model for Passive Array of Memristive Devices. *IEEE Trans. Circuits Syst. II Express Briefs* **2010**, *57*, 986–990. [[CrossRef](#)]

© 2018 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).