

## Article

# Effects of Gate-Length Scaling on Microwave MOSFET Performance

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**Abstract:** This paper focuses on the extraction of an accurate small-signal equivalent circuit for metal-oxide-semiconductor field-effect transistors (MOSFETs). An analytical modeling approach was developed and successfully validated through the comparison between measured and simulated scattering parameters. The extraction of the equivalent circuit elements allowed for the estimation of the intrinsic unity current-gain cutoff frequency, which is a crucial figure of merit for assessing the high-frequency performance. The experimental data show that the cutoff frequency of the tested devices exhibits a nearly ideal scaling behavior with decreasing gate length.

**Keywords:** equivalent circuit; gate length; MOSFET; microwave frequency; scattering parameter measurements

## 1. Introduction

The extraction of an accurate small-signal equivalent circuit is of great importance for evaluating microwave field-effect transistor (FET) performance. This is because the equivalent circuit provides a physically meaningful description of the physical device structure. Furthermore, the extraction of the circuit elements allows for the estimation of relevant figures of merit, such as the intrinsic unity current-gain cutoff frequency ( $f_T$ ). The determination of this figure of merit is essential to assess the potential of the device for high-frequency operation. Driven by the ever-growing demand for high-frequency applications, continuous efforts are being made to develop innovative materials and architectures (e.g., high-mobility III-V and Ge channels, high-k dielectrics, and multiple-gates) [1–5]. The intrinsic  $f_T$  is expected to remarkably increase with decreasing gate length and to be roughly independent of the gate width. Hence, a significant improvement of the high-frequency performance can be achieved with gate-length downscaling. Typically, the equivalent circuit is extracted from scattering ( $S$ -) parameters, which can be straightforwardly and accurately measured with a vector network analyzer. To accomplish this goal, several numerical optimization [6–9] and analytical [10–16] procedures have been proposed in the last four decades. The numerical optimization approach can yield non-physical values of the circuit elements, by which the results can critically depend on the initial element values, local minima, and the optimization technique itself. These drawbacks can be overcome by adopting the analytical approach that is based on first extracting the extrinsic bias-independent elements, then de-embedding their contributions with simple matrix manipulations, and finally calculating the intrinsic bias-dependent elements from the intrinsic admittance ( $Y$ -) parameters. The determination and subsequent de-embedding of the extrinsic elements is essential to access the performance of the intrinsic FET that is not directly measurable, since the intrinsic section of the FET is experimentally inaccessible. The extrinsic elements are usually determined using “cold”  $S$ -parameter measurements ( $V_{DS} = 0$  V, i.e., passive device) [10–16], passive test structures [13–17], and full-wave

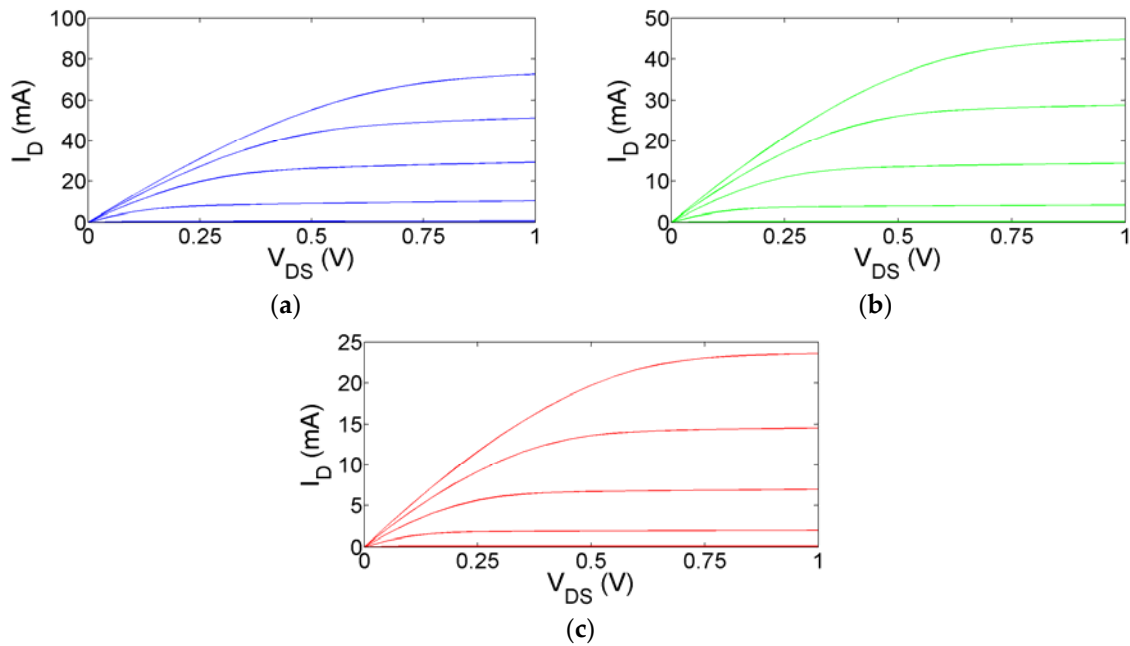
electromagnetic simulations [18–21]. In practice, the “cold” approach is the most used, since it does not require additional dummy structures or detailed information about the FET layout.

The present study aims to develop an analytical modeling technique to determine a small-signal equivalent circuit for three metal-oxide-semiconductor field-effect transistors (MOSFETs) with different gate lengths. In particular, the extrinsic capacitances are obtained from  $S$ -parameters measured on an open structure, whereas the extrinsic resistances and inductances are determined from “cold”  $S$ -parameter measurements. The open structure is used to extract the extrinsic capacitances, since the standard “cold” approach does not allow distinguishing clearly between extrinsic and intrinsic output capacitances [10,22]. The de-embedding of the extrinsic elements enables the calculation of the intrinsic elements, thereby allowing the estimation of  $f_T$  and the analysis of the impact of the gate-length scaling on this figure of merit. It is noteworthy that a lossy substrate resistance is included in the intrinsic model in order to obtain good agreement between the measured and simulated output reflection coefficient.

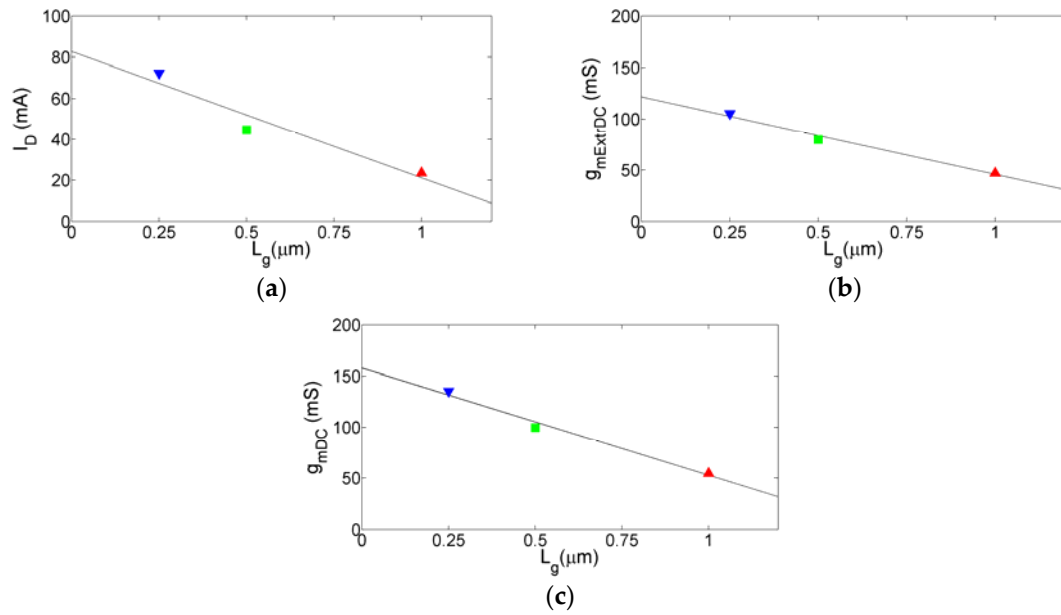
The remainder of this paper is structured as follows: the next section contains a description of the tested devices and of the proposed modeling technique, the subsequent section discusses the experimental results, and the last section summarizes the main conclusions of this study.

## 2. Model Extraction

The tested devices are three multi-cell, multi-finger MOSFETs with a gate width of  $192\ \mu\text{m}$  ( $W = 16 \times 4 \times 3$ ,  $8 \times 4 \times 6$ , and  $8 \times 4 \times 6\ \mu\text{m}$ ) and different gate lengths ( $L_g = 0.25$ ,  $0.5$ , and  $1\ \mu\text{m}$ ). The measured DC output characteristics are reported in Figure 1. As can be observed, a quite good scaling of the drain current is achieved. This is highlighted in Figure 2, showing that the drain current and transconductance increase roughly linearly with inverse gate length. Although the extrinsic contributions imply a reduction of the transconductance, both extrinsic and intrinsic transconductances ( $g_{m\text{ExtrDC}}$  and  $g_{m\text{DC}}$ ) exhibit good scaling. It should be underlined that the scaling of DC and RF properties are strongly correlated with each other, since RF performance strongly depends on the associated DC bias point.



**Figure 1.** DC output characteristics for three MOSFETs with different gate lengths: (a)  $0.25\ \mu\text{m}$ ; (b)  $0.5\ \mu\text{m}$ ; and (c)  $1\ \mu\text{m}$ .  $V_{GS}$  is varied from 0 to 1 V in steps of 0.2.



**Figure 2.** Behavior of (a)  $I_D$ ; (b)  $g_{mExtrDC}$ ; and (c)  $g_{mDC}$  versus gate length for three MOSFETs at  $V_{DS} = 1$  V and  $V_{GS} = 1$  V.

Figure 3 illustrates the small-signal equivalent circuit that is used to reproduce the measured S-parameters of the tested MOSFETs. This circuit can be divided into two main sections: the extrinsic and intrinsic parts. The extrinsic section is composed by eight bias-independent elements ( $C_{pg}$ ,  $C_{pd}$ ,  $L_g$ ,  $L_s$ ,  $L_d$ ,  $R_g$ ,  $R_s$ , and  $R_d$ ), while the intrinsic section consists of eight bias-dependent elements ( $C_{gs}$ ,  $C_{gd}$ ,  $C_{ds}$ ,  $R_{gs}$ ,  $R_{ds}$ ,  $R_{sub}$ ,  $g_m$ , and  $\tau$ ). In order to take into account the distributed effects, the extrinsic capacitances are split into two equal parts, placed outermost and innermost of the three extrinsic inductances. The extrinsic capacitances  $C_{pg}$  and  $C_{pd}$  are straightforwardly extracted from the imaginary parts of the Y-parameters of an open structure that has been fabricated on the same die of the same wafer of the tested MOSFETs. In general, the open structure can be represented with a pi network composed of three capacitances modeling the capacitive coupling between the pads. In most cases, as in the present one, the feedback capacitance can be disregarded, thereby allowing the determination of the input and output capacitances from the imaginary parts of  $Y_{11}$  and  $Y_{22}$ , respectively. As illustrated in Figure 4, the extrinsic capacitances are extracted by using the frequency range from 0.3 to 10 GHz. After removing the effects of  $C_{pg}$  and  $C_{pd}$ , the extrinsic resistances and inductances are, respectively, obtained from the real and imaginary parts of Z-parameters with  $V_{DS} = 0$  V and  $V_{GS} \gg V_{TH}$  by using the frequency range from 10 to 40 GHz. Under this bias condition, the intrinsic section of the MOSFET can be modeled through a distributed channel resistance and a distributed gate capacitance, leading to the following expressions of the Z-parameters [13]:

$$Z_{11} = R_g + R_s + \frac{R_{ch}}{3} + j\left(\omega L_g - \frac{1}{\omega C_g}\right) \quad (1)$$

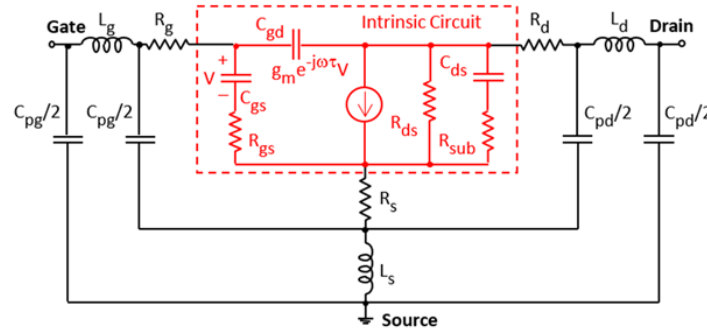
$$Z_{12} = Z_{21} = R_s + \frac{R_{ch}}{2} + j\omega L_s \quad (2)$$

$$Z_{22} = R_d + R_s + R_{ch} + j\omega(L_d + L_s) \quad (3)$$

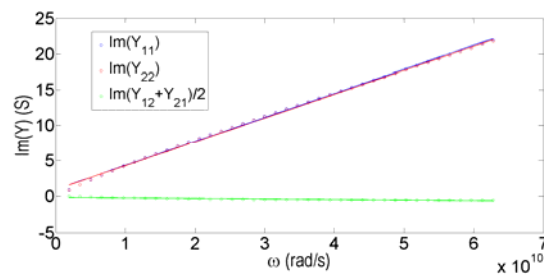
where  $C_g$  and  $R_{ch}$  are the gate capacitance and the channel resistance, respectively.

By assuming  $R_{ch}$  to be proportional to  $1/(V_{GS} - V_{TH})$  at “cold” condition [13], the extrinsic resistances can be straightforwardly determined from the intercept coefficients of the three linear regressions of  $Re(Z_{ij})$  versus  $1/(V_{GS} - V_{TH})$  (see Figure 5). In order to minimize the frequency dependence of  $Re(Z_{ij})$  associated with an incomplete capacitance de-embedding and/or intrinsic

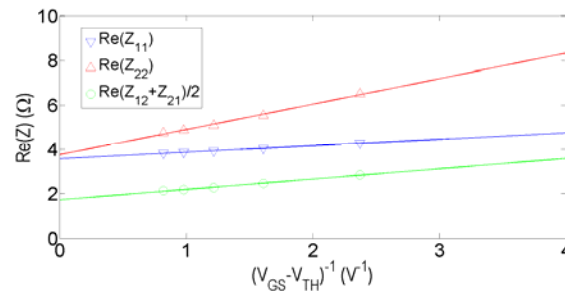
capacitive effects,  $Re(Z_{ij})$  is obtained at each gate voltage from the slope of the straight line approximating  $\omega^2 Re(Z_{ij})$  versus  $\omega^2$ . The extrinsic inductances are extracted from the slopes of the straight lines approximating  $\omega Im(Z_{ij})$  versus  $\omega^2$  (see Figure 6).



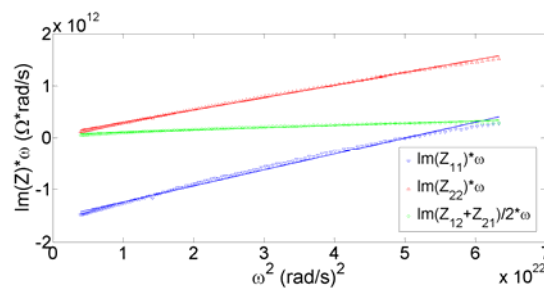
**Figure 3.** Small-signal equivalent circuit for the tested MOSFETs.



**Figure 4.** Behavior of  $Im(Y_{ij})$  versus  $\omega$  for the open structure. The extracted extrinsic capacitances are:  $C_{pg} = 338$  fF and  $C_{pd} = 335$  fF.



**Figure 5.** Behavior of  $Re(Z_{ij})$  versus  $1/(V_{GS} - V_{TH})$  for a MOSFET with a gate length of  $0.25 \mu\text{m}$  at  $V_{DS} = 0$  V. The extracted extrinsic resistances are:  $R_g = 1.9 \Omega$ ,  $R_s = 1.7 \Omega$ , and  $R_d = 2 \Omega$ .



**Figure 6.** Behavior of  $\omega Im(Z_{ij})$  versus  $\omega^2$  for a MOSFET with a gate length of  $0.25 \mu\text{m}$  at  $V_{DS} = 0$  V and  $V_{GS} = 1.4$  V. The extracted extrinsic inductances are:  $L_g = 26.6$  pH,  $L_s = 4.3$  pH, and  $L_d = 19.5$  pH.

After de-embedding all of the parasitic effects' elements by means of simple matrix operations, the intrinsic elements can be obtained from the intrinsic  $Y$ -parameters at each bias condition. It is worth noting that, analogously to what has been done for fin field-effect transistors (FinFETs) [14],  $R_{ds}$ ,  $C_{ds}$ , and  $R_{sub}$  are determined from the real and imaginary part of the intrinsic  $Y_{22} + Y_{12}$ . In particular,  $R_{ds}$  is calculated at low frequencies by treating the  $R_{sub}C_{ds}$  series network as an open circuit, and then its contribution is removed to enable the extraction of  $C_{ds}$  and  $R_{sub}$ :

$$R_{ds} = \frac{1}{\text{Re}(Y_{22} + Y_{12})} \quad (4)$$

$$Z_{ds} = (Y_{22} + Y_{12} - R_{ds}^{-1})^{-1} \quad (5)$$

$$R_{sub} = \text{Re}(Z_{ds}) \quad (6)$$

$$C_{ds} = -\frac{1}{\omega \text{Im}(Z_{ds})} \quad (7)$$

The introduction of  $R_{sub}$  does not affect the calculation of the intrinsic  $f_T$ , which is determined with the output short-circuited. The intrinsic unity current-gain cutoff frequency can be straightforwardly estimated from the intrinsic elements of the equivalent circuit as follows:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (8)$$

This equation shows that  $f_T$  is directly proportional to  $g_m$  and inversely proportional to the total gate capacitance  $C_{gg}$ , given by the sum of  $C_{gs}$  and  $C_{gd}$ . The capacitance  $C_{gg}$  should be directly proportional to both gate width and gate length, while the conductance  $g_m$  should be directly proportional to the gate width and inversely proportional to the gate length. As a result,  $f_T$  is expected to be inversely proportional to the square of the gate length and to be roughly independent of the gate width. However, deviations from this ideal behavior can be observed, due to non-ideal effects such as thermal phenomena and short channel effects. For example,  $f_T$  can be found to inversely scale with the gate length, due to saturation velocity in short channel devices. In such a case, the cutoff frequency can be used to estimate the saturation velocity as  $2\pi L_g f_T$ . Furthermore, under- and/or over-de-embedding of the extrinsic contributions may critically affect the results of the scaling analysis for the intrinsic section.

### 3. Model Validation and Discussion

The validity of the proposed technique is confirmed by the good agreement between the measured and simulated  $S$ -parameters. As an illustrative example, Figure 7 shows the comparison between the measured and simulated  $S$ -parameters from 0.3 to 40 GHz for the three tested devices at  $V_{GS} = 1$  V and  $V_{DS} = 1$  V. It should be highlighted that, by decreasing the gate length, the magnitude of the low-frequency forward transmission coefficient  $S_{21}$  increases, due to the improvement of the transconductance, and the starting point of output reflection coefficient  $S_{22}$  moves farther from the open circuit condition, due to the reduction of the drain-source resistance. This result can be easily explained by considering that, as the frequency tends to zero, the transconductance delay can be neglected and all inductors and capacitors can be, respectively, replaced with short and open circuits, and thereby  $S_{21}$  and  $S_{22}$  can be defined as follows [23]:

$$S_{21} = -2g_{m\text{Extr}}(R_0 / R_{ds\text{Extr}}) \quad (9)$$

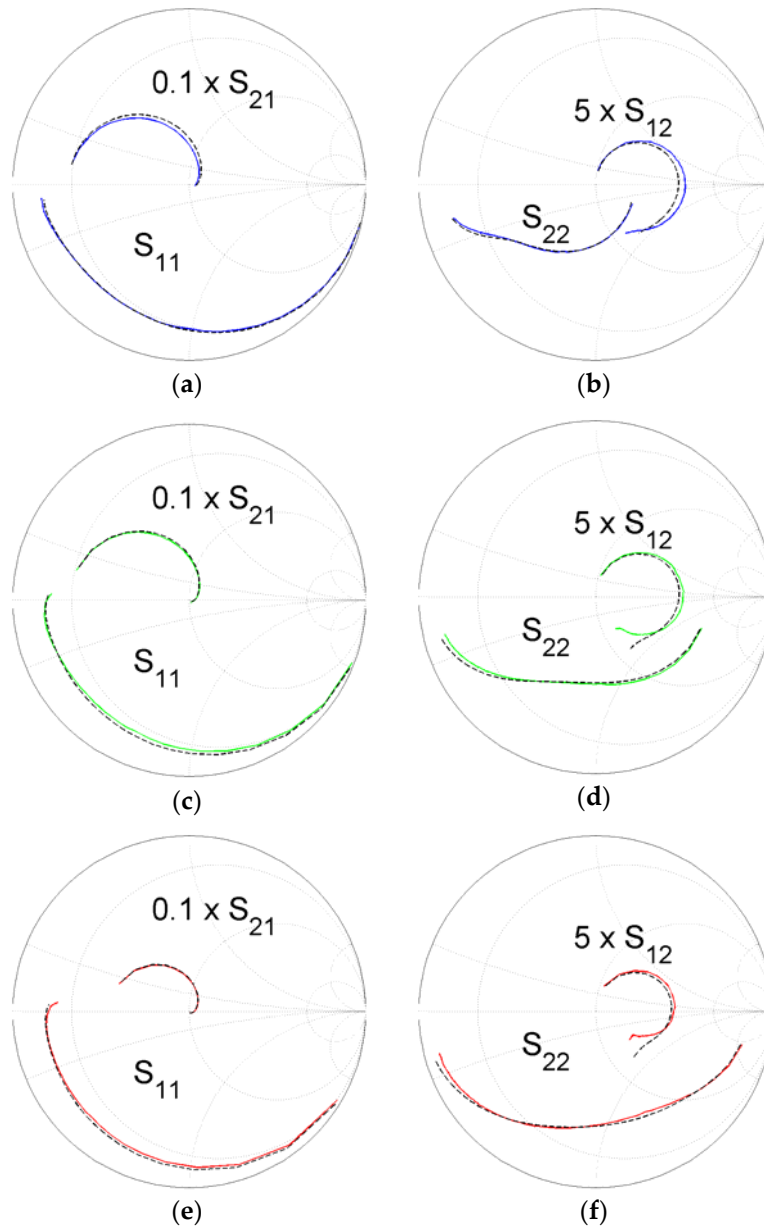
$$S_{22} = \frac{R_{ds\text{Extr}} - R_0}{R_{ds\text{Extr}} + R_0} \quad (10)$$

where  $R_0$  is the characteristic resistance (i.e., 50  $\Omega$ ), while  $g_{m\text{Extr}}$  and  $R_{ds\text{Extr}}$  represent the extrinsic transconductance and drain-source resistance:

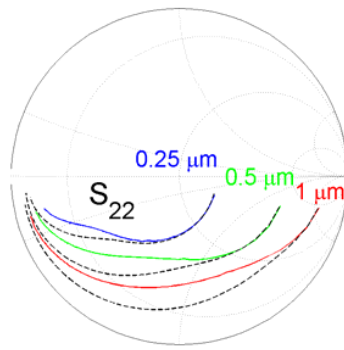
$$g_{mExtr} = \frac{g_m}{1 + g_m R_s + R_{ds}^{-1}(R_s + R_d)} \quad (11)$$

$$R_{dsExtr}^{-1} = \frac{g_{ds}}{1 + g_m R_s + R_{ds}^{-1}(R_s + R_d)} \quad (12)$$

To illustrate the necessity of including  $R_{sub}$  in the model, Figure 8 shows that the measured  $S_{22}$  is not accurately reproduced by disregarding  $R_{sub}$ . As a matter of fact,  $R_{sub}$  is required to add a resistive contribution in order to enhance the accuracy of the simulated  $S_{22}$ .

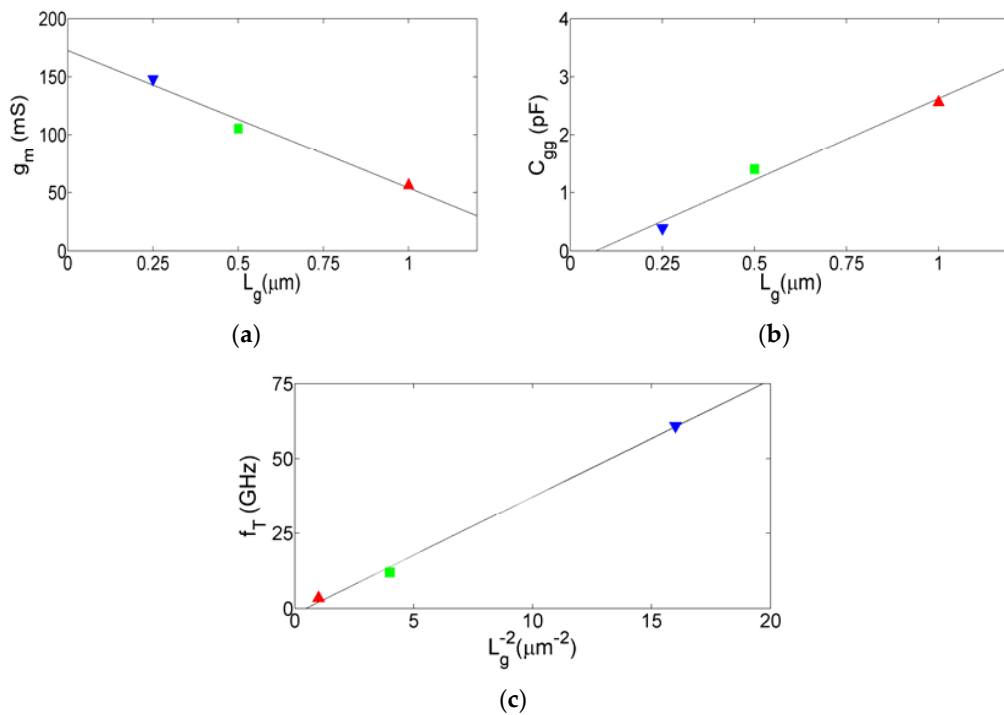


**Figure 7.** Measured (solid colored lines) and simulated (dashed black lines)  $S$ -parameters from 0.3 to 40 GHz at  $V_{DS} = 1$  V and  $V_{GS} = 1$  V for three MOSFETs with different gate lengths: (a,b)  $0.25 \mu\text{m}$ ; (c,d)  $0.5 \mu\text{m}$ ; and (e,f)  $1 \mu\text{m}$ .

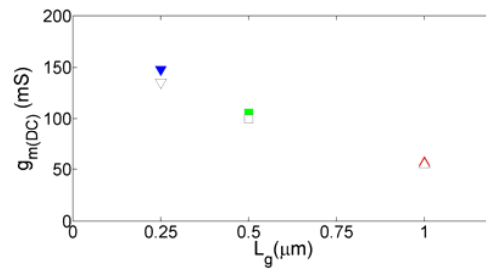


**Figure 8.** Measured (solid colored lines) and simulated (dashed black lines)  $S_{22}$  from 0.3 to 40 GHz at  $V_{DS} = 1$  V and  $V_{GS} = 1$  V for three MOSFETs with different gate lengths: 0.25  $\mu\text{m}$ , 0.5  $\mu\text{m}$ , and 1  $\mu\text{m}$ . The simulations are performed by omitting  $R_{sub}$  in the model.

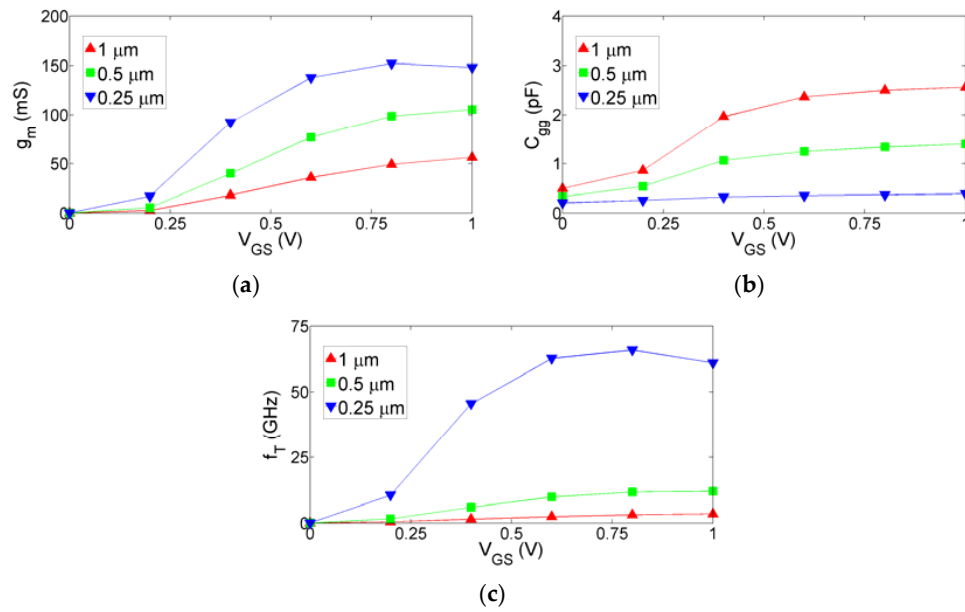
By focusing the analysis on the scaling of  $f_T$ , Figure 9 shows that a significant improvement of  $f_T$  is achieved with decreasing gate length. In particular,  $f_T$  scales inversely with the square of the gate length, as in the ideal case. In agreement with the expectation, this result is due to the achieved good scaling of  $g_m$  and  $C_{gg}$  with the gate length. Although  $C_{gg}$  is usually mostly determined by  $C_{gs}$ ,  $C_{gd}$  has been considered to estimate  $f_T$ , since its contribution becomes relevant by decreasing  $V_{DS}$  and/or  $V_{GS}$ . Furthermore, it is noteworthy that, although some slight discrepancy is observed with decreasing gate length, the achieved values of  $g_m$  are very close to those of the intrinsic transconductance calculated from DC measurements, indicating that the low-frequency dispersion plays a negligible role (see Figure 10). For the sake of completeness, the scaling of  $f_T$ ,  $g_m$ , and  $C_{gg}$  versus the gate length is analyzed under a wide range of bias conditions (see Figures 11 and 12). By fixing the input or the output voltage, a good scaling of  $f_T$  with decreasing gate length is always obtained, due to the increase of  $g_m$  and the reduction of  $C_{gg}$ .



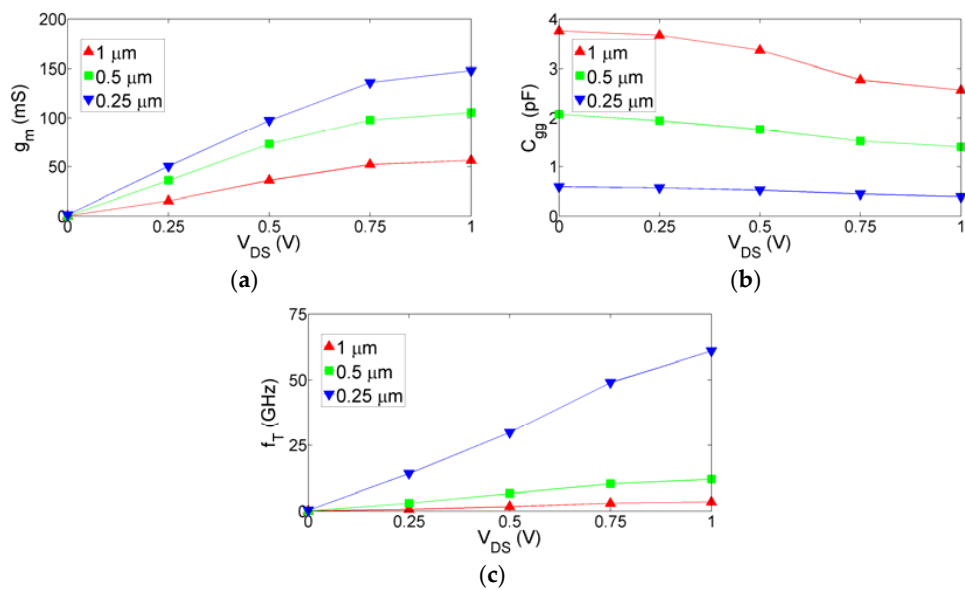
**Figure 9.** Behavior of (a)  $g_m$ ; (b)  $C_{gg}$ ; and (c)  $f_T$  versus gate length for three MOSFETs at  $V_{DS} = 1$  V and  $V_{GS} = 1$  V.



**Figure 10.** Behavior of  $g_m$  (colored symbols) and  $g_{mDC}$  (white symbols) versus gate length for three MOSFETs at  $V_{DS} = 1$  V and  $V_{GS} = 1$  V.



**Figure 11.** Behavior of (a)  $g_m$ ; (b)  $C_{gg}$ ; and (c)  $f_T$  versus  $V_{GS}$  for three MOSFETs with different gate lengths at  $V_{DS} = 1$  V.



**Figure 12.** Behavior of (a)  $g_m$ ; (b)  $C_g$ ; and (c)  $f_T$  versus  $V_{DS}$  for three MOSFETs with different gate lengths at  $V_{GS} = 1$  V.



Finally, it should be pointed out that the achieved good scaling of the intrinsic performance of the tested devices implies that the extraction of the model for a few gate lengths allows for the prediction of the intrinsic performance, as well as for other lengths that fall into the studied range.

#### 4. Conclusions

An analytical technique has been proposed to extract the small-signal equivalent circuits for MOSFETs. The extrinsic elements have been determined using an open structure and “cold” FET measurements. The validity of the obtained models has been confirmed by the achieved good agreement between the measured and simulated S-parameters. The experimental data have shown that the presence of the substrate resistance in the intrinsic model is necessary to accurately reproduce the behavior of the measured output reflection coefficient. Furthermore, it has been found that the intrinsic unity current-gain cutoff frequency of the tested devices scales inversely with the square of the gate length, exhibiting a nearly ideal scaling.

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**Author Contributions:** Giovanni Crupi performed the experimental analysis and wrote the article. Dominique M. M.-P. Schreurs and Alina Caddemi supervised the research, provided technical feedback, and reviewed the article.

**Conflicts of Interest:** The authors declare no conflict of interest.

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