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Review

Carbon Nanotubes and Graphene Nanoribbons: Potentials for Nanoscale Electrical Interconnects

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Abstract: Carbon allotropes have generated much interest among different scientific communities due to their peculiar properties and potential applications in a variety of fields. Carbon nanotubes and more recently graphene have shown very interesting electrical properties along with the possibility of being grown and/or deposited at a desired location. In this Review, we will focus our attention on carbon-based nanostructures (in particular, carbon nanotubes and graphene nanoribbons) which could play an important role in the technological quest to replace copper/low-k for interconnect applications. We will provide the reader with a number of possible architectures, including single-wall as well as multi-wall carbon nanotubes, arranged in horizontal and vertical arrays, regarded as individual objects as well as bundles. Modification of their functional properties in order to fulfill interconnect applications requirements are also presented. Then, in the second part of the Review, recently discovered graphene and in particular graphene and few-graphene layers nanoribbons are introduced. Different architectures involving nanostructured carbon are presented and discussed in light of interconnect application in terms of length, chirality, edge configuration and more.

Keywords: carbon nanotubes; graphene nanoribbons; nanoscale interconnects

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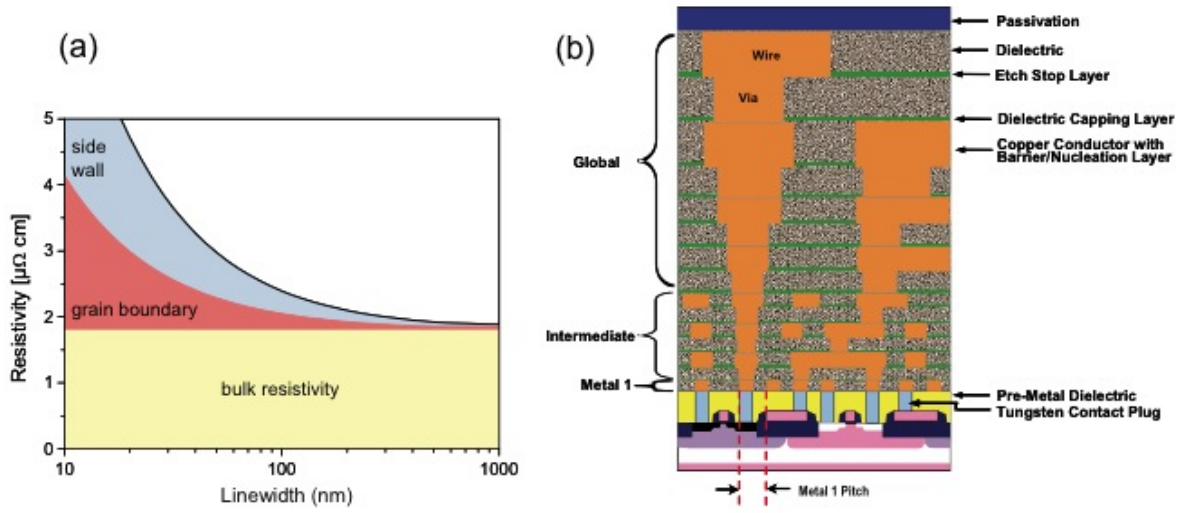
1. Introduction

Over the past few decades, the increasing progress in most technological areas from biomedicine to strategic deployment to meteorological forecasting has been largely benefitting from continuous and massive advances achieved in the field of computational technologies. With the need for larger quantities of data processing at faster pace within smaller volumes, the microelectronics industry has so far been steadily downsizing its basic active and passive building blocks. Those components are currently capable of operating at higher clock-speeds, delivering higher number of computations per second and, at the same time they occupy less physical space and consume less power. Nevertheless, the rapid progress towards gigascale miniaturization of those components faces a number of difficult challenges in terms of materials, architectures, fabrication and integration of nanoscale active and passive elements with expected performance in terms of reliability, speed, compatibility, and power consumption [1]. In this scenario, a fundamental issue of considerable difficulty is the development of the next generation interconnects for microprocessor units (MPUs). Interconnects are wiring systems which distribute clock and other signals and provide power and ground, to and among the various circuits and systems functioning on a chip. As the various active and passive elements of the MPU reduce in dimension below 100 nm, also the corresponding interconnects will consistently follow. Existing interconnect technologies involving Cu/low-k lines and theirs evolutionary downsizing for sub-100 nm size interconnects face a number of important challenges. As the lateral dimension of interconnects approaches the mean free path of copper (~40 nm at room temperature [2]), the impact of grain boundary scattering, surface scattering, and the presence of a high-resistivity material as a diffusive barrier layer causes a rapid increase in the overall resistivity. Figure 1a shows how the resistivity of copper significantly and rapidly increases above its bulk value as interconnect lateral dimension shrinks below 100 nm [3], following which major degradation of reliability, signal transfer properties and thermal management issues start to become important. In addition, larger current densities for increasingly small interconnect lines will lead to an enhanced electro-migration failure. Tightly packed conducting material immersed in a dielectric environment will further introduce significantly larger parasitic capacitance, enhancing the delay of the signal propagation and limiting the overall operational bandwidth. This scenario clearly suggests that any length below 22 nm, which represents the current microelectronics community standard, copper will reveal to be inadequate for interconnect applications. Hence, a revolutionary new high-conducting material with higher failure current density and comparable or better performance metrics (such as specific capacitance and RC delay) is indeed in need for future copper replacement. Figure 1b represents the cross-sectional schematic of a typical Integrated Circuit (IC), reproduced from the International Technology Roadmap for Semiconductors (ITRS) map from 2009. In a typical IC, interconnect structures are scaled into local, intermediate, and global wiring levels based on optimization of delay, power, and bandwidth *etc*. and where each level has diverse requirements and at the same time poses different challenges. At the local (or M1) levels, resistivity and failure current density represent major bottlenecks, mostly in terms of delay. Global interconnects, which are the longest, will be impacted most by the degraded RC delay (*i.e*., interconnect RC delay of 1892 ps for 1 mm Cu intermediate wire is thus not compatible). Significant effort has also been invested in tuning and modifying the dielectric properties of the interconnect material itself. Although the effective dielectric constant has been predicted to be

progressively reduced (from 4 to 1.5) with developing technologies [4], nevertheless we have now reached a point in which no further important decrease is possible. Currently, the lowest value of the effective dielectric constant ranges between 2.5 and 3 and it has been stable over the last few years [5]. While some progress has been made in terms of evolutionary downsizing of existing technologies which will possibly work in the near-term (~22 nm), it is becoming increasingly evident that revolutionary new materials and/or processes are required to address long-term (<16 nm) scaling down of interconnects.

Figure 1. (**a**) Resistivity of copper as function of the interconnect linewidth; (**b**) Typical cross-section of hierarchical scaling (microprocessor unit (MPU) device) showing different interconnect scaling levels [3].



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Different replacements for copper-based architectures have been proposed in the form of 3D Integrated Circuits, optical interconnects and carbon nanotubes (CNTs). Ongoing research in each of these field shows that those materials and structures could possibly successfully overcome the delay, power and bandwidth limitations of traditional interconnects, at one or more scaling levels. Nonetheless, in every single case, much remains to be done before one or more of these technologies can be realistically integrated with existing CMOS platforms while retaining their novel high-performance capabilities.

In this Review, we will focus our attention on carbon-based nanostructures (in particular carbon nanotubes and graphene nanoribbons) which could play an important role in the technological quest to replace copper/low-k for interconnect applications. We will provide the Reader with a number of possible architectures, including single-wall as well as multi-wall carbon nanotubes, arranged in horizontal and vertical arrays, and regarded as individual objects as well as bundles or arrays. Modification of their functional properties in order to fulfill interconnect applications requirements are also presented. Then, in the second part of the Review, recently discovered graphene and in particular graphene and few-graphene layers nanoribbons are introduced. Different architectures involving

nanostructured carbon are presented and discussed in light of interconnect applications in terms of length, chirality, edge configuration and more.

We refer the Reader to more detailed literature regarding alternatives to carbon-based interconnects here presented (3D Integrated Circuit and Optical Interconnects) [6–8].

2. Carbon Nanotubes

The ability to withstand current densities larger than 10^9 A/cm^2 (more than three orders of magnitude more than copper) even at ~1 nm diameter distinctly renders carbon nanotubes (CNTs) ideal candidates for nanoscale electrical interconnects [9]. CNTs are one-dimensional (1D) quantum conductors that have been shown to have ballistic transport with mean free paths of the order of microns [10,11], which is significantly larger than copper. Carbon nanotubes can have diameters ranging from <1 nm (Single-Wall Nanotubes, SWNTs) up to tens of nanometers (Multi-Wall Nanotubes, MWNTs). While SWNTs can be either metallic or semiconducting, MWNTs are mostly metallic. In addition to their attractive ballistic conduction capabilities, these chemically and mechanically stable strands of carbon are extremely strong (tensile strength ~ 100 GPa) and possess very high thermal conductivity [12,13]. It has been shown that metallic SWNTs present values of the conductance close to their theoretically predicted values of 4 e^2/h and they are capable of functioning at tens of GHz range both as transistors and as interconnects [14,15]. Above everything else, CNTs have the natural geometrical shape for being a wire, *i.e.*, a nanometers-diameter cylinder with a large aspect ratio (it will be shown later on that it is easy to fabricate SWNTs that are microns long, and MWNTs that are centimeters long). All those favorable physical, electrical and geometric properties of carbon nanotubes make them an attractive and suitable choice as nanoscale electrical interconnects [16,17].

As compared to Cu/low-k interconnects, CNTs offer numerous advantages, as a results of the very strong nature of the C-C bonds, their 1D tubular shape and the electronic band structure. To benchmark Cu-based interconnects, carbon nanotubes have specific properties and fulfill the following requirements: (i) *reduced resistance*, in fact in the limit of short interconnects there exists a limitation associated to the quantum resistance of a single tube (for metallic SWNTs, the quantum of resistance is 6.5 kΩ [18], while for long interconnects the conductivity of nanotubes in densely-packed bundles is predicted to outperform copper counterpart; (ii) *resistance to electromigration*, due to the strong carbon-to-carbon bonds within the hexagonal lattice of the shell(s), resulting in the possibility by the tube to sustain elevated current density (10^9 A/cm^2), while for copper equivalent current density of 10^6 A/cm^2 already is capable of producing structural damages; (iii) large *thermal conductivity*, in fact isolated carbon nanotubes are predicted to have large values of thermal conductivity (few thousands W/mK [19,20]).

Increased resistance resulting when reducing size in *vias* structures can be addressed using bundles of carbon nanotubes; an additional degree of improvement can be obtained by increasing the site density. Further, since the energy gap of carbon nanotubes is inversely proportional to their diameters, it is important to control the growth of CNTs, which is always a mixture of metallic as well as semiconducting SWNTs, thus small-diameter SWNT must be reduced since will limit the conduction of the bundles and *vias* architectures.

2.1. Carbon Nanotubes for High-Density Integration

In nearly all calculations and most experiments, carbon nanotubes in the form of aligned arrays have been used to benchmark future interconnects against copper existing architectures. These structures could be of circular or rectangular cross sections, made of SWNTs or MWNTs bundles, and can be commonly treated as parallel nanotube architectures (PNAs). Those structures can potentially replace Cu/low-k interconnects at most levels of interconnect hierarchy except in places where low-resistance short interconnects are needed (*i.e*., local interconnects), where CNT interconnects would be significantly more resistive than minimum-size copper wires since nanotubes as short as the gate pitch would be needed. In addition to the *classical* problems such as scattering associated with downsizing of copper interconnects, at the nanoscale, quantum confinement effects additionally play an important role. Recent computational predictions [21] have demonstrated that from a purely quantum-mechanical point of view, the resistance of carbon nanotube bundles is smaller than that of the copper wires for dimensions below 60 nm. Further, transmission line models [22] suggest that while ohmically contacted all-metallic SWNT bundle interconnects at local levels may be equivalent to copper in terms of RC delay, nevertheless the reduction in power dissipation and the increase of current density rendered them preferable even for the local level case. At the intermediate or global levels, RC delay becomes a crucial factor. In this case, larger diameter MWNT bundles, being chirality-independent all-metallic and having large mean free-paths, can achieve smaller signal delay than copper interconnects, with the improvements becoming more significant with technology scaling and increasing wire lengths. Saraswat *et al*. have predicted that for global levels, carbon nanotubes PNAs will outperform copper both in terms of latency as well as energy per bit of operation [23]. Monolayer or multilayer SWNTs PNAs can offer up to 50% reduction in capacitance and power dissipation with up to 20% improvement in latency if short enough (less than 20 μm) [24–27]. For semi-global interconnects, both latency and power dissipation can be substantially improved using bundles of SWNTs with reduced cross-sectional dimensions. From the electrical point of view, MWNT PNAs can outperform both SWNT and Cu at intermediate and global length scale in terms of conductivity. In addition, all-metallic SWNT PNAs appear to have much lower capacitance per unit length compared to copper and hence are ideal for local interconnects in terms of latency and power dissipation. This, in the long-term (sub-22 nm technology node) at all scaling levels, densely packed, all metallic PNAs, either SWNTs or MWNTs would be suitable copper replacements in terms of resistivity, failure current density, power dissipation, and delay. In the following sections, we will discuss some recent technological breakthroughs in terms of materials development, processing, structure fabrication, performance characterization, performance enhancement, and modeling of realistic SWNT and MWNT architectures that can potentially overcome the challenges faced by downward scaling of Cu/ low-k interconnects in terms of their projected performance metrics.

2.1.1. Scalable Ultra-High Density, Super Aligned SWNT PNAs

In order to compare or outperform Cu in terms of conductivity, it is essential to build highly aligned, short or/and long parallel arrays of CNTs with very high number density. For 1 nm diameter SWNTs the ideal density for a densely-packed all-metallic bundle is 0.66 SWNTs/nm^2 has been

proposed [1]. Jung *et al*. [28] have developed a template-based fluidic assembly process to build highly organized aligned single-wall nanotubes PNAs on SiO_2/Si substrate. Figure 2a schematically describes the steps involved in the fabrication of these structures. First, a plasma treatment is used to enhance the hydrophilic nature of SiO_2 surface, on which subsequently lithographically patterned photoresist is used to fabricate "channels". Substrates are then dip-coated into an appropriately functionalized SWNTs dispersion and the tubes selectively adhere to the SiO_2 trenches. Removal of the resist leaves behind highly organized, dense, aligned arrays of SWNTs, the thickness of which (~tens of nanometers) can be controlled by the initial SWNT concentration and dipping speed. The dense filling factor and high degree of alignment of the structure is maintained end-to-end of the PNA structure, as shown in Figure 2b. The lateral size of the interconnect structures is limited only by the lithography process, with which sub-100 nm channels can be easily achieved. So-fabricated devices are characterized by an overall resistance ranging from few kΩ to tens of kΩ depending on the channel size (see Figure 2c), and they are able to withstand current density of ~10^7 A/cm^2. A very important and encouraging aspect of this technique is that the degree of alignment and the overall density appears to increase with smaller channel widths, which represents a great advantage in the perspective of interconnect applications. Further, the possibility of increasing the length in case of SWNTs by adding titanium to the catalyst surface leads to millimeter-long, small-diameter, single-wall carbon nanotube as a results of enhanced oxygen affinity [29]. Additional approach have also been proposed to fabricate SWNTs two-dimensional arrays such as electric field-assisted direct growth [30], low-feeding gas flow driven method [31] and AC dielectrophoresis (DEP) [32] from a solution of SWNTs, the last one leading to planar arrays of controllable density between pre-fabricated electrodes ranging from 0.5 SWNT/μm to more than 30 SWNT/μm, depending on the concentration of tubes in solution, as shown in Figure 2d,e. This approach leads to highly oriented PNAs with sheet resistance as low as few kΩ/□ depending on the density of carbon nanotubes (much lower compared to thin film of random nanotubes or nanotube cross bar junctions [33]) and the electrical properties of which can be tuned by the removal by breakdown of metallic SWNTs. Han and co-workers have demonstrated that the modification of the surface properties of single wall carbon nanotubes with short DNA linkers can favor the formation of parallel arrays where nanotubes are arranged one parallel to the others. In this case, DNA behaves as a spacer with a potential control of the inter-distance between adjacent tubes of less than 3 nm and the entire arrays can be easily transferred [34]. In principle this approach is very powerful (not limited to carbon nanotubes), however a post-fabrication densification step is in need to further increase the density of tubes.

2.1.2. Densely Packed Ultra-Long MWNTs

Multi-wall carbon nanotubes PNAs are ideally suitable for intermediate or global level interconnects since they are nearly all metallic due to larger diameters and they are characterized by μm-long mean free path. Each shell of properly contacted MWNTs can contribute to the conduction leading to low resistance conductive wires. Long MWNTs, with lengths ranging from 500 μm (intermediate) to 1000 μm (global), could potentially achieve significantly smaller signal delays [35] (as low as 15%) compared to copper equivalent. Various methods have been developed to grow very long and aligned MWNT bundles, with high yield and repeatability [36–38]. Li *et al*. have shown that

ultra-long bundles can be grown in highly aligned parallel arrays of MWNTs, each nanotube running continuously end-to-end and that a selective control over the tube diameter (usually in the 25–40 nm range) can be obtained by adjusting the growth parameters [39]. Extraordinary growth can also be achieved through a multi-step *bottom-up* growth of self-supporting vertically aligned MWNTs, which can easily reach mm long *Vias*-type structures with large degree of alignment [40], as shown in Figure 3.

Figure 2. (**a**) Schematic of template-based fluidic assembly of high density, super aligned, sub-μm single-wall nanotube (SWNT) parallel nanotube architectures (PNAs); (**b**) High-magnification SEM images showing the degree of alignment of the SWNTs within channel widths of 1 μm. Scale bars = 200 nm; (**c**) Resistance histograms of SWNT-PNAs for different channel length (700, 500 and 200 nm, as labeled); (**d**) Schematic of the dielectrophoresis (DEP) assembly method; (**e**) SEM images for a typical DEP assembly with varying nanotube densities (1, 10, 20 and 30 tubes/μm). [28,32]

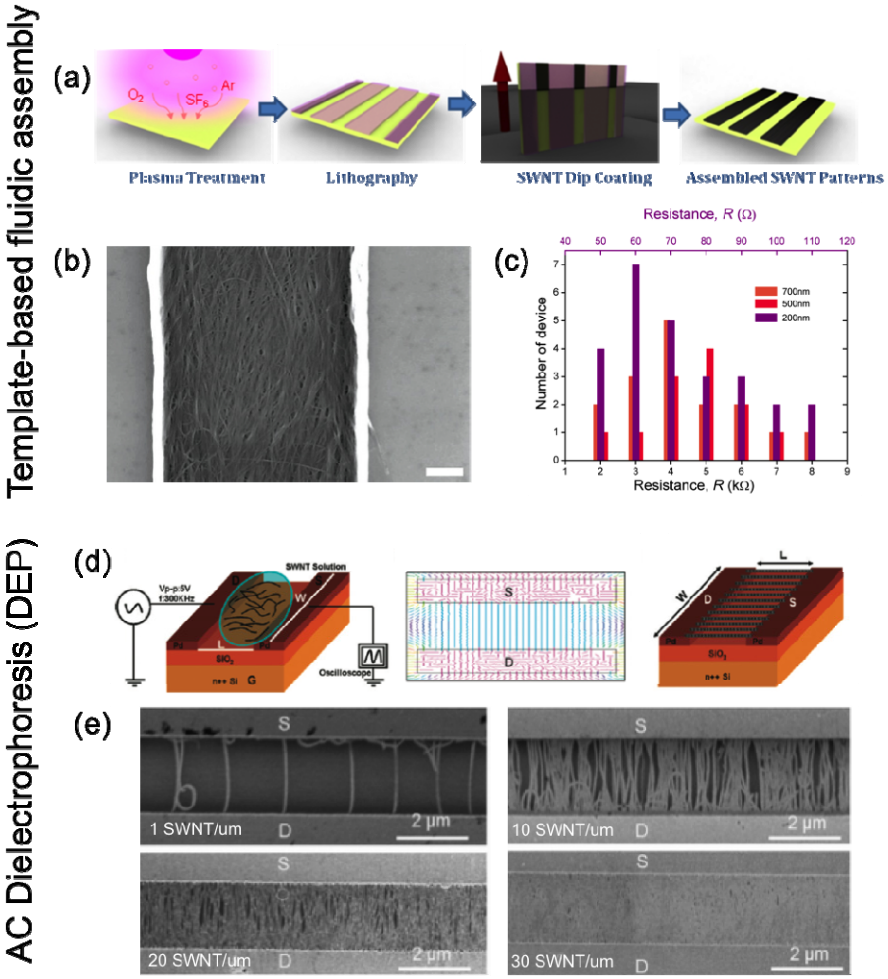

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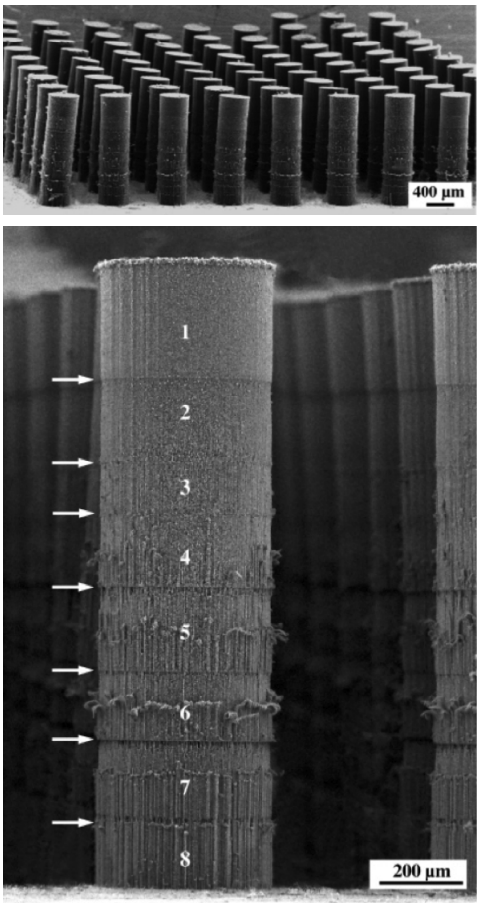
Figure 3. (Top) SEM image showing a two-dimensional array of pillars, each made of eight stacks of vertically aligned nanotube layers. Eight separate chemical vapor deposition (CVD) steps were used to grow the eight stack pillars on pre-patterned SiO_2. (Bottom) Higher-magnification SEM image showing the interfaces indicated by arrows between the separate stacks of nanotubes in a single pillar. The stacks are numbered 1 to 8, corresponding to the first to the eighth stack grown sequentially [40].



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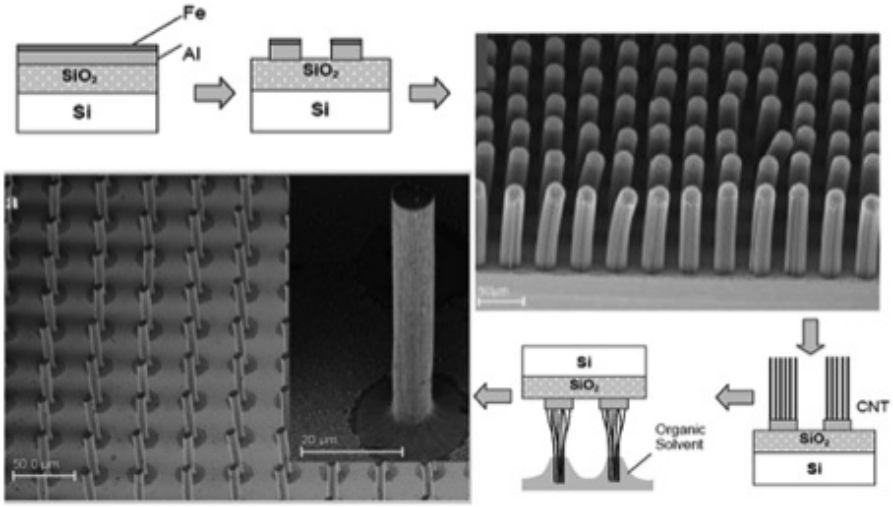
In addition, closely-packed carbon nanotube bundles are predicted to be characterized by higher conductivity when compared to copper; however, it is still extremely difficult to controllably grow those structures. Varying the feedstock flux during the CVD process (also known as "pulsed" CVD) can lead to dense array of all vertically aligned nanotubes: changing the gas flux and the duration of the pulse allows for the growth in predetermined length intervals, with precise density of the array over sub-µm lengths and tailored heights if growth can be reinitiated after each pulse [41]. Design and engineering of the catalyst offer the possibility of growing ultrahigh density, aligned forests of carbon nanotubes. Cyclic and repeated deposition/annealing/immobilization of catalyst thin films lead to nanotube forests with an area density of at least $10^{13}/cm^2$, over 1 order of magnitude higher than existing values, and very close to the limit of a fully dense forest [42]. Additional improvement (up to $10^{14}/cm^2$) can be reached if tube diameter can be further reduced. Post-growth methods have also been proposed in order to densify MWNTs arrays. Natural shrinking has been observed after immersion in

solution due to simple solvent evaporation [43]. In as-grown aligned CNT arrays, the site density of nanotubes is about 60 CNTs/μm^2, orders of magnitude smaller than the effective maximum achievable site densities (~10^4 CNTs/μm^2). A solvent-assisted capillary coalescence method [44] is used to densify aligned CNT arrays in vertical pillars, shape very well suitable for vertical interconnect assemblies and vias, as shown in Figure 4.

Figure 4. Schematics and SEM images describing capillary coalescence-driven densification using an organic solvent in aligned MWNT PNAs [44].



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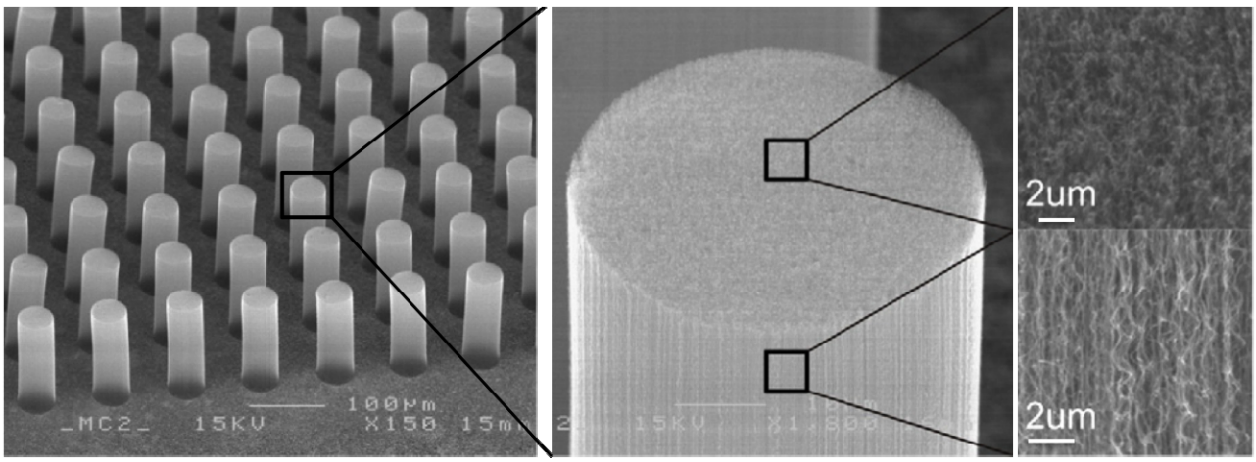
The resultant pillars retain their cylindrical nature while uniformly shrinking in diameter, with site densities of approximately 900 CNTs/μm^2, with a densification factor of about 15. However, such structures will still present a significant unoccupied volume between individual CNT strands, and this could provide room for further densification. On the other hand, growth in templates (alumina, in most cases) allows for selective fabrication of all-vertically aligned and closely packed tubes with diameter as small as 30 nm [45]. Those structures, when still in template, could in principle allow for *all-walls top and bottom electrically contacted* nanotubes with uniform length and diameter. However, tubes grown in template are of poor quality when compared to arc-discharge tubes with a high level of defects which makes them highly resistive and, at the same time, the density (tube/μm^2) is very low.

2.1.3. Selective Growth of Metallic Tubes

Statistically, about one third of as-grown SWNTs are metallic. These single shell tubes realistically represent the ultimate interconnects due their small radius and high conductance. However, there are no simple methods for selectively grow only metallic nanotubes, especially in more complex structures. Although great efforts have been put toward growth of controlled-diameter [46,47] and metallic SWNTs, very few reports have shown a certain degree of control over the growth. Yield of metallic SWNTs up to 65% of the final product has been achieved using as carbon source during the growth process monohydroxy alcohol homologues with a different ratio of carbon to oxygen content. It has been demonstrated that the yield of metallic SWNTs can be improved by increasing the relative

concentration of carbon to oxygen [48]. Further, Harutyunyan *et al*. were successful in achieving a fraction of metallic SWNTs of 91% by modifying the noble gas ambient during thermal annealing of the catalyst and in combination with oxidative and reductive species of the Fe nanocatalysts deposited on SiO_2/Si substrates. This work has clearly demonstrated the very strict connection between the catalysts morphology and the growing tube [49]. Modification of the catalyst properties (metallic phase and crystalline structure) can be a powerful and potential route in order to selectively tune the growth of carbon nanotubes with designated chirality [50,51]. Further on, detailed investigation of the effect of introducing iron pentacarbonyl ($Fe(CO)_5$) vapor during the growth process (arc-discharge) has shown the possibility of obtaining up to 90% of single wall metallic tubes [52]. Otherwise, it is possible to controllably grow double wall carbon nanotubes (DWNTs); in fact, due to their larger diameter, DWNTs have extremely small band-gaps, and at room or elevated temperatures, these tubes behave like near-zero gap metallic CNTs. Fu and coworkers have recently demonstrated the possibility of grow pillars on gold films of highly vertically aligned nanotubes, 80% of which are double wall carbon nanotubes [53], as shown in Figure 5. As compared to standard growth on Si substrate, it has been possible to considerably increase the number of DWNTs and less dispersive for other types of tubes. Water-assisted chemical vapor deposition on precisely-controlled thickness of iron catalytic films can be also applied to grow vertically aligned doubled-walled carbon nanotube forests with more than 2 mm in height with a yield of DWNTs approximately of 85% [54]. This synthesis approach also produces nearly catalyst-free DWNT forests with very high carbon purity (99.95%), which then potentially guarantees that the tube properties will not be affected by the presence of the catalyst. Koshio and coworkers have shown the possibility to obtain double-wall carbon nanotubes starting from highly dense small diameter MWNTs as a result of vacuum heat treatment at 2200 °C or higher, where, at these elevated temperature a selective removal of 1 to 3 shells within the MWNT takes place [55].

Figure 5. CNT bundles grown on the Au film, 80% of which are double wall carbon nanotubes (DWNTs). Top and side view show the large degree of vertical alignment of the tubes within the array [53].



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Different post-growth approaches have also been proposed to selectively differentiate SWNTs, according to their chirality (and thus their electrical properties). An electric field-based treatment [56,57]

can be used to separate all metallic tubes from semiconducting ones, leaving behind a parallel device array composed of a randomly grown mixture of metallic and semiconducting to reach densely packed devices in parallel where high density are required. In solution, single wall tubes can be well separated by density gradient ultracentrifugation (DGU), a technique traditionally used to separate and isolate different sub-cellular components, such as DNA and RNA. This method has been developed for sorting tubes based on chiral numbers and diameters, consisting in adding the SWNTs suspension in centrifuge tubes with varying density profile liquid mixtures; upon centrifugation, the tubes are separated and moved to regions (liquid) with matching densities [58–60]. Single-wall nanotubes can additionally be sorted using alternating current as a result of different dielectric constants depending on their electrical nature (metallic or semiconducting), as shown by Krupke and co-workers which have successfully separate in suspension metallic from semiconducting tubes [61].

2.1.4. Directional Growth of CNTs

Horizontal carbon nanotubes arrays represent still a challenge in the race for controllable and selective growth of carbon nanotubes. Interconnects applications are intrinsically in need of all the CNT to be of metallic nature. Being the energy gap of CNTs inversely proportional to the their diameter, the possibility of controlling the diameter during growth can allow for a control of the electronic properties of the tubes (and in particular their resistance [25,62,63]. There are three different approaches to achieve horizontal growth of carbon nanotubes: (i) electric-field based assembly/growth [64]; (ii) laminar gas flow [65] and (iii) step-templated growth on quartz/sapphire substrates [66,67]. Each of these methods unfortunately lead to very low nanotube densities or, as in the case of growth on quartz and sapphire, those are not compatible with growth on a chip. Further, one can think of first growing CNTs along the vertical direction and then proceed to flip them over.

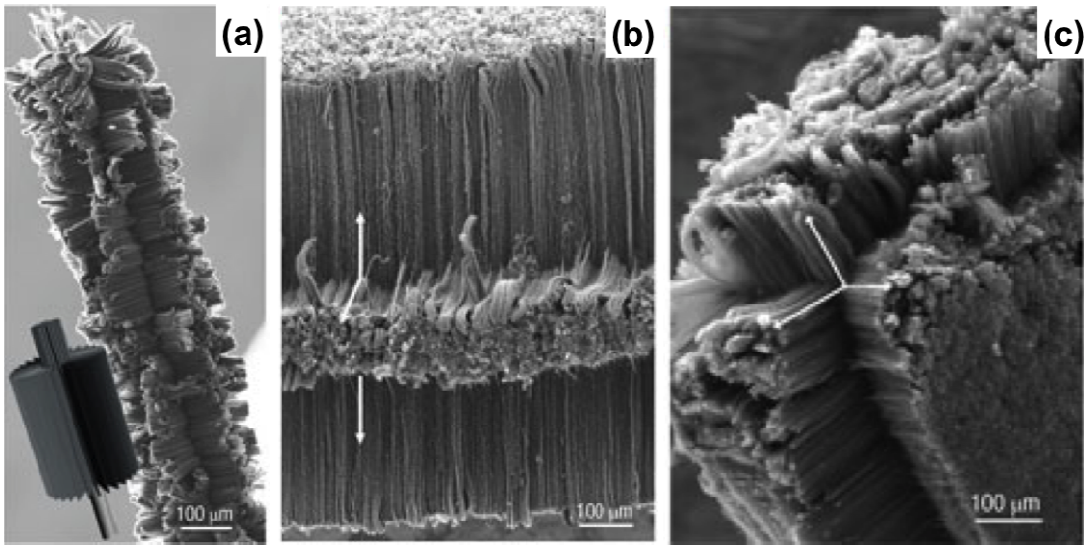
Chai and coworkers have demonstrated that by controlling the catalyst thickness [68] on substrate (and the size of nanoparticles), it is possible to grow in the presence of an electric field bundles of MWNT with precise diameters along the horizontal direction [69]; in particular thicker catalyst films (5 nm) lead to large diameter tubes (25–35 nm) while in the case of thinner catalysts (1.2 nm), the diameter distribution of the grown tubes is around 5–7 nm. One other interesting outcome of this work is that catalyst thickness also allows for a certain control over the sites density of the CNTs bundles, where thinner catalyst leads to denser bundles.

Chiodarelli and coworkers have recently proposed a novel method to achieve horizontal growth of CNTs-based interconnects with lateral dimension comparable with current Cu equivalent [70]. CNTs are first grown vertically within pre-determined vias structures (diameters 200–300nm), then flipped horizontally and electrically contacted on both sides through metallization process. The as-fabricated interconnect structures then consist of carbon nanotube bundles with wall density of approximately $10^{13}/cm^2$, wire lengths of tens of μm and tube diameter of approximately 50 nm, characterized by nanotube resistivity as low as 1.1 mΩ·cm, value which is still larger than copper equivalent but which becomes closer and closer.

The placement of catalysts on a vertical surface makes the horizontal growth harder to achieve than the vertical growth. Yan and coworkers have shown that a tilt evaporation technique can achieve catalyst patterning on vertical surfaces [71]. Upon demonstrating that $CoSi_2$ is a good catalyst support

material in CNT interconnect application since it can be easily patterned on a vertical surface and support high density CNT growth, they have grown CNTs from the vertical surface with wall density of 6×10^{11} walls/cm^2 [72]. In case of single-wall and double-wall tubes, this challenge can be achieved using for example previously described template-based fluidic assembly methods, in case of MWNTs this can be achieved, to a large extent, by using floating vapor catalyst assisted CNT growth directly on metals [73]. Talapatra *et al*. have developed a standardized and unique technique for growing 3-D architectures of aligned bundles of carbon nanotubes on bulk metals, as shown in Figure 6 [74].

Figure 6. SEM of aligned MWNT arrays grown on metallic substrate showing growth directions conformal to the substrate orientation. Growth of carbon nanotubes on (**a**) metal wire, (**b**,**c**) metal sheets showing the highly directional nature of the CNT growth, with the orientation of the nanotubes being perpendicular to the substrate surface. The arrows indicate the direction of CNT growth [74].



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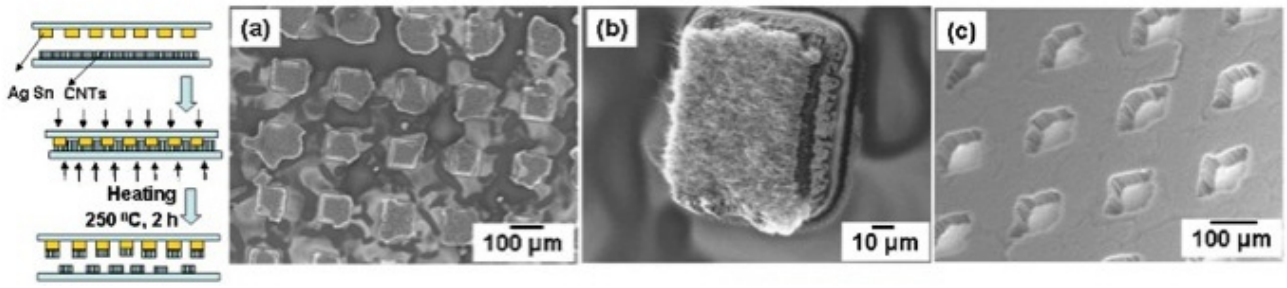
Growth on metal substrates has also the advantage of additionally providing an easy solution for growing electrically end-contacted carbon nanotubes. Parameters such as growth temperature and growth time can be selectively adjusted in order to obtain a specific tube length, as well in part their degree of alignment [75]. Electrically end-contacted dense bundles of aligned CNTs are promising candidates for interconnects and *via* structures at the sub-50-nm length scale. For optimal performance in these architectures, any metallization of individual tubes has to be on their ends, such that individual shell can be accessed by each electrode, and each nanotube in the bundle has to be individually metalized in this way. Post-growth metallization techniques are yet to reliably meet these criteria on a large scale. The unique advantage of the direct growth of CNTs on metallic substrates is that, within the array, every individual nanotube is electrically end-connected *in-situ*, overcoming several obstacles to applications in interconnect and contact technologies.

2.2. Carbon Nanotubes Devices and Architectures

2.2.1. Towards Low-Resistance Contacts

Large contact resistance represents still a technological challenge in order to realize interconnects. In the case of single-wall nanotubes PNAs, the sidewall resistance can be dramatically reduced using a cyclic high-current induced contact resistance annealing. This causes "hot-spots" at the contacts since that is where the resistance lies. The current density (~10^8–10^9 A/cm^2) is large enough to anneal the contacts, but causes no damage to the tubes. Electrical annealing treatment performed in a cyclic fashion on SWNT bundles of 0.5 μm in length, shows that the overall resistance change of more than 3 orders of magnitude due to contact annealing, bringing the total resistance below 1 kΩ. This method is potentially suitable for short SWNT PNAs. Rapid thermal annealing (RTA) at elevated temperatures (600–800 °C) for few tens of seconds can decrease the contact resistance between a carbon nanotube and metal electrodes (Ti/Au) by several orders of magnitude, becoming stable in the long-term as a result of a better adhesion of the carbon shell to the titanium film [76]. Welding at the nanoscale by a vibrating force at ultrasound frequency has been successful in contacting SWNTs onto metal electrodes, where the formed contact is mechanically robust and it is a stable low-Ohmic with resistances in the range of 8–24 kΩ (for a 1 μm long metallic single wall tubes at room temperature) [77]. For vertical integration, however different approaches have been considered such as pressure contacted soldering method [78], where lithographically patterned carbon nanotubes array grown on silica by chemical vapor deposition (CVD) are transferred of low-temperature (Ag/Sn) coated substrate. Figures 7a,b show the SEM images of carbon nanotubes arrays transferred onto solder pads (positive pattern) using the scheme described on the left as well as the CNTs transferred between the solder pads (negative pattern) in Figure 7c. Infiltration of CNT vias and subsequent polishing in order to expose open MWNT ends is also proposed for such types of architectures [44].

Figure 7. (**a**,**b**) SEM images of CNTs transferred onto solder pads (positive pattern) using the scheme described on the left; (**c**) CNTs transferred between the solder pads (negative pattern) [78].



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Introduction of an interfacial carbon layer has also been proposed in order to reduce the contact resistance as a result of the improvement of the wetting capability and to the formation of chemical bonding to the tube [79]. Also, the contact area is larger due to the presence of the additional carbon layer.

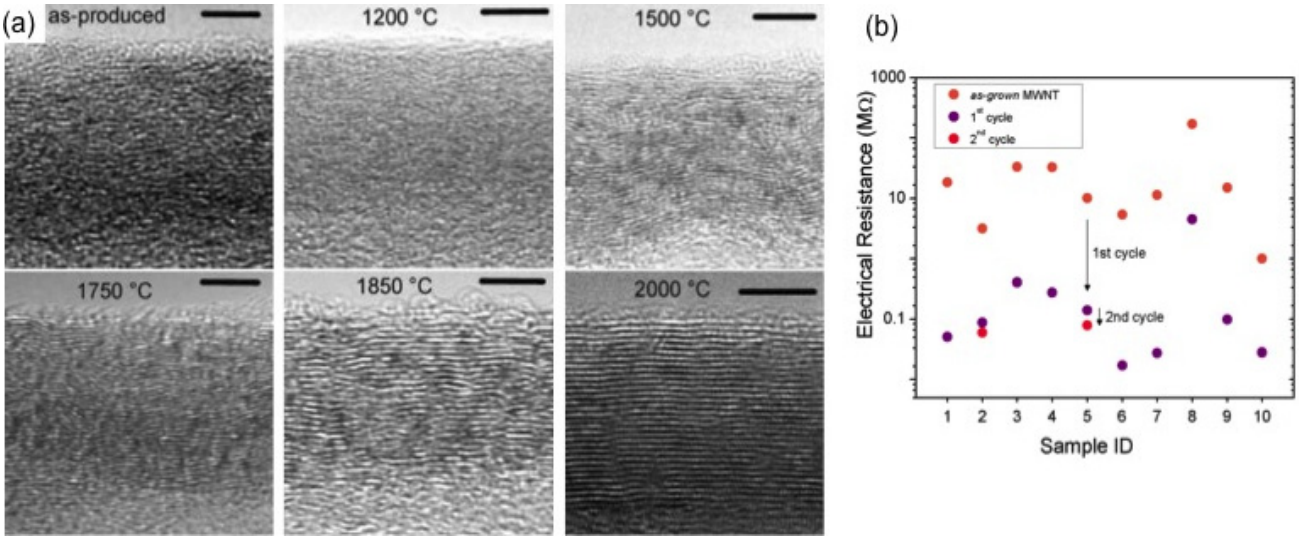
2.2.2. Towards Defect-Free CNTS

Most high-quality CNTs are grown at extremely elevated temperatures (>1000 °C), thus resulting in carbon nanostructures with very low-defect densities. However, in carbon nanotubes grown at lower temperatures, post-growth methods are indeed in need for defects reduction. Ultrafast microwave annealing has been suggested as possible route towards the reduction of defect density in vertically aligned carbon nanotubes, for which only 3-minute-long exposure is necessary to induce a defect reduction, as suggested by Raman spectroscopy and thermogravimetric analysis. Mechanical as well as electric properties are also found to be enhanced upon microwave irradiation [80]. In the presence of a metal catalyst, defects formed during the addition of carbon atoms can be efficiently removed at the tube-catalyst interface, in a self-healing-type of approach. Simulations in fact show that potentially a defect-free CNT wall with 10^8–10^{11} carbon atoms can be achieved, thus leading to a potentially 0.1–100 cm long SWNT [81]. This effect is expected to take place through ring isomerization, leading to the removal of few (5–7) adatoms and monovacancy defects. The timescale of this process is of the order of several picoseconds and depended largely on the catalyst morphology and surface. This healing mechanism also potentially represents a way to control the chirality (n, m) of a growing SWNT during the growth process [82]. Among various catalysts, Fe has demonstrated to be the most efficient in defect healing [81].

Thermal annealing at high temperature has been proposed as an effective method to reduce defects in nanotubes [83–86]. Annealing at different high temperatures (>1000 °C) of CVD-grown multi-wall carbon nanotubes at relatively low temperatures (650 °C) in porous alumina template lead to a different degree of rearrangement of the imperfect graphitic structure and removal of weakly bounded defects, leading to the reconstruction of the hexagonal carbon lattice along the shell in a more ordered fashion. Transmission electron microscope (TEM) images in Figure 8a demonstrate the increase degree of graphitic order for increased temperatures.

Thermal reduction can also be used to purify and reduce chemical defects in the carbon lattice of single-wall carbon nanotubes, where a combination of first a high-temperature reactions in as-grown nanotubes in a pressurized chamber with a slow annealing process in vacuum environment is used [84]. Application of a rapid large bias across two terminals of a carbon nanotube not only decreases contact resistance, but also can dramatically reduce the number of defects. It has been shown that for highly defective MWNTs [87] (*i.e.*, grown in alumina template), a rapid cycling of the applied voltage across the electrodes of a device generates sufficient Joule heating to anneal defects in the CNT. This can drastically increase the mean free path (by 1–2 orders of magnitude) and reduce the resistance of tubes by orders of magnitude, as shown in Figure 8b [88]. Further, the investigation of the low-temperature charge transport properties allows estimating the defect density in those systems. Certain key transport parameters, such as number of quantum channels, disorder density (or equivalently, the mean free path), and *e-e* interactions play a strong role in determining the electronic properties of the interconnect itself. Using a combination of low-T transport measurement and application of field-theoretical models such as Lüttinger-liquid theory and Al'tshuler-Aronov [87] corrections can be used to estimate the number of quantum channels and mean free path in carbon nanotubes.

Figure 8. (**a**) Transmission electron micrographs of the walls of as-produced nanotubes grown in alumina template and at different annealing temperatures (as labeled). The initial, disordered carbon structure is converted into a more and more perfect graphitic structure with an increasing annealing temperature. Scale bar is 5 nm; (**b**) Variation of the electrical resistance in individual alumina template grown carbon nanotubes as function of the number of electrical cycles. [85]



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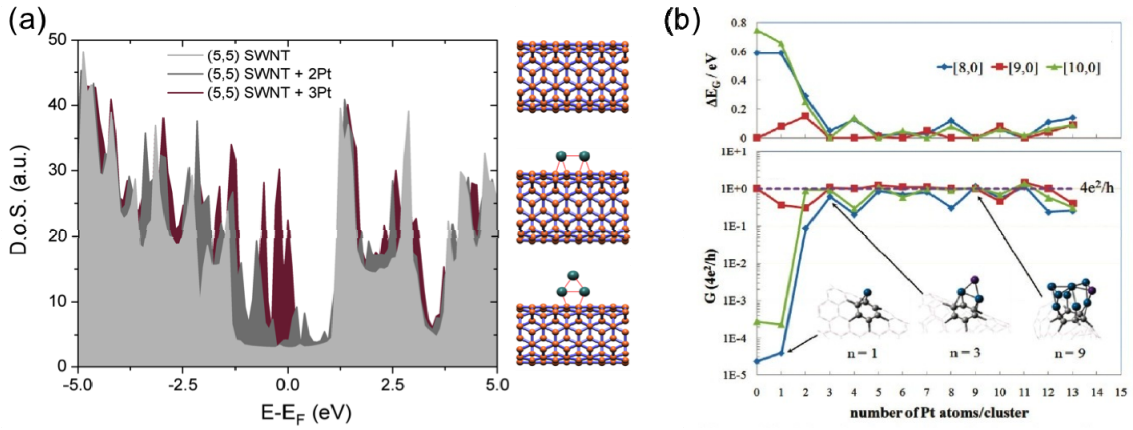
2.2.3. Conductance Enhancement via Metal Decoration and Doping

Theoretical and experimental works have shown that modification of the structure of carbon nanotube can drastically affects the electronic properties. In particular, Density Functional Theory (DFT) calculations [89] show that decoration of SWNTs with platinum nanoclusters adds a number of electronic levels and enhances their density of states (DoS) near the Fermi level for both metallic and semiconducting carbon nanotubes, as shown in Figure 9a.

Figure 9b shows the effect of Pt nanocluster decoration on (top) the band-gap and (bottom) the conductance of two semiconducting ((8,0) and (9,0) and a metallic (10,0) single wall nanotube [28]. In case of semiconducting SWNTs, the addition of more than three atoms per cluster sizably brings down its band gap to values very close to zero, and remains close to zero for further decoration. In case of metallic SWNTs, the gap remains closed for values of n larger than 3. Further, calculation of conductance shows that in all three cases, platinum decoration causes the SWNT to approach or remain at the quantum limit of G~4 e^2/h, independently of the tube chirality. Calculations based on more rigorous GW approximation confirm metallic nature of Pt-decorated carbon nanotube [90]. Hence, decoration of carbon nanotubes by metal (Pt) clusters represents a general approach to convert semiconducting nanotubes into metallic, with a consequent effect of improving the overall conductivity of the SWNT PNAs. This process does not require neither selective growth nor post-growth selection of metallic SWNTs for interconnects applications. Encouraging results by electrochemical deposition of minute amounts of platinum on aligned SWNT PNAs have shown that those structures present negligible changes in surface morphology upon metal decoration and a

dramatic decrease in resistivity of the order of approximately 75%. Experimentally, it has been demonstrated that decoration of platinum nanoclusters in MWNT has a significant enhancement of conductance. The process of metal decoration is achieved through a high-bias application procedure, which increases the number of quantum channels and decreases the defect density, and their combined effect can be extremely large (several orders of magnitude).

Figure 9. (**a**) Effect of platinum atom decoration on the (top) band-gap and (bottom) conductance of a metallic (9,0) and two semiconducting (8,0) and (10,0) SWNTs. For number of atoms > 3, all semiconducting SWNTs become metallic and their conductance approach the quantum limit of 4 e^2/h. Metallic tube remains metallic; (**b**) Cyclic high-bias treatment (HBT) treatment produced a Pt-nanoclusters decoration of the outer surface of the tube along with a conductance enhancement. (Inset) Platinum-decorated multi wall carbon nanotubes upon HBT [28].



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Chemical doping has also been proposed to enhance the conductivity of carbon nanotubes, both as individual objects as well as bundles [91–93]. The density of states (DoS) in doped carbon nanotubes reveals the possibility of increasing the conductivity of MWNTs; in fact, chemical doping of the outer shell has the overall effect of shift upwards the Fermi energy, leading to increased conductivity. Being the DoS independent from the tube diameter, elevated conductance values can be expected in case of metallic MWNTs rather than in metallic SWNTs as a results of both larger surface area available for doping and for the fact that any additional conduction channel is close to the Fermi energy in MWNTs. Doping with aryldiazonium and oxonium salts have been shown to be capable of reducing the resistance of MWNTs by almost 20% [94]. Lee *et al*. have shown that bulk samples of SWNTs grown by vapor phase reaction in the presence of bromine and potassium (each one as an example of *e* and *h*-type doping) can lead to an enhancement of the room temperature conductivity of a factor of about 30, which can outperform copper equivalent interconnects [95]. Doping multi wall carbon nanotubes with nitrogen (at low levels) and then performing thermal annealing at temperature of approximately 1000 °C, an elevated decrease in the electrical resistance of individual tubes is observed (about two orders of magnitude), where nitrogen is observed to be stable up to 1500 °C [96]. In case of SWNTs mats, increasing the dopant exposure (Cs) produces first a decrease and then an increase of

their electrical resistance, allowing tunability of the dopant level to maximize conductivity of nanotubes structures [97]. In SWNTs mats, one or two order of magnitude increase in conductance can be achieved [95,97,98]. Conduction properties of potassium-doped individual ropes of SWNTs can also be modulated with a gate bias, further showing the intrinsic nature of *h*-doping in pristine tubes [99].

Zhao and coworkers have shown the possibility of fabricating iodine-doped, double-walled nanotube cables having electrical resistivity reaching ~10^{-7} Ω.m. The low-density and their specific density values outperform their copper counterpart and become comparable (one order of magnitude difference) with the highest specific conductivity metal such as sodium. In this case, elevated current handling capacity is also found (10^4–10^5 A/cm^2), along with no degradation of their electrical properties and freedom in terms of size and dimensions growth. Interestingly, a practical application in its preliminary form has been presented by using those doped-nanotubes cables in partly replacing metal connections in a commercially available light bulb circuit [100].

2.2.4. Breakdown in Carbon Nanotubes

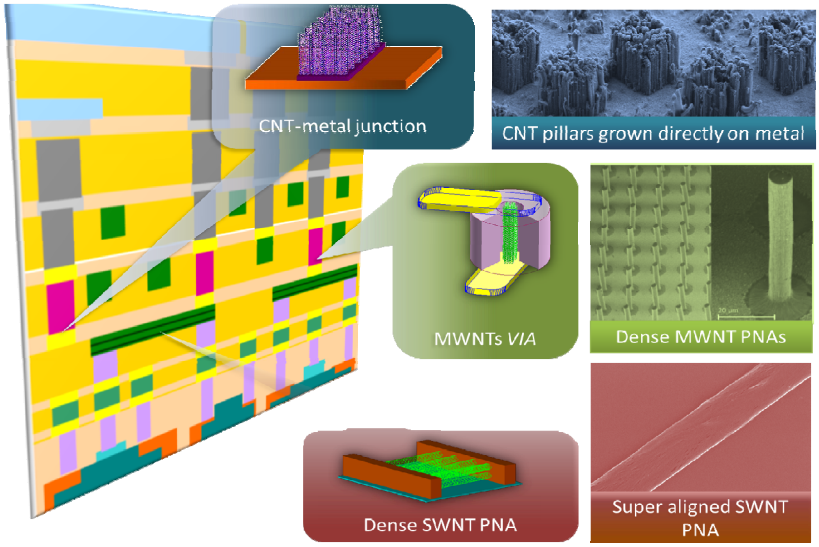
One important aspect concerning CNT and their application as interconnects to be considered for realistic exploitation in ICs is the maximum current (density) the tube (or the array/bundle of tubes) can sustain before it breaks or partially loose their electrical properties. Carbon nanotubes both as individual object as well as in arrays/bundles can be tested for breakdown. It is important here to distinguish between single wall and multi wall carbon nanotubes, since the breaking of one single wall in SWNT will lead to the complete breakdown of the tubes, thus failure of the corresponding IC while in the case of MWNTs, there could be multiple and subsequent breakdowns accompanying the breaking of individual shells, leading to variation of the entire conduction properties prior to complete breakdown.

In most cases, breakdown in carbon nanotubes is induced by producing enough Joule heating to completely destroy the continuous carbon shell(s) or, if there are contacts, the contacts themselves. Joule heating can be produced thermally by direct heating and electrically by forcing a current along the tube(s) [101].

In case of single-wall carbon nanotube, electrical breakdown leads to an abrupt drop to zero of the current flowing within the tube, while in the case of multi wall carbon nanotubes and bundles exhibit higher current and multiple breakdown steps. Collins and coworkers have experimentally demonstrated that in arc-grown nanotubes, monitoring the current passing through the tube shows a staircase-shape where each step is associated with the progressive breakdown of adjacent and individual shells (12 μA/ shell) [102]. Similar experimental and theoretical results have been obtained on similar tubes grown by different techniques [18,103,104]. In some cases, the progressive removal of shell in carbon nanotubes, up to complete failure of the tubes, has been shown through electron microscopy (scanning and transmission) [105,106]. As mentioned, breakdown can also be induced thermally by simply heating the tubes. In air conditioning, due to presence of oxygen and self-heating, breakdown temperature is very well known of being approximately 600 °C. Hata and coworkers have carried out experiments both in vacuum (10^{-5} torr) and air and they observed that, in vacuum, carbon nanotubes breakdown takes place at much higher temperatures (approximately 1800 °C) [107]. This

implies that oxidation cannot be the only cause leading to breakdown; different works have proposed an important role played by the presence of defects [108,109] and by the underlying substrate and its physical properties (*i.e.*, SiO_2 begin to melt at 1700 °C). Numerous studies have shown that the breakdown in carbon nanotubes is favored and initiated by the presence of oxygen (in air) which tends to etch the outermost shell [102], to the presence of defects along the wall where thus electric field (and consequently heat are intensified) [110,111], as well as to the poor thermal contact between CNTs and metal electrodes which prevents efficient heat removal [112]. It has been observed that metallic carbon nanotubes present the failure point at middle point location [113,114] (most likely corresponding to the hottest point) while semiconducting nanotubes breaks closer to one of the electrodes [111,115] (closer to drain), most likely corresponding to the area of the largest electric field and lower carrier density. Both these results indicate the diffusive nature of the heat dissipation and charge transport within the tube [116,117]. It has been demonstrated that a carbon nanotube grown by CVD with diameter of 18 nm can handle in vacuum a maximum current density up to 8×10^7 A/cm^2 with associated power of 0.6 mW (as compared to 0.16 mW and 2×10^7 A/cm^2 in air) [118]. Decoration with electrochemically deposited Ni particles allows protection of the CNT interconnect against oxidation and improvement of the heat release through the surrounding environment (about 1.5 mW before breaking down under vacuum, with a corresponding maximum current density as high as 1.2×10^8 A/cm^2). The Joule heating melts the nickel particles and promotes the formation of titanium carbon nitride with the overall results of improving the electrical contact between the CNT and the electrodes.

Figure 10. Schematic of a future Integrated Circuit (IC) chip with various interconnects potentially conceivable with CNT-based architectures, as described in the text which can hierarchically enable partial or full integrations in future IC chip [3,28,44,74].



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The present Review has so far described various research efforts in the field of fabrication, characterization and development of ultra-high density, super-aligned nanotubes PNA-based high performance horizontal and vertical interconnect assemblies which can be possibly integrated into existing CMOS platforms. Figure 10 shows a typical cross section of an IC circuit (see Figure 1) and potential areas where various CNT-based architectures could begin to replace copper interconnect in the coming years. While it is important to fabricate high-performance CNT PNAs, one has to keep in mind the compatibility and integration considerations in terms of resistivity, failure current density, RC delay and operation bandwidth at appropriate individual scaling levels.

3. Graphene and Graphene Nanoribbons

3.1. Graphene as Two-Dimensional Crystal

Upon its experimental evidence in 2004, graphene has soon entered in the quest for the search of a new material for replacement for CMOS-compatible structures [3]. Graphene is a monolayer of *sp2*-bonded carbon atoms packed in a hexagonal lattice, arrangement that makes it rigorously a two-dimensional material [119]. Graphene has gathered the interest of the scientific and technological communities and, the investigation as well as implementation has been exponentially increasing due to the existing technology platform and knowledge, mostly borrowed from the decades-long carbon nanotube community. We refer the Reader to more specific literature for an in-depth and detailed description of the remarkable and interesting properties of this material [120,121]. In the present context, we will focus on some of the properties and characterization that are valuable and of great importance for interconnect applications.

Graphene is a zero bandgap semiconductor, in which electrons behaves as massless Dirac fermions and which could in principle offer less power consumption and enhanced performance due to increased carrier velocities. The ambipolar nature of graphene makes it a very versatile material since it can be used both as an *n*- and *p*-channel material. In fact, charge carriers have been observed to "puddle" in graphene layers at zero field so that both *n*- and *p*-carriers can co-exist within the same layer. Although graphene is a rather new material, a timeline for potential real applications in expected rather soon within the current decade (by 2019–2020 according to International Technology Roadmap for Semiconductors—Emerging Research Materials Section in 2009 [122]).

There exist a variety of methods to produce graphene, ranging from CVD-*like* methods or epitaxial growth on a silicon wafer [123], to mechanical exfoliation [124], chemical oxidation [125] or solvent exfoliation from highly oriented pyrolytic graphite (HOPG) [126,127], direct CVD epitaxy on single crystal metal substrates [128] and sublimation of silicon from SiC [129]. Recently proposed approaches such as growth on polymers (polyethylene terephtalhate, PET or polydimethylsiloxane, PDMS) further provide a new class of flexible and transparent substrates (mechanical bending and twist up to 11% without any loss in conductivity). So far, mechanical exfoliation of graphene has produced high quality films on silicon [119]. Nevertheless, this method is not currently capable of selective placement of graphene at a specific location, which makes it an inadequate route to device fabrication of integrated circuit technologies. Thickness control of several monolayers on a millimeter scale and carrier mobility of 25,000 cm^2/Vs have been demonstrated for grapheme grown on SiC (as a

result of Si sublimation), where annealing temperature of at least 1200 °C in H_2 ambient condition are required [130]. Deposition of a thin layer of SiC [131] on a Si wafer followed by silicon evaporation has led to few-atomic layers thin graphene. A common drawback for the above-mentioned techniques is the high temperatures required during processing which might introduce additional defects in 300 mm and 450 mm wafers-line production or might not be compatible with some of the subsequent processes to be performed. Graphene can be grown on single crystal substrates (Ni [132], Ir [133], Pt [134]); however, this process has so far been revealed to be quite expensive. Continuous graphene films have been successfully grown by ambient pressure CVD on polycrystalline Ni which can then be subsequently transferred (by Ni wet-etching) on arbitrary substrates [128], producing films with sheet resistances as small as 280 Ω/□ and mobilities as high as 3700 cm^2/Vs. Large-scale graphene growth can be achieved on copper [135] with room temperature electron mobilities of more than 4000 cm^2/Vs. Post-growth transfer of those large-scale graphene domains represents a cheaper (compared to CVD) and effective route for real implementation into industrial standards.

Other techniques such as the solvent exfoliation [127] or the chemical route through production of graphene oxide are currently explored; firstly, graphene can be exfoliated in solvents from HOPG [126] with ultrasound, but solvent choices are very limited because of solvent surface energy thermodynamics. As for graphene oxide, this is a century-long well-established production method consisting first of oxidizing graphene (thermal or chemical intercalation), and then dispersing it in a solvent. However, graphene oxide shows fundamentally different electronic properties than individual graphene layer obtained by mechanical exfoliation or supported growth, thus requiring a chemical reduction step (in hydrazine or hydrogen plasma environment) to retrieve original electronic properties. Solution of chemically reduced grapheme oxide is found to consist primarily of monolayer graphene with mobility between 10 and 1,000 cm^2/Vs, with the conduction dominated by hopping transport through regions of highly ordered graphene surrounded by disordered grapheme [136].

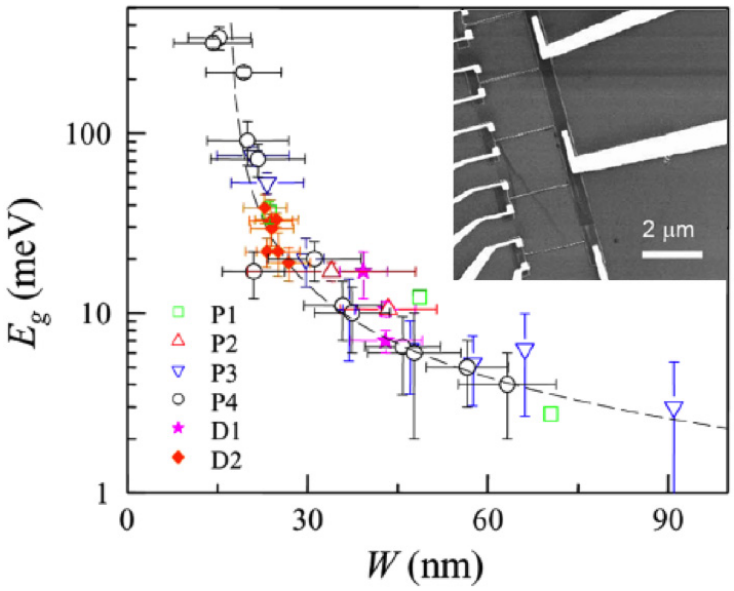
Graphene elevated value of electron mobility at room temperature has rather quickly opened the way to the investigation of a variety of physical phenomenon, ranging from mesoscopic physics [137], Berry's phase [138] and unusual quantum Hall effect [139]. In the case of supported graphene devices, there is a fundamental upper limit of 40,000 cm^2/Vs [140] at room temperature due to trapped charges in the substrate itself [141]. Efficient screening [142] and/or complete removal of the underlying substrate are indeed required in order to enhance the mobility of graphene [143]. Further, it has been shown that in suspended and annealed graphene-based devices, the value of the mobility exceed 200,000 cm^2/Vs, which so far represents the highest value for a semiconductor or a semimetal [144,145]. The mobility is little affected by chemical doping [146] or high electric-field-induced carrier concentrations, suggesting the possibility of achieving rather easily ballistic transport regime on a sub-micrometer scale at 300 K [147].

3.2. Graphene and Few-Graphene Layers Nanoribbons

Although graphene behaves as a semi-metal, it has been shown that it is indeed possible to create an energy gap in graphene through different methods as (i) the inclusion of sp3 hydrocarbon defects in the sp2 lattice [148]; (ii) the distortion of the honeycomb lattice under uniaxial strain [149,150] and (iii) lateral confinement in *ribbon*-like shape [151]. While the first two approaches showing promising

results are not seemingly likely to be implemented for interconnect applications, graphene nanoribbons could indeed represent valid and successful candidates [152]. It has been theoretically shown that the electronic properties of graphene nanoribbons can be tuned from perfectly metallic (zero bandgap) [153], in the case of zig-zag edge ribbons (ZGNR), to semiconducting for armchair ribbons (AGNR), where the engineered energy gap varies with the ribbon width and length. The origin of this energy gap in the band-structure of nanoribbons is attributed to edge roughness [151]. In addition, first principle calculations suggest that the carbon-carbon interatomic distance in the vicinity of the edges armchair GNRs is slightly smaller (~3.5% [154]) than the corresponding equivalent distance in two-dimensional graphene (1.42 Å), which can also induce the opening of an energy gap. This can also be favored if the spin component of zigzag GNRs is also considered. It has been recently shown that multilayer armchair GNRs are characterized by different bandgaps, depending on their width as a result of the interlayer interaction between adjacent layer which determines the magnetic polarization and band structures [155]. Various methods have been proposed to fabricate graphene nanoribbons. In particular, *e*-beam lithography allows producing nanoribbons with tailored lateral dimensions starting form graphene sheet, as shown in Figure 11 where the energy gap of NR varies as function of its width. However, these approaches are limited to a ribbon minimum width of approximately 20 nm, along with great difficulties in achieving smooth edges (roughness edges—larger than 5 nm—will affect the electronic properties of the ribbon itself) [151,156]. On the other hand, chemical routes leading to graphene oxide sheets and nanoplatelets can be followed for specific applications; nevertheless, reduction processes are needed to recover conductive properties of graphene [157,158], step that might not be compatible with interconnect technology process.

Figure 11. Energy gap dependence from ribbon width in lithographically fabricated graphene nanoribbons. Dashed lines in the inset show the value of as predicted by the empirical scaling of versus W. (Inset) SEM image of a representative graphene nanoribbon-based device [151].



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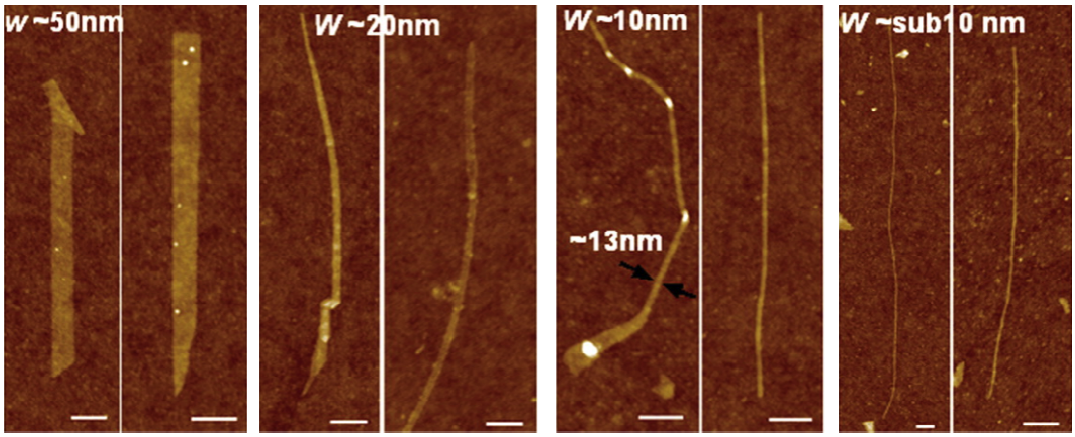
Bottom-up approaches based on the molecular building-up of one-dimensional chains of polyaromatic carbon precursor have been developed [159]; even if this route surely represent a potentially extremely precise method to fabricate graphene nanotibbons with an accurate control over the edge roughness, it is indeed clear that its potential application to large-scale production are not yet ready.

Currently, solution-based methodologies are surely the most promising routes towards the production of graphene nanoribbons, where a very stable compromise between quantity and quality of the ribbons can be reached. Dai and coworkers [160] have shown a simple method to produce GNRs, starting from expandable graphite [161], as shown in Figure 12. Graphite is exfoliated by rapid heating at elevated temperature (1000 °C) in forming gas (Ar/H), dispersed in 1,2-dichloroethane (DCE) solution of poly(*m*-phenylenevinylene-co-2,5-dioctoxy-*p*-phenylenevinylene) and then sonicated. Once a homogeneous solution is obtained, centrifugation is used to separate large and heavy graphite pieces from light and narrow graphene small platelets. Ribbons with different widths down to sub-10 nm region can be thus produced. The same group has lately developed an unconventional and alternative approach based on unzipping mildly oxidized multi-walled carbon nanotubes through mechanical sonication. Quality of these ribbons in terms of disorder and edge roughness is very high, with conductance and mobility of 5 e^2/h and 1500 cm^2/Vs for 10–20 nm long ribbons [162].

Figure 12. Atomic force microscopy images of selected chemically-derived Graphene Nanoribbons (GNRs) with widths of 50, 30, 20, 10 nm and sub-10-nm, respectively. Scale bar is 100 nm. [160]



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Despite the fact that fully metallic GNRs might be hard to produce, this does not rule out the potential of GNRs as interconnects. In fact, semiconducting GNRs have a bandgap smaller than 0.1 eV, value that is equivalent to a copper interconnects with a diameter of 11 nm. If the Fermi energy is larger than half bandgap (few k_BT are sufficient), the first conduction band becomes adequately populated. Hence, for such GNRs, there would be a negligible difference between the ideal conductance of metallic and semiconducting GNRs [163]. Zig-zag and armchair nanoribbons (Fermi Energy = 0.2 eV, interlayer spacing = 0.35 nm) have significantly smaller resistivity than Cu equivalent and densely packed SWNT bundles. For the case of stack of non-interacting GNRs with

smooth edges and Fermi energies above 0.2 eV has been predicted to outperform those of copper wires, especially at small cross-sectional dimensions and long lengths [162]. When compared to Cu/low-k interconnects, graphene nanoribbons hold promising potentials for the following reasons: (i) higher conductivity, with electron mean free path as large as a few hundred nanometer [130]; (ii) resistance to electro-migration due to the strong inherent carbon-carbon bonds which accounts for an extraordinary mechanical strength and a very large current conduction capacity of ~10^9 A/cm^2 (as compared to ~10^6 A/cm^2 in Cu) and (iii) larger in-plane thermal conductivity of approximately 5,300 W/Km, very much comparable to SWNTs bundles [164]. Nevertheless, there exist important current technological limitations and issues that prevent a much faster implementation for graphene nanoribbons in current interconnect applications.

Wafer-scale synthesis of high-quality graphene sheets on arbitrary substrates remains a major challenge. Successful small- and large-scale growths have been obtained on metals and on SiC substrates; however, the non-dielectric nature of the substrate (SiC) limits its applicability as interconnect. Much needed uniformity and grain size compatible with large-scale integration are indeed still in need. Then, to realistically implement the fabrication of GNRs, the crucial effect that edges play on the overall electronic properties of the GNR has to be taken into consideration. In fact, while the mean free path of non-patterned 2D graphene can be as large as several hundred nanometers, in the case of interaction between conducting electrons and edges, the effective mean free path becomes much smaller and hence, edge scattering becomes an a key issue in the electronic transport at the interconnect length scale. The mean free path associated with edge scattering depends on the edge quality (roughness), GNR width, and the ratio of transverse to longitudinal electron speed. Chemically derived GNRs have been shown to have smoother edges when compared to lithographically patterned ones, with a backscattering probability soon increasing from of 0.2, in the first case to 1 [165]. The product of GNR width and the ratio of longitudinal to transverse velocity determine the average length electrons move before interacting with edges [80]. In addition, doping could be used to shift the Fermi energy of graphene layers from the neutrality as a result of the charge accumulated at the graphene/substrate interface. However, this effect diminishes exponentially for upper layers because of the screening effect [166]. To use all the layers within a multilayer ribbon, the Fermi energy of upper layers must be shifted either through edge functionalization or doping, without any effect on the mean free path of electrons, otherwise, the conductance would become considerably smaller because of their bandgap. This conductance degradation is more severe for narrower GNRs with large bandgap.

In the case of GNRs, contact resistance still represent one of the key aspect/challenge in the real implementation of those structures into real interconnects. In fact, in a FET configuration, source-drain contacts have to be characterized by a low resistance contact, while maintaining unaltered the properties of the ribbon itself (*n*- or *p*-channel nature of the device). As in the case of charge transfer to generate doping, modeling has proposed the use of weak bonding contact metals to generate *n*-type contacts at work functions greater than 5.4 eV [167]. More recently, graphene nanoribbon edge states have been doped *n*-type through high temperature electrochemical ammonia treatment [168]. Experiments have demonstrated that *n*-type graphene can be produced through deposition of NH_3 and CH_4 [169], while *p*-type graphene can be produced through deposition of H_2O and NO_2 [170]. Experiments on graphene ribbons indicate that edges can convert to *p*-type, while the center of the ribbon remains *n*-type [171]. The challenge with these doping techniques will be to maintain the

carrier doping in an integrated structure with interconnects. Ohmic contact formation may be easier than in small diameter carbon nanotubes, but a lot still has to be explored in this regard.

Once those numerous technological issues are addressed and overcome, GNRs could potentially be integrated for on-chip interconnect applications in the following two main categories:

(i) *Graphite-like NRs* in place for lower interconnect resistance, especially for short interconnects. In the case of multiple layers, is indeed necessary that the layers in within the stack are electronically decoupled [81,120,172], condition which preserves graphene properties [173]. Further, in this case, all layers need to be electrically contacted.

(ii) *Few-layer GNR interconnects* suitable in order to reduce the interconnect capacitance (~ as much as 50%), delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects in which the delay is dominated by capacitive loading and not resistivity.

4. Conclusions and Future Challenges

Carbon-based nanostructures, and in particular carbon nanotubes and graphene nanoribbons, due to their numerous potential and outstanding properties, have rather quickly attracted the interest within different scientific communities in the quest towards replacement of presently used interconnects.

The present Review has provided the reader with a broad overview of such types of materials and architectures which might be suitable to replace current copper/low-k interconnects at various locations onto an integrated circuit. In particular, carbon nanotubes and graphene nanoribbons both hold great potentials at one or more interconnect levels. Although great advances have so far been achieved since the discovery of CNTs in the early 90s and more recently with the experimental evidence of graphene, many challenges and issues are still open regarding their complete exploitation in working devices. Carbon nanotubes and graphene nanoribbons have shown promising results in terms of RC delay, thermal management and conductance, both on individual objects as well as on assemblies in specific architectures; however, much remains to be advanced in order to achieve a full implementation of these architectures into commercially available IC in the next few years.

In fact, while moving towards the 16-nm technology node, crucial bottlenecks are now going to be faced. When downsizing elements below 100 nm size, interconnects face a number of important challenges. As the lateral dimension of interconnects approaches the mean free path of copper the impact of grain boundary scattering, surface scattering, and the presence of a high-resistivity material as a diffusive barrier layer causes a rapid increase in the overall resistivity. Thus, these phenomena cannot be neglected any further. A full integration of CNTs and GNRs in a real MPU requires the precise and strict control of material properties as well as processes to place those elements at desired locations. At the nanoscale, where at times only few hundreds/thousands of atoms are involved, it becomes of crucial importance to understand the nature of interfaces and any possible dynamics taking place at an interface. In this scenario in fact, metal contacts and electrodes on nanoscale objects behave differently when compared to micro- and macroscopic devices.

Precise control over the nature of defects and their density and location within carbon nanotubes and graphene nanoribbons is also significant and of key importance, since the electronic properties are very sensitive to the presence of any defect and their specificity. For example, controlling the edge

roughness in the case of graphene ribbons is still an open and challenging issue that, if solved, might open the way to a massive use and exploitation of those materials within realistic architectures. Chirality engineering in carbon nanotubes and controlled growth of high-quality graphene at wafer-scale will surely be further needed towards the full implementation of these materials and their architectures in commercially available devices.

It is also important to note that in the last two decades (and more recently for GNRs), great advances have been achieved in placing CNTs/GNRs at precise location or within predefined arrays (with techniques such as dielectrophoresis or fluidic-based approaches); however, it is mandatory that those methods have to be compatible with any current MPU fabrication process. Further, any proposed materials, whether ultralong carbon nanotubes for long distance interconnects or graphene nanoribbons for short local interconnects, have to retain their properties throughout the entire MPU entire fabrication process.

Last, but not least, the economic impact of the introduction of these new materials in the large scale production of integrated circuits has to be considered. With confidence, the best materials to replace copper/low-*k* interconnects would be the ones that will surely bring innovation and improvement of the performances of both materials and devices. However, to reach a full implementation, at the same time, those materials and technologies will have to have less impact on the infrastructures currently related to the interconnects market.

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Conflicts of Interest

The authors declare no conflicts of interest.

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