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An Optoelectronic CMOS Transimpedance Amplifier Using an FVF-Based Low-Dropout Regulator for PSRR Enhancement

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Abstract

This paper presents a flipped-voltage-follower low-dropout regulator (FVF-LDO) for power supply rejection enhancement and low-power operation in CMOS transimpedance amplifiers for optical receiver applications. The proposed FVF-LDO ensures high stability and reliable regulation over a wide range of load conditions by employing a flipped-voltage follower for fast local feedback and improved power supply rejection, while a super-source follower enhances the transient response through increased current-driving capability. A bandgap reference with a 3-bit trimming DAC is adopted to compensate process variations and support stable LDO operations, achieving a temperature coefficient of 19.6 ppm/°C over a wide range of −25 °C to 125 °C. The FVF-LDO exhibits a 101 mV undershoot under a 100 µA-to-10 mA load step with a 100 ns edge time. When applied to an optoelectronic inverter-based active-feedback transimpedance amplifier (TIA), the regulated supply improves the power supply rejection ratio (PSRR) from −6 dB to −38.3 dB. The proposed optoelectronic TIA realized in a 180 nm CMOS process achieves 67 dBΩ transimpedance gain, 869 MHz bandwidth, 66 dB dynamic range, 6.68 pA/$\sqrt{\text{Hz}}$ input-referred noise current spectral density, and 4.68 mW power consumption from a single 1.8 V supply. The proposed TIA chip occupies a core area of 940 × 162 µm^2.

Keywords: BGR; CMOS; LDO; optoelectronic; PSRR; TIA

1. Introduction

State-of-the-art optical receiver systems for short-range sensing and communication applications have attracted significant attention due to their growing usage in areas such as indoor mapping and navigation, LiDAR monitoring, and energy-efficient interconnects. These applications mandate compact and fully integrated circuit solutions that achieve low power consumption while maintaining reliable signal processing performance. In such systems, power supply noise has emerged as a critical bottleneck, particularly in low-voltage implementations where supply fluctuations directly degrade analog front-end performance.

In a typical optical receiver, incident optical signals are converted into electrical currents by a photodetector and subsequently processed by a transimpedance amplifier (TIA) that is followed by post-amplification and digital processing stages. Among these building blocks, the TIA plays a critical role in determining the overall system performance, as it directly amplifies weak input currents and sets the noise and bandwidth characteristics of the optical receivers [1–3].

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As an example, Figure 1 shows the block diagram of a light detection and ranging (LiDAR) sensor system that equips a TIA as the front-end circuit, demanding low-noise and low-power characteristics.

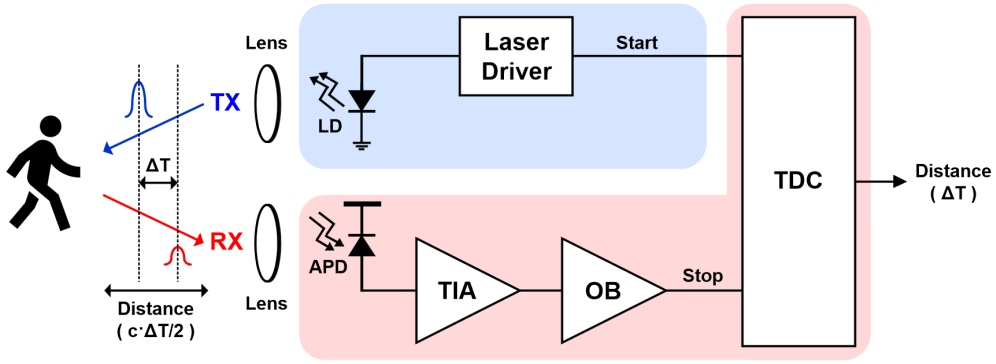


Figure 1. Block diagram of a LiDAR sensor system.

Particularly for the purpose of low-power operations, the inverter-based TIA architecture has been widely adopted due to its high transconductance efficiency [4]. However, unlike conventional current-biased designs, inverter-based TIAs inherently rely on the supply voltage to establish their operating point. Therefore, key parameters such as transconductance, gain, and output common-mode level are strongly dependent on the supply voltage. Consequently, supply noise directly modulates the operating point and effective transconductance of the amplifier, leading to output signal alterations and degradation in gain stability, linearity, and input-referred noise. This issue becomes more critical under low-voltage operations, where limited voltage headroom further signifies the impact of supply variations.

Figure 2 illustrates the effect of power supply noise on inverter-based TIAs, comparing cases without and with supply regulation. In Figure 2a (without LDO), supply noise is directly coupled to the TIA, resulting in output signal variations and degraded performance. This direct coupling yields poor power supply rejection ratio (PSRR), as supply fluctuations are readily transferred to the output.

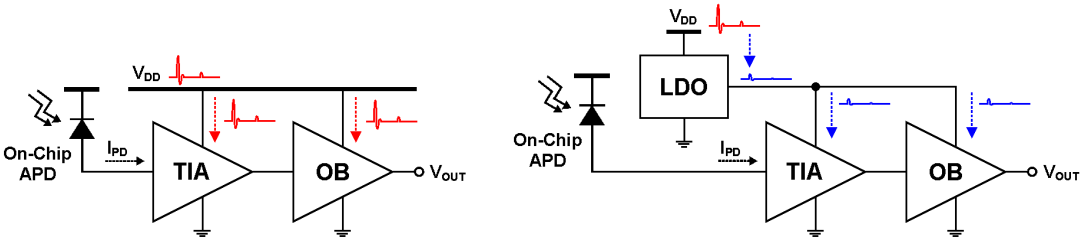


Figure 2. Supply noises in TIA (**a**) w/o LDO and (**b**) w/LDO.

In contrast, Figure 2b shows the case with supply regulation, where an LDO is employed to suppress supply noise before it reaches the TIA. Conventional approaches typically use off-chip LDOs with large output capacitors to improve PSRR and stabilize circuit operations. However, such solutions are not well suited for fully integrated systems due to their reliance on bulky external components, increased system complexity, and limited scalability [5]. More importantly, these approaches typically treat the TIA and power regulation as independent blocks, without explicitly addressing the intrinsic coupling between supply noise and the TIA operating point. Hence, supply-induced variations are

not effectively suppressed at the circuit level, particularly in inverter-based architectures where the operating point is highly sensitive to supply fluctuations.

To alleviate these challenging issues, this paper presents a co-designed TIA-LDO architecture, i.e., an on-chip LDO based on flipped-voltage follower (FVF), which provides low output impedance and fast transient response while enabling full integration without large external capacitors [6]. To ensure stable operations across a wide range of load conditions, a super-source follower (SSF) is incorporated to enhance the loop stability [7]. In addition, a bandgap reference (BGR) is employed to provide a stable and supply-independent voltage reference because the regulation accuracy of LDOs is fundamentally determined by the stability and precision of their reference voltage [8]. However, practical BGR implementations exhibit deviations due to the notorious process variation and device mismatch, which consequently degrades the overall regulation accuracy under process, voltage, and temperature (PVT) conditions.

To compensate for these non-idealities, a trimming digital-to-analog converter (DAC) is integrated to enable post-fabrication calibration of the reference voltage, thus improving robustness and accuracy. Moreover, this paper proposes an integrated receiver front-end circuit featuring an inverter-based TIA with an on-chip FVF-based LDO, as shown in Figure 3. The proposed architecture improves the circuit robustness against supply variations while maintaining low power consumption, hence making it well suited for compact and energy-efficient optical receiver applications.

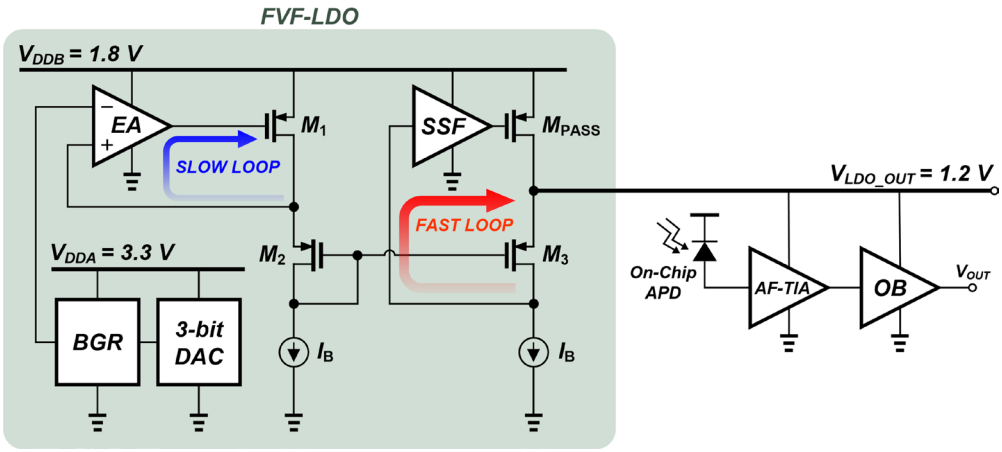


Figure 3. Block diagram of the proposed optical receiver front-end.

2. Optoelectronic TIA with FVF-Based LDO

2.1. Bandgap Reference with 3-Bit DAC

2.1.1. Bandgap Reference Circuit

Bandgap reference (BGR) is well known to generate a stable reference voltage for LDOs. Therefore, LDOs can regulate the supply voltage delivered to the load and suppress disturbances caused by load variations. This reference voltage should be insensitive even to severe PVT variations [9]. Figure 4 shows the schematic diagram of the proposed BGR circuit, where two reference voltages (V_{REF} and V_{BIAS}) are generated. The core of the BGR adopts the Brokaw-cell topology, in which two bipolar transistors (Q_1 and Q_2) with different emitter areas generate a base–emitter voltage difference ΔV_{BE}, which is given by

$$\Delta V_{BE} = V_T ln(n) \quad (1)$$

where n represents the emitter area ratio between Q_1 and Q_2.

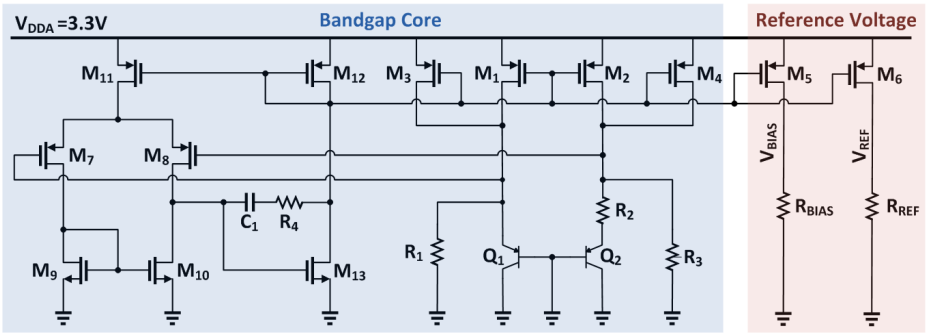


Figure 4. Schematic diagram of the proposed BGR circuit.

This voltage difference is applied across the resistor R_2, thereby generating a proportional-to-absolute-temperature (PTAT) current that is given by

$$I_{PTAT} = \frac{V_T ln(n)}{R_2} \tag{2}$$

On the other hand, the base–emitter voltage (V_{BE1}) exhibits a complementary-to-absolute-temperature (CTAT) characteristic. When applied across the resistor R_3, it generates a current which can be expressed as

$$I_{CTAT} = \frac{V_{BE1}}{R_3} \tag{3}$$

These currents are mirrored through the PMOS current mirrors and converted into a reference voltage across the resistor R_{REF}. Therefore, the final reference voltage is given by

$$V_{REF} = R_{REF}\left(\frac{V_T ln(n)}{R_2} + \frac{V_{BE1}}{R_3}\right) \tag{4}$$

In this work, two PMOS current-mirror branches are implemented to provide both the reference voltage for the LDO and the bias voltage for internal circuits. By adjusting the resistor ratios in each branch, two stable voltages (V_{REF} and V_{BIAS}) are generated. Furthermore, the supply voltage for the BGR is separated from that of the LDO, effectively isolating the BGR voltage generation from the LDO load variations. This separation helps to minimize the influence of transient currents and enhances the overall circuit stability. Hence, both the LDO reference voltage and the internal bias voltage can maintain high accuracy, while reducing the sensitivity to supply noise effectively.

2.1.2. Trimming DAC Circuit

As mentioned above, the BGR circuit must provide a stable reference voltage against the variations in supply voltage and temperature. However, process variations might introduce deviations in the output reference voltage. To compensate for these process-induced variations, a trimming DAC circuit should be incorporated into the proposed design, as depicted in Figure 5.

The overall architecture of the proposed 3-bit trimming DAC employs a 3-to-8 decoder to control a switch array. Accordingly, the decoder outputs selectively activate switches connected to the trimming resistor network, therefore determining the current paths within the network. The trimming resistor network is implemented using parallel resistors with a uniform step size of 600 Ω, allowing the effective resistance to be adjusted from 600 Ω to 4.8 kΩ. By controlling the current flowing through the trimming resistors, the output voltage of the BGR can be finely tuned. This trimming mechanism compensates for the

process variations and ensures that the reference voltage remains close to the target value across various chips [10].

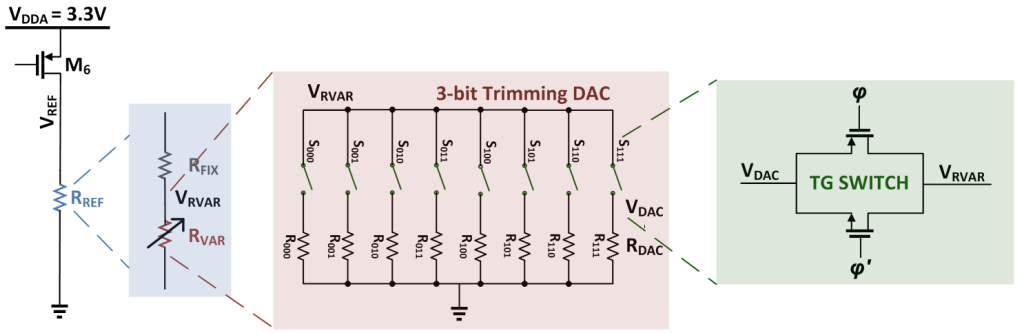


Figure 5. Simplified architecture of the proposed 3-bit trimming DAC.

Since the trimming DAC operates in a block requiring precise voltage control, accurate voltage transmission through the switches is essential. For this purpose, transmission gate (TG) switches are employed for bit selection. This TG structure enables stable voltage transmission across the entire output voltage range through the complementary operations of the two transistors, thereby mitigating the signal-level-dependent resistance variation that may occur in a single MOS switch. Also, the channel width of the switching transistors is increased to reduce the on-resistance, while the channel length is also enlarged to suppress resistance variations caused by short-channel effects and channel length modulation. Furthermore, increasing the switch device area reduces the device mismatch, thus improving the voltage tuning accuracy of the DAC. Hence, the proposed trimming DAC achieves stable voltage transfer characteristics and improved voltage adjustment accuracy.

2.2. FVF-LDO Regulator with SSF

2.2.1. Circuit Description

Figure 6 shows the schematic diagram of the proposed flipped-voltage-follower low-dropout regulator (FVF-LDO) with a super-source follower (SSF), consisting of five main building blocks, i.e., an error amplifier (M_1–M_4), a V_{SET} generator (including M_5, M_6, and C_1), and an FVF-based output stage (M_7–M_{10}), the PMOS pass transistor (M_P), and the feedfowrad network (R_Z–C_F). The current sources (I_1–I_5) provide the required bias currents for each sub-block.

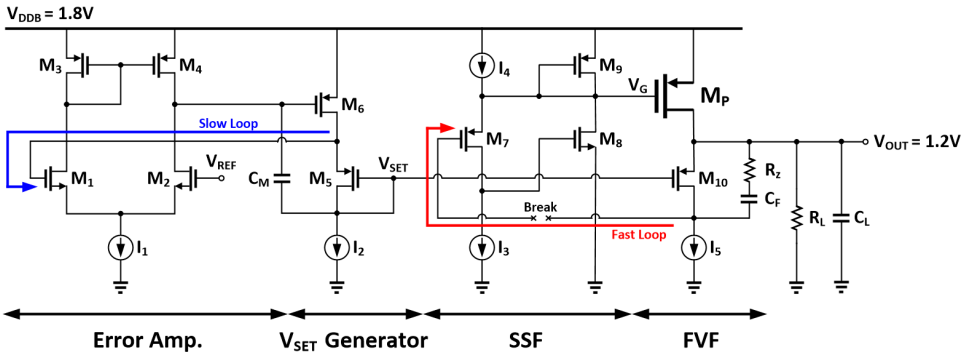


Figure 6. Schematic diagram of the FVF-LDO with SSF.

In the error amplifier (EA), M_1 and M_2 form the differential input pair while M_3 and M_4 act as active loads. The gate of M_2 is connected to the reference voltage (V_{REF}), and the other input senses the feedback information derived from the output regulation path. Therefore, EA compares the output-related feedback signal with V_{REF} and generates

an error signal that controls the subsequent V_{SET} node. In other words, this EA block determines the low-frequency regulation accuracy of the LDO [11].

The intermediate generator produces the internal control voltage (V_{SET}). Instead of directly driving the pass-transistor gate from the EA output, the proposed structure first establishes V_{SET} that serves as the interface between the slow loop and the fast loop [12]. The slow loop determines the desired regulation level, while the fast loop rapidly reacts to load-induced output disturbances. In particular, a capacitor (C_M) is introduced to shape the frequency response of this node and to stabilize the slow loop.

Transistors M_7–M_{10} form the local FVF and SSF structure, and M_P acts as the pass-device supplying the load currents from V_{DDB} to V_{OUT}. The output node is loaded by R_L and C_L, which represent the equivalent load resistance and capacitance seen by the LDO. In addition, the series network R_z–C_F is connected near the output stage to improve the loop stability by introducing a zero and reshaping the non-dominant poles [13,14].

The principal operations of the FVF-LDO can be understood as the combination of a slow loop and a fast loop. The slow loop starts from the EA, passes through the V_{SET} generator, and determines the long-term DC regulation of the output voltage. In contrast, the fast loop is locally formed by the FVF and SSF around M_7–M_{10} and M_P, and it rapidly suppresses output variations caused by the load transients. Therefore, the proposed FVF-LDO regulator can achieve accurate output regulation, high stability, and fast transient response simultaneously.

2.2.2. Small Signal Analysis

Figure 7 shows the small-signal model of the fast loop in the proposed FVF-LDO, where $g_{m,SSF}$, g_{mp}, and g_{m10} denote the effective transconductance of the SSF block, the transconductance of M_p, and the transconductance of M_{10}, respectively. Also, R_G and C_G represent the parastic resistance and capacitance at V_G. In addition, R_{B5} and C_{B5} represent the drain-source resistance and parasitic capacitance of I_{B5}.

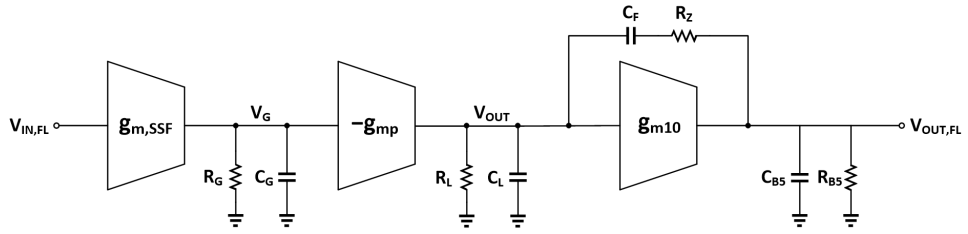


Figure 7. Small-signal model of the fast loop in the FVF-LDO with SSF.

Based on this small-signal model, the transfer function of the fast loop is given by

$$H(s) = \frac{V_{out,FL}}{V_{in,FL}} = \frac{g_{m,SSF}g_{mp}g_{m10}R_GR_LR_{B5}\left(1 - sC_F\left(\frac{1}{g_{m10}} - R_z\right)\right)}{(1 + sR_GC_G)(1 + sa_1 + s^2a_2 + s^3a_3)} \tag{5}$$

where the denominator coefficients are described as follows.

$$a_1 = R_L[C_L + C_F(1 + g_{m10}R_{B5})] + R_{B5}(C_{B5} + C_F) + C_FR_z \tag{6}$$

$$a_2 = R_LR_{B5}(C_LC_{B5} + C_LC_F + C_{B5}C_F) + R_zC_F(R_LC_L + R_{B5}C_{B5}) \tag{7}$$

$$a_3 = R_LR_{B5}R_zC_LC_{B5}C_F \tag{8}$$

Hence, the low-frequency (LF) gain of the fast loop is obtained at $s \to 0$ as

$$A_0 = g_{m,SSF}R_G \cdot g_{mp}R_L \cdot g_{m10}R_{B5} \tag{9}$$

It is clearly seen that the LF gain is determined by the cumulative gain contribution of the SSF, the common-source stage, and the common-gate stage. Such a large LF gain enables strong corrective action even for small output-voltage perturbations and directly contributes to suppressing the transfer of supply ripple or disturbance to the output node. Therefore, the large A_0 can be interpreted as one of the key factors supporting the PSRR improvement at low frequencies in the proposed structure [15].

From the numerator of the transfer function, the zero frequency can be written as

$$z_1 = \frac{1}{C_F\left(\frac{1}{g_{m10}} - R_z\right)}. \tag{10}$$

The zero location in (10) is determined by the relative magnitudes of R_z and $1/g_{m10}$. When $R_z < 1/g_{m10}$, the zero is located in the right-half plane (RHP), whereas it is placed in the left-half plane (LHP) when $R_z > 1/g_{m10}$. When $R_z = 1/g_{m10}$, the zero is pushed to a very high frequency and becomes practically negligible [16]. In this design, R_z was chosen such that $R_z > 1/g_{m10}$ over the intended operating region so that the zero is placed in the LHP. This helps alleviate the phase degradation caused by non-dominant poles, thus leading to a more favorable phase margin and improved loop stability [17]. The poles can be summarized as follows:

$$p_1 \approx \frac{1}{R_L[C_L + C_F(1 + g_{m10}R_{B5})] + R_{B5}(C_{B5} + C_F) + C_F R_z} \tag{11}$$

$$p_2 = \frac{1}{R_G C_G} \tag{12}$$

$$p_3, p_4 : \ obtained\ from\ 1 + sa_1 + s^2a_2 + s^3a_3 \tag{13}$$

where p_1 is the dominant pole associated with V_{OUT}, and both the load capacitance and the feedforward compensation path contribute to the effective time constant. p_2 is the high-frequency pole formed at V_G, while p_3 and p_4, together with p_1, are the higher-order poles determined from the cubic denominator and reflect the coupled response of V_{OUT} and $V_{OUT,FL}$. In addition, C_F forms the feedforward compensation path and affects the overall pole-zero distribution. If the Miller effect is sufficiently strong, p_1 can be approximated as

$$p_1 \approx \frac{1}{R_L C_F g_{m10} R_{B5}} \tag{14}$$

indicating that the dominant pole is mainly determined by the Miller-amplified compensation capacitance seen at V_{OUT}.

This pole-zero structure is directly related to the PSRR enhancement of the proposed FVF-LDO. Noise components contained in the supply voltage tend to propagate to the output node through the pass transistor [18]. However, the proposed fast loop rapidly senses the output-voltage variations and immediately adjusts the operating condition of the pass transistor through the internal control node. In this process, the large LF gain effectively suppresses the LF supply ripple, while the zero generated by the R_z–C_F compensation path compensates for the phase degradation caused by non-dominant poles in the mid- and high-frequency range, thereby extending the frequency range over which effective supply-noise suppression can be maintained [19]. Furthermore, when the pole at the gate-control node is shifted to sufficiently high frequencies, the charging and discharging speed of the pass-transistor gate is improved, allowing correct action to take place before the supply disturbance is fully transferred to the output. Therefore, the PSRR improvement of the proposed FVF-LDO can be understood as the combined results of large LF gain, fast gate control, and the pole-zero characteristics shaped by the R_z–C_F compensation

network. Figure 8 shows the small-signal model of the SSF block, where the effective transconductance of the SSF is given by

$$g_{m,SSF} = \frac{g_{m7}r_{o7}}{g_{m7}r_{o7} + 1 + \frac{1}{g_{m8}r_{o8}}} \tag{15}$$

$$R_{o,SSF} \approx \frac{1}{g_{m8} + g_{m7}r_{o7}g_{m8} + \frac{1}{r_{o8}}} \tag{16}$$

where $g_{m7,8}$ and $r_{o7,8}$ are the transconductance and output resistance of M_7 and M_8, respectively.

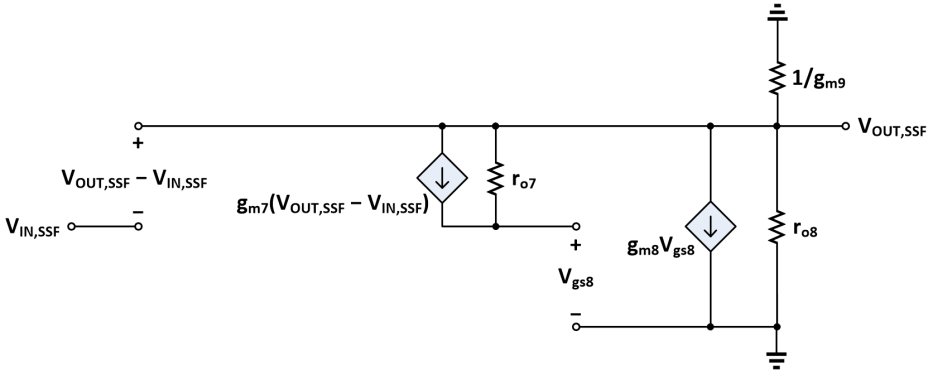


Figure 8. Small-signal model of the SSF.

The SSF in the proposed fast loop provides a lower output resistance and stronger gate-driving capability than a conventional source follower (SF). In a conventional SF, the output resistance is fundamentally limited, which restricts the charging and discharging speed when driving the pass-transistor gate with a large parasitic capacitance. This limit slows down the internal control node and eventually constrains the loop bandwidth, the transient response, and the supply-noise rejection capability [20]. By contrast, the proposed SSF can achieve a lower output resistance through its active local feedback, enabling faster drive of the pass-transistor gate. This reduces the driving resistance seen at the gate-control node and shifts the corresponding pole to a higher frequency, which in turn improves both the speed and stability of the fast loop. Such a low output resistance also enhances the charging and discharging speed, thus allowing faster corrective action against the output perturbations and enabling the gate control to respond before supply-voltage variation is fully transferred to the output node. Hence, the SSF in the proposed structure should not be regarded simply as a buffer replacement, but rather as a deliberate choice to overcome the driving limitation of a conventional SF while simultaneously improving the fast loop bandwidth, the transient response, and the PSRR performance.

2.2.3. Power Supply Rejection (PSR)

In the absence of regulation, variations at the supply node are transferred to the output through the finite small-signal resistance ($r_{ds,p}$) of the pass device [21]. In the proposed FVF-LDO, however, the fast loop senses the resulting output variation and adjusts the pass-transistor gate voltage, thus reducing the effective output impedance at the regulated node and suppressing the propagation of the supply noise. The open-loop shunt impedance seen at the output node is given by

$$Z_{o,FL}(s) = \frac{1}{\frac{1}{R_L} + \frac{1}{R_{B5}} + s(C_L + C_{B5})}. \tag{17}$$

When R_{B5} is sufficiently large and C_{B5} is much smaller than C_L, it can be approximated as

$$Z_{o,FL}(s) \approx R_L \parallel \frac{1}{sC_L}. \tag{18}$$

Since the closed-loop output impedance is reduced by the fast loop gain, the output impedance of the FVF-LDO (in the frequency range where the fast loop gain is sufficiently large) is given by

$$Z_{o,LDO}(s) \approx \frac{Z_{o,FL}(s)}{A_{FL}(s)}. \tag{19}$$

Substituting this equation into the PSR definition gives

$$PSR_{LDO}(s) = \frac{Z_{o,LDO}(s)}{r_{ds,p} + Z_{o,LDO}(s)} \approx \frac{Z_{o,FL}(s)/A_{FL}(s)}{r_{ds,p} + Z_{o,FL}(s)/A_{FL}(s)} \approx \frac{1}{1 + A_{FL}(s)\frac{r_{ds,p}}{Z_{o,FL}(s)}} \tag{20}$$

which clearly reveals that the PSR is determined by two main factors: the output-node open-loop shunt impedance and the fast loop gain [22]. As $A_{FL}(s)$ increases, the effective output impedance decreases, and the amount of supply ripple transferred to the output is correspondingly reduced. Therefore, the PSR improvement of the proposed FVF-LDO can be interpreted as the result of the active impedance reduction at the output node by the fast loop. At low frequencies, the output-node impedance is dominated by the load resistance, such that

$$Z_{o,FL}(0) \approx R_L. \tag{21}$$

Also, the LF fast loop gain is given by

$$A_{FL}(0) = A_0 = g_{m,SSF}R_G \cdot g_{mp}R_L \cdot g_{m10}R_{B5}. \tag{22}$$

Accordingly, the LF PSR (if $A_0 \gg 1$) can be approximated as

$$PSR_{LDO}(0) \approx \frac{1}{1 + A_0\frac{r_{ds,p}}{R_L}} \approx \frac{R_L}{A_0\, r_{ds,p}}. \tag{23}$$

This equation indicates that the LF PSR is inversely proportional to the LF fast loop gain, confirming that a larger fast loop gain directly improves the rejection of supply ripple. In the mid- and high-frequency range, the PSR behavior is additionally affected by the compensation path [23]. This path helps to maintain the effectiveness of the fast loop by preventing an abrupt degradation of the loop response, thereby extending the frequency range over which supply-noise suppression is preserved.

In addition, the low output resistance of the SSF enables faster charging and discharging of the pass-transistor gate, which allows the FVF-LDO regulator to respond more quickly to supply disturbances. Consequently, the proposed structure improves PSR by actively lowering the output impedance through fast loop action over a wide frequency range.

2.3. Active-Feedback Transimpedance Amplifier

A transimpedance amplifier (TIA) is employed as the front-end circuit of an optical receiver to convert an input photocurrent signal into an output voltage. The input photocurrent is generated by an on-chip P^+/N-well avalanche photodiode (APD), which is a previously fabricated and experimentally characterized device reported in [24]. The APD implemented in a 180 nm CMOS process exhibited a responsivity of 2.72 A/W with a junction capacitance of approximately 490 fF. These parameters are based on the measured results from the prior work and are used in this work to enable a realistic device-level

evaluation of the proposed receiver front-end. Figure 9 shows the block diagram of the active-feedback transimpedance amplifier that comprises an inverter-based CMOS TIA and an inverter-based output buffer (OB). Both blocks are powered by the proposed FVF-LDO. The TIA topology is based on the one previously described in [25], such that a shunt-feedback inverter-based amplifier stage is followed by an OB.

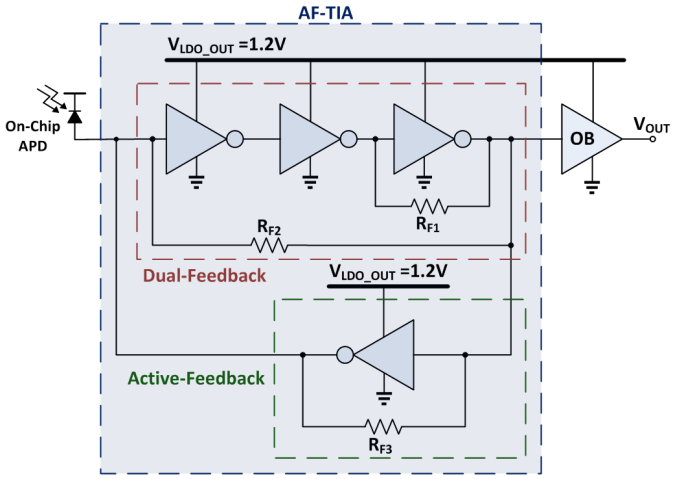


Figure 9. Block diagram of the active-feedback TIA.

In this architecture, the inverter-based multi-stage amplifier provides sufficient voltage gain while maintaining a relatively low input resistance that reduces the input current loss and extends the bandwidth. By utilizing the FVF-LDO, the TIA operates with a supply voltage of 1.2 V. It should be noted that the available voltage headroom becomes limited under a reduced supply voltage, making the circuit more susceptible to supply noise and variations. Therefore, stable supply regulation is crucial to ensure reliable operations. Finally, an OB is employed to isolate the load capacitance from the core amplifier and to match the output impedance close to 50 Ω, facilitating standard measurements. This configuration enables convenient interface with external test instruments as well as potential sensor systems.

3. Layout and Simulation Results

Figure 10 illustrates the layout of the proposed optoelectronic TIA with an FVF-LDO, where the chip core occupies an area of 940 × 162 μm^2. Specifically, an on-chip avalanche photodiode was integrated together with the active-feedback TIA not only to facilitate the PC-board designs for testing but also to avoid the unnecessary signal distortions attributed to the well-known inductance effect of bond-wires on chip.

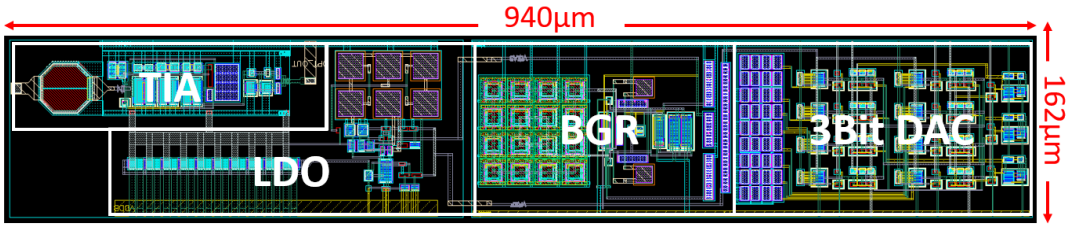


Figure 10. Layout of the proposed optoelectronic TIA.

Post-layout simulations were conducted by utilizing the model parameters of a standard 180 nm CMOS process. First, the performance of the proposed BGR with an integrated 3-bit trimming DAC was evaluated through temperature, supply, transient, and power-

supply variation simulations across multiple process corners. The trimming DAC provides fine adjustment of the BGR output voltage V_{REF} to compensate for process variations.

Figure 11a shows the temperature coefficient (TC) of the reference voltage (V_{REF}) over the range of −30 °C to 130 °C. The simulated TC values are 18.8 ppm/°C (TT), 29.6 ppm/°C (SS), 71.6 ppm/°C (FF), 20.6 ppm/°C (SF), and 17.0 ppm/°C (FS), respectively.

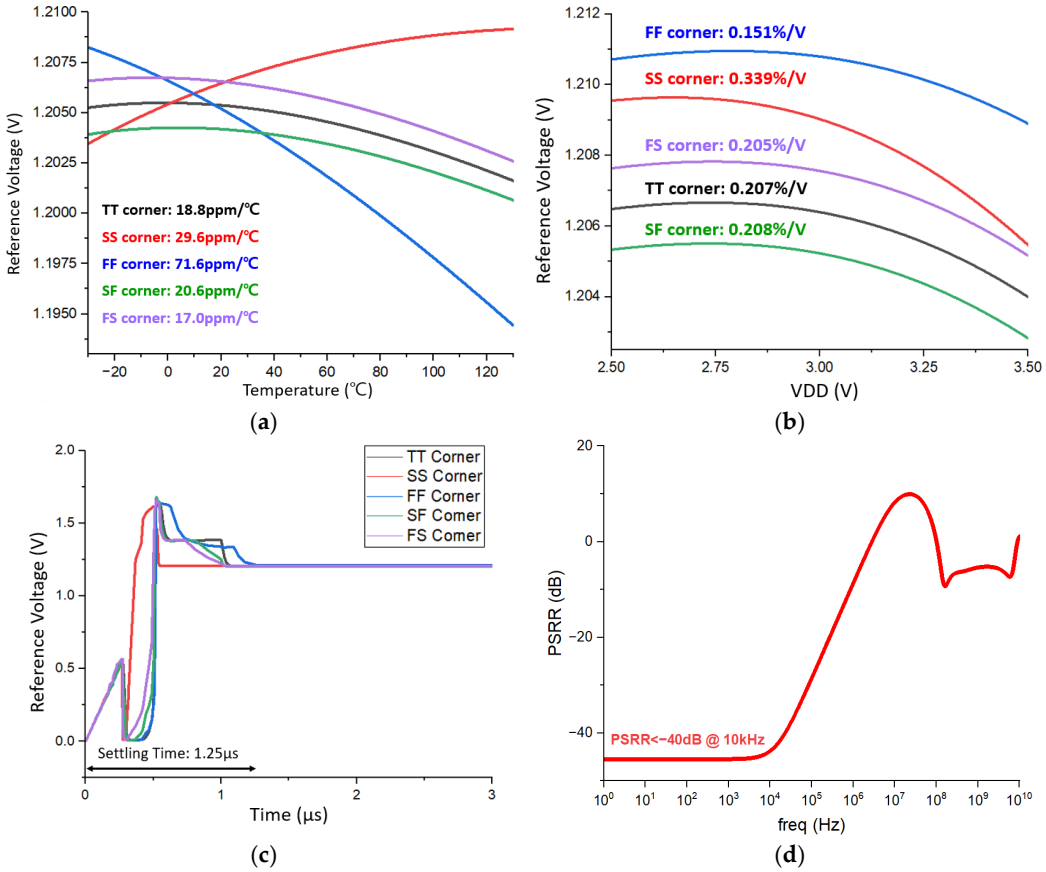


Figure 11. Simulated results of the proposed BGR across TT, SS, FF, SF, and FS corners: (**a**) TC of the reference voltage from −30 °C to 130 °C. (**b**) Line regulation with VDD ranging from 2.5 V to 3.5 V. (**c**) Startup transient response across TT, SS, FF, SF, and FS corners. (**d**) PSRR of V_{REF}.

These results indicate that the 3-bit trimming DAC effectively stabilizes V_{REF} across corners, with the FF corner exhibiting slightly higher variation. Figure 11b presents the line regulation of V_{REF}, obtained by sweeping the supply voltage V_{DD} from 2.5 V to 3.5 V. The simulated deviations are 0.207%/V (TT), 0.339%/V (SS), 0.151%/V (FF), 0.208%/V (SF), and 0.205%/V (FS), demonstrating the robust immunity of the BGR output to the supply voltage fluctuations across all corners. In Figure 11c, the dynamic performance of V_{REF} is assessed through transient simulations with a 1 μs ramp input. The output voltage is settled within 1.25 μs in all the process corners, confirming fast and stable startup behavior. Figure 11d depicts the power supply rejection ratio (PSRR) of the BGR with the trimming DAC, achieving a PSRR of −45.5 dB. Despite the presence of the switching network and TG-based circuitry, the PSRR remains adequate for practical applications. Overall, these post-layout simulation results demonstrate that the proposed BGR with the integrated TG-based trimming DAC provides stable reference voltage generation across process, voltage, and temperature variations.

The frequency response of the slow loop and fast loop of the proposed FVF-LDO is shown in Figures 12 and 13, respectively. All results were evaluated under the SS, TT, and FF process corners. In the slow loop response of Figure 12, the phase margins are 84°, 83.6°,

and 81.6° at the SS, TT, and FF corners, respectively, indicating sufficient stability margin. Also, these values remain the same under both light load and heavy load conditions. Furthermore, the variation across process corners is small, demonstrating that the proposed structure operates stably against both load and process variations.

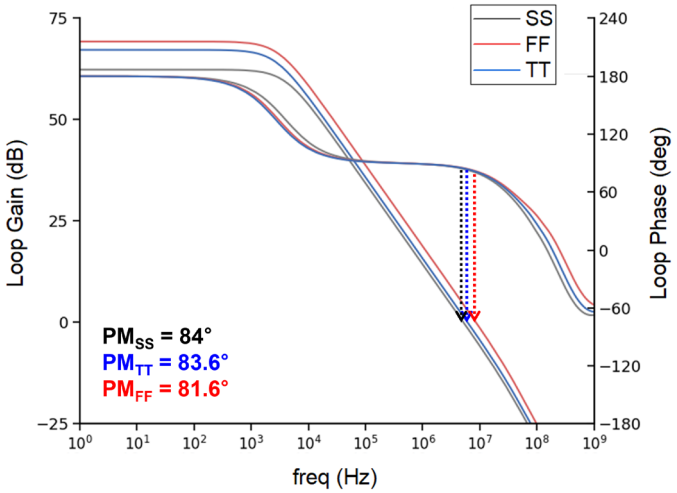


Figure 12. Simulated frequency response of the slow loop of the FVF-LDO with SSF.

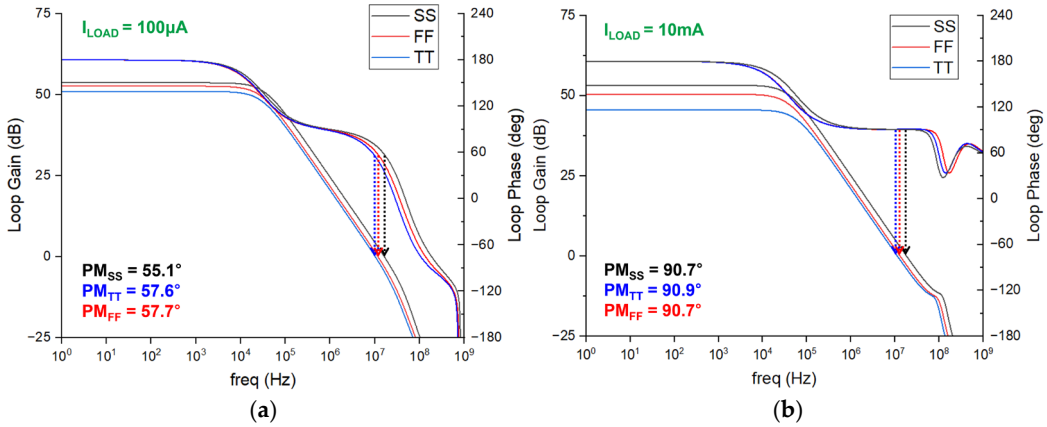


Figure 13. Simulated frequency response of the fast loop of the FVF-LDO with SSF with (**a**) I_{LOAD} = 100 µA and (**b**) with I_{LOAD} = 10 mA.

For the fast loop, the phase margins under the light load condition are 55.1°, 57.6°, and 57.7° for the SS, TT, and FF corners, respectively, confirming sufficient stability margin even at light load. Under the heavy load condition, the phase margins are 90.7°, 90.9°, and 90.7° respectively, therefore showing a larger stability margin than in the light load case. Moreover, the variation in phase margin across process corners is small in both load conditions, indicating that the proposed structure maintains stable operation against process variation. These results confirm that both the slow loop and fast loop of the proposed dual-loop FVF-LDO maintain sufficient stability margin over a wide load range and across process corners.

Figure 14 shows the load transient response of the FVF-LDO, where the load current varies between 100 µA and 10 mA, with both the rising and falling edge times set to 100 ns. Under this condition, the undershoot and overshoot are 67 mV and 59 mV at the FF corner, 101 mV and 89 mV at the TT corner, and 130 mV and 114 mV at the SS corner, respectively. Although the magnitudes of the output-voltage variation differ across process corners, the output voltage quickly returns to its steady-state value without severe ringing in all

PVT corners. This demonstrates that the proposed fast loop effectively controls the pass-transistor gate during abrupt load current changes while maintaining sufficient damping.

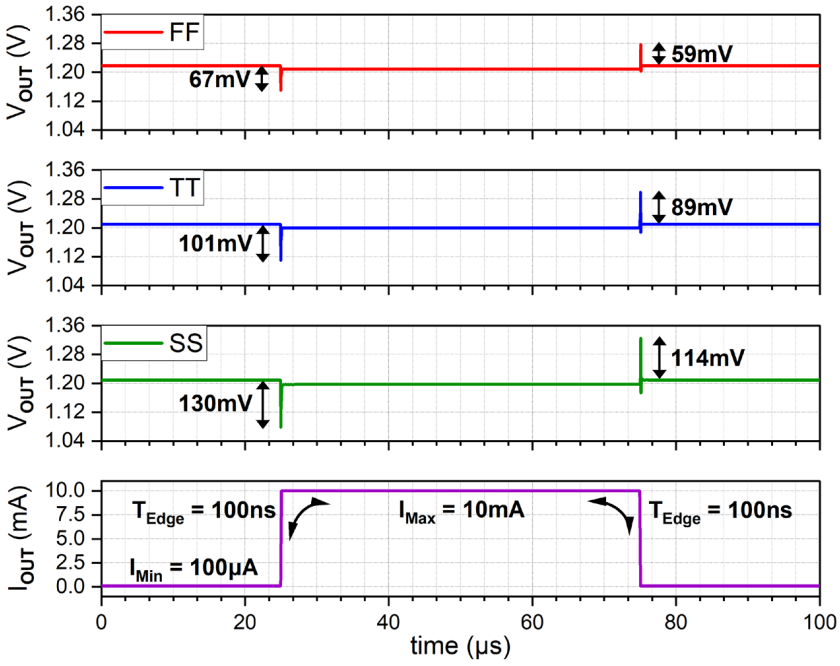


Figure 14. Simulated load transient response of the FVF-LDO with SSF.

Figure 15 shows the simulated PSR characteristics of the proposed FVF-LDO under different load current conditions and process corners. For the PSR simulations, the BGR was biased with a constant supply, while the supply ripple was injected only into the LDO supply. Under the light load condition, the low-frequency PSR is −30 dB, −32.5 dB, and −33.4 dB for the SS, TT, and FF corners, respectively, while under the heavy load condition, the corresponding values are −27.7 dB, −32 dB, and −33.5 dB, respectively. The low-frequency PSR is mainly determined by the low-frequency fast loop gain. As the frequency increases, the PSR degrades due to the reduction in loop gain. The peaking observed in the mid- and high-frequency range may be attributed to the pole-zero characteristics of the internal loop. These results show that the PSR of the proposed FVF-LDO is determined by both the fast loop gain and its frequency response characteristics.

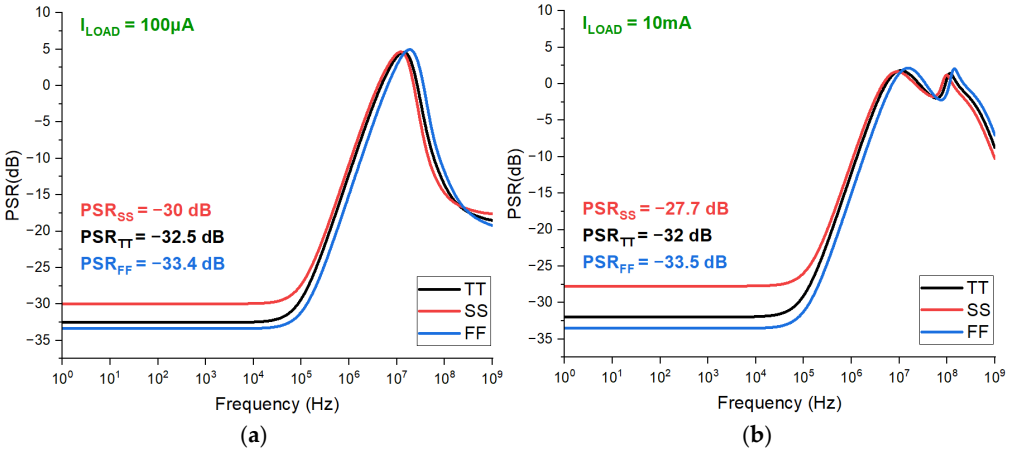


Figure 15. Simulated PSR of the fast loop of the FVF-LDO with SSF with (**a**) I_{LOAD} = 100 µA and (**b**) I_{LOAD} = 10 mA.

Figure 16 shows the post-layout simulation results of the proposed optoelectronic TIA, achieving a transimpedance gain of 67 dBΩ, a −3 dB bandwidth of 869 MHz, and an average input-referred noise current spectral density of 6.68 pA/$\sqrt{\text{Hz}}$ over the frequency range of interest.

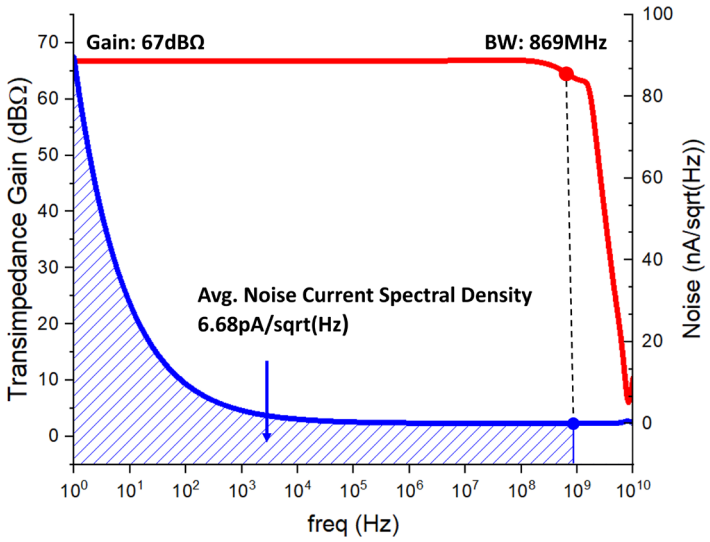


Figure 16. Simulated results of the proposed optoelectronic TIA in terms of transimpedance gain, bandwidth, and input-referred noise.

Figure 17 illustrates the simulated pulse response of the proposed optoelectronic TIA under varying input current amplitudes ranging from 1 μA_{pp} to 1.5 mA_{pp}. As the input current increases, the output voltage amplitude correspondingly increases. However, beyond 150 μA_{pp}, the output pulse amplitude begins to saturate and remains nearly constant for larger input currents.

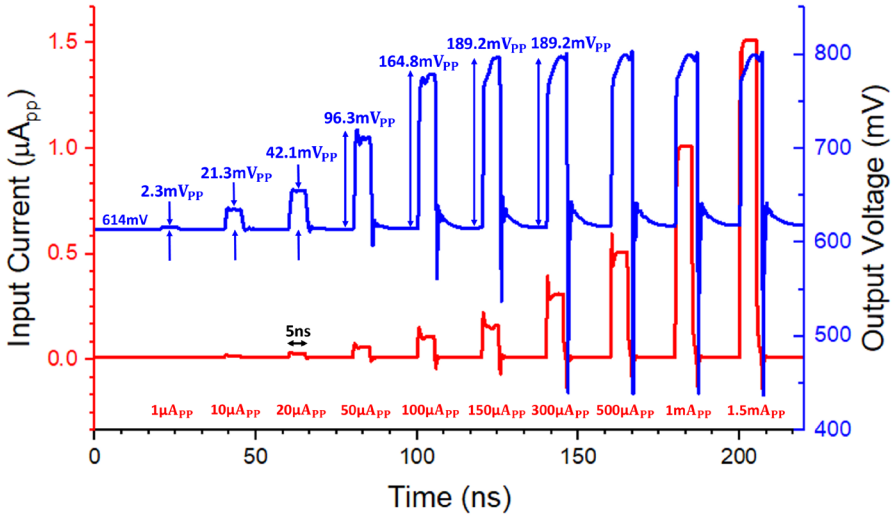


Figure 17. Simulated pulse response of the proposed optoelectronic TIA for different input currents.

Figure 18 shows the simulated eye-diagrams of the proposed optoelectronic TIA under the different input current levels and data rates. At a fixed data rate of 500 Mb/s, the simulated eye-diagrams are presented for two input currents of 1 μA_{pp} and 50 μA_{pp}, respectively. Although slight fluctuations are observed, the eye-openings remain clearly distinguishable in both cases.

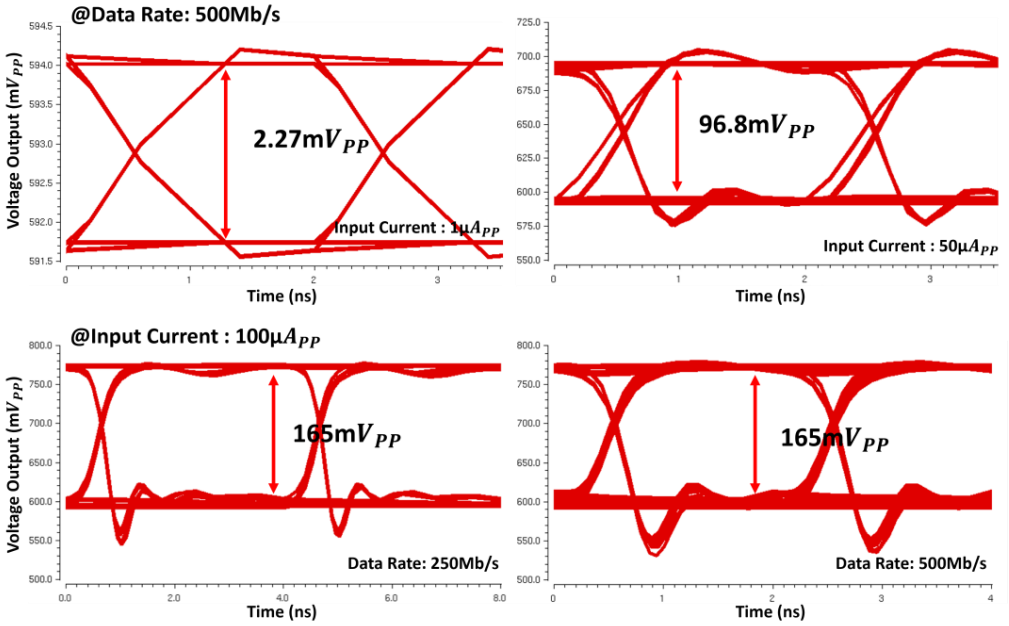


Figure 18. Simulated eye-diagrams of the proposed optoelectronic TIA at different input current levels and data rates.

With the input current amplitude fixed at 100 μA_{pp}, the eye-diagrams at the two different data rates of 250 Mb/s and 500 Mb/s exhibit consistently open eyes, indicating stable signal integrity across the evaluated data rates.

Figure 19 compares the PSRR of the proposed TIA with and without the on-chip FVF-LDO. The TIA with the FVF-LDO shows an improvement of ~30 dB in PSRR when compared to the case without the FVF-LDO. This confirms that the inclusion of the on-chip FVF-LDO effectively reduces the supply noise and therefore enhances the robustness of the TIA against supply variations.

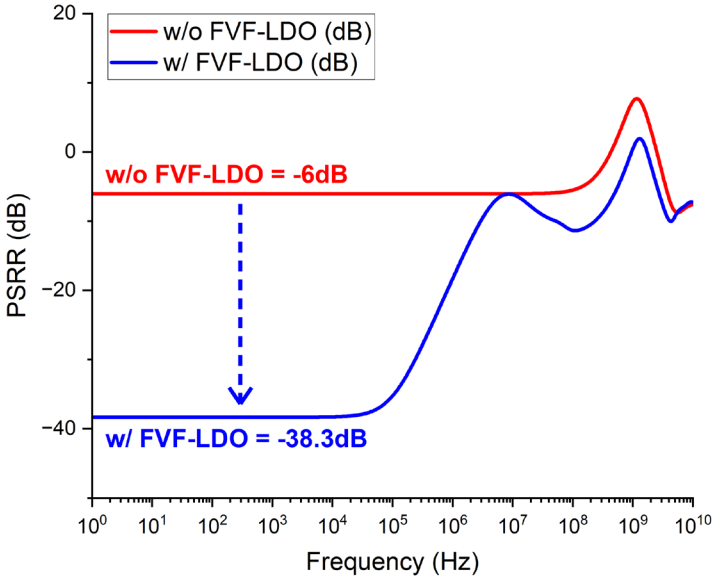


Figure 19. Simulated PSRR comparison of the proposed optoelectronic TIA with and without the on-chip FVF-LDO.

Table 1 compares the performance of the proposed optoelectronic TIA with prior CMOS works. Ref. [26] realized a differential optical receiver in a 28 nm CMOS, targeting high-speed operations with a wideband TIA featuring high power supply rejection.

However, the power dissipation per channel was considerable, and the noise current spectral density was also relatively high, therefore demonstrating its limited applicability in low-power, low-noise optical interconnects.

Table 1. Performance comparison with previously published CMOS optical receivers.

Parameters		[26]	[27]	[28]	[29]	[30]	**This Work**
CMOS technology (nm)		28	65	130	130	180	180
LDO		On-chip	On-chip	Off-chip	Off-chip	Off-chip	On-chip
PD	Type	Off-chip (N/A)	Off-chip (PIN PD)	Off-chip (Equiv. PD)	Off-chip (Equiv. PD)	Off-chip (Equiv. PD)	On-chip (APD)
	C_{pd} (pF)	-	0.25	0.2	0.5	1.5	0.5
	Responsivity (A/W)	-	0.4	-	-	-	2.72
	Wavelength (nm)	-	850	-	-	-	850
Input configuration		Diff.	Single-ended	Single-ended	Diff.	Diff.	Single-ended
Max. TZ gain (dBΩ)		66	42	65	86	100	67
Bandwidth (MHz)		21,000	24,000	8500	516	260	867
Dynamic range (dB)		-	56.6 *	-	56.2 *	79.3	57.6
Noise current spectral density (pA/$\sqrt{}$Hz)		12.3	16	14.4	7.5	3.3	6.68
PSRR (dB) @ 1 kHz		≤ -70 **	-	-100 *	-23 **	-61 **	-38.3
PSRR (dB) @ 100 kHz		≤ -70 **	-	-50 *	-	-61 **	-35.3
Power dissipation per channel (mW)		17.7	3.0	23.5	24	153	4.68
Chip area (mm^2)		-	0.08	0.072	0.022	0.012 (TIA only)	0.15
*** FoM ($\times 10^4$)		19.2	6.3	4.47	5.72	5.15	6.21

* Values estimated from the published figures. ** Values reported in the original publication (no frequency-specific data provided). *** $FoM = \frac{Z_T}{i_n} \cdot \frac{BW}{PD}$.

Ref. [27] employed an off-chip PIN photodiode with a wideband TIA for high-speed operations. However, the inherently low responsivity of the PIN photodiode degraded the achievable sensitivity, thus requiring relatively high optical input power. Moreover, the bandwidth-oriented design constrained the transimpedance gain, reducing its effectiveness in low signal conditions. In addition, the usage of a wire-bonded photodiode introduced parasitic effects, leading to signal distortion and increased system complexity.

Ref. [28] presented a single-ended optical receiver using an off-chip photodiode in a 130 nm CMOS, achieving a similar transimpedance gain to this work. Yet, the bandwidth was significantly higher, approximately ten times wider. Therefore, the noise current spectral density was relatively high and the power dissipation per channel was excessive, over four times that of the proposed optoelectronic TIA. This would limit its suitability for energy-efficient optical interconnect applications.

Ref. [29] reported a fully differential optical receiver in a 130 nm CMOS, showing a high transimpedance gain. The differential architecture enabled a PSRR of −23 dB even without an on-chip LDO. However, the absence of on-chip regulation led to limited PSRR and higher power consumption.

Ref. [30] suggested a differential optical receiver in a 180 nm CMOS using an off-chip equivalent photodiode. The design demonstrated a very high PSRR of −61 dB, revealing excellent supply-noise rejection performance. However, this enhancement was achieved at

the cost of substantial power consumption (153 mW). These results confirm the tradeoff between high PSRR and energy efficiency in differential architectures.

On the contrary, the proposed optoelectronic TIA integrates an on-chip LDO and an on-chip avalanche photodiode (APD) in a 180 nm CMOS. This approach enables the effective suppression of supply noise through local regulation while maintaining low-noise operations at the input stage. In addition, the on-chip integration of the photodiode eliminates the parasitic effects associated with off-chip bond-wire interconnections, thereby reducing signal distortion and system complexity. In consequence, the proposed optoelectronic TIA architecture provides a balanced solution in terms of low noise, low power consumption, and enhanced supply-noise rejection for optical receiver applications.

4. Conclusions

This paper presents an integrated chip-level solution combining an optoelectronic TIA with an on-chip LDO. The proposed system employs an FVF-based LDO whose output voltage is directly determined by the reference voltage (V_{REF}). To ensure accurate regulation under process variations, a BGR with an integrated 3-bit trimming DAC is incorporated, enabling the precise tuning of V_{REF} and consequently a stable LDO output voltage. By incorporating the on-chip FVF-LDO, the proposed optoelectronic TIA achieves low-noise performance even under low-power operation, while significantly improving immunity to supply noise. The optoelectronic TIA demonstrates an improvement of more than 30 dB in PSRR compared to the baseline condition. Post-layout simulation results verify that the proposed optoelectronic TIA provides a stable and reliable analog front-end solution, achieving low noise, enhanced PSRR, and robust operation under the severe PVT variations. Hence, the proposed architecture is well suited for low-power and high-sensitivity optical receiver applications.

Author Contributions: Conceptualization, S.-M.P.; methodology, S.-M.P.; software, S.C. (Suwon Cho) and S.C. (Sieun Choi); validation, S.C. (Suwon Cho) and S.C. (Sieun Choi); formal analysis, S.C. (Suwon Cho), S.C. (Sieun Choi), and S.-M.P.; investigation, S.C. (Suwon Cho), S.C. (Sieun Choi), and S.-M.P.; writing—original draft preparation, S.C. (Suwon Cho), S.C. (Sieun Choi), and S.-M.P.; writing—review and editing, S.C. (Suwon Cho), S.C. (Sieun Choi), and S.-M.P.; visualization, S.C. (Suwon Cho) and S.C. (Sieun Choi); supervision, S.-M.P.; project administration, S.-M.P.; funding acquisition, S.-M.P. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data are contained within the article.

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