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Full-Area 3D Simulation and Experimental Analysis of IGBT Failure in UIS Due to Current Filamentation

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Abstract

In spite of the importance of a detailed description of the filamentary current constriction of the IGBT during the turn-off operation that could lead to the device's failure, there are to date no quantitative 3D simulation results of the filament growth and dynamic that can be compared with experimental results. In this paper we present 3D numerical simulations on the failure mode in the Unclamped Inductance Switching (UIS) test operation, extended to the full device area, which will be usefully compared with detailed experimental results on a large number of trench IGBT test samples. For the first time extended 3D dynamic electrothermal simulations of the whole die are made, to take into account both the electric and thermal effects of the filamentary conduction in avalanche mode. The onset of a filament growth condition for a current level just above the turnover voltage evaluated by the 3D simulations, and the area of the filament, obtained for the first time, are well in agreement with the quantitative data extracted by the experimental evaluations. Moreover, the thermal heating due to the filament formation is found to be quite independent from the current level, because it depends on the current density in the filament, rather than on the injected current. The delay time between the filament formation and the final failure time seen in the experimental results is verified to be due to the movement of the filament all around the chip surface in search of a cooler spot. The movement of the filament along the whole die area is verified for the first time by full area 3D electrothermal dynamic simulations, with times in agreement with the experimental delay between filament formation and final failure seen in all the failure reports.

Keywords: 3D-TCAD simulations; TCAD; IGBT; punch-through IGBT; unclamped inductive switching test; avalanche; breakdown

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1. Introduction

One of the most critical operations performed by the IGBT is the one encountered in the drive of electric vehicles during the inductive turn-off switching, due to the inductance loads that bring the collector voltage up to avalanche mode to force the current into the off state. For this application the IGBT ruggedness must be checked by the Unclamped Inductive Switching (UIS) test that determines the amount of energy needed to survive under unclamped switching off with a large inductive load.

The failure mechanism for this kind of failure in large-area high-voltage IGBT devices has been widely discussed in past years, since the first papers indicating that the failure is mainly due to the generation of a filamentary current conduction in avalanche mode [1,2]. The cause of the current filamentation during the UIS test has been discussed in many papers [3,4],

and the filamentary conduction was explained to be due to a Negative Differential Resistance region (NDR) in the avalanche IV curve. The presence of the NDR region above a threshold current will cause current constriction in a small device area and the formation of a filament. This filamentary conduction will cause in turn an anomalous heating in a small area, and eventually device failure.

Physics giving rise to the NDR region and to filamentary conduction have been explained and clarified in subsequent papers, as in [4–8], both for Punch-trough (PT) and Field Stop (FS) devices [9] and supported by experimental detection on different devices [10–12].

The motion of the current filaments across the die area seem to play a relevant role in determining the final failure. In [8,13] an observation of the filament motion across the chip area due to the thermal effect generated by current constriction was experimentally reported.

However, in spite of the importance of this failure mechanism, there is still to date a lack of detailed numerical simulations that could give a quantitative (even if approximate) detection of the thermal effects generated by the filament formation and growth at different currents, and of the current level that could generate a failure.

In most papers, as in [8,9,14,15], a simulation of filament formation and movement has been attempted by using a 2D electro-thermal simulation of only a few elementary cells of the IGBT structure, but without any quantitative comparison of the simulation results with the experimental ones. The simulation work on IGBT failure based on one or a few elementary cells has been largely used, and extended up to the last published papers in 2024–2026 [15–18], where no information on the filament area and current density was extracted from the cell evaluation during UIS operation.

This lack of quantitative results in this field is due, in our opinion, to two main reasons: (a) the 2D numerical simulations of the current filaments are solutions that in the real 3D case should appear on the chip area as stripes instead of circular-like spots, giving rise to erroneous thermal effects, because in the 2D simulations the filament simulated is assumed to be uniform along the direction perpendicular to the simulated plane [8]; and (b) the filament area, as it has been detected in [10], is much larger than the area of a few elementary cells, so the assumptions obtained in a very small area are not applicable to the failure of the whole IGBT die. When filament formation is evaluated by simulating only a few elementary cells (1–10), the modeled area is approximately 10^6 times smaller than the actual device area. As a consequence, the resulting current density and thermal effects are not representative of the real device behavior.

In fact the formation of the filament in real cases is strongly dependent on the total area of the device, because all the current that was previously evenly distributed on the whole device area is now concentrated on a very small area; therefore, the failure analysis must consider the total area of the device under investigation to make a correct evaluation of the current density in the filament, which will generate the electrical and thermal effects leading to the failure.

Despite the large number of studies addressing IGBT failure under UIS conditions and its robustness during the unclamped switching operation, no quantitative numerical evaluation of the filament area after full growth, nor of the associated thermal stresses due to current constriction, has yet been reported using full-area 3D simulations of the actual device.

However, performing a detailed 3D electrothermal simulation of the entire device to investigate filament dynamics and the related thermal effects is computationally impractical, as it would require explicitly modeling the complex cell structure replicated over the millions of cells typically present in the die. To date, the only study reporting a 3D electrothermal analysis of filament formation and motion is [19]. However, even in that

work the simulations were performed on a relatively limited area (up to 160 × 160 μm^2). The authors themselves acknowledged that "in the small-scale 3D simulations, the current density in the avalanche-induced filament is not sufficient to trigger local latch-up… The calculated UIS failure energy becomes much larger than that of the actual device. Large-scale 3D simulation is mandatory to reproduce the correct UIS failure phenomena."

Then up to now, a lot of questions remain open and are not afforded in the numerical simulations presented so far regarding the critical current needed for filament formation, the dynamic of the filament growth, the area of the filament as a function of the UIS current, the thermal stress induced in the die after its formation, and the effect of the filament movement across the die area. These points are crucial in terms of a possible evaluation of the failure mechanism and in the quantitative evaluation of the thermal stresses that will lead to the failure of the device.

The scope of this paper is then to try to make a suitable simplification of the device structure, to make possible 3D numerical simulations on the full area die, and to do a quantitative analysis of the filament growth and dynamic during the UIS test, by taking into account both the electric and thermal effects on the filament formation. The numerical results will then be compared with the experimental results on the failure mode in UIS operation.

2. Simulation of the Elementary Cell and Comparison with Experimental Data

As discussed in previous works, the filament formation is due to the NDR of the I–V avalanche curve. The NDR region that gives rise to the filamentary conduction is generated, both for the PT and FS IGBT devices, by the minority carriers injected into the drift layer from the collector side, so we need to describe in the best way this effect due to the buffer layer and the collector substrate.

To collect the experimental data of UIS failures we used a multicellular PT Trench IGBT with an area of 77 mm^2 and a voltage of 1200 V made by Toyota. For these structures the elementary cell has an area of 6 × 4 μm; the simulated 3D structure of the cell with the TCAD device simulator is the one reported in Figure 1. The injection efficiency of the buffer layer/collector substrate region was controlled by Helium implantation from the back surface. Based on our evaluation of the defects induced by Helium irradiation in silicon [20], we assumed in the buffer layer the given defect distribution due to the implant energy, with an energy level of the defect: E_T = 0.23 eV (distance from the conduction band in the upper bandgap), with the values $\sigma_n = 1.4 \times 10^{-14}$ s, $\sigma_p = 4.37 \times 10^{-14}$ s for the electron and hole trap cross sections. The defect concentrations that define the lifetime values in the buffer layer were then extracted by making a fitting with the I_C/V_{CE} experimental curves at different temperatures, as reported in Figure 2. In the low doped Epi-layer, we assumed a constant lifetime according to the Scharfetter model, with $\tau_{nmax} = 2.68 \times 10^{-6}$ s, $\tau_{pmax} = 2.98 \times 10^{-6}$ s, and E_{trap} = 0.21 eV. The above values were extracted by fitting with the experimental data of the leakage current I_{C0} in the blocking state at different temperatures. The results after the fitting procedure are reported in Table 1. The results of the comparison between the simulation results and the experimental ones are quite good, and this confirms that the modeling of the recombination centers induced by the helium irradiation was correctly done in the simulator.

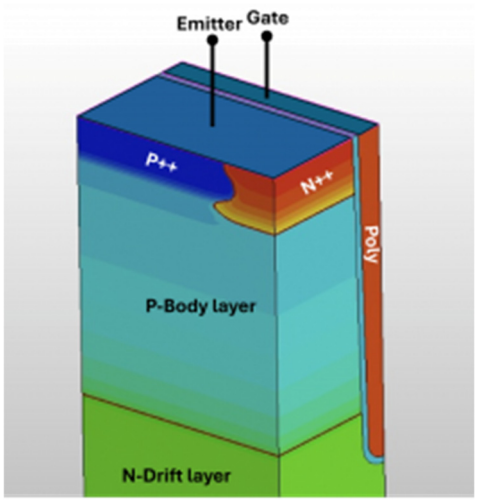


Figure 1. 3D structure of the elementary cell (a quarter cell is used by cutting the cell with two symmetry planes).

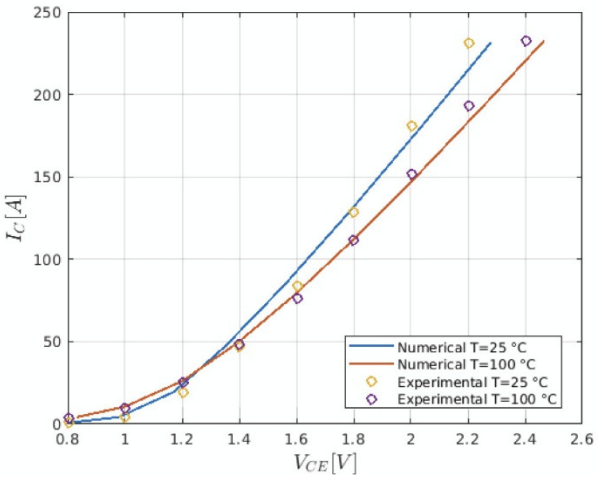


Figure 2. I_C = f (V_{CE}) at 25 °C and 100 °C (lines: simulation; dots: experimental).

Table 1. Leakage collector current (I_{CO}) and VBR for the IGBT test device.

Temperature (°C)		**−40**	**25**	**100**
I_{CO}@V_{CE} = 1000V (A)	Exp.	7×10^{-9}	1×10^{-6}	3×10^{-4}
	Simul.	1×10^{-9}	1×10^{-6}	1×10^{-4}
V_{BR} (V)	Exp.	1150	1220	1310
	Simul.	1100	1210	1300

3. Experimental Device Failure During UIS Test

To better investigate the onset of the failure mechanisms we performed a detailed experimental analysis of failure under the UIS test for 54 IGBT samples, by recording the voltage and current waveforms during the UIS test before and after the device failure, together with thermal images of the chip areas during the repetitive UIS cycles at increasing currents before the final failure.

To clarify the physics of failures during the UIS test, we made the failure tests by using an UIS tester with a special crowbar circuit that can be activated at a variable delay with respect to the gate turn-off time, shorting the current flowing into the inductance to protect the DUT from an excessive amount of energy during the failure, as shown in [21].

The UIS voltage and current waveforms for a typical tested sample are reported for different currents in Figure 3. At a low UIS current (about 6 A) we found a voltage plot like the one reported in Figure 3a, with a sudden voltage drop of more than 100 V after some µs from the UIS start-up. This voltage drop clearly indicates a transition from a distributed current flow to a filamentary current one, the latter concentrated in a quite small area with no further increase in voltage but only with a change in the area of the filament.

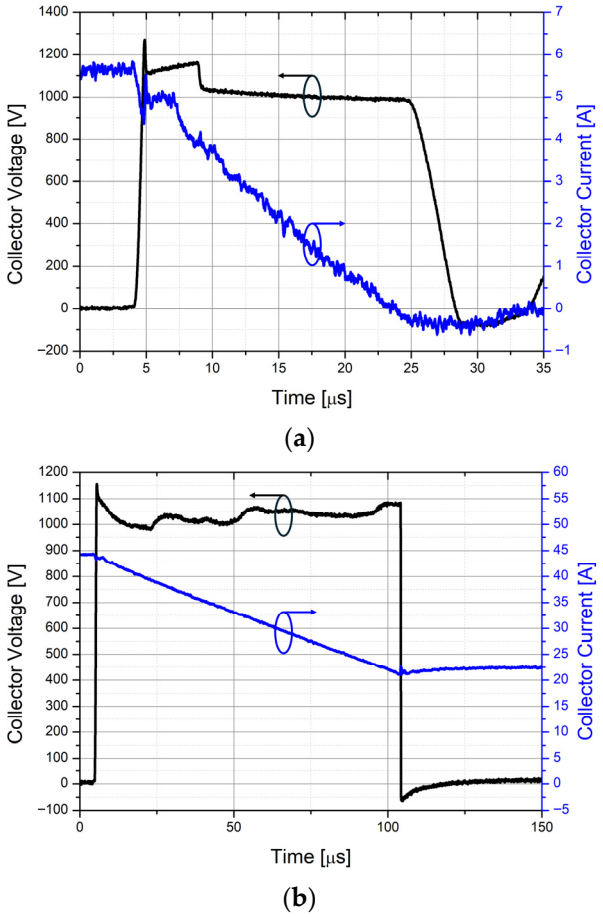


Figure 3. (**a**) UIS voltage (black line) and current (blue line) at low current; (**b**) same plot at failure point at high current (voltage: black line; current: blue line).

The time-delay between the turn-off and the voltage drop reduces as the UIS current increases, and it merges with the rising voltage edge at currents of about 10 A. At higher currents, like the one in Figure 3b, the sample eventually fails after some time during the linear decrease down to zero, and a constant IC current flows in the device.

An experimental verification for the analysis of the filamentary conduction can be done by performing a thermographic analysis of the devices, to obtain the power distribution across the device after the voltage drop, using the transient Lock-in Thermography (LIT) technique. The following analysis was conducted through the experimental setup and technique already reported in [21]; the thermographic analysis has been utilized also in recent papers [22,23] as a useful analysis for power devices.

In Figure 4 the thermographic image taken on a sample, tested at low current, shows that the current is flowing in a very small area (red circle), which indicates a filamentary current conduction. The area of this filamentary conduction from the picture comes out to be about 1/220 of the total active area., i.e., an area of about 0.35 mm^2 (we will compare that value with the one obtained by 3D simulations).

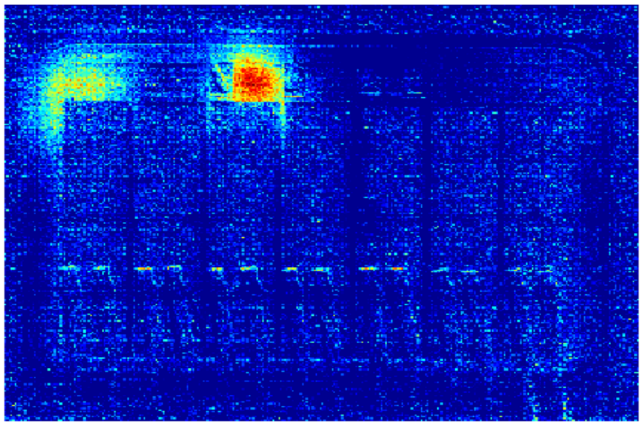


Figure 4. Termographic image with transient lock-in technique of a sample tested at I_{MAX} = 7.4 A, with T_{CROW} = 12 µs. The red area is the actual filament area detected.

The results for all the 54 samples tested up to failure in the UIS test give some important assessments, i.e., that the initial UIS current applied, indicated as IUIS, is always much larger than the one reached at the failure point, indicated as Ifail, due to the linear current slope dictated by the inductance value (in our case 4.7 mH). Moreover, the time to failure T_{fail} after the starting time of the UIS is quite long, ranging from a minimum of 55 µs up to a maximum of 145 µs, as indicated in Table 2. The distribution of the failure current I_{fail} detected in the 54 samples is reported in Figure 5, and it can be seen that the peak values of this distribution range around 11–12 A, much less than the starting I_{UIS} that range around 38–40 A. A possible explanation of the above results is that the initial filament growth in some points of the chip area did not cause the device failure, because the heating of this area caused a quick move of the filament toward a cooler spot, and the continuous movement caused an initial spreading of the heating across a large part of the chip area, because the thermal constant of the cooling in our test chip was more than 300 µs, as we will see in Section 5.

Table 2. ICRIT, IFAIL and TFAIL distribution in the tested samples.

Quantity	Min	Mean	Max
I_{crit} (A)	1	4	9
I_{fail} (A)	5	13	27
T_{fail} (µs)	55	104	145

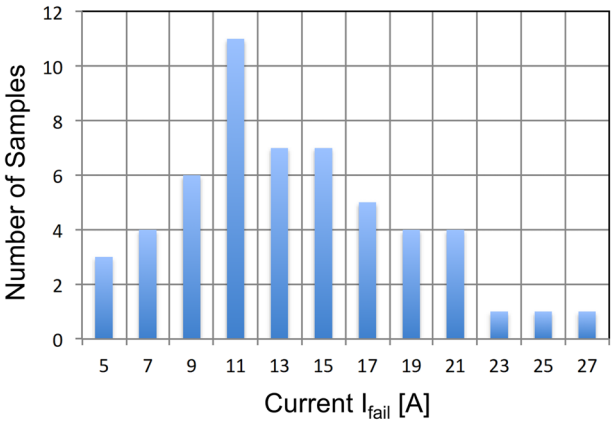


Figure 5. I_{fail} distribution for the 54 IGBT samples tested with UIS test at the failure point.

For most of the samples tested in the UIS test, the motion of the current filament across the chip area was detected by the thermographic chip images taken with equivalent-time thermal transient analysis on some samples, like the ones already reported in [6]. The movement of the filament due to thermal effects has already been suggested in [21,24], and demonstrated by 2D simulations in [10,25].

The final failure can be generated when the filament stays for a given time in some areas, without further movement; this latter case can be due either to the even heating of a large part of the chip area due to the previous filament motion, or to some boundary constraint that may be due to the pad contacts.

4. Simulations of the Filament Formation of the IGBT Structure in Avalanche Conduction

The static avalanche IV curve of our device, obtained by a detailed simulation of the elementary cell at ambient temperature, is reported in Figure 6 in log scale. In this plot one can see the turnover point where the first NDR region starts, at few A/cm^2, and the valley (saddle) point at more than 3.10^3 A/cm^2.

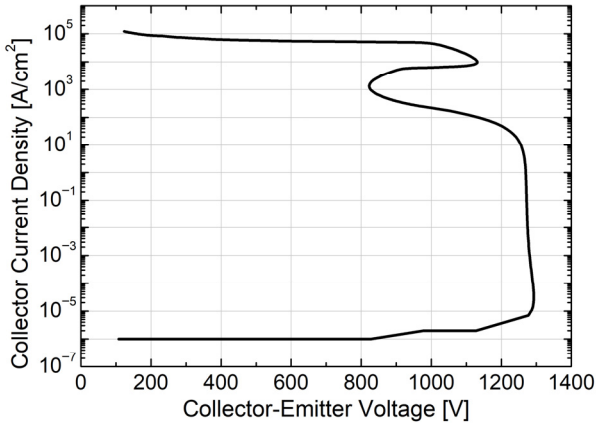


Figure 6. I-V curve in the avalanche condition of the IGBT structure obtained by a 2D numerical simulation of the elementary cell.

A detailed analysis of the filament formation when the device is reaching the NDR region during the UIS test is then needed to understand the failure mechanism seen due to the filament formation. But, as indicated in the previous section, we cannot perform 3D electrothermal simulations of the whole area device, by considering in detail all the cells made in the real device (in our case about 5 million cells); we must then make necessary simplifications in the device structure.

With reference to the equivalent electric circuit of the IGBT reported in Figure 7, which comprises the vertical MOS between the emitter and the epilayer through the channel made under the trench oxide; the lateral NPN transistor between emitter, body layer and epilayer; and the vertical PNP transistor between body, epilayer and collector (substrate) region, we note that after the turn-off the MOS section is inactive because the N channel is closed, and the collector current in the avalanche mode of operation flows only through the PNP parasitic vertical transistor.

The basic approach to make a suitable simplification in the simulated structure of the whole die during turn-off is to eliminate in any cell the trench oxide and the gate contact, leaving only the vertical body, epilayer, buffer layer and substrate collector. The approach considered is furthermore justified by the consideration that the filament area, as seen in Figure 4, is much larger than the area of a single cell (actually it could contain more than 10.000 cells).

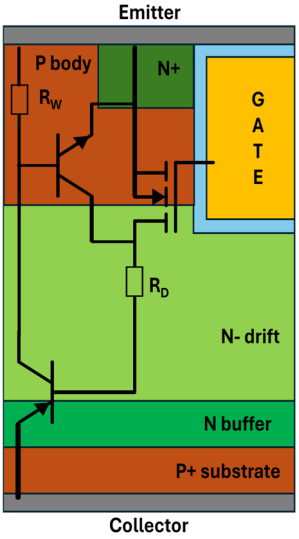


Figure 7. The equivalent electrical circuit of the IGBT, comprising the MOS, the lateral NPN bipolar transistor, and the PNP vertical bipolar transistor.

However, a further point must be considered to run suitable 3D TCAD simulations for the analysis of current filaments. When the filament occurs, the current density switches from a uniform distribution to the new condition where all the current injected is flowing in a very small area of the device. Therefore, the typical approach used, i.e., making the simulation of a portion of the device with area AS and choosing a suitable area factor ($AF = A_{TOT}/AS$, where A_{TOT} is to the total area of the device) to compute the overall current flowing into the real device $I = I_{CELL} \cdot AF$, where I_{CELL} is the current flowing in the reduced area TCAD model, is not suitable for the simulation of the device subjected to transient current filamentation.

In fact, when the current crowds into a single filament, all the current flowing into the overall device flows through the filament. When this happens, the realistic simulation of the current filament comes from forcing all the injected current I into the reduced area AS used for the 3D TCAD simulations. Then, the correct 3D simulation after the filament formation requires that the total current I will be used in the reduced area AS. The presence of the multiplication factor AF forces the maximum current flowing in the filament to the lower value $I_{CELL} = I/AF$. The analysis of the current filament shape, moreover, requires that the 3D TCAD reduced area AS should have a size big enough to contain the area of the current filament, even if much less than the total chip area.

In Figure 8 the current filament for a quite low current, equal for the two cases, is plotted for two 3D TCAD areas: (i) 500 × 500 µm and (ii) 1500 × 1500 µm. The current density profiles at a plane in the structure center shows that the two current filaments are identical in terms of current density. This result is fundamental, since it shows that the analysis performed on the 500 × 500 µm structure is equivalent to the one of 1500 × 1500 µm with the same overall forced current, allowing a faster numerical analysis. The isothermal 3D simulations of the 500 × 500 µm structure show that up to an injected current of 2 A (value refers to the real device area) the current flows uniformly across the whole area, thus indicating that the NDR region is not reached. But at currents larger than 2 A a current constriction in the center of the device starts to appear, due to the abrupt voltage drop seen in the voltage waveforms. It is worth noting that this max current value of 2 A for uniform distribution, indicated as I_{crit}, obtained by the numerical simulations is in very good agreement with the experimental values found in the tested devices, reported in Table 2, where the mean Icrit found for all the tested samples is reported to be 4 A. Many 3D dynamic simulations were made by using a structure with a reduced area AS of 1.5 × 1.5 mm. To

avoid the filament generating spontaneously in any possible area of the device (and often it will be generated in the area corner) we assumed a central area of the simulated device (of 100 × 100 μm) with an emitter depth reduced by 0.4 μm with respect to its nominal value, to ensure the filament formation was always in the center of the simulated structure.

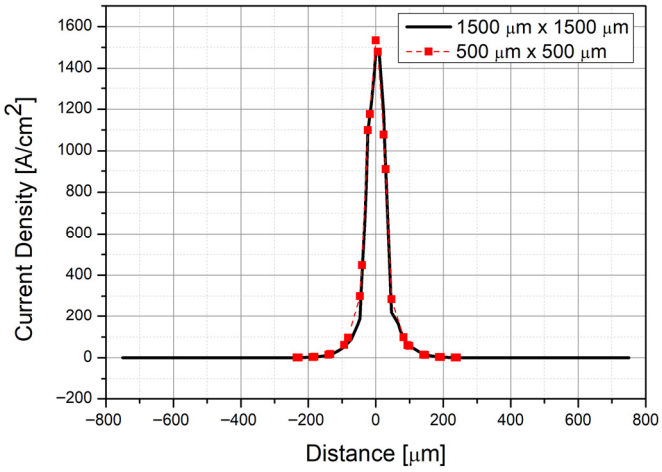


Figure 8. Comparison of the filament shape obtained on a 500 × 500 μm area compared with the one obtained on a 1000 × 1000 μm area at the same injected current.

The filament formation is clearly shown from the results of the 3D simulations of the 1.5 × 1.5 mm simulated structure, at increasing injected currents of 5, 10, 15, and 20 A, reported in Figure 9. We can see that, for all currents used, the area of the filament is always contained in the reduced area of the structure, and this ensures that the current injected in this area is equal to the one injected in the real device area.

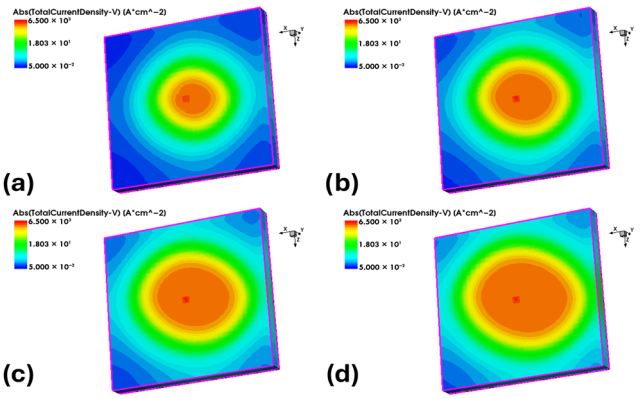
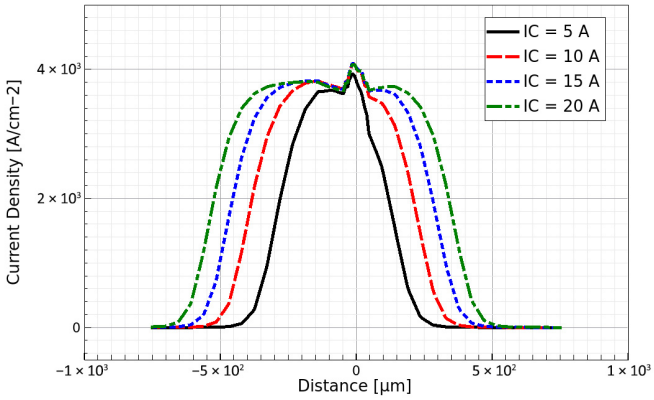


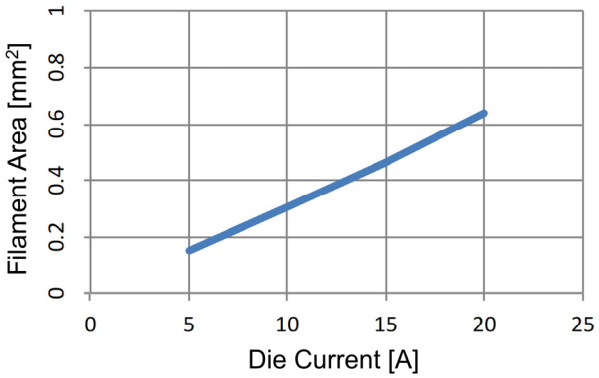
Figure 9. Current density distribution obtained by the 3D isothermal simulations on the 1.5 × 1.5 mm structure at 5, 10, 15, and 20 A injected currents, from (**a**–**d**) respectively.

As can be seen from the plots of Figure 9, the filament area enlarges as the injected current increases. The important comment on these results can be better extracted from the plots of the current density in the filament in a cutting plane passing through the center of the area, which are reported in Figure 10 for the same currents.

A very interesting data from the plot of Figure 10b is the area of the filament that, for a current of 7.4 A gives an area of 0.22 mm^2, which agrees quite well with the experimental one seen in Figure 4, of about 0.35 mm^2.



(**a**)



(**b**)

Figure 10. (**a**) Cutline of the current density distributions in the filament for the four current levels considered (red: 5A; green: 10A; blue: 15A; cyan: 20A); (**b**) plot of the area of the current filaments referred to the diameter taken at 1/2 of their height.

From the four plots of Figure 10a we found that the maximum current density in the filament remains quite constant at about 4×10^3 A/cm^2, a value that corresponds to the current density at the valley point of the avalanche curve (see Figure 6), while the area of the filament is shown to increase linearly with the current injection. In effect the valley point is the point where the NDR terminates and the filament can reach a stable shape, after a fast increase due to the lateral instability. This point was forecast based on the physics of the current instability due to the NDR region found even in early works on the subject [1], but never verified by numerical simulations. This is an important statement that allows us to forecast the current density level and the area of the filament at different currents, and it will affect also the thermal stresses due to the filament formation, as we will see in the next section.

5. Heating Effects Due to Current Filamentation

The next step of this work is to add thermal effects on the 3D simulations to evaluate the heating effects due to the filament formation. The overall scope is to make a comparison between the actual failures detected by experimental UIS tests in our test samples and the thermal data extracted by 3D simulations of the whole structure for the different injected currents.

For this goal, we cannot rely on the simulations on a reduced area device, like the one used in the previous section. In fact, by injecting the current value of the real device area (77 mm^2) in the reduced area structure (2.25 mm^2), the current density generated during the first times—i.e., before the current constriction in a filament—will be 34 times larger

than the real one, and it will produce in the reduced area AS an anomalous heating of the sample and premature filament growth compared to the real case.

Additional simplifications were therefore introduced to correctly account for the thermal effects induced across the entire chip area by filament formation at different current levels. This was achieved by adopting a coarser numerical mesh than that used in the reduced-area simulations, providing an effective trade-off between accuracy, given that the filament diameter is always larger than 500 μm, and computational efficiency.

Furthermore, while a fine mesh is kept for the vertical direction (y-axes) discretization of the structure (about 1 μm), along the lateral direction of the structure (both y-axes and z-axes) a larger discretization is used (about 125 μm) to properly discretize the filament.

Moreover, we have eliminated the small emitter depth reduction in the area center adopted for isothermal simulations because it could contrast the possible filament movement due to thermal effects. The only thermal boundary condition of the actual die to be checked is the one due to the thermal contact of the actual die molded on the metal plate. This latter was extracted by comparing the thermal constant of the temperature decrease, detected with the LIT technique on the 54 experimental samples with the one obtained by the thermal analysis of this latter structure with different thermal resistance RTh of the bottom boundary.

The experimental thermal decay, detected by the transient lock-in technique, presented a time constant of about 300 μs, and by a fitting of the experimental values with the simulation we extracted the R_{Th} value of 0.01 m^2 K/W.

The dynamic of the filament formation and of the heating generated inside the filament can be clearly evidenced in the 3D electrothermal simulations made on the whole device area (77 mm^2); here the metal pad is assumed to be of circular shape, to avoid a rectangular one that would cause an increase in the field in the corners. Even with the large mesh size adopted (in the order of 50 μm) the dimension of the filament found (see plot in Figure 11) is practically the one detected in the small area simulations of Figure 11.

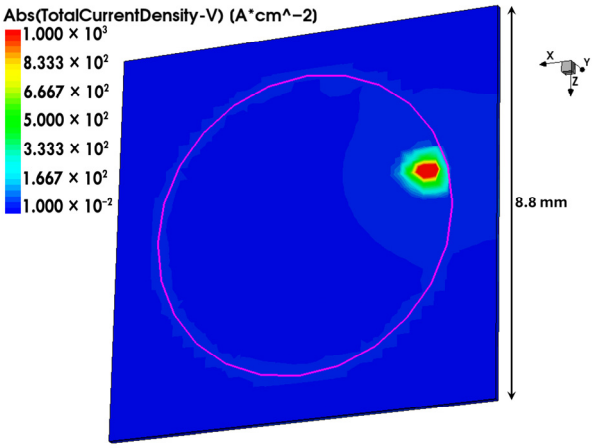


Figure 11. Filament area for a current of 5 A obtained in the 3D simulation of a full area device.

The first results of the thermal 3D simulations, reported in Figure 12, give us important information on the filament formation and on thermal stresses created by the filament formation in the die. Here the simulations show that the filament is generated for a current between 2 and 4 A, in good agreement with the experimental data, and it reaches full growth at the end of the voltage drop in much less than 1 μs. The max temperature increase rate in a given time from the filament formation is practically equal for all the filamentary currents considered in the thermal analysis (taking into account the shift in time from filament generation for the different currents). This happens because the max temperature in the filament area depends on the current density of the filament, and the latter, after the

filament growth, is always the one of the valley point ($\approx 4 \times 10^3$ A/cm^2 in our case), as we found in Section 4. The thermal stress sustained by the die in the filamentary condition, at any current level applied, is about the same, independent from the current level.

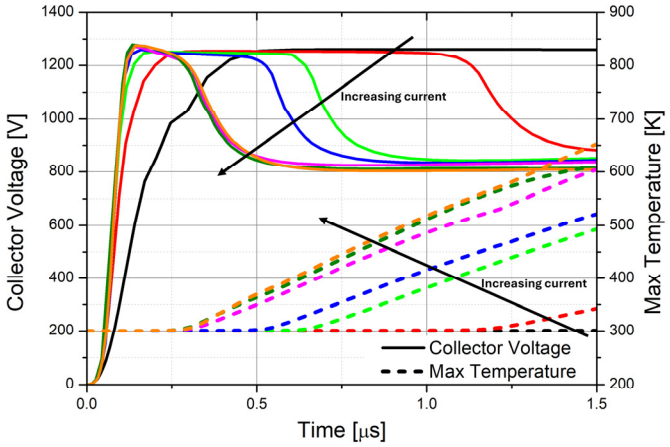


Figure 12. Filamentary conduction starting and increasing for different injected currents in the full die area (black: 1A; red: 2A; green:3A; blue: 4A; pink: 5A; dark green: 10A; orange: 15A).

The very fast increase in temperature during the filament growth in the initial position is stopped by the movement of the filament due to this heating from the hot location to a cooler one. This mode is due to the strong dependence of the ionization factors by the temperature: the strong heating of the first localization of the filament will cause a strong decrease in avalanche multiplication at that point that will move to a cooler point for the same voltage. This will cause the movement of the filament to the nearest cool location, that will be heated at its turn, thus causing the continuous movement of the filament. The simulation results of Figure 13 show for the first time this filament movement in the 3D simulations of the whole die, and the related effect on the max temperature of the die. Here the motion of the filament along a large part of the die and the subsequent temperature track left by the filament moves are reported for different time intervals. From that plot it can be seen the temperature rise is very fast in the first μs where the filament is not moving, and it would quickly reach a temperature larger than 800 K (and eventually failure due to the triggering of the parasitic thyristor) if it stayed in the same position. However, the temperature rise will make the filament move from the initial position. During the filament move the temperature of the whole filament track remains quite constant, as seen by the temperature track in Figure 13b and in the plot of Figure 14. This latter point could also explain why the initial filamentary conduction at large injected currents does not determine the immediate failure of the IGBT, and it takes some time to reach the failure point.

During that time the current in the UIS test is linearly decreasing due to the inductance, and after a given time the large part of the die is heated, due to heating due to the filament motion along the die surface, and it remains heated because the thermal time constant in the temperature decay of the die is quite long, about 300 μs. Only after a widespread heating of the whole die area will the filament no longer find a cooler position to move onto, and it will stay in the same location up until the time when the temperature increase will determine the triggering of the PNPN parasitic thyristor, leading to the final device failure.

As a reference, in our simulations the time spent on the filament movement from a lateral side to the opposite one of the die area was about 15 μs. This in some way could explain the quite large values of the mean time to failure Tmean detected in the experimental data, if one considers that in real cases the motion is not a straight line across the opposite die boundaries, and that a large number of paths is needed to take up the greater part of the die area.

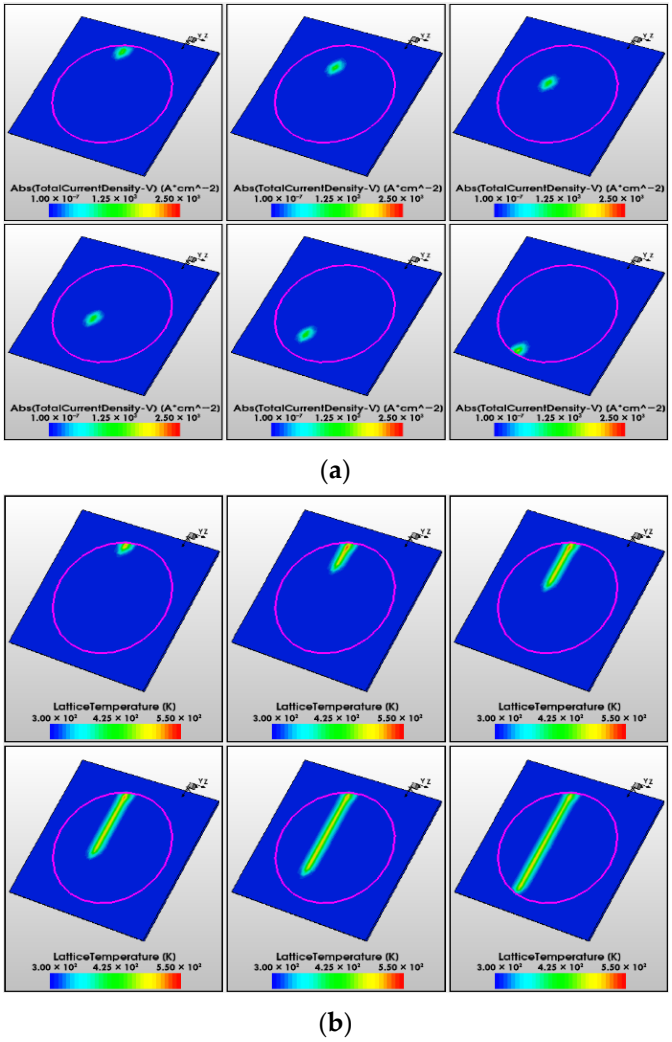


Figure 13. Filamentary current (**a**) and temperature motion (**b**) after the growth for the current of 5A—frames are at 2.45 μs time intervals.

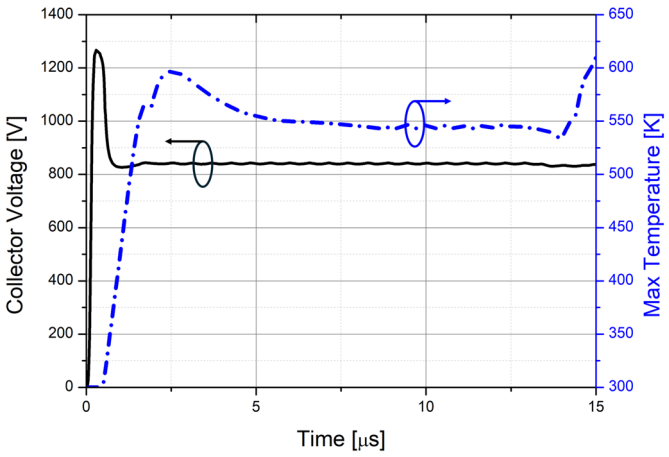


Figure 14. Voltage plot and max temperature on the die for I = 5A, detected during the filament motion along 15 μs time interval.

6. Conclusions

A lot of test IGBT high voltage trench devices rated 1200 V have been used to extract detailed experimental results of failure mode in UIS operation, and to compare them with 3D electrothermal simulations.

The main results of this research are summarized in the following items:

- The 3D simulations were performed on the whole die area, using a suitable simplification of the die structure, which is necessary to simulate the whole die area and correctly evaluate the IGBT operation after turn-off.
- The critical current Icrit during UIS operation that triggers the filament formation was evaluated by the simulation as 2 A, in very good agreement with the value of about 4 A experimentally detected.
- The filament area after the growth was evaluated at different IUIS currents with a detailed mesh, and the results are significant: (a) the area evaluated by 3D simulation for a current of 7.4 A gives an area that agrees quite well with the experimental one; and (b) the current density in the filament remains constant at the value corresponding to the one of the valley point of the NDR region of avalanche curve, while the filament area increases linearly with the injected current IUIS.
- The added electrothermal simulations on the whole die area show that (a) the increase in temperature due to filament formation for different IUIS currents is consistent, because the heating is caused by the current density in the filament that is the same for different currents; (b) the initial fast increase in the filament temperature is stopped at a value well below the one of intrinsic temperature (about 750 K [8]) because of the filament movement to a cooler region; and (c) the filament movement across the die area keeps the temperature along its track constant, so the heating is evenly distributed along the whole die area after more passes, because the filament movement along the die area is much faster than the cooling of the die. The above effects have been in fact experimentally detected through transient thermal maps.

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