

Article

A Dual-Phase Dual-Path Hybrid Buck-Boost Converter with Offset-Controlled Zero-Current Detection Achieving 95.88% Peak Efficiency

Sungjun Moon ^{1,2}, Jonghun Chae ^{1,2}, Gyumin Kim ^{1,2}, Junseong Hwang ^{1,2}, Jieun Kim ^{1,2} and Inho Park ^{1,2,*}

¹ Department of Electrical and Computer Engineering, Inha University, Incheon 22212, Republic of Korea; msj0916@inha.edu (S.M.); whdgjs25@inha.edu (J.C.); 12201456@inha.edu (G.K.); gnoes0428@inha.edu (J.H.); potatoeunee@inha.edu (J.K.)

² Program in Semiconductor Convergence, Inha University, Incheon 22212, Republic of Korea

* Correspondence: ihpark@inha.ac.kr

Abstract

This paper presents a dual-phase dual-path hybrid buck–boost (DPBB) converter with an offset-controlled zero-current detector for Li-ion battery applications. Compared with inductive buck–boost converters, the proposed hybrid converter has a continuous input current, reducing the input voltage (V_{IN}) ripple, which is caused by the parasitic inductance of the bonding wire. The proposed switching operation of the DPBB topology shows a low inductor current ripple with the continuous output delivery current; therefore, the ripple of the output voltage (V_{OUT}) is reduced with the efficiency improvement. Compared with the prior hybrid buck–boost converters, it supports the buck and boost modes only by adjusting the duty cycle, so this addresses the issues of mode transitions. The proposed work utilizes the dual-phase operation to lower the conduction loss and improve the dynamic range. The proposed offset-controlled zero-current detector compensates for the timing error owing to the propagation delay of the control signals to reduce the reverse current from the output. The chip is fabricated using a 180-nm BCD process. It regulates V_{OUT} at 3.3 V with a wide V_{IN} range of 2.8 V to 4.2 V. Peak efficiencies of 95.88% and 93.08% are achieved in the buck and boost modes, respectively, with 140 m Ω of inductor DC resistance.

Keywords: hybrid buck–boost converter; multiphase; DC–DC converter; output delivery current; inductor current; zero-current detector



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1. Introduction

As the types and numbers of mobile devices increase, managing the rechargeable Li-ion batteries equipped in these devices has become an important research topic. Because the voltage of Li-ion batteries varies from 2.8 V to 4.2 V depending on the operating conditions, research on the stable regulation of an output voltage (V_{OUT}) from various battery voltage levels has been widely conducted over the past several years. In particular, many hybrid buck–boost converters have been presented with various design approaches to overcome the drawbacks of conventional inductive buck–boost converters, such as discontinuous input current (I_{IN}), output delivery current (i_{DLV}), and a high average inductor current (i_L).

Early hybrid buck–boost converters were primarily designed to achieve a continuous i_{DLV} [1–4]. However, they utilized the conventional inductive buck configuration for the buck mode without using a flying capacitor (C_F). Therefore, they still have all the drawbacks of inductive buck converters, such as discontinuous I_{IN} and an average i_L level higher than

I_{LOAD} . Moreover, these converters typically operate in more than two modes to support buck–boost operation, which results in complex mode transitions.

Figure 1 illustrates the operations of state-of-the-art hybrid buck–boost converters. To address the drawbacks of inductive buck–boost converters, prior hybrid DC–DC converters included the following two main design approaches: (1) topologies for dual current delivery paths [3,5–11] and (2) switched-inductor-capacitor topologies [1,2,9–15]. The dual-path current strategy supplies i_{DLV} with i_L and a capacitor current (i_C). Figure 1a shows a state-of-the-art dual-path hybrid buck–boost (DPBB) converter [7]. Similar to the prior DPBB converter, the i_{DLV} of certain hybrid DC–DC converters is composed of i_L and i_C alternately during a clock cycle (T_{CK}) [5,7]. Otherwise, as shown in Figure 1b, other hybrid buck–boost converters have a reduced average i_L by implementing a phase in which i_{DLV} consists of both i_L and i_C simultaneously [6,8–11].

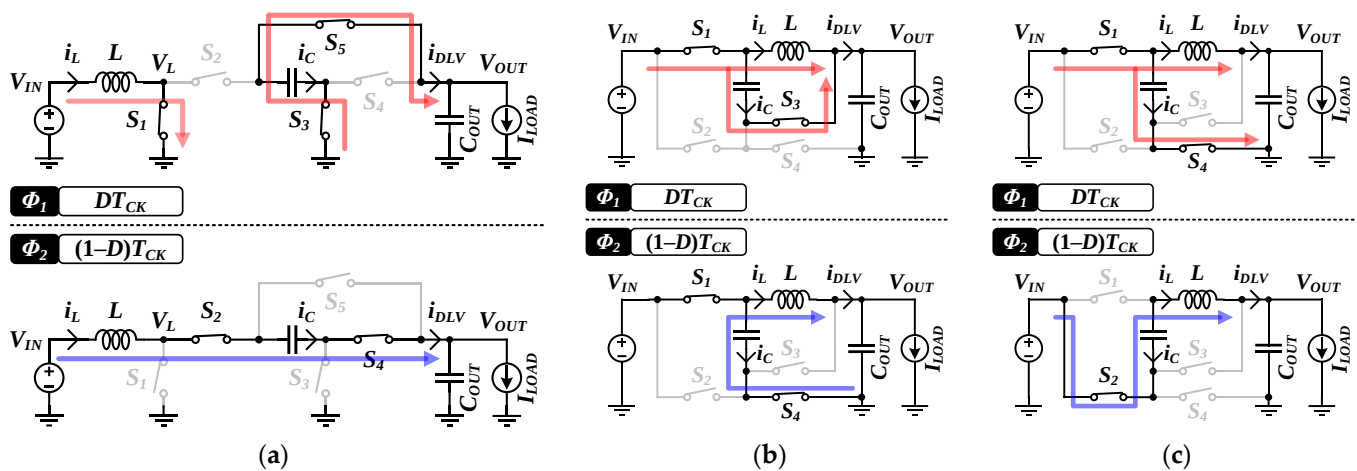


Figure 1. Operations of prior methods; (a) DPBB converter in [7], (b) the buck mode, and (c) the boost mode of the four-phase hybrid buck–boost converter in [9].

The switched-inductor-capacitor topologies can be reconfigured to reduce the average i_L by placing the inductor at either the input or output terminal depending on the boost or buck mode, respectively, as shown in Figure 1c [9]. The conventional inductive buck–boost and boost converters have discontinuous i_L and i_{DLV} ; therefore, the average level of i_L is always higher than the load current (I_{LOAD}), causing a large conduction loss (P_{CD}) owing to the DC resistance of the inductor (DCR) [16]. In inductive buck and boost converters, the inductor is placed at the input and output terminals, respectively. Consequently, depending on the voltage conversion ratio and the relationship between the input and output powers, both buck and boost converters exhibit an average i_L higher than I_{LOAD} . Therefore, they generally achieve lower power conversion efficiency than that of state-of-the-art hybrid DC–DC converters.

In addition to hybrid topology approaches, multiphase configurations provide an effective way to reduce the average i_L level. Compared with single-phase DC–DC converters, multiphase configurations provide several advantages, such as low input and output ripples, fast load-transient response, and low i_L [8–10,17,18]. As multiphase DC–DC converters have lowered i_L levels for each inductor, they operate in discontinuous conduction mode (DCM) more often than single-phase DC–DC converters. Therefore, a highly accurate zero-current detector (ZCD) is required for an efficient operation. Many techniques have been proposed to detect the exact zero-crossing point of i_L . Certain designs utilize voltage comparators to compare the voltage drops across the power switches to sense the zero-current point [19–22]. The resistance of the power switches must be increased to improve

accuracy. However, this leads to efficiency loss. Therefore, they suffer from a tradeoff between timing error and efficiency.

Another approach is to detect the zero-crossing point of i_L through an indirect voltage profile using digital circuits [23–26]. The exact switch-off timing is typically controlled with digitally controlled delay cells; however, they occupy a large silicon area. Moreover, the resolution of a digitally controlled ZCD is directly related to its accuracy. To increase the resolution, coarse and fine tuning of the delay cell was designed in [26], but this increases the circuit complexity.

To address the aforementioned issues, this paper presents a dual-phase dual-path DPBB architecture whose power stage is similar to that in [7], but with an additional phase (Φ_3). The inclusion of Φ_3 slightly improves the conduction loss and ripple characteristics by modifying the current flow and switching sequence. Furthermore, due to the dual-phase operation, the current flowing through each power stage is halved, which further reduces the overall conduction loss. In addition, an offset-controlled ZCD is employed to effectively minimize the power loss caused by reverse inductor current under light-load conditions. The remainder of this article is organized as follows. Section 2 describes the working principles and power loss analysis of the proposed DPBB operation. Section 3 presents the circuit implementation of the proposed method. Section 4 presents the measurement results of the fabricated chip. Finally, conclusions are presented in Section 5.

2. Proposed Dual-Path Hybrid Buck-Boost Operation

2.1. Proposed Power Stage Operation

Figure 2 shows the proposed operation of a DPBB converter with a single stage. The conventional method in [7] has two operating phases with the same DPBB topology, as shown in Figure 1a. However, the proposed method operates in four phases, two of which are identical, as shown in Figure 2. Compared to prior converters, the proposed converter divides the duty cycle (D) by half and operates in two identical phases (Φ_1).

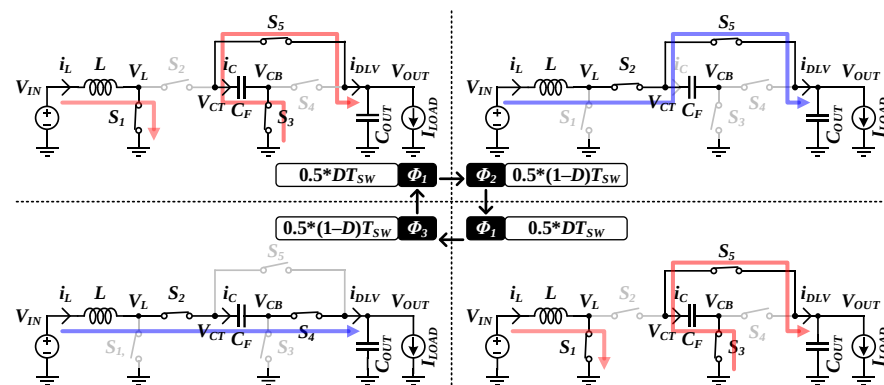


Figure 2. Proposed switching operation of the single-phase DPBB converter.

Figure 3 shows the waveforms of the proposed operation with a single power stage. As shown in Figures 2 and 3, Φ_1 is the first and third phases to charge i_L via switch S_1 . During Φ_1 , i_C flows to V_{OUT} through charge sharing, and C_F is discharged to V_{OUT} . The second phase (Φ_2) is the period during which the inductor is directly connected to V_{OUT} . In this phase, only i_L flows to V_{OUT} . In this phase, the first node of the inductor is always connected to V_{IN} , and the second node is connected to V_{OUT} . Therefore, i_L builds up when the power stage operates in the buck mode, and i_L is discharged when it operates in the boost mode. After the second Φ_1 , the inductor and C_F are connected in series during the last phase (Φ_3), and current flows to the load. In this phase, i_C is the same as $-i_L$, and it satisfies the inductor volt-second rule.

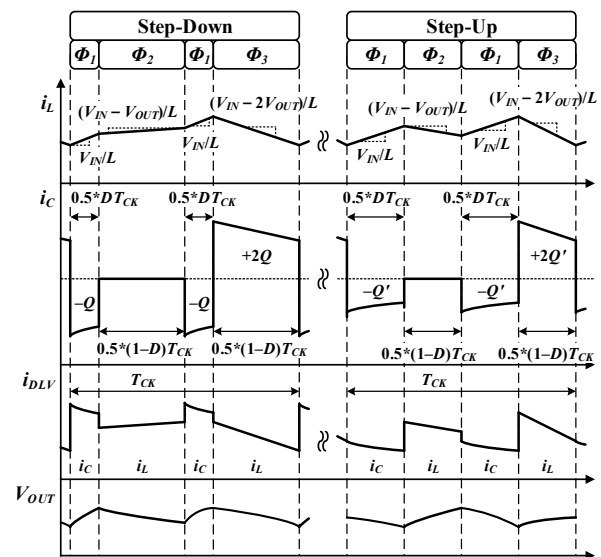


Figure 3. Waveforms of the proposed single-phase operation.

The conversion ratio of the proposed method (M_{PROP}) is expressed by the volt-second rule on the inductor as follows:

$$DV_{IN} + 0.5(1-D)(V_{IN} - V_{OUT}) + 0.5(1-D)(V_{IN} - 2V_{OUT}) = 0 \quad (1)$$

$$M_{PROP} = \frac{2}{3(1-D)}, \quad (0 < D < 1), \quad (2)$$

where V_{IN} denotes the input voltage of the DC–DC converter.

The proposed switching operation, in (2), has a conversion ratio of $2/3$ to ∞ . Figure 4 shows the conversion ratio according to D . As shown in Figure 4a, the proposed converter operates as a buck converter when D is less than $1/3$ and as a boost converter when D is greater than $1/3$. As the proposed method is designed for Li-ion batteries, the target V_{IN} ranges from 2.8 V to 4.2 V. Therefore, D of the proposed method ranges from 0.152 to 0.434 for the target V_{OUT} of 3.3 V, as shown in Figure 4b. Prior hybrid buck–boost converters have mode-transition issues, in which the converters are controlled differently according to the operating modes. Therefore, complex control methods are required to achieve seamless mode transitions [1–4,9,11,13]. Most conventional works cannot cover the range of the conversion ratio to around unity. However, the operating mode of the proposed method is determined only by D , and M_{PROP} ranges from $2/3$ to ∞ without any missing regions.

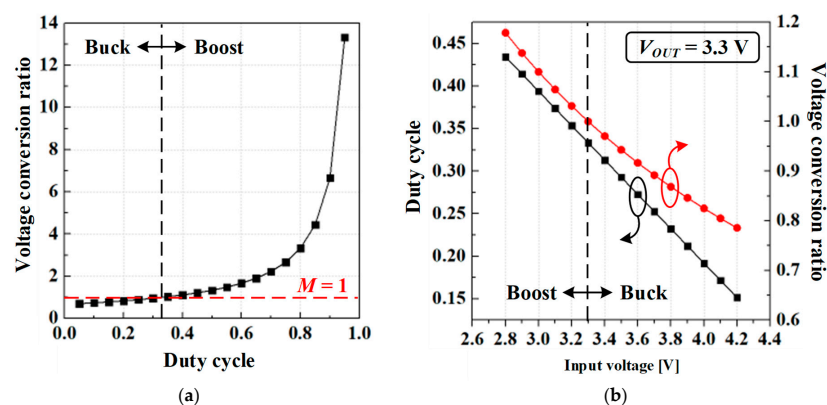


Figure 4. (a) Voltage conversion ratio curve according to the duty cycle, and (b) duty cycle according to V_{IN} for $V_{OUT} = 3.3$ V, where the black line represents the duty cycle and the red line represents the voltage conversion ratio.

2.2. Analysis of Conduction Loss

Many hybrid DC–DC converters have been designed to reduce the conduction loss by reducing the average value of i_L (I_L). Similarly, the proposed method utilizes a dual-path current design approach such that i_C and i_L flow to V_{OUT} .

As shown in Figure 3, C_F is discharged by i_C during two Φ_1 s and charged by i_L during Φ_3 . The charge balance of C_F is expressed as follows:

$$\int_0^{0.5DT_{CK}} |i_C(t)| dt + \int_{0.5T_{CK}}^{0.5(1+D)T_{CK}} |i_C(t)| dt = \int_{T_{CK}-0.5(1-D)T_{CK}}^{T_{CK}} i_C(t) dt. \quad (3)$$

In Φ_3 , the inductor and C_F are connected in series, and the same current flows through them. Therefore, the charge that flows through C_F during Φ_3 is the same as the charge that simultaneously flows through the inductor, and it is expressed as follows:

$$\int_{T_{CK}-0.5(1-D)T_{CK}}^{T_{CK}} i_C(t) dt = \int_{T_{CK}-0.5(1-D)T_{CK}}^{T_{CK}} i_L(t) dt = 0.5(1-D)T_{CK}I_L. \quad (4)$$

Using (4), the average value of i_C during Φ_1 ($I_{C,1}$) can be expressed as follows:

$$0.5DT_{CK}I_{C,1} + 0.5DT_{CK}I_{C,1} = 0.5(1-D)T_{CK}I_L \quad (5)$$

$$I_{C,1} = \frac{1-D}{2D}I_L. \quad (6)$$

From the charge balance of the output capacitor (C_{OUT}), the relationship between I_L and I_{LOAD} can be derived as follows:

$$\int_0^{0.5DT_{CK}} i_C(t) - I_{LOAD} dt + \int_{0.5DT_{CK}}^{0.5T_{CK}} i_L(t) - I_{LOAD} dt + \int_{0.5(1+D)T_{CK}}^{0.5T_{CK}} i_C(t) - I_{LOAD} dt \quad (7)$$

$$+ \int_{T_{CK}-0.5(1-D)T_{CK}}^{T_{CK}} i_L(t) - I_{LOAD} dt = 0$$

$$D(I_{C,1} - I_{LOAD}) + (1-D)(I_L - I_{LOAD}). \quad (8)$$

By substituting (6) into (8), I_L can be expressed as

$$I_L = \frac{2}{3(1-D)}I_{LOAD} = M_{PROP}I_{LOAD}. \quad (9)$$

As shown in (9), I_L of the proposed method in the buck mode is equal to the value that is reduced by the conversion ratio in I_{LOAD} . In an inductive buck–boost converter, I_{IN} and i_{DLV} are discontinuous. Therefore, I_L is always greater than I_{LOAD} , and it causes large P_{CD} , increased V_{OUT} ripple, and higher switching noise. As I_{LOAD} increases, these issues become more critical. However, the proposed work, including that of state-of-the-art hybrid DC–DC converters, solves the issue of the discontinuous i_{DLV} and improves the power conversion efficiency.

When the converter operates under medium-to-heavy load conditions, the ripple component of the inductor current is relatively small compared to its DC component. Therefore, for analytical simplicity, the inductor current is approximated by its DC component when estimating conduction loss in the following analysis. To compare the effectiveness of the proposed operation, P_{CD} of the proposed method ($P_{CD,PROP}$) is analyzed as

$$P_{CD,PROP} = 2 \times 0.5D \left\{ I_L^2(R_{ON} + R_{DC}) + 2I_{C,1}^2R_{ON} \right\} + 2 \times 0.5(1-D)I_L^2(2R_{ON} + R_{DC}), \quad (10)$$

where R_{ON} denotes the on-resistance of each power switch, and R_{DC} denotes the DCR of the inductor. In this analysis, the R_{ON} of the power switches is assumed to be the same. By substituting (6) and (9) into (10), $P_{CD,PROP}$ can be expressed by I_{LOAD} as follows:

$$P_{CD,PROP} = D \left\{ M_{PROP}^2 I_{LOAD}^2 (R_{ON} + R_{DC}) + 2 \left(\frac{1-D}{2D} \right)^2 M_{PROP}^2 I_{LOAD}^2 R_{ON} \right\} \\ + (1-D) M_{PROP}^2 I_{LOAD}^2 (2R_{ON} + R_{DC}) \\ = M_{PROP}^2 I_{LOAD}^2 \left[R_{ON} \left\{ \frac{(1-D)^2}{2D} - D + 2 \right\} + R_{DC} \right]. \quad (11)$$

Because the DC component of each current causes P_{CD} , the ac current is ignored in this analysis. Table 1 presents a comparison of the characteristics of the proposed DPBB operation with those in prior works. As shown in Table 1, I_L of the inductive buck–boost converter is always larger than I_{LOAD} because the converter has discontinuous i_{IN} and i_{DLV} . However, the hybrid buck–boost converters, including the proposed work, have a continuous i_{DLV} ; therefore, they achieve a lower I_L than I_{LOAD} in the buck mode. The DC–DC converter in [9] has two different operating modes for the buck–boost converter, as shown in Figure 1b,c. Therefore, mode transition issues occur when V_{IN} and V_{OUT} become similar, and a complex control system is required to solve these issues. However, as mentioned previously, the proposed work has a single-mode operation, and therefore, it generates a target V_{OUT} level even in a wide range of V_{IN} through only duty control without the mode transition issues.

Table 1. Comparison with prior buck–boost DC–DC converters.

	Conversion Ratio	Average i_L (I_L)	Conduction Loss (P_{CD})	i_L Ripple (Δi_L)
Proposed	$M_{PROP} = \frac{2}{3(1-D)}$	$\frac{2}{3(1-D)} I_{LOAD}$	$M_{PROP}^2 I_{LOAD}^2 \left[R_{ON} \left\{ \frac{(1-D)^2}{2D} - D + 2 \right\} + R_{DC} \right]$	$\frac{V_{IN} T_{CK}}{L} \times \frac{2M_{PROP}-1}{3M_{PROP}}$
[7]	$M_{R7} = \frac{1}{2(1-D)}$	$\frac{1}{2(1-D)} I_{LOAD}$	$M_{R7}^2 I_{LOAD}^2 \left[R_{ON} \left\{ \frac{2(1-D)^2}{D} - D + 2 \right\} + R_{DC} \right]$	$\frac{V_{IN} T_{CK}}{L} \times \frac{2M_{R7}-1}{2M_{R7}}$
[9]	Buck mode $M_{R9,BCK} = \frac{1}{2-D}$	$\frac{1}{2-D} I_{LOAD}$	$M_{R9,BCK}^2 I_{LOAD}^2 \left[R_{ON} \left\{ \frac{(1-D)^2+1}{D} + 1 - D \right\} + R_{DC} \right]$	$\frac{V_{IN} T_{CK}}{L} \times \frac{(1-M_{R9,BCK})(2M_{R9,BCK}-1)}{M_{R9,BCK}}$
	Boost mode $M_{R9,BST} = 1 + D$	I_{LOAD}	$M_{R9,BST}^2 I_{LOAD}^2 \left\{ R_{ON} \left(D + \frac{D^2+1}{1-D} \right) + R_{DC} \right\}$	$\frac{V_{IN} T_{CK}}{L} (2 - M_{R9,BST})(M_{R9,BST} - 1)$
Inductive buck–boost	$M_{BB} = \frac{D}{1-D}$	$\frac{1}{1-D} I_{LOAD}$	$M_{BB}^2 I_{LOAD}^2 \left(\frac{2R_{ON}+R_{DC}}{D^2} \right)$	$\frac{V_{IN} T_{CK}}{L} \times \frac{M_{BB}}{1+M_{BB}}$

Figure 5 shows a comparison of the normalized P_{CD} based on the analysis presented in Table 1. P_{CD} as shown in Figure 5a is normalized by I_{LOAD}^2 , and P_{CD} as shown in Figure 5b is normalized by P_{CD} of the inductive buck–boost converter ($P_{CD,BB}$). As shown in Figure 5a, the proposed method always shows a lower P_{CD} than that of the inductive buck–boost converter. In the inductive buck–boost converter, I_L is always higher than I_{LOAD} due to the discontinuous i_{DLV} .

For a fair comparison with state-of-the-art works, P_{CD} is compared by considering the operating conditions of Li-ion batteries. The target V_{IN} ranges from 2.8 V to 4.2 V, and the target V_{OUT} is 3.3 V for mobile applications. Figure 5b shows a comparison of $P_{CD,PROP}$ to each P_{CD} of the prior works under the operating conditions such that their respective V_{IN} , V_{OUT} , and clock frequency (f_{CK}) are the same. As shown in Figure 5b, the proposed method shows a lower P_{CD} than that of the converter in [7]. The longer the period of DT_{CK} , the higher the P_{CD} , because I_L increases with D . For the same V_{OUT} level, D of the proposed method is always lower than that in [7]. This implies that the proposed method always has a lower I_L than the prior method, and therefore, the proposed method shows lower P_{CD} even with the same power stage topology.

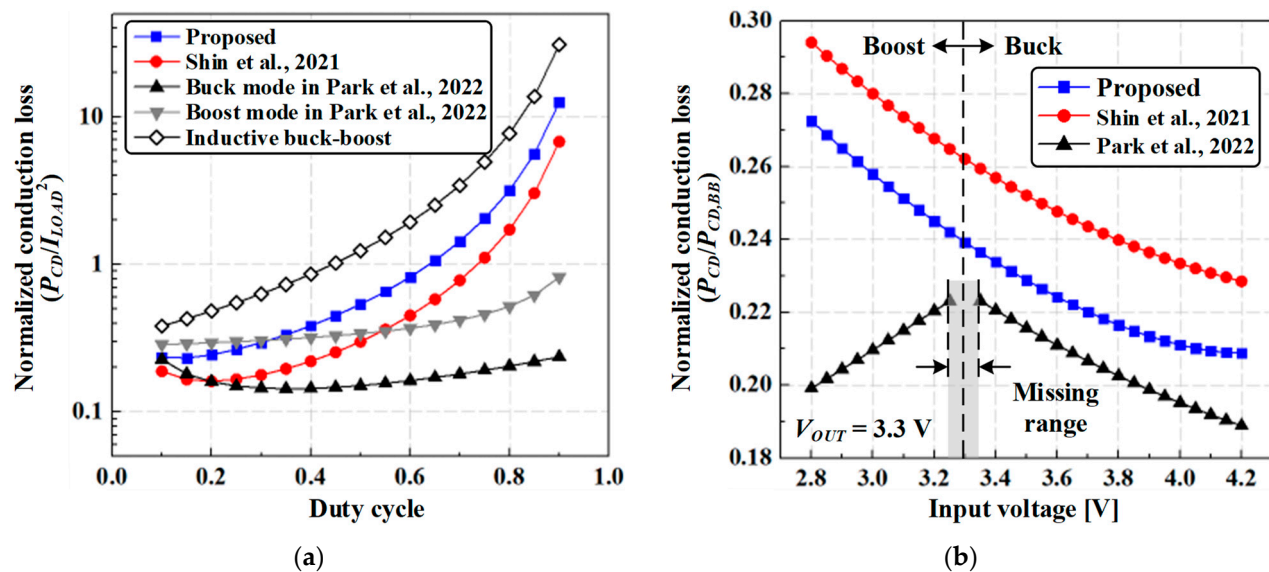


Figure 5. Comparisons of the normalized conduction loss according to (a) the duty cycle and (b) input voltage, comparing the proposed work with those in [7,9].

In the case of the boost mode, the proposed method and the method in [7] have a larger I_L than I_{LOAD} because the inductor is always connected to V_{IN} . Therefore, I_L increases as the conversion ratio increases. However, the hybrid buck–boost converter in [9] always has a lower I_L than I_{LOAD} because it utilizes the switched-inductor-capacitor topology and dual-path current technique in the boost and buck modes, respectively. Moreover, the number of power switches in the current path is smaller than that in the proposed method. Although the converter in [9] shows lower P_{CD} , the difference in power loss decreases when V_{IN} approaches 3.3 V. In addition, regulating V_{OUT} becomes difficult because of the missing conversion-ratio range.

2.3. Analysis of Inductor Current Ripple

One advantage of the proposed method is its low i_L ripple. As shown in Figure 3, the i_L ripple of the proposed method can be expressed as follows:

$$\begin{aligned} \Delta i_L &= \frac{V_{IN}}{L} \times (0.5DT_{CK}) + \frac{V_{IN}-V_{OUT}}{L} \times \{0.5(1-D)T_{CK}\} + \frac{V_{IN}}{L} \times (0.5DT_{CK}) \\ &= \left| \frac{V_{IN}-2V_{OUT}}{L} \right| \times \{0.5(1-D)T_{CK}\} \end{aligned} \quad (12)$$

$$\Delta i_L = \frac{V_{IN}T_{CK}}{2L} \times \left| 1 - \frac{2V_{OUT}}{V_{IN}} \right| \times (1-D), \quad (13)$$

where Δi_L denotes the ripple of i_L . Using (2), D is expressed by M_{PROP} to compare the ripple of i_L according to the conversion ratio. Subsequently, i_L can be expressed as follows:

$$D = \frac{3M_{PROP} - 2}{3M_{PROP}} \quad (14)$$

$$\Delta i_L = \frac{V_{IN}T_{CK}}{2L} \times |1 - 2M_{PROP}| \times \left(1 - \frac{3M_{PROP} - 2}{3M_{PROP}} \right) = \frac{V_{IN}T_{CK}}{L} \times \frac{2M_{PROP} - 1}{3M_{PROP}}. \quad (15)$$

The i_L ripple of the prior converters is also analyzed according to the conversion ratio, as shown in Table 1. As mentioned previously, the converter in [7] comprises the same power stage as that in the proposed work, but it operates only in two phases (Φ_1 and Φ_3). It always builds up i_L with the voltage across the inductor of V_{IN} , and discharges with $(V_{IN} - 2V_{OUT})$. However, the proposed method operates in three phases, and whether

i_L is charged or discharged during Φ_2 is determined by the operating mode. Unlike Φ_3 , a voltage of $(V_{IN} - V_{OUT})$ is applied across the inductor in Φ_2 . Therefore, as shown in Figure 3, i_L builds up more in the buck mode and is discharged in the boost mode during Φ_2 . In this case, the inductor voltage during Φ_2 is lower than that during Φ_3 , and this makes the ripple of i_L 33.33% smaller than that in the conventional work.

With respect to the conversion ratio, the two-phase operation regulates V_{OUT} down to a low voltage close to $1/2$ of V_{IN} , but the proposed method regulates down to $2/3$ of V_{IN} for low i_L ripple. When considering the applications of Li-ion batteries, the conversion ratio of $(2/3 < M_{PROP} < \infty)$ is sufficient for V_{OUT} to reach the target voltage of 3.3 V.

i_{DLV} of the DPBB topology comprises i_L and $i_{C,1}$. In the capacitor-delivery phase, the i_{DLV} is determined by the charge-sharing process between capacitors, which results in an exponential current profile. Compared with the linearly varying inductor current, this behavior produces a larger instantaneous variation in the delivered current, leading to increased i_{DLV} ripple. To analyze this behavior, the capacitor current $i_{C,1}$ during the charge-sharing process can be expressed as

$$i_{C,1} = I_0 e^{-\frac{t}{\tau}} \quad (16)$$

where τ is the time constant composed of both resistance and capacitance including C_F . The charge balance of the C_F defines the coefficient I_0 of (16). In other words, both the average values of $i_{C,1}$ and $i_{L,3}$, which is the L-path current in Φ_3 , should be the same in steady state, which is expressed as follows:

$$\begin{aligned} \int_0^{DT_{CK}} i_{C,1}(t) dt &= \int_{0.5(1+D)T_{CK}}^{T_{CK}} i_L dt \\ \int_0^{DT_{CK}} I_0 e^{-\frac{t}{\tau}} dt &= 0.5(1-D)I_L T_{CK} \\ I_0 &= \frac{0.5(1-D)I_L T_{CK}}{\tau(1-e^{-DT_{CK}/\tau})} \end{aligned} \quad (17)$$

Substituting (17) into (16), $i_{C,1}$ is given by

$$i_{C,1} = \frac{0.5(1-D)I_L T_{CK}}{\tau(1-e^{-DT_{CK}/\tau})} e^{-\frac{t}{\tau}} \quad (18)$$

From (18), the $i_{C,1,pp}$ (peak-to-peak $i_{C,1}$) can be expressed as

$$i_{C,1,pp} = \frac{0.5(1-D)I_L T_{CK}}{\tau(1-e^{-DT_{CK}/\tau})} \left(1 - e^{-\frac{0.5D}{\tau}}\right) \quad (19)$$

Figure 6 compares the capacitor current ripple of the proposed structure and that of [7]. Here, $i_{C,1,pp,norm}$ denotes the normalized capacitor current ripple, defined as $I_L T_{CK}/\tau$. As shown in Figure 6, the proposed structure exhibits a smaller capacitor current ripple than [7] over the entire buck–boost conversion-ratio range.

Figure 7 shows the simulation results of the V_{OUT} ripple according to I_{LOAD} in the buck and boost modes. As shown in Figure 7a, the V_{OUT} ripple increases as I_{LOAD} increases in all the cases.

In the case of the converter in [9], i_L is always delivered to V_{OUT} , and it utilizes a longer D than the others. Therefore, the V_{OUT} ripple is smaller than that in other works. When compared to the operation in [7], the proposed method shows a smaller ripple of V_{OUT} because it has a smaller capacitor current ripple, as discussed in Figure 6. In the case of the boost mode, the method in [9] shows the smallest ripple of V_{OUT} since i_{DLV} is equal to i_L , as shown in Figure 7b. When compared to the prior DPBB converter, the proposed method also shows a smaller V_{OUT} ripple.

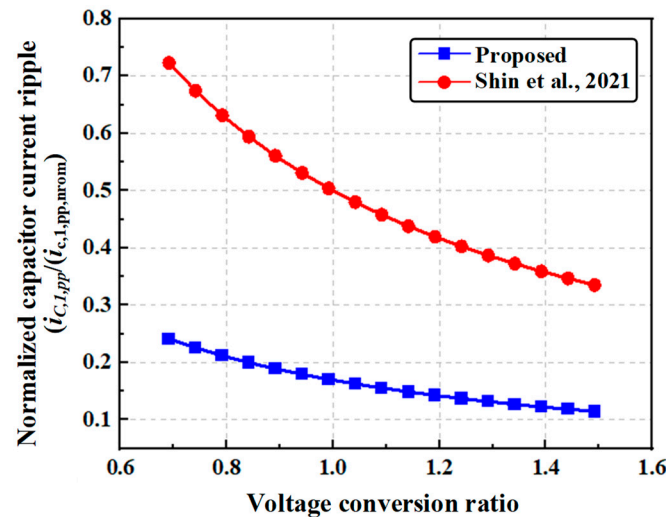


Figure 6. Comparisons of the normalized capacitor current ripple, comparing the proposed work with that in [7].

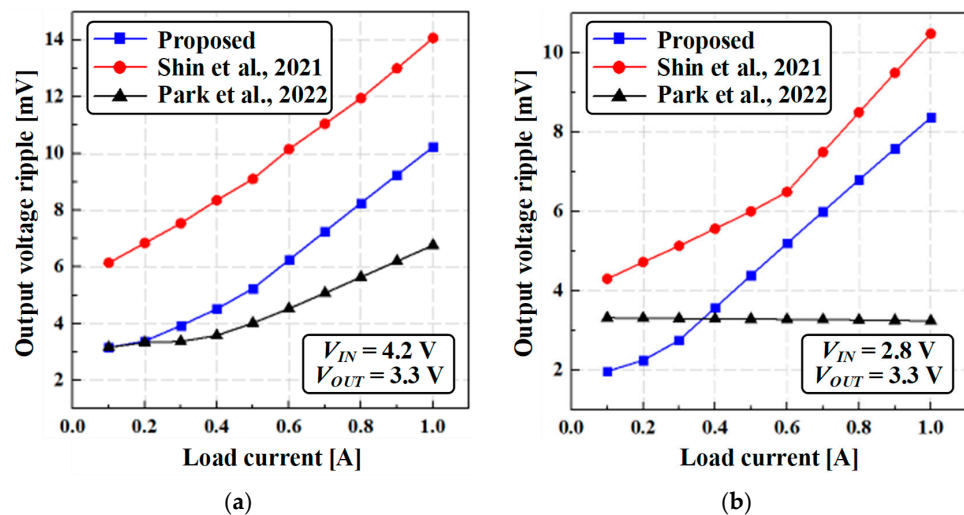


Figure 7. Comparisons of the output voltage ripple between the proposed work and conventional works in [7,9]: (a) buck mode and (b) boost mode.

3. Circuit Implementation

3.1. Dual-Phase Dual-Path Buck-Boost Converter

Figure 8 shows the top block diagram of the proposed hybrid dual-phase DPBB converter. It has two DPBB stages which operate with a phase difference of 180° . D is determined by the error voltage (V_{ERR}) and ramp signal, which is compensated by the current sensor [27] for low-sided power switches. The proposed work adopts a dual-phase structure with $2.2\text{ }\mu\text{H}$ commercially available shielded ferrite-core inductors (Bourns, Riverside, CA, USA). Due to the low power level and limited flux swing, the magnetic core loss is negligible compared to conduction and switching losses at 1 MHz . In addition, the proposed offset-controlled ZCD is implemented to enhance efficiency under light-load conditions. The level shifters and inverter-based drivers employ a VDD selector to drive the power switches.

between single- and dual-phase DPBB converters. As shown in Figure 10b, the dual-phase operation achieves a V_{OUT} ripple reduction of up to 2.567 mV (67.5%).

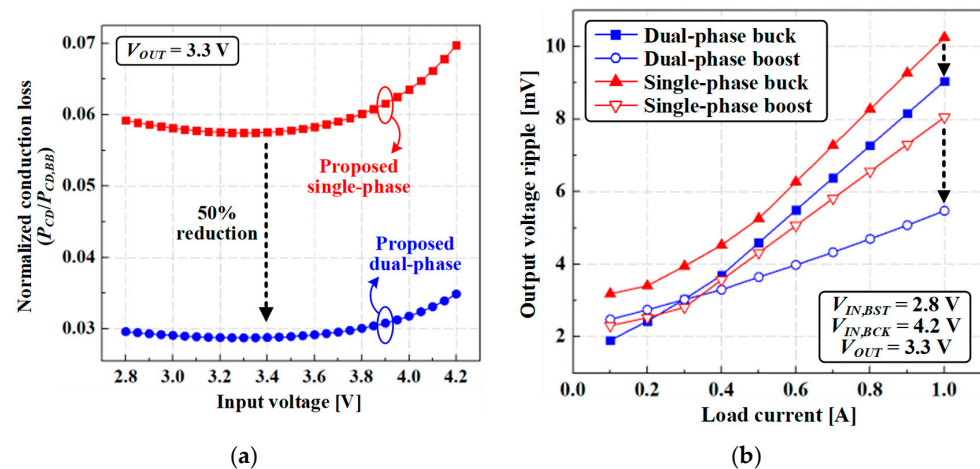


Figure 10. Comparison of the (a) conduction loss and (b) output voltage ripple.

Figure 11 shows the simulated loss breakdown of the proposed dual-phase DPBB converter according to I_{LOAD} with different input voltages. P_{SW} includes both the voltage-current overlap loss during switching transitions and the gate charging and discharging loss. Figure 11a shows the loss breakdown with $V_{IN} = 2.8$ V. When compared to that with $V_{IN} = 4.2$ V, it shows a larger P_{CD} with the same I_{LOAD} because the conductivity of the power switches is less with lower supply voltage. Under the light-load condition of $I_{LOAD} = 100$ mA, the total loss is calculated as an average of 15.09% of the output power. At $I_{LOAD} = 1.3$ A, the portion of the power loss is reduced in efficiency, and the total loss is calculated as 4.423% of the output power on average.

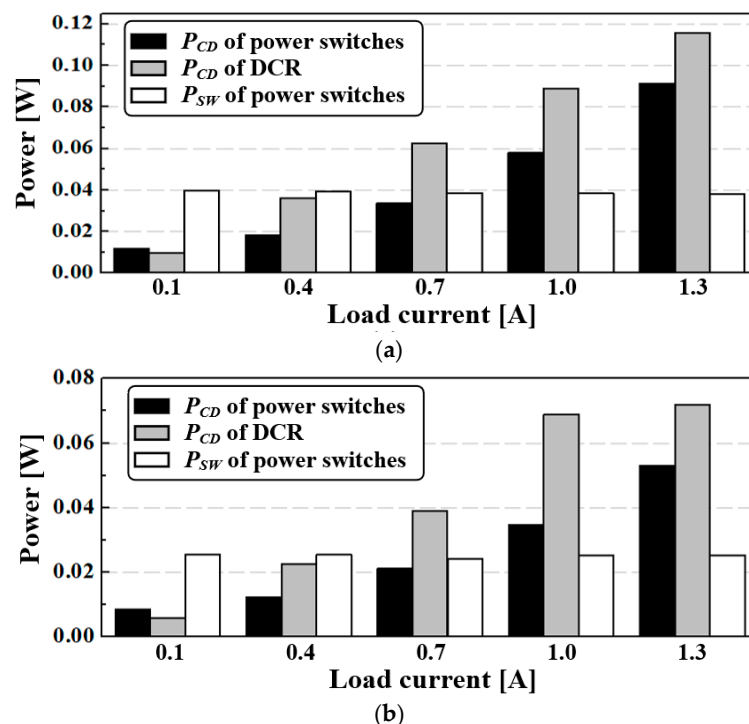


Figure 11. Loss breakdown of the proposed dual-phase DPBB converter according to I_{LOAD} at (a) $V_{IN} = 2.8$ V and (b) $V_{IN} = 4.2$ V.

3.2. Proposed Offset-Controlled Zero-Current Detector

As mentioned previously, the proposed dual-phase hybrid buck–boost converter operates in DCM over a wider I_{LOAD} range than single-phase converters. In conventional implementations, ZCD is typically performed using a single static comparator that compares the relevant node voltages. Figure 12 shows the waveforms of DCM operation with the conventional static comparator. As shown in Figure 12, although the static comparator ideally detects the zero-current point when V_{CB} equals V_{OUT} , its propagation delay causes the power switches ($S_{4,A}$ and $S_{4,B}$) to turn off after i_L reaches 0 A. Consequently, reverse inductor current flows, leading to additional power loss.

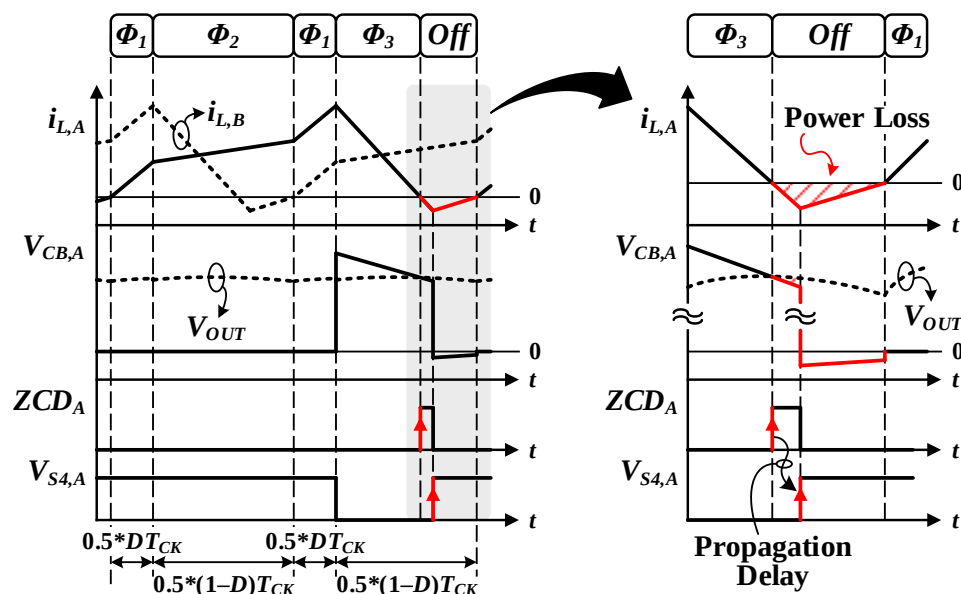


Figure 12. Waveforms of the proposed dual-phase DPBB converter with the strong-armed-latch comparator in DCM.

To compensate for the timing mismatch owing to the propagation delay, an offset-controlled ZCD is proposed. The block diagram is shown in Figure 13a, and it consists of an offset-controlled comparator, a charge pump, and a dynamic comparator. A schematic of the offset-controlled strong-arm latch comparator for the proposed ZCD is shown in Figure 13b. It is designed with the duty-cycled type to reduce power consumption [28]. When input voltage (V_{CB}) falls below the negative input voltage (V_{OUT}), an intentional offset voltage (V_{OS}) is introduced at the negative input transistor (M_1) by connecting an offset-injecting transistor (M_{OS}) in parallel. For the analytical derivation, both M_1 and M_{OS} are assumed to operate in the saturation region, and the large-signal MOS drain current equation is used. The resulting V_{OS} is calculated as follows:

$$\begin{aligned} \frac{1}{2}\mu_n C_{OX} \left(\frac{W}{L}\right)_1 (V_{CB} - V_{th})^2 + \frac{1}{2}\mu_n C_{OX} \left(\frac{W}{L}\right)_{OS} (V_{CTRL} - V_{th})^2 \\ = \frac{1}{2}\mu_n C_{OX} \left(\frac{W}{L}\right)_1 (V_{CB} + V_{OS} - V_{th})^2 \end{aligned} \quad (20)$$

$$V_{OS} = \sqrt{(V_{CB} - V_{th})^2 + \frac{(W/L)_{OS}}{(W/L)_1} (V_{CTRL} - V_{th})^2} - (V_{CB} - V_{th}) \quad (21)$$

where V_{CTRL} denotes the control voltage of M_{OS} .

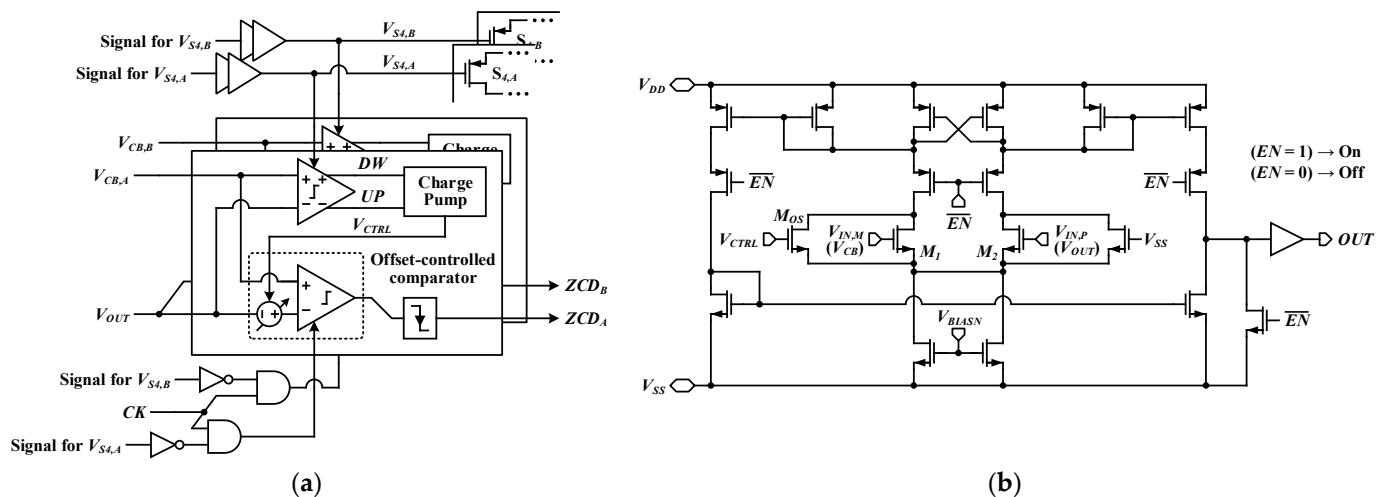


Figure 13. Block diagram of the proposed (a) offset-controlled ZCD, and (b) offset-controlled strong-arm latch comparator.

Figure 14 shows the waveforms of the proposed ZCD. When the buffered gate signals ($V_{S4,A}$ and $V_{S4,B}$) are triggered to turn off the power switches, the dynamic comparator determines whether V_{CB} or V_{OUT} is higher. If V_{CB} is lower than V_{OUT} , the charge pump increases the offset voltage (V_{CTRL}), and the output signals of the offset-controlled ZCD (ZCD_A and ZCD_B) are triggered earlier. Otherwise, if V_{CTRL} is higher than the optimum point, $S_{4,A}$ and $S_{4,B}$ are turned off when V_{CB} is higher than V_{OUT} . This implies that the power switches are turned off when each i_L is still positive, and that some charge remains to be transferred to V_{OUT} . Therefore, the charge pump decreases V_{CTRL} to reduce the offset voltage of the proposed ZCD, as shown in Figure 14.

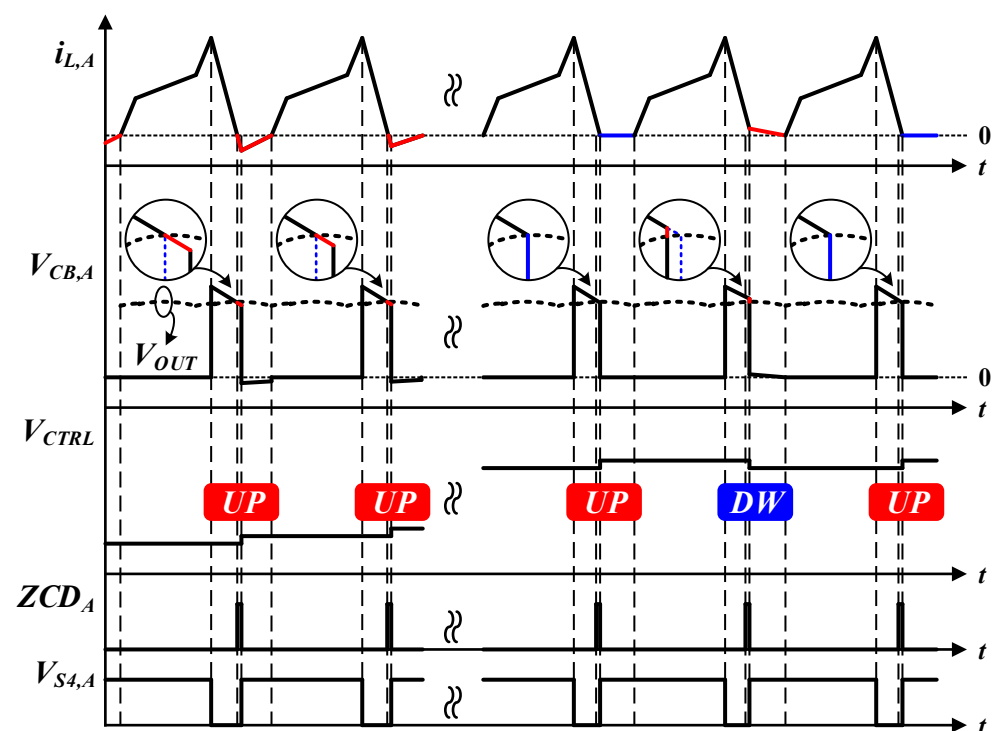


Figure 14. Waveforms of the proposed offset-controlled ZCD.

Figure 15 shows the simulation results of the proposed ZCD. With 3.3 V of V_{OUT} , each V_{CTRL} is regulated at 2.833 V on average. Figure 15b compares the accuracy of the proposed

ZCD with the conventional work, which comprises the strong-arm-latch comparator. The conventional work suffers from both propagation delay and comparison time; therefore, the power switches are turned off at $I_{L,A}$ of -8.502 mA. However, the proposed ZCD turns off the power switch at -0.543 mA of $I_{L,A}$ by intentionally applying and adjusting the offset to the comparator.

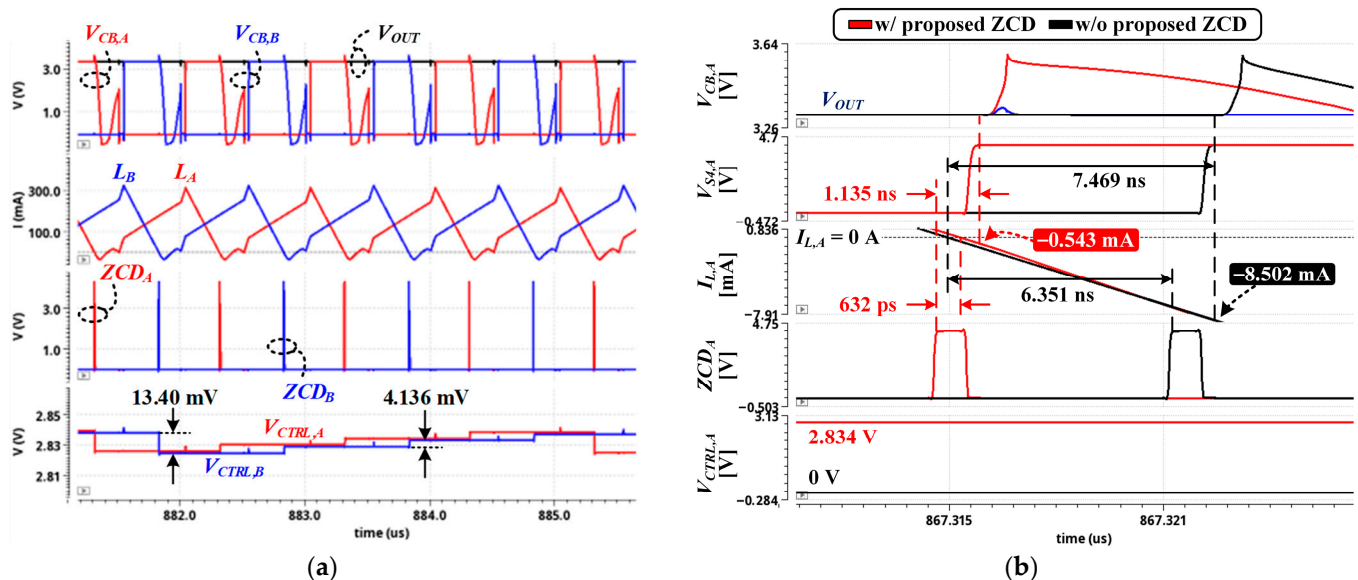


Figure 15. Simulation results of (a) the steady-state operation of the proposed ZCD and (b) comparison to the conventional work.

The bias-control ZCD forms a bang-bang feedback loop that iteratively adjusts the comparator offset. Since the resulting timing correction step is much smaller than the comparator decision time, the loop converges stably without oscillation.

Figure 16 shows the simulation results of the timing error according to I_{LOAD} . As the input voltage decreases, the bandwidth of the comparator used in the ZCD decreases, which degrades timing error. In addition, the propagation delay of the logic and driver also increases as the input voltage decreases, resulting in a larger timing error. On the other hand, the slope of the inductor current is determined by the voltage difference across the inductor. Therefore, the decreasing slope of the inductor current is only weakly affected by I_{LOAD} . As a result, for a fixed V_{IN} , the variation in timing error with respect to I_{LOAD} is relatively small.

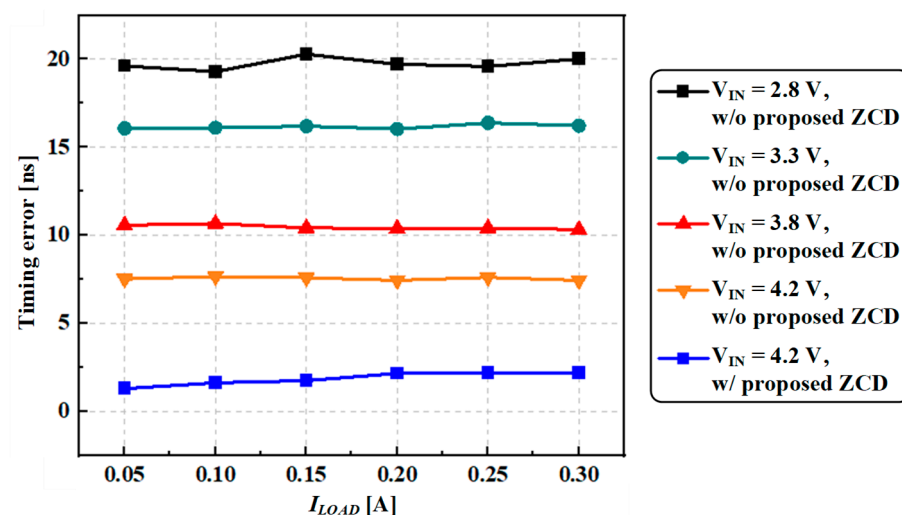


Figure 16. Comparison of timing error with and without the proposed ZCD.

Figure 17 shows the relationship between the required comparator offset V_{OS} and the load current. As the load current increases, the magnitude of the required offset increases from approximately $-40 \mu\text{V}$ to $-100 \mu\text{V}$. This is because the slope of V_{CB} becomes steeper near the zero-crossing point as the load current increases. As a result, a larger offset is required to compensate for the ZCD sensing delay and to suppress reverse inductor current.

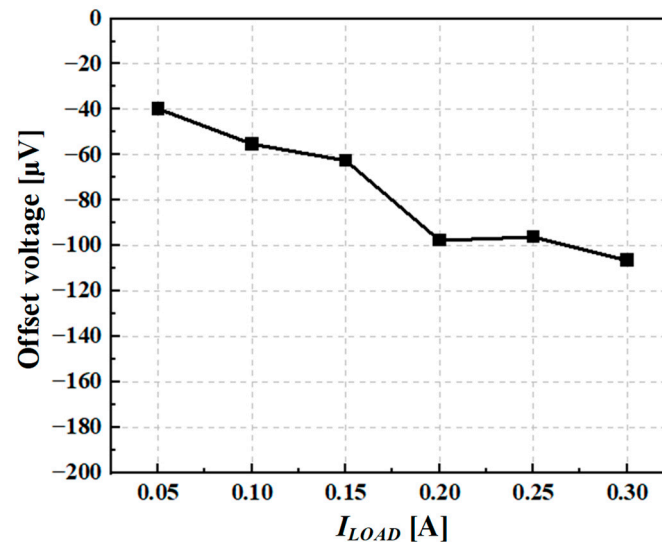


Figure 17. Variation of the comparator offset voltage with load current.

4. Measurement Results

Figure 18 shows a chip micrograph of the proposed dual-phase DPBB converter. The chip is fabricated using a 1P6M 180-nm BCD process for performance verification. The chip area is 5.897 mm^2 and the core area is 3.82 mm^2 . Two inductors of $2.2 \mu\text{H}$ ($\text{DCR} = 140 \text{ m}\Omega$) are used, and the size of both C_F and C_{OUT} is $10 \mu\text{F}$. The switching period of the system is designed to be 1 MHz . V_{OUT} is regulated to 3.3 V , and the chip is measured while changing V_{IN} and I_{LOAD} .

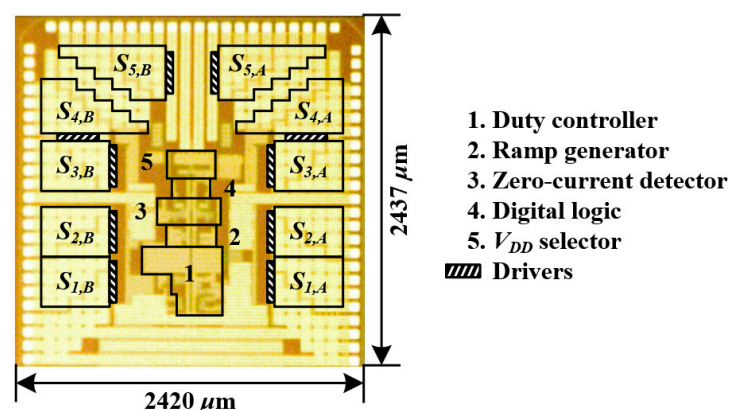


Figure 18. Chip micrograph.

Figure 19a shows the measured waveforms of the buck mode at $V_{IN} = 4.2 \text{ V}$ and $I_{LOAD} = 500 \text{ mA}$. The ripple of V_{OUT} is measured as 8 mV , excluding the switching noise owing to the equivalent series resistance of C_{OUT} . Figure 19b shows the steady-state waveforms of the boost mode at $V_{IN} = 2.8 \text{ V}$ and $I_{LOAD} = 500 \text{ mA}$. In this case, the V_{OUT} ripple is measured as approximately 7 mV . Because i_{DLV} of the proposed work is always continuous with alternative i_L and i_C , the V_{OUT} ripple is reduced under the similar operating conditions when compared to that of the conventional works [5,9]. Figure 19c shows the

ripple of V_{OUT} and gate signals with $D = 0.43$. Figure 19d shows the total i_{DLV} with the ripple of V_{OUT} . The waveform of the total i_{DLV} corresponds to 25% of the actual i_{DLV} under the light-load condition.

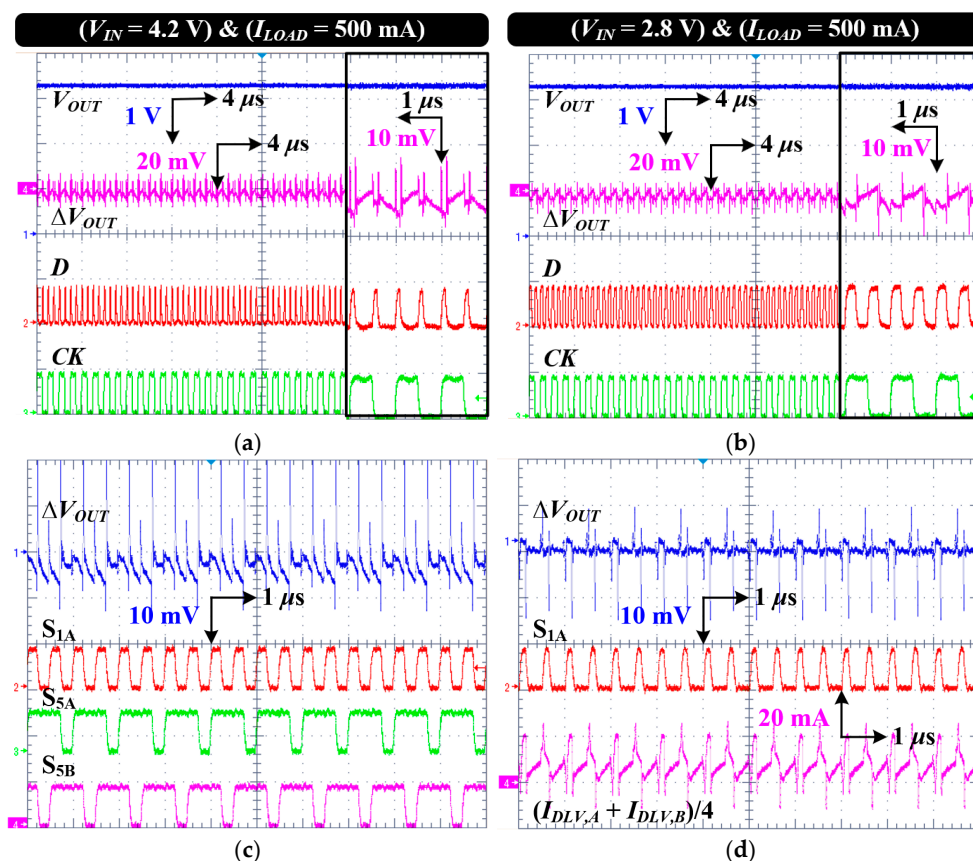


Figure 19. Measured steady-state waveforms: (a) buck mode at $V_{IN} = 4.2$ V and $I_{LOAD} = 500$ mA; (b) boost mode at $V_{IN} = 2.8$ V and $I_{LOAD} = 500$ mA; (c) V_{OUT} ripple and gate signals at $D = 0.43$; (d) total i_{DLV} with the V_{OUT} ripple.

Figure 20 shows the load-transient response of the proposed work. As shown in Figure 20a, I_{LOAD} is changed between 0.1 A and 1.701 A with $V_{IN} = 4.2$ V. The undershoot of V_{OUT} is measured to be approximately 100 mV, and the settling time is measured to be 160 μ s. The overshoot is measured at approximately 100 mV with a settling time of 100 μ s. Figure 20b shows the load-transient response with $V_{IN} = 2.8$ V. As V_{IN} decreases, the overall response deteriorates for similar I_{LOAD} change. The topology in this work stores the energy in the inductor during D , and this delays the energy transfer the input to V_{OUT} under light-to-heavy load transition. Therefore, it has a right-half-plane zero due to indirect energy transfer.

The measured power conversion efficiency of the proposed work is shown in Figure 21. The efficiency is measured V_{IN} ranging from 2.8 V to 4.2 V for the Li-ion battery applications. The peak efficiency in the boost mode is measured to be 95.88% at $V_{IN} = 4.2$ V and $I_{LOAD} = 800$ mA. The peak efficiency in the buck mode is measured to be 93.08% at $V_{IN} = 3.1$ V and $I_{LOAD} = 800$ mA. The proposed work is designed to a higher I_{LOAD} range exceeding 1 A; therefore, the sizes of the power switches are designed to be larger than those of certain prior hybrid buck–boost converters. As shown in Figure 21, the lower the V_{IN} , the lower the conductivity of the power switches, and consequently, the lower the efficiency. When V_{IN} decreases by 100 mV, the power conversion efficiency decreases by approximately 2.1%. However, the proposed hybrid buck–boost converter maintains more than 90% efficiency for I_{LOAD} larger than 300 mA over all V_{IN} ranges.

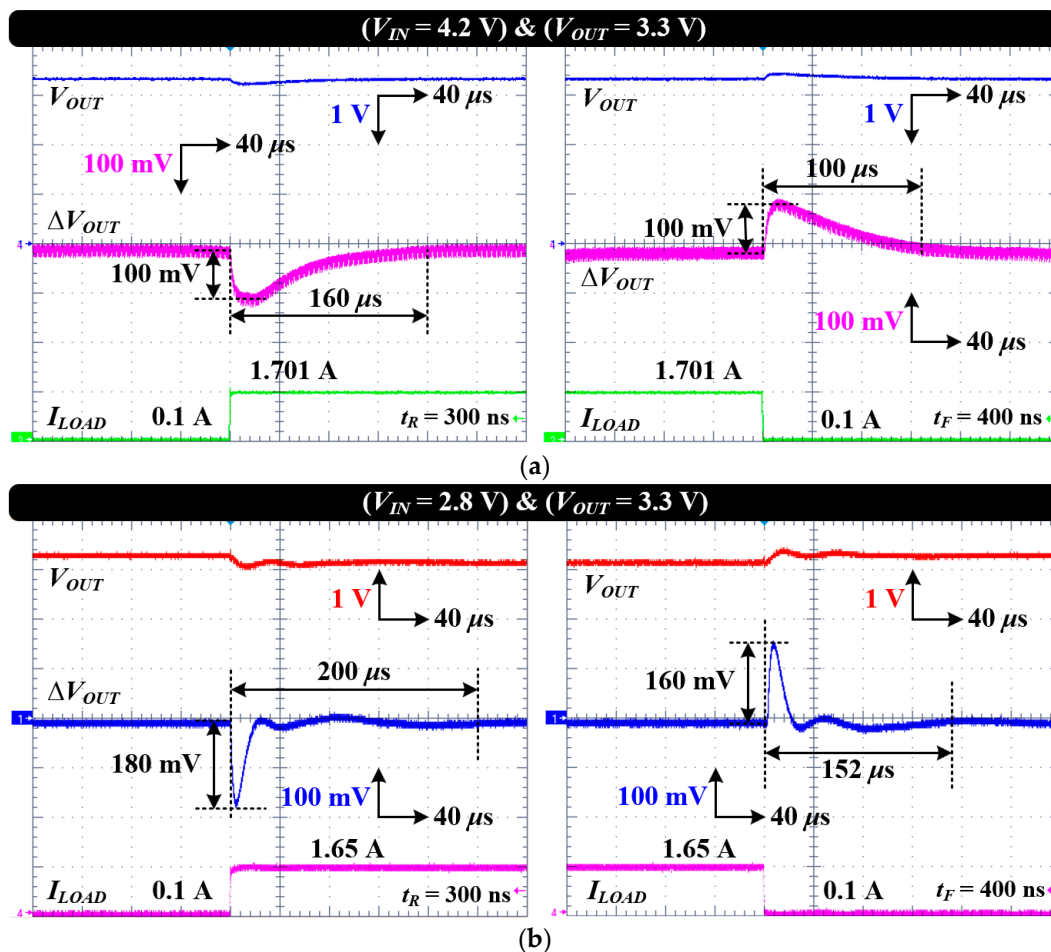


Figure 20. Measurement load-transient response with (a) $V_{IN} = 4.2$ V and (b) $V_{IN} = 2.8$ V.

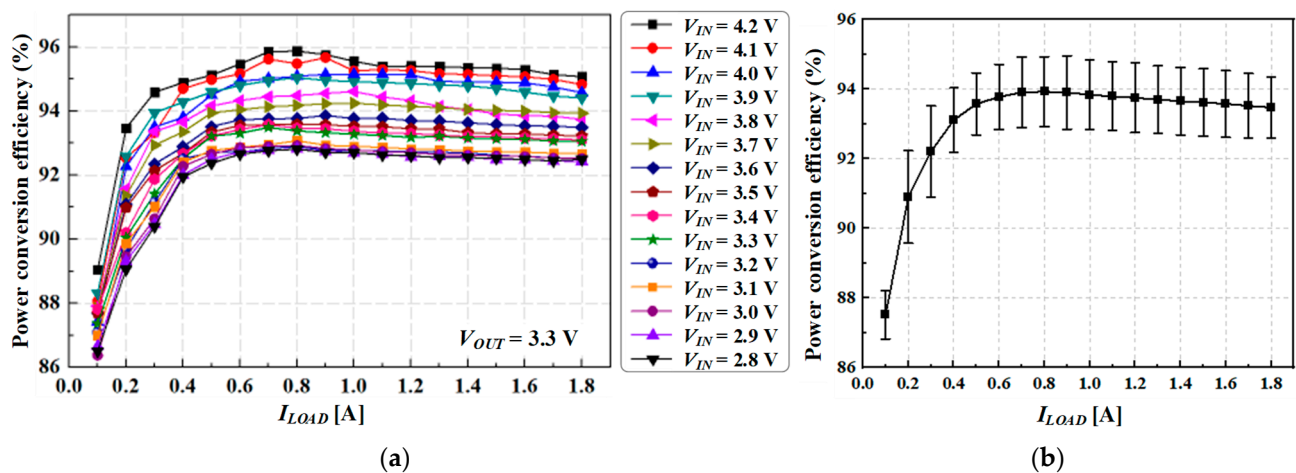


Figure 21. Measurement power conversion efficiency curves: (a) PCE versus I_{LOAD} for different V_{IN} ; (b) PCE with error bars.

Figure 21b shows the average efficiency with error bars derived from the results in Figure 21a. The error bars represent the standard deviation of the efficiency obtained under different input voltage conditions. The standard deviation remains around $\sim 1\%$ and reaches a maximum of approximately 1.3% across the load range. This result indicates that the efficiency variation with respect to the input voltage is relatively small, demonstrating that the proposed converter maintains stable efficiency over the wide input voltage range.

By comparing the measured PCE (power conversion efficiency) and the post-layout simulation results at room temperature (25 °C), the two results exhibit a similar trend. Although a larger deviation appears in the light-load region, the difference is around 1% in the normal load region. Based on this observation, the temperature-dependent PCE characteristics from 0 °C to 100 °C are analyzed through post-layout simulation in this work.

Figure 22 shows the temperature-dependent power conversion efficiency characteristics of the proposed converter. Figure 22a illustrates the PCE curves with respect to load current at five different temperatures. As the temperature increases, the PCE slightly changes due to the temperature-dependent characteristics of the power devices and passive components. Figure 22b presents the average PCE with error bars derived from the results in Figure 22a. The error bars indicate the standard deviation of the PCE across the different temperature conditions, while the solid line represents the mean value.

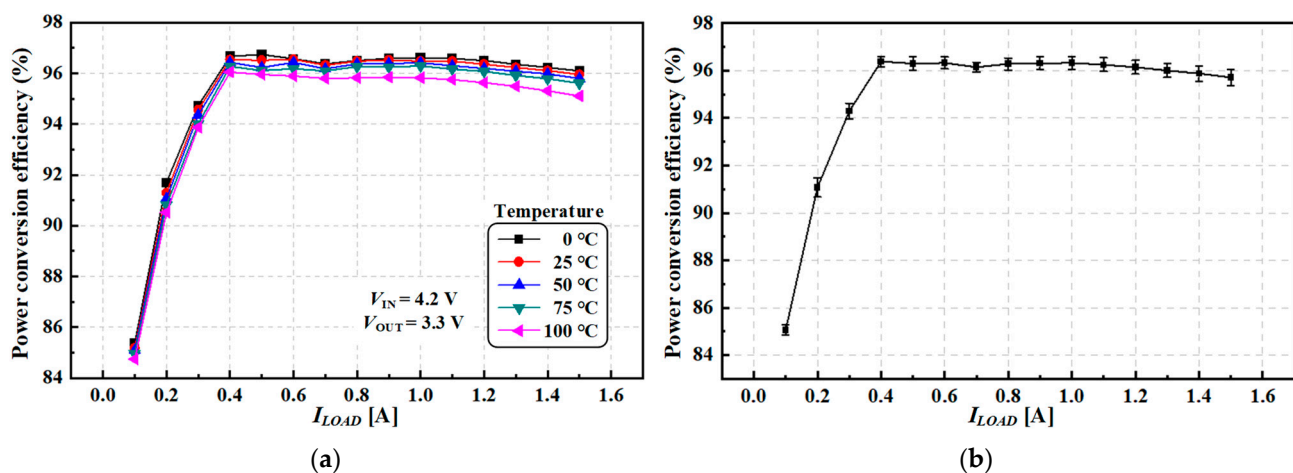


Figure 22. Simulation results of temperature-dependent power conversion efficiency curves: (a) PCE versus I_{LOAD} for different temperature; (b) PCE with error bars.

Table 2 presents a performance summary of the proposed work with a comparison to the state-of-the-art hybrid buck–boost converters. When compared to that in [7], the proposed work is designed with the same topology as that of the power stage. However, the proposed work is configured with dual phases to drive a wider range of I_{LOAD} . As a result, smaller i_L ripples and V_{OUT} ripples are obtained with four operating phases per cycle. In addition, several hybrid buck–boost converters reported in [29–31] are included in Table 2 to provide a broader performance comparison. The comparison results indicate that the proposed work achieves competitive efficiency compared with the prior works.

Furthermore, the load-transient response of the proposed structure is compared with the prior work in [7]. The proposed structure is capable of delivering a significantly larger load current. Specifically, the proposed structure achieves a current density of 0.68 A/mm², which is higher than 0.32 A/mm² reported in [7], indicating a stronger load driving capability per unit area. In terms of load-transient performance, the proposed structure also demonstrates competitive dynamic characteristics. The proposed structure achieves a T_{SETTLE} (settling time) of 160 μ s for a load step of 1.6 A, whereas [7] reports a T_{SETTLE} of 150 μ s for a load step of 0.45 A. When compared with the converters in [29–31], the proposed converter also demonstrates higher current density, implying improved load driving capability per unit chip area. Despite experiencing approximately more than three times larger load step, the proposed structure maintains a comparable T_{SETTLE} to that of [7]. These results verify that the proposed structure provides fast and stable load-transient response even under large load current variations.

Table 2. Performance comparison with prior hybrid buck-boost converters.

	This Work	ISCAS'21 [4]	SOVC'21 [7]	TPE'22 [9]	JSSC'21 [11]	ISSCC'20 [13]	JSSC'23 [29]	TPE'23 [30]	JSSC'24 [31]
Technology	180-nm BCD	180-nm BCD	180-nm BCD	180-nm BCD	0.5- μ m CMOS *	90-nm CMOS	180-nm BCD	180-nm BCD	180-nm BCD
Topology	Dual-path buck-boost	Switched- <i>L-C</i> buck-boost	Dual-path buck-boost	Dual-path buck /switched- <i>L-C</i> boost	Three-switch buck-boost	Three-level buck-boost	Dual-path buck-boost	Dual-path buck-boost	Dual-path buck-boost
# of phase	2	1	1	4	1	1	1	1	1
# of modes	1	3	1	2	2	3	1	1	1
V_{IN} [V]	2.8–4.2	2.5	2.8–4.2	1.2	9–45	2.8–5	2.9–4.2	2.7–4.2	2.7–4.2
V_{OUT} [V]	3.3	1.4–5	3.3	0.7–2.0	24	0.4–9	3.3	3.4	3.4
I_{LOAD} range [A]	0.1–1.8	0.3–1.5	0.2–1	0.08–2	0.3–2	0–1	0.2–1	0.02–0.7	0–1
L [μ H]	2×2.2	4.7	4.7	4×0.0047	12, 0.47	2.2	4.7	4.7	4.7
C_F [μ F]	2×10	10	10	4×0.1	22	10	2×10	10	2×10
C_{OUT} [μ F]	10	10	10	0.05	20	4.7	4.7	10	10
f_{SW} [MHz]	1	1	1	25	2	0.8–3	1, 1.5	1	1
i_L reduction	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Continuous I_{IN}	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes
DCM operation	Yes	No	No	Yes	No	No	No	No	No
Active area (mm ²) **	2.63	4.15	3.14	2.59	1.1	3.38	3.7	1.25	2.2
Current density (A/mm ²) ***	0.68	0.36	0.32	0.77	1.82	0.29	0.27	0.56	0.45
T_{SETTLE} [μ s] @ ΔI_{LOAD} [A]	160 @ 1.6	N.A	150 @ 0.45	0.3 @ 1.8	N.A	N.A	N.A	N.A	22 @ 1
Peak efficiency (DCR of L)	95.88% (140 m Ω)	92.87% (250 m Ω)	96.6% (N.A)	89.49% (60 m Ω)	97.6% (N.A)	96.8% (N.A)	93.8% (175 m Ω)	95.63% (288 m Ω)	95.5% (250 m Ω)

* Driving circuit for GaN switches ** Estimated from die micrograph *** Current Density = Max. I_{LOAD} / Active Area.

The prior hybrid buck-boost converters require more than two operating modes for the buck and the boost modes. However, the proposed work has only one switching operation, and the operating mode is determined by only D to address the mode transition issues. Most hybrid buck-boost converters have a continuous i_{DLV} , but I_{IN} is not continuous. Therefore, they have a dip in the power efficiency with the bondwire parasitic inductance [32]. However, both I_{IN} and i_{DLV} of the proposed work are continuous; therefore, the input capacitor could be smaller than in the prior works. Moreover, as the average i_L level is reduced with the dual-path strategy, the efficiency is improved by reducing the conduction loss owing to DCR. The maximum power conversion efficiency is measured to be 95.88% with 140 m Ω of DCR.

When compared to the prior work in [7], the switching loss of the proposed work can be slightly larger, because the proposed operation causes more switching operations. However, it is expected that the conduction loss due to $i_{L,rms}$ is smaller because Δi_L is smaller. In addition, comparable efficiency is expected with a small-sized inductor [33].

5. Conclusions

In this paper, a dual-phase dual-path hybrid buck–boost converter with an offset-controlled zero-current detector was presented for Li-ion battery applications. The proposed DPBB switching scheme enables seamless buck and boost operation using a single duty-cycle control, while the dual-phase architecture reduces conduction loss and improves current handling capability. In addition, the offset-controlled ZCD compensates for the propagation delay of control signals, effectively suppressing reverse current and supporting reliable DCM operation. As a result, the proposed converter achieves reduced inductor current ripple, lower conduction loss, and improved output voltage regulation.

The prototype was implemented in a 180-nm CMOS process and demonstrated peak efficiencies of 95.88% and 93.08% in the buck and boost modes, respectively, with an inductor DCR of 140 mΩ. A detailed EMI evaluation was not included in this work, since accurate EMI characterization requires a dedicated PCB-level implementation and standardized measurement setup. Such evaluation is strongly influenced by package parasitics and board layout rather than the intrinsic IC-level circuit topology.

The proposed converter employs a dual-phase architecture in which two power stages operate in parallel. Ideally, the currents of the two phases should be balanced. However, in the prototype implemented in this work, a dedicated current-balancing technique is not employed, and therefore current imbalances between the two phases may occur. In particular, if the voltages of the two C_F s are not perfectly matched, a mismatch between the inductor currents $I_{L,A}$ and $I_{L,B}$ of the two power stages can arise.

Figure 23 shows the simulation results of the inductor current mismatch caused by the voltage imbalance between the two flying capacitors. As I_{LOAD} increases from 100 mA to 1.3 A, the maximum difference between the two average $I_{L,A}$ and $I_{L,B}$ is calculated to be 38.9 mA when the voltage mismatch reaches 57 mV.

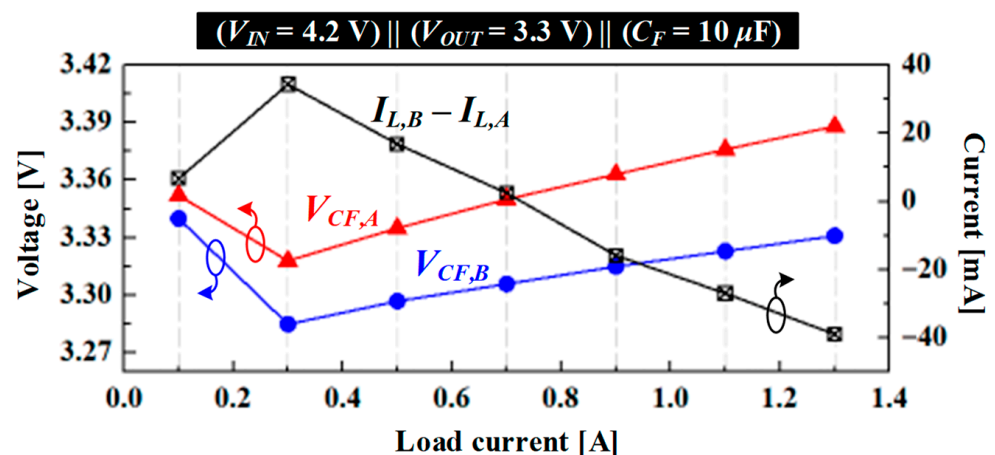


Figure 23. Current mismatch due to the voltage imbalance between two C_F s.

In practical implementations, the capacitor and inductance values of the two power stages may not be perfectly identical. To investigate the impact of such component mismatches, parametric simulations were performed by varying the C_F and inductance values. Figure 24a,b shows the variations in the V_{OUT} ripple and the inductor currents of each phase due to the mismatch of C_F and inductance, respectively. As shown in Figure 24a, when the capacitance varies by $\pm 10\%$, the V_{OUT} ripple changes by up to 1 mV (1.53%). In the case of inductance variation, the V_{OUT} ripple changes up to 1.03 mV (1.34%) with an inductance variation of $\pm 10\%$, as shown in Figure 24b.

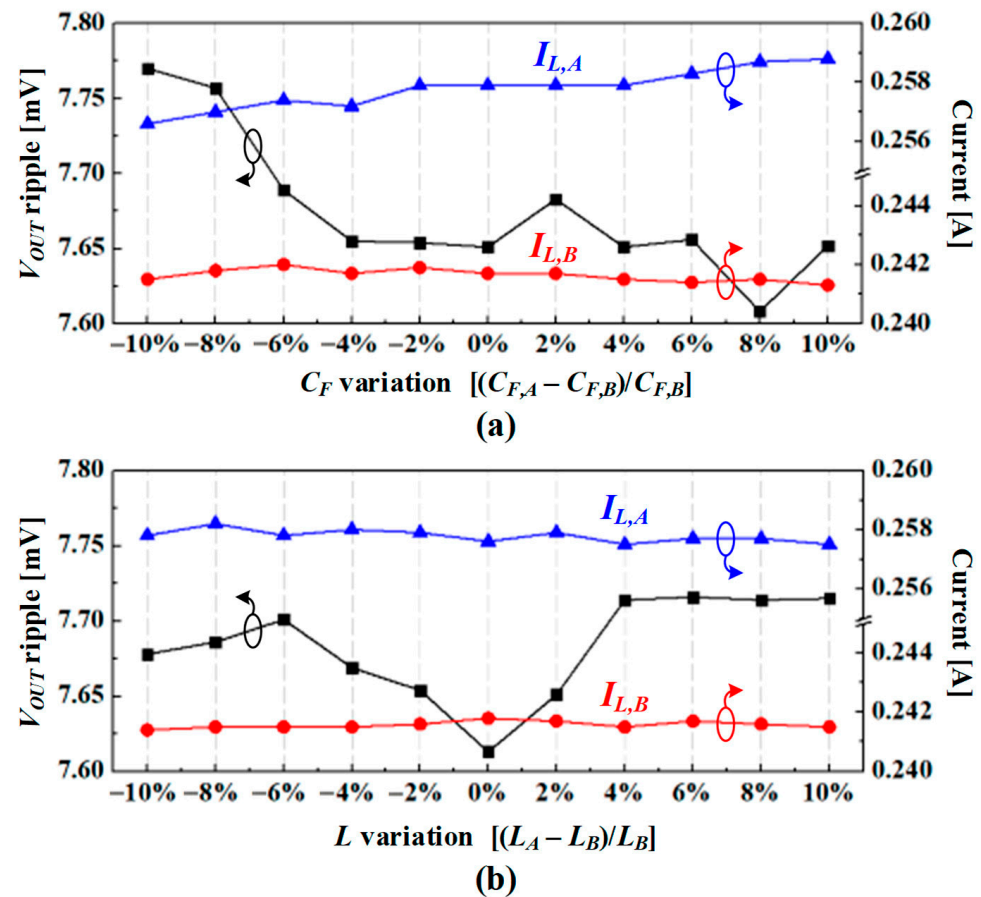


Figure 24. Transient waveforms with current mismatch in (a) conventional multiphase and (b) proposed dual-phase buck-boost converters.

Future work may focus on addressing the limitations discussed above. For example, a current-balancing technique that senses the voltages of the two flying capacitors and compensates for their voltage difference could be introduced to mitigate the current imbalance which occurs in the dual-phase architecture. Such an approach could help maintain better current balance between the two phases and further improve the overall performance of the dual-phase converter.

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Symbols

The following symbols are used in this manuscript:

V_{IN}	Input voltage
V_{OUT}	Output voltage
I_{IN}	Input current
i_{DLV}	Output delivery current
i_L	Inductor current
C_F	Flying capacitor
I_{LOAD}	Load current
i_C	Capacitor current
T_{CK}	Clock cycle
P_{CD}	Conduction loss
Φ_1	Switching phase 1
Φ_2	Switching phase 2
Φ_3	Switching phase 3
M_{PROP}	Conversion ratio of the proposed method
I_L	Average value of inductor current
$I_{C,1}$	Capacitor current during Φ_1
C_{OUT}	Output capacitor
$P_{CD,PROP}$	Conduction loss of the proposed method
R_{ON}	On-resistance of each power switch
R_{DC}	DCR of the inductor
f_{CK}	Clock frequency
$i_{C,1}$	Capacitor current during Φ_1
τ	Time constant
$i_{L,3}$	Inductor current during Φ_3
$i_{C,1,pp}$	Peak-to-peak of $i_{C,1}$
$i_{C,1,pp,norm}$	Normalized capacitor current ripple
V_{ERR}	Error voltage
P_{SW}	Switching loss
V_{CB}	Voltage at the bottom node of the flying capacitor
V_{OS}	Offset voltage
M_1	Positive-input transistor of the comparator
M_{OS}	Offset injecting transistor
V_{CTRL}	Control voltage of M_{OS}
T_{SETTLE}	Settling time
$i_{L,rms}$	RMS inductor current
$I_{L,A}$	Inductor current of 0° stage
$I_{L,B}$	Inductor current of 180° stage

Abbreviations

The following abbreviations are used in this manuscript:

DPBB	Dual-phase hybrid buck-boost
DCR	DC resistance
DCM	Discontinuous conduction mode
ZCD	Zero-current detector
D	Duty cycle
PCE	Power conversion efficiency
EMI	Electromagnetic interference

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