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An Enhanced Dynamic Bias Comparator with a Reference-Compensated Offset Calibration Technique

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Abstract

An enhanced dynamic bias comparator with a reference-compensated offset calibration technique is implemented in a 180 nm CMOS process. In order to reduce the delay time of the comparator, an enhanced structure is used. To reduce the power consumption, a dynamic bias technique is applied to the comparator. A novel reference-compensated offset calibration technique is introduced to achieve offset calibration. Spectre simulation results indicate that the proposed comparator achieves a delay time of 190.3 ps and an energy consumption of 324.2 fJ/comparison under operating conditions of 150 MHz and an input differential amplitude of 0.1 V, compared to a delay time of 235.5 ps and an energy consumption of 636.6 fJ/comparison for the conventional comparator. Furthermore, the application of a reference-compensated offset calibration technique facilitates a reduction in the offset voltage of the comparator from 18.1 mV to 6.3 mV.

Keywords: comparator; dynamic bias; reference compensation; offset calibration; analog-to-digital converter

1. Introduction

The main function of comparators is to quantize the input signal by comparing it to a reference signal, which produces a digital output level [1]. They determine the precision, speed, area, and noise characteristics of the entire system [2,3]. As a result, the performance of comparators is crucial. Static and dynamic comparators are the two main types. Static comparators have very high power consumption since they are constantly operating. Their speed is also severely constrained in the absence of positive feedback [4]. Dynamic comparators overcome the issue of slow speed through clock-controlled positive feedback, and exhibit no static power consumption [5,6]. Conventional single-stage dynamic comparators require a high voltage margin because they directly stack the input transistor with a cross-coupled differential latch [7]. Single-stage dynamic comparators have advantages in static power consumption, but high-speed circuits cannot be satisfied by their sluggish speed. The two-stage dynamic comparator consists of two sections [8–10]: the first stage is a pre-amplifier, which amplifies the input signal to increase the sensitivity of the comparator while isolating kickback noise generated by the second stage. The dynamic latch in the second stage amplifies the difference between the output signals of the pre-amplifier and uses positive feedback to determine which input signal is greater. However, the low gain of the first-stage pre-amplifier restricts its capacity to efficiently amplify the input signal. This limitation also leads to inadequate noise suppression performance, which has a detrimental



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effect on the speed and accuracy of the comparator [11]. Therefore, developing a technique to enhance the speed of comparators is crucial.

Another important performance metric is comparator mismatch, which is typically characterized by offset voltage. Significant physical and electrical mismatches can still occur even with the most symmetrical arrangement and the minimal distances between transistors in the layout [12]. Static mismatch and dynamic mismatch are two types of mismatch. The performance of the comparator is reduced by both kinds of mismatch since they produce an arbitrary offset voltage [13,14].

Traditional auto-zeroing techniques for comparators are primarily classified into input offset storage (IOS) and output offset storage (OOS) [15]. In IOS, the offset is stored on input coupling capacitors, enabling superior residual offset suppression and accommodating high-gain pre-amplifiers [16,17]. However, its performance is constrained by closed-loop stability requirements, resulting in extended settling times and reduced calibration throughput. Conversely, OOS achieves higher operational speeds by storing the offset on output capacitors [18]; nonetheless, it is susceptible to output saturation when integrated with high-gain pre-amplifiers, which can introduce significant nonlinearity and limit the effective dynamic range.

The recent literature suggests that the fundamental approach to mitigating comparator mismatch involves introducing a controlled imbalance. For instance, ref. [19] implements capacitive load imbalance at intermediate nodes using six binary-weighted p-type MOSFET capacitors. Current-compensated calibration is demonstrated in [20], where an auxiliary current path is adjusted using a resistor ladder reference. Similarly, a 5-bit resistor digital-to-analog converter (RDAC) is utilized in [21] to generate a control voltage that regulates an auxiliary current path, thereby compensating for the comparator offset. Leveraging technology-specific features, ref. [22] utilizes the back-gate biasing of 28 nm FDSOI input transistors, controlled by an R-2R ladder, to achieve precise offset calibration. The method proposed in [23] compensates for the input-referred offset voltage by trimming the effective transconductance of the second-stage PMOS input pairs. Additionally, ref. [24] employs a combination of IOS/OOS and transconductance trimming to suppress offset levels. Beyond the hardware overhead of the digital circuitry, these techniques necessitate auxiliary analog circuits to facilitate the calibration process, which inevitably increases the design complexity, area, and power consumption of the analog system.

This paper proposes an enhanced structure to increase the speed of the comparator. A dynamic bias technique is applied to reduce power consumption. Moreover, a reference-compensated offset calibration is suggested to improve the mismatch performance of the comparator. The remainder of this paper is organized as follows. The structure of the proposed comparator is introduced in Section 2. The reference-compensated offset calibration technique is described in Section 3. The simulation results are shown in Section 4. Finally, a discussion is provided in Section 5.

2. Analysis and Design of Comparator

Despite their simplicity and low power dissipation, traditional single-stage comparators suffer from limited speed. This study investigates the delay characteristics of cross-coupled architectures, identifies the primary limiting factors through mathematical derivation, and introduces an improved design to overcome these constraints.

2.1. Analysis of Conventional Comparator

The circuit diagram and timing diagram of the conventional single-stage comparator are shown in Figure 1 [25]. The entire circuit consists of two parts: a dynamic comparator and a clock-gated latch. The comparator makes a decision based on the input signal and

generates an output using positive feedback. The clock-gated latch stores the output data and enhances the output drive capability.

When clock CK is high, the circuit is in the reset state. MP3 is off, and MN3 and MN4 are turned on; nodes X and Y are discharged to V_{SS} . In the clock-gated latch, v_{OP} and v_{ON} are reset to V_{SS} .

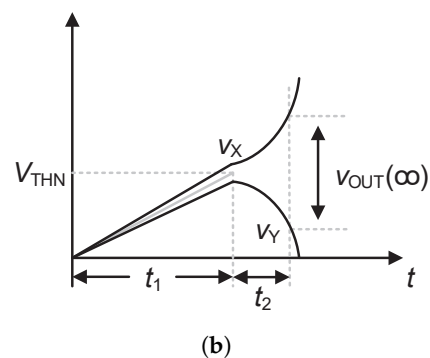
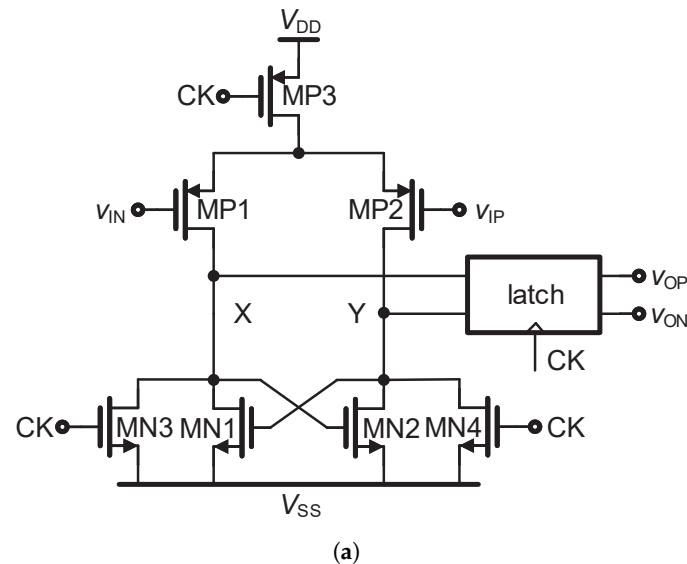


Figure 1. Conventional comparator: (a) circuit diagram; (b) timing diagram.

When clock CK goes low, the comparator begins to work. MP3 is turned on, and MN3 and MN4 are turned off. MN1 and MN2 charge the parasitic capacitances C_X and C_Y at nodes X and Y. The voltages at node X and Y begin to increase. The time taken for voltages v_X and v_Y to rise from V_{SS} to the threshold voltage V_{THN} is called the charge time t_1 , which can be expressed as

$$t_1 = \frac{V_{THN}C_P}{I_{CM}}, \quad (1)$$

where C_P equals the parasitic capacitances C_X and C_Y of nodes X and Y. I_{CM} is the common-mode current. From Formula (1), it can be seen that the charge time is related to the parasitic capacitance at its output node; the smaller the parasitic capacitance, the smaller the charge time. Additionally, the charge time is correlated with the common-mode current; the higher the common-mode current, the smaller the charge time. It is evident that a voltage difference between v_{IN} and v_{IP} results in amplified disparities in the charge currents of MP1 and MP2, leading to an enhancement in the voltage difference between v_X and v_Y , which can be written as

$$v_{XY0} = g_{mp}(v_{IP} - v_{IN})t_1 = \frac{V_{THN}}{I_{CM}}g_{mp}(v_{IP} - v_{IN}), \quad (2)$$

where g_{mp} equals the small-signal transconductance g_{mp1} and g_{mp2} of input transistors MP1 and MP2, respectively. The cross-coupled pairs MN1 and MN2 become active once the voltages at nodes X and Y reach the threshold voltage V_{THN} . The positive feedback around these transistors eventually brings one output back to V_{SS} while allowing the other to rise to V_{DD} .

Assuming that MN1 and MN2 are in the saturation region, an equivalent circuit diagram can be drawn as shown in Figure 2. The regeneration time t_2 can be calculated as

$$t_2 = \frac{C_p}{g_{mn}} \ln\left(\frac{v_{XY}(\infty)}{v_{XY0}}\right) = \frac{C_p}{g_{mn}} \ln\left(\frac{v_{XY}(\infty)I_{CM}}{V_{THN}g_{mp}v_I}\right), \quad (3)$$

where v_I is the differential input voltage, and equals $v_{IP} - v_{IN}$, and $v_{XY}(\infty)$ is the final output voltage.

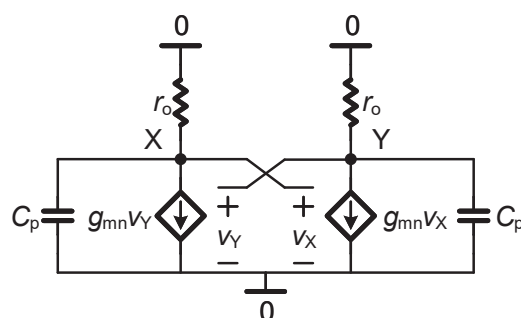


Figure 2. The equivalent circuit of the comparator.

Thus, the total delay of the comparator can be given as

$$t_d = t_1 + t_2 = \frac{V_{THN}C_p}{I_{CM}} + \frac{C_p}{g_{mn}} \ln\left(\frac{v_{XY}(\infty)I_{CM}}{V_{THN}g_{mp}v_I}\right), \quad (4)$$

As demonstrated in Formula (4), an increase in the common-mode current I_{CM} is associated with a decrease in the charging time t_1 and an increase in the regeneration time t_2 . This occurs because a higher common-mode current I_{CM} shortens the time needed for the parasitic capacitance to charge to a voltage close to the threshold voltage V_{THN} . However, an increase in the common-mode current also results in a decrease in the initial output voltage v_{OUT0} , which in turn leads to an increase in the regeneration time t_2 .

The transconductance g_m of the MOS can be expressed as

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{CM}}, \quad (5)$$

where μ denotes the electron mobility of the MOS, and C_{ox} represents the gate-oxide capacitance per unit area for the MOS. As can be seen from Formula (5), increasing the common-mode current I_{CM} can increase the transconductance g_m while maintaining the same MOS dimensions.

Substituting Formula (5) into Formula (4) yields

$$t_d = \frac{V_{THN}C_p}{I_{CM}} + \frac{C_p}{\sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{n1,2} I_{CM}}} \ln\left(\frac{v_{XY}(\infty)}{V_{THN}v_I} \sqrt{\frac{I_{CM}}{2\mu_p C_{ox} \left(\frac{W}{L}\right)_{p1,2}}}\right), \quad (6)$$

To analyze the factors influencing delay further, Formula (6) was processed using MATLAB, as shown in Figure 3. It is evident that when the common-mode current is increased from 50 μA to 400 μA , the delay decreases significantly. At low common-mode

current I_{CM} levels, the delay is primarily dominated by the charge time t_1 . With increasing common-mode current, the charging process is significantly accelerated, resulting in a rapid reduction in the charge time t_1 and thus a pronounced decrease in the overall delay. However, with further increase in the common-mode current, the reduction in delay time becomes progressively smaller. This is because, as the common-mode current I_{CM} increases, the charge time t_1 decreases at a much faster rate than the regeneration time t_2 , causing the regeneration time t_2 to gradually become the dominant component of the overall delay. With further increase in the common-mode current I_{CM} , the increase in the transconductance g_{mn} of the cross-coupled transistors MN1 and MN2 becomes less significant, leading to a reduced rate of decrease in the regeneration time t_2 . Consequently, the regeneration time t_2 approaches a constant value.

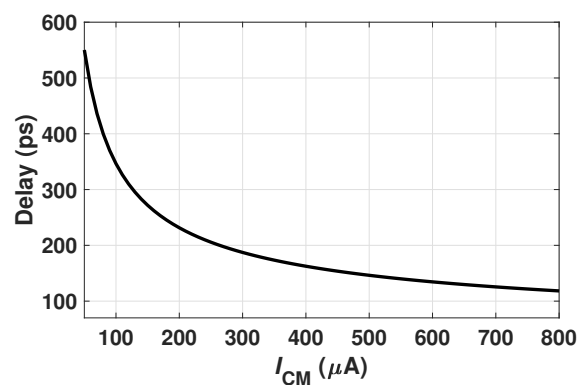


Figure 3. Delay across common-mode current range using MATLAB.

However, excessively large common-mode currents pose a significant challenge for circuit design. As shown in Figure 4, the common-mode current I_{CM} of a PMOS depends on the gate-source voltage V_{GS} , which is determined by both the common-mode voltage V_{CM} and the source voltage V_S . Specifically, the common-mode current increases as the common-mode voltage decreases, and conversely, it decreases as the common-mode increases. Assuming both input transistors MP1 and MP2 are in the saturation region, the common-mode current can be written as [26]

$$I_{CM} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_{p1,2} (V_{CM} - V_S - V_{THP})^2, \quad (7)$$

where μ_p denotes the electron mobility of MP1 and MP2, C_{ox} represents the gate-oxide capacitance per unit area for MP1 and MP2, V_{CM} and V_S are the input common-mode voltage and the source voltage of MP1 and MP2, respectively, and V_{THP} is the threshold voltage of MP1 and MP2. According to Formula (7), two challenges are apparent in circuit design. Firstly, excessive common-mode current requires larger input transistors. Oversized input transistors not only increase the layout area but also enlarge gate-drain parasitic capacitance, which increases the output load. Secondly, comparators must operate over a range of input common-mode voltages. Since the common-mode current is proportional to the square of the input common-mode voltage, any variation in the input common-mode voltages directly changes the common-mode current, thereby altering the delay time of the comparator. Excessively high or low common-mode voltages can cause malfunctions in comparators.

As demonstrated in the preceding analysis, it can be observed that the delay of the comparator depends on the common-mode current I_{CM} . It is clear that simply increasing the size of the input transistor is not the optimal approach, as parasitic capacitance increases with the size of the input transistor. This increased capacitance leads to an increase in the delay and power consumption of the comparator. Furthermore, the delay of the comparator

is sensitive to the common-mode voltage, and alternations in the common-mode voltage can result in substantial fluctuations in the delay.

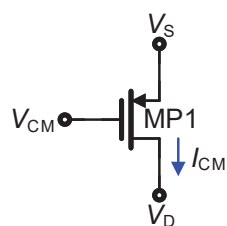


Figure 4. Common-mode current model for PMOS.

2.2. Proposed Enhanced Dynamic Bias Comparator

It has been demonstrated that increasing the common-mode current can enhance the speed of the comparator. However, a trade-off between the common-mode current and the size of the input transistor must be resolved. The proposed enhanced dynamic bias comparator is presented in Figure 5. To increase the common-mode current I_{CM} , additional transistors MP4 and MP5 are introduced; this provides the required common-mode current while maintaining a compact size. If the common-mode current contributed by the input transistor is negligible compared to that supplied by MP4 and MP5, then the dependence of the delay on the input common-mode voltage can also be minimized. To conserve power, a dynamic bias technique is employed [27], which turns off the bias of the comparator after the comparator has completed its comparison. The effect of dynamic bias on the delay time of the comparator is negligible, with the only overhead being the additional logic circuitry required. The circuit is composed of two sections: the comparator and the logic circuit. In the logic circuit section, the comparator output signals v_{OP} and v_{ON} pass through an XOR gate and an inverter, and then are combined with the clock CK via a NAND gate to generate the final control signal fnh . The main purpose of the control signal fnh is to dynamically enable or disable the comparator, thereby reducing power consumption.

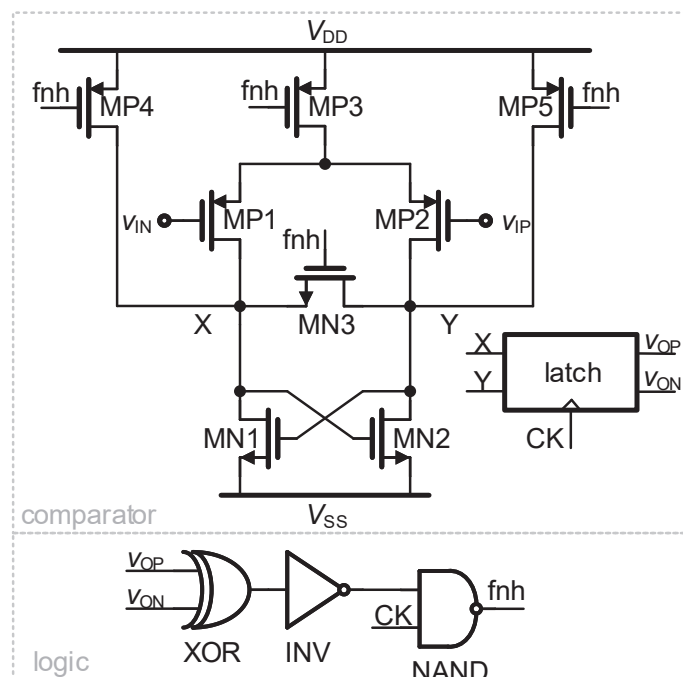


Figure 5. Proposed enhanced dynamic bias comparator circuit.

When the clock CK is low, the comparator is in the reset state. The control signal fnh is high, causing MP3, MP4, and MP5 to turn off, MN3 to turn on, and the comparator is

disabled. At the same time, MN3 connects nodes X and Y to equalize the voltages v_X and v_Y . And the output v_{OP} and v_{ON} are reset to zero in the latch.

When the clock CK transitions from low to high, the comparator begins operation. The control signal fnh transitions from high to low, causing MP3, MP4, and MP5 to turn on while MN3 turns off. The additional current provided by MP4 and MP5 charges nodes X and Y. Simultaneously, the common-mode current from MP1 and MP2 also charges nodes X and Y. During this process, the input signals v_{IP} and v_{IN} provide differential current to nodes X and Y through MP1 and MP2. This stage is referred to as the charging phase of the comparator.

The cross-coupled pair MN1 and MN2 become active once the voltages at nodes X and Y reach the threshold voltage V_{THN} . The positive feedback around these transistors eventually brings one output back to zero while allowing the other to rise to V_{DD} . Subsequently, the latch stores the outputs of the comparator and passes them to the subsequent stage.

Once the output is settled, the output voltages v_{OP} and v_{ON} are always at complementary levels (V_{DD} and V_{SS} , respectively). Consequently, the control signal fnh transitions from a low level to a high level, disabling the bias of the comparator and reducing its dynamic power consumption. When the clock CK goes low, the comparator and the latch re-enter the reset state. Voltages v_{OP} and v_{ON} are reset to zero, while voltages v_X and v_Y are reset to near the threshold voltage V_{THN} . As the clock CK is low, the control signal fnh remains high, waiting for the next enable cycle.

The proposed enhanced dynamic bias comparator offers two main advantages. First, the addition of auxiliary current paths accelerates the speed of the comparator. Second, dynamic bias of the comparator is achieved through the implementation of simple logic circuits. This reduces the power consumption of the comparator, thereby enhancing its overall energy efficiency.

3. Design of the Offset Calibration Technique

In pipelined analog-to-digital converters, although inter-stage digital redundancy provides some fault tolerance, comparator offset exceeding the error correction range of the substage circuit will cause the residual voltage to exceed the range of subsequent stages, leading to missing codes. It is evident that by actively reducing physical discrepancies caused by process variations, offset calibration technology effectively resolves the design trade-off between accuracy, speed, and power consumption. This ensures system robustness under high-precision requirements and significantly enhances overall energy efficiency and dynamic range.

In the following section, the working principle of the comparator will first be introduced, followed by a detailed description of the proposed calibration technique.

3.1. Working Principle of the Comparator

The circuit diagram and timing diagram of a comparator with offset for voltage comparison is shown in Figure 6. During the sampling phase, clock φ_1 is high, while clock φ_2 is low. The top plates of sampling capacitors C_{sp} and C_{sn} are connected to the common-mode voltage V_{CM} , while their bottom plates are connected to the input signals v_{IP} and v_{IN} , respectively. During the comparison phase, clock φ_1 goes low, while clock φ_2 goes high. The bottoms of sampling capacitors C_{sp} and C_{sn} are connected to the reference signals V_{RP} and V_{RN} , respectively. At time t_1 , the comparator begins operation.

The input differential voltage of the comparator can be expressed as

$$v_{I,cmp}(t_1) = v_I(t_0) - (V_{REF} - V_{OS}), \quad (8)$$

where $v_I(t_{0-})$ and V_{REF} can be written as

$$\begin{aligned} v_I(t_{0-}) &= v_{IP}(t_{0-}) - v_{IN}(t_{0-}), \\ V_{REF} &= V_{RP} - V_{RN}, \end{aligned} \quad (9)$$

From Formula (8), it is evident that the presence of the offset voltage V_{OS} results in a shift in the reference comparison point of the comparator by an amount equivalent to $-V_{OS}$. If the offset voltage of the comparator is large, it will have a detrimental effect on the performance of the analog-to-digital converter.

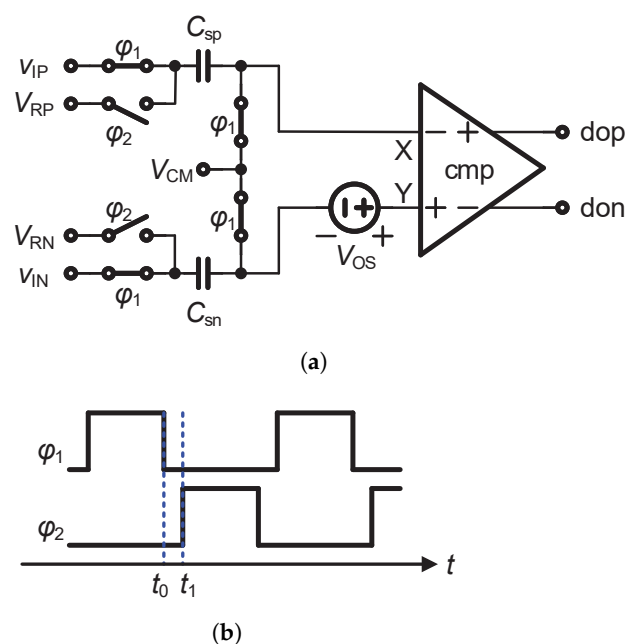


Figure 6. Operating principle of the comparator with offset: (a) circuit diagram; (b) timing diagram.

3.2. Proposed Reference-Compensated Offset Calibration Technique

The schematic diagram of the comparator with reference-compensated technique is presented in Figure 7. The alteration of the reference voltage at the comparison point serves as a method to compensate for the offset voltage of the comparator. When the reference voltage is changed, Formula (8) can be rewritten as

$$v_{I,cmp}(t_{1-}) = v_I(t_{0-}) - V_{REF} - (\Delta V - V_{OS}), \quad (10)$$

From Formula (10), it can be seen that when ΔV equals V_{OS} , the offset voltage of the comparator can be eliminated. The step size of ΔV is directly proportional to the precision of the calibration. Higher calibration accuracy corresponds to a smaller step size of ΔV , whereas lower accuracy requires a larger step size of ΔV .

The schematic diagram of the proposed calibration scheme is presented in Figure 8. The entire calibration circuit consists of four sections: the comparator under calibration, the voltage generation circuit, the counter, and the digital logic control circuit. At the start of calibration, the sampling capacitor is connected to the reference voltages V_{RP} and V_{RN} via clock ϕ_1 during the sampling phase, rather than to the input signals v_{IP} and v_{IN} . The sampling capacitor is connected to the reference voltage with a compensation offset αV_c via clock ϕ_2 during the comparison phase. The calibration voltage V_c represents the step size of ΔV and is directly proportional to the calibration accuracy. α is a multiple of $1/2$, and in this design, it takes nine values: -2 , $-3/2$, -1 , $-1/2$, 0 , $1/2$, 1 , $3/2$, and 2 . The digital control logic commands the voltage-generation circuit to adjust the compensation level of the reference

voltage. Simultaneously, the counter collects the output of the comparator to estimate the offset magnitude. Ultimately, the compensation of the reference voltage is adjusted to an appropriate level, reducing the offset voltage V_{OS} to a system-acceptable value.

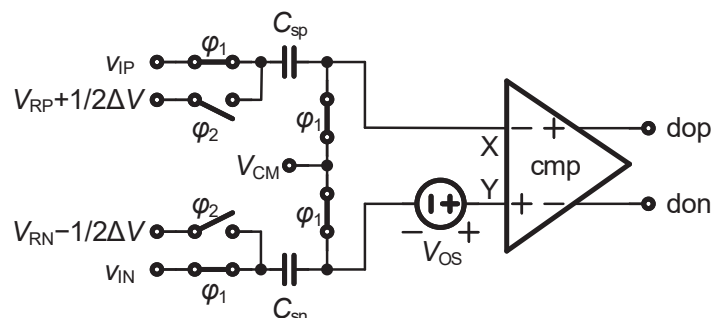


Figure 7. Operating principle of the comparator with reference-compensated technique.

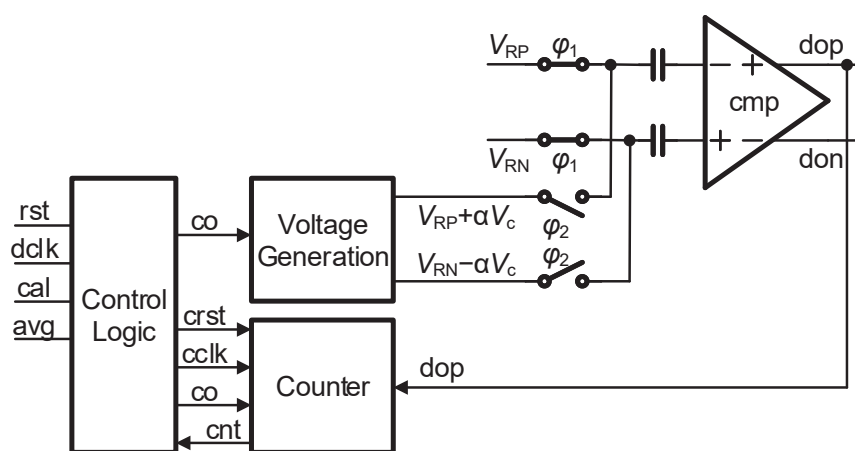


Figure 8. Schematic diagram of the reference-compensated offset calibration technique.

The control logic circuit is driven by the digital clock $dclk$. When the falling edge of the reset signal rst arrives, the offset calibration process of the comparator starts. If the calibration-enable signal cal is 1, the calibration circuit proceeds to the next stage; if it is 0, calibration ends. The control word co generated by the control logic is sent simultaneously to the voltage generation circuit and the counter. The default value of co is 1. The voltage generation circuit adjusts the coefficient α from -2 to 2 based on the control word co ranging from 1 to 9. The counter increment is based on the current output result. The counter increments only when the comparator output dop is 1. After completing avg comparisons and counts, the algorithm determines the compensation point that exhibits the minimum offset voltage. This compensation point is then designated as the reference comparison point for the normal operation of the comparator.

In conventional pipelined ADCs, the reference comparison point of the comparator is obtained from a resistive voltage divider. The voltage generation circuit can be realized by segmenting the original resistor string into smaller equal-valued resistors, thereby introducing additional reference-compensation points around the nominal comparison point. The main advantage of this approach is that it avoids extra analog circuitry, which reduces both the hardware overhead and the power consumption typically incurred by analog calibration circuits.

The reference-compensated offset calibration technique proposed in this paper achieves offset calibration for comparators without altering their structure. The analog circuit requires only a small number of additional voltage-division resistors, making this technique well suited for offset calibration of comparators in most pipelined ADCs.

4. Results

Both the proposed and conventional comparators were simulated by Spectre under TSMC 180 nm technology, as shown in Figure 9. The simulation conditions were as follows: a supply voltage of 1.8 V, a common-mode voltage of 0.9 V, an input differential voltage of 100 mV, an operating frequency of 150 MHz, and a comparator load of 5 fF. The Spectre transient simulation was performed with transient noise enabled. As shown in the results, the clock CK crossed 0.9 V at 128 ps. The output v_{op_prop} of the proposed comparator reached 1.62 V (approximately $0.9V_{DD}$) at 320 ps. In contrast, the output v_{op_conv} of the conventional comparator attained the same level after a further delay of 55 ps. Thus, the delay from the clock rising edge to the output is about 190 ps for the proposed comparator, whereas it is approximately 245 ps for the conventional design, resulting in a difference of around 55 ps.

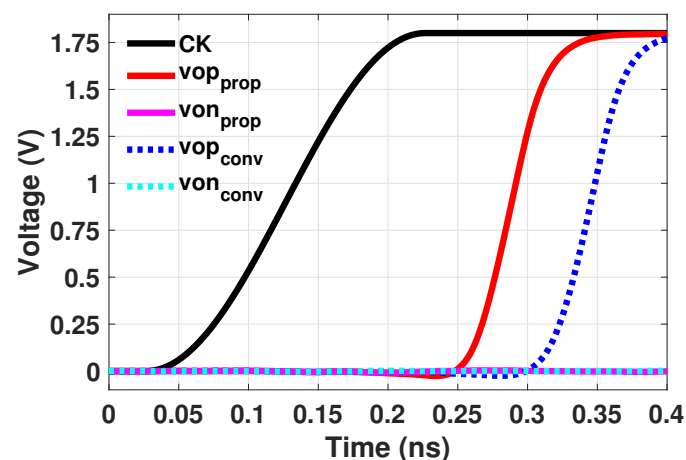


Figure 9. Transient simulation curves of the proposed and conventional comparators.

Under a 1.8 V supply voltage in the 180 nm process, the common-mode voltage is typically defined as half of the supply. Hence, it is set to 0.9 V. The detailed results of the delay time and the energy per comparison are presented in Appendix A Table A1. As shown in Figure 10a, the Spectre simulation results in the TSMC 180 nm process indicate the variation in the delay time with the differential input voltage at a fixed common-mode voltage of 0.9 V. At the differential input voltage of 0.1 mV, the proposed comparator has a delay of about 298 ps, while the conventional comparator has a delay of approximately 387 ps, which is roughly 89 ps longer. This indicates a significant advantage for the proposed comparator when processing very small input signals. Furthermore, the proposed comparator exhibits a delay time variation of approximately 115 ps over the entire differential input voltage range, compared to 172 ps for the conventional comparator, indicating that the conventional comparator has a 57 ps greater variation in delay time. These results demonstrate that the proposed comparator maintains excellent stability even under wide variations in the differential input voltage.

Figure 10b shows the Spectre simulation results when varying the energy consumption with the differential input voltage at a common-mode voltage of 0.9 V. At a differential input voltage of 0.1 mV, the energy consumption of the proposed comparator is 419 fJ/comparison, compared to 778 fJ/comparison for the conventional comparator. At 200 mV input, the corresponding values are 320 fJ/comparison and 536 fJ/comparison, respectively. These results indicated that the proposed comparator has a lower delay while consuming the same amount of energy. This is facilitated by the application of dynamic bias, which minimizes the dynamic power consumption of the proposed comparator.

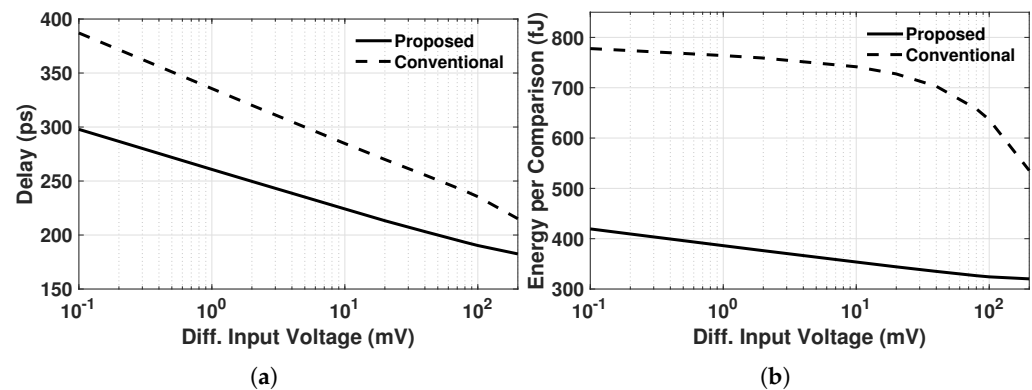


Figure 10. (a) Simulated delay time and (b) energy per comparison versus the differential input voltage at the common-mode voltage of 0.9 V.

The differential input voltage was swept from 0.1 mV to 200 mV in the Spectre simulation. The delay time at the mid-point value of 100 mV serves as a representative benchmark across this range. The detailed results of the delay time and the energy per comparison are presented in Appendix A Table A2. Figure 11a shows the Spectre simulation results when varying the delay time with changes in the common-mode voltage for the differential input voltage of 0.1 V. At a common-mode voltage of 0.7 V, the proposed comparator has a delay time of 185 ps. The delay increases gradually with the common-mode voltage, reaching 200 ps at 1.1 V. Over the entire common-mode voltage range, the delay variation of the proposed comparator is only about 15 ps. In contrast, the conventional comparator shows a delay of 186 ps at 0.7 V. Its delay increases rapidly as the common-mode voltage rises, reaching a maximum of 390 ps at 1.1 V. The overall delay variation of the conventional comparator across the same range is about 204 ps, approximately 13 times larger than that of the proposed one. These results indicate that the proposed comparator maintains excellent performance under common-mode voltage variations, whereas the traditional comparator is significantly affected by changes in the common-mode voltage.

Figure 11b shows the Spectre simulation results display when varying the energy consumption with the common-mode voltage at a differential input voltage of 0.1 V. At a common-mode voltage of 0.7 V, the energy consumption of the proposed comparator is 352 fJ/comparison, compared to 1116 fJ/comparison for the conventional one—a larger difference of 764 fJ/comparison. As the common-mode voltage increases, the energy consumption of both comparators decreases. At a common-mode voltage of 1.1 V, the energy consumption of the proposed comparator is 299 fJ/comparison, while the conventional comparator consumes 296 fJ/comparison, resulting in a much smaller difference of only 3 fJ/comparison. More importantly, over the entire common-mode voltage range, the proposed comparator exhibits a much smaller variation of 53 fJ/comparison in energy consumption, compared to 820 fJ/comparison for the conventional comparator. These results demonstrate that the proposed comparator maintains highly stable energy efficiency across common-mode voltage variations.

A Monte Carlo simulation was performed on the comparator with the common-mode voltage set to 0.9 V. The calibration step size was 15.6 mV, and the coefficients α took the following values: -2 , $-3/2$, -1 , $-1/2$, 0 , $1/2$, 1 , $3/2$, and 2 . Figure 12 presents the results of a 3600-sample Monte Carlo simulation under PVT (process, voltage, temperature) variations. The offset voltage of the comparator is reduced from 18.1 mV before calibration to 6.3 mV after calibration—an improvement of 11.8 mV. As shown in Figure 13, the Monte Carlo simulation with 400 samples under the TT process reveals that, before calibration, the offset voltage shows significant dispersion, with a maximum value of around 60 mV. However,

after calibration, the offset voltage is constrained between approximately ± 15.6 mV, which demonstrates that the calibration technique enhances the mismatch performance of the comparator. The offset statistics are listed in Table 1. The Monte Carlo simulation results indicate that the reference-compensated offset calibration technique plays a significant role in improving the offset of the comparator.

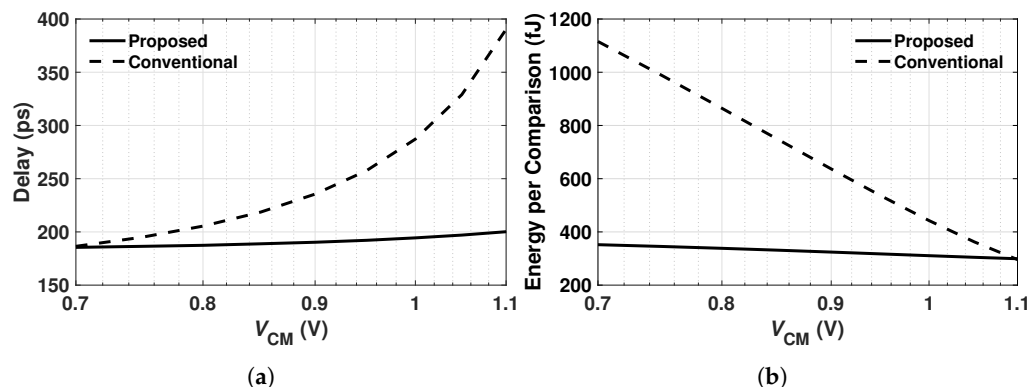


Figure 11. (a) Simulated delay time and (b) energy per comparison versus the common-mode voltage at the differential input voltage of 0.1 V.

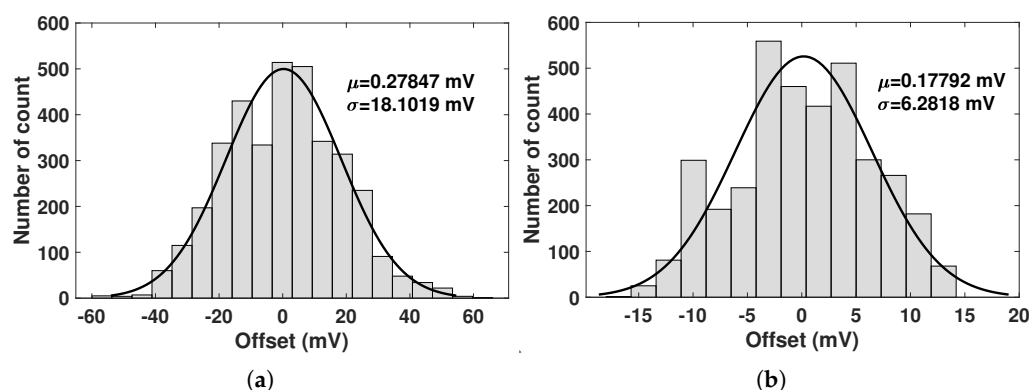


Figure 12. Histograms of the offset voltage: (a) before calibration; (b) after calibration.

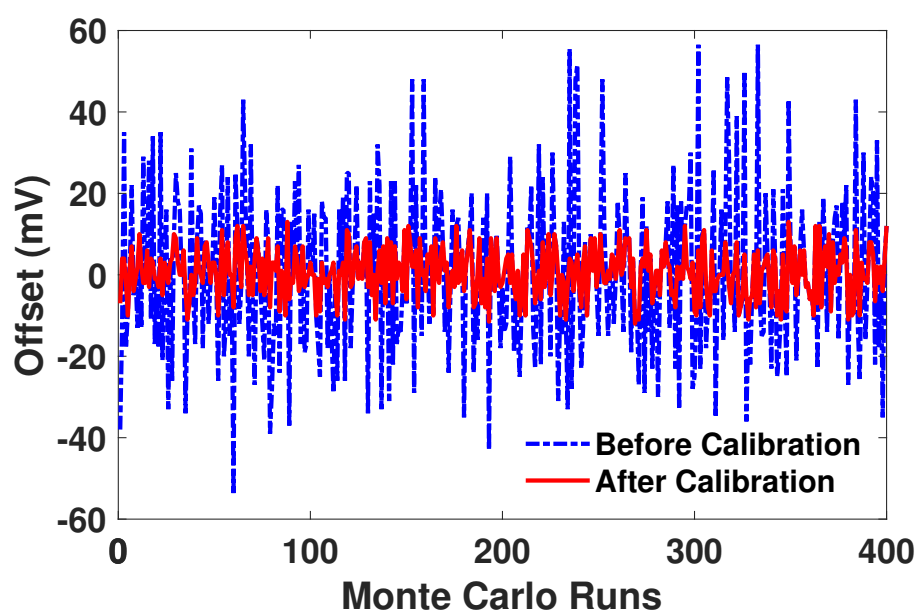


Figure 13. The 400-sample Monte Carlo simulation results under TT process.

Table 1. Offset statistics without and with calibration for 3600-sample Monte Carlo simulation.

	μ	σ	Min	Max
Without calibration (V)	0.28 m	18.1 m	−15.6 m	13 m
With calibration (V)	0.18 m	6.28 m	−56 m	65 m

As shown in Table 2, several methods have been proposed to reduce the delay time and power consumption of the comparator. Ref. [27] presents a dynamic bias technique that disables the bias of the comparator after the output is resolved. Ref. [28] utilizes positive feedback in the pre-amplifier to accelerate the comparison process. The latching stage in [29] uses separated gate-biasing cross-coupled transistors, which leads to a much faster comparison and lowers power consumption. A heuristic algorithm is proposed in [30] to jointly optimize the delay time and power consumption by sizing the transistors in a double-tail dynamic comparator. Fabricated using the same process technology, the proposed comparator achieves a significant speed advantage, with a delay time of 190.3 ps, compared to a minimum delay time of 268 ps in other works. Compared to other comparators, the proposed comparator shows advantages in terms of power consumption. However, there is still significant room for improvement in the power consumption. Thanks to the application of the offset calibration technique, the proposed comparator achieves an offset voltage of just 6.3 mV. This indicates that there is further potential for optimization in its algorithm and structure. However, the increased common-mode current in the proposed comparator leads to significantly higher input-referred noise compared to the conventional one. Consequently, further optimization of its noise performance is necessary.

Table 2. Comparison between the proposed comparator and other comparators.

	This Work	Conventional	[27]	[28]	[29]	[30]
Technology (nm)	180	180	180	180	180	180
Supply voltage (V)	1.8	1.8	1.2	1.2	1.8	1.8
Operating frequency (MHz)	150	150	2150	2000	500	1600
Delay time (ps)	190.3	235.5	550	268.6	300	761
Energy/comparison (fJ)	324.2	636.6	560	112.5	300	418
Offset voltage (mV)	6.3	–	7.8	7.3	2.4	3.67
Input-referred noise (mV)	4.85	1.74	0.4	–	–	–

5. Conclusions

This paper proposes an enhanced dynamic bias comparator and employs a novel reference-compensated offset calibration technique. First, the delay of the comparator is analyzed and validated through MATLAB simulation, revealing its dependence on the common-mode current. Based on this insight, an enhanced structure is introduced, which not only increases the speed of the comparator but also mitigates the impact of common-mode voltage variations on the delay. Then, a dynamic bias is applied to reduce the dynamic power consumption of the comparator. Furthermore, to address comparator mismatch, a reference compensation technique is proposed to improve mismatch performance without altering the structure of the comparator. Finally, circuit simulations are conducted in Spectre using TSMC 180 nm technology to verify the functionality of the comparator architecture and its offset calibration capability.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

Table A1. Delay and energy per comparison versus the differential input voltage.

	0.1 mV	100 mV	200 mV	Diff.
Delay _{prop} (ps)	297.8	190.3	182.5	115.3
Delay _{conv} (ps)	387.1	235.5	215.1	172
Energy/comparison _{prop} (fJ)	419.5	324.2	320.2	99.3
Energy/comparison _{conv} (fJ)	777.8	636.6	535.5	242.3

Table A2. Delay and energy per comparison versus the common-mode voltage.

	0.7 V	0.9 V	1.1 V	Diff.
Delay _{prop} (ps)	185.5	190.3	200.2	14.7
Delay _{conv} (ps)	186.5	235.5	390.4	203.9
Energy/comparison _{prop} (fJ)	352	324.2	299.2	52.8
Energy/comparison _{conv} (fJ)	1115.6	636.6	296	819.6

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