

Article

A Fast-Recovery Transimpedance Amplifier with Ambient Light Cancellation for Automotive LiDAR Systems

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Abstract

To address the challenges of ambient light interference and slow overload recovery in transimpedance amplifiers (TIAs) for automotive Light Detection and Ranging (LiDAR) systems, this paper proposes a high-performance TIA with integrated ambient light cancellation and fast recovery capabilities. The core design includes an adaptive ambient light cancellation (ALC) loop that eliminates background currents up to 3 mA without relying on AC coupling capacitors, achieving a low-frequency cutoff frequency of 321 kHz to ensure the signal-to-noise ratio (SNR) of weak target signals. A multi-stage clamping and current transfer mechanism is employed to realize rapid overload recovery: under 100 mA heavy overload conditions, the recovery time is controlled around 8.7 ns, and the pulse broadening is limited to 2.7 ns, avoiding measurement blind zones. Implemented in a 0.18- μm SiGe BiCMOS process, the proposed TIA occupies a compact area of 0.15 mm², with a transimpedance gain of 80 dB Ω (10 k Ω) and a -3 dB bandwidth of 421 MHz. The input-referred noise current spectral density is 4.7 pA/ $\sqrt{\text{Hz}}$, and the integrated equivalent input noise current from 1 Hz to 250 MHz is 73.6 nA_{rms}. Operating over a temperature range of -40 °C to 125 °C, the TIA meets the rigorous requirements of automotive-grade applications. Performance comparisons with commercial products and state-of-the-art designs demonstrate its competitive ambient light rejection and fast recovery capabilities, validating its potential for use in direct time-of-flight (dToF) LiDAR systems for autonomous driving.

Keywords: automotive LiDAR; transimpedance amplifier (TIA); ambient light cancellation; fast overload recovery; SiGe BiCMOS process



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1. Introduction

As autonomous driving technology advances to Level 4 (L4) and higher grades, the detection accuracy, anti-interference capability, and real-time response performance of vehicle-mounted LiDAR (as a core sensor for environmental perception) directly determine driving safety [1–3]. Direct Time of Flight technology has become the mainstream solution for vehicle-mounted LiDAR due to its long detection range and high resolution. The transimpedance amplifier (TIA), as the core unit of the analog front end, undertakes the key task of converting the nanoampere-level weak photocurrent output by the Avalanche Photodiode (APD) into processable voltage signals. Its performance directly restricts the detection distance, dynamic range, and signal fidelity of LiDAR [4–6].

Figure 1 shows the typical application scenario of the TIA chip in the LiDAR system. The weak current signal output by the photodetector after receiving reflected light completes current-to-voltage conversion and preliminary amplification via the TIA. The fully differential amplifier (FDA) further suppresses common-mode noise and adjusts signal levels to match the input range of the Analog-to-Digital Converter (ADC). The ADC converts continuous analog signals into discrete digital signals, capturing the time-domain characteristics of the reflected waveform, such as amplitude and edge shape, in full. Finally, the Digital Signal Processor (DSP) or Field Programmable Gate Array (FPGA) calculates the time of flight through algorithms, including time-domain correlation and frequency-domain transformation, and inversely derives target reflectivity and surface characteristics from waveform information simultaneously, realizing multi-target discrimination and anti-interference optimization.

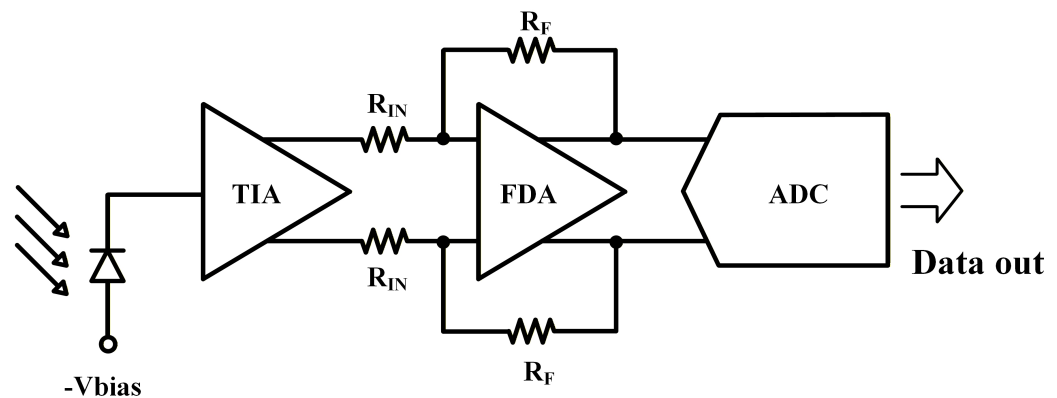


Figure 1. ADC-Based System Scheme.

As emphasized by Citroni et al. [7], ultra-low power techniques and energy harvesting are indispensable for modern sensor systems like LiDAR, where power efficiency and autonomous operation are critical to coping with complex on-vehicle environments. The complexity of vehicle-mounted scenarios poses dual stringent challenges to TIAs: On the one hand, LiDAR needs to operate stably under extreme illumination conditions, such as direct strong light and multi-light source superposition. Ambient light causes the APD to generate microampere to milliamper-level background current, which, when superimposed with weak signals reflected by targets, easily occupies the TIA's dynamic range, causes output baseline drift, and even drowns weak signals in noise, seriously affecting the detection of long-distance, low-reflectivity targets [8–10]. On the other hand, short-distance, high-reflectivity targets (e.g., preceding vehicles, road signs) produce strong reflected light, causing the TIA input current to far exceed its linear operating range and enter an overload state. A slow recovery speed will lead to “blind zones” in subsequent signal processing and damage the real-time measurement continuity of high-sampling-rate LiDAR, which is unacceptable for vehicle-mounted scenarios requiring rapid response to sudden obstacles [11–13].

Existing studies have explored solutions to the above problems: some TIAs adopt AC coupling to isolate the DC component of ambient light, but the additional coupling capacitor not only occupies extra board space but also degrades the overload recovery speed [14,15]. The ambient light suppression scheme based on a DC servo loop inherently fails to effectively eliminate excessive offset currents due to their voltage-based feedback limitation [16]. In terms of overload recovery for automotive LiDAR TIAs, academic studies are extremely limited—few works specifically address the critical requirement of balancing recovery speed and signal integrity in vehicle-mounted scenarios. Most existing academic efforts lack dedicated overload recovery mechanisms, often resulting in excessive pulse

broadening after overload and leading to measurement blind zones [8–10]. Although existing schemes have made progress in indicators such as gain and bandwidth, TIA designs that can simultaneously achieve efficient ambient light elimination and nanosecond-level fast recovery remain scarce, failing to fully meet the rigorous scenario requirements of vehicle-mounted LiDAR [17,18].

To address the above bottlenecks, this paper proposes a high-performance transimpedance amplifier for vehicle-mounted LiDAR systems, with core innovations focusing on two key characteristics: ambient light elimination and fast recovery. By integrating an adaptive ambient light cancellation loop, it can accurately offset background currents within 3 mA without AC coupling capacitors, with a low-frequency cutoff frequency of 321 kHz, ensuring the signal-to-noise ratio for weak signal detection. A multi-stage clamping and current transfer mechanism is designed, controlling the TIA's recovery time around 8.7 ns under 100 mA heavy overload conditions, with pulse broadening not exceeding 2.7 ns. The proposed TIA is implemented based on a 0.18- μm BiCMOS process, with a circuit area of only 0.15 mm², a transimpedance gain of 80 dB Ω , and a -3 dB bandwidth of 421 MHz, fully meeting the requirements of automotive-grade applications.

The architecture of the paper is organized as follows: Section 1 is the introduction, explaining the application requirements of TIAs for automotive LiDAR systems, bottlenecks of existing solutions, and core objectives of this study. Section 2 presents the core circuit structure of the proposed TIA, including theoretical analysis of gain, bandwidth, stability, and noise characteristics. Section 3 describes the design principle and key parameters of the fast recovery circuit. Section 4 illustrates the implementation scheme of the adaptive ALC loop and its frequency characteristics. Section 5 shows post-layout simulation results and performance comparison with mainstream designs. Section 6 summarizes the core achievements, application value, and future research directions.

2. Core Structure of the Transimpedance Amplifier

Figure 2 illustrates the main architecture of the TIA proposed in this design. The key performance metrics of the circuit, including working principle, gain, bandwidth, stability, and noise, are elaborated as follows:

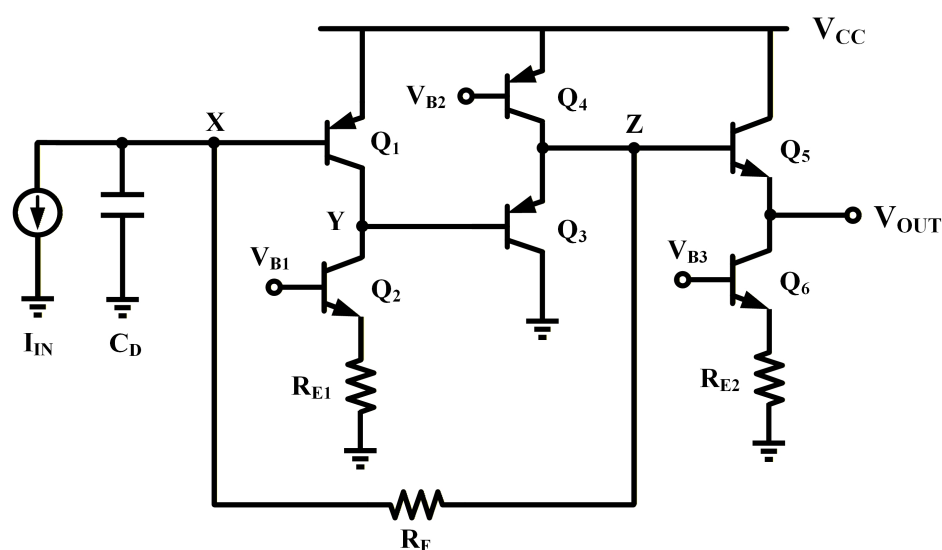


Figure 2. Core circuit structure of the proposed TIA.

In Figure 2, the resistor R_F acts as the feedback resistor of the TIA. The internal amplifier of the TIA consists of a common emitter gain stage formed by a bipolar junction transistor (BJT) Q_1 and an emitter follower stage formed by Q_3 . The common emitter stage

provides the overall gain of the amplifier, and the load of the amplifying Q_1 adopts a current source load composed of Q_2 and emitter degeneration resistor R_{E1} . The emitter follower stage isolates the load effect caused by R_F and the input capacitance of the subsequent stage. The output of the TIA in this design needs to drive the ALC loop and the subsequent fully differential amplifier (FDA) circuit. To mitigate stability issues and enhance load driving capability, a third stage emitter follower Q_5 is introduced as the output stage of the TIA.

2.1. Gain

Under the effect of the feedback component R_F , the operational amplifier operates in deep negative feedback. The voltage at node X is almost virtually shorted to AC ground in the AC domain, meaning that the variation in the input signal ΔI_{IN} generates an output voltage variation $\Delta V_Z = R_F \cdot \Delta I_{IN}$ at node Z. The transimpedance gain of the feedback TIA is approximately equal to the value of the feedback resistor R_F .

2.2. Bandwidth

In the above design, Q_1 utilizes a large device size and achieves high voltage gain from node X to node Y. The node impedance at node Y is the parallel combination of the output impedance of Q_1 , the output impedance of Q_2 with the source degeneration resistor, and the input impedance of the follower Q_3 . Thus, the gain A_{XY} from node X to node Y is nearly equal to the intrinsic gain of Q_1 , which is also the gain of the internal operational amplifier of the TIA:

$$A_{XY} \approx g_{m1} r_{o1} \quad (1)$$

Benefiting from the sufficiently high intrinsic gain of the BJT, the Miller multiplied capacitance of the parasitic capacitance C_{XY} at nodes X and Y (mainly composed of the collector junction capacitance C_{μ} of Q_1 and the junction capacitance of the Schottky diode described in the next section) becomes the dominant pole capacitance. The bandwidth f_{-3dB} of the TIA is given by

$$f_{-3dB} \approx \frac{1}{2\pi} \cdot \frac{1}{(A_{XY} C_{XY} + C_D) \frac{R_F}{A_{XY}}} \quad (2)$$

$$f_{-3dB} \approx 1 / (2\pi \cdot R_F \cdot C_{XY}) \quad (3)$$

Due to the extremely high intrinsic gain of the BJT, a relatively large equivalent capacitance exists at the input terminal. To achieve a better overload response (described in the next subsection), this design does not suppress the Miller effect, which has a significant impact on bandwidth performance. On the other hand, the bandwidth of this design is relatively independent of the parasitic capacitance of most APD products, endowing the circuit with additional characteristics.

2.3. Stability

Referring to the classical second-order system model in control theory, to ensure ideal response speed and stability of the feedback system, the secondary pole ω_{p2} formed at circuit node Y is required to be sufficiently far from the dominant pole ω_{p1} of the loop. The secondary pole ω_{p2} can be expressed as

$$\omega_{p2} \approx \frac{1}{r_{o1} \cdot C_Y} \quad (4)$$

The impedance at node Y is almost equal to the output impedance of Q_1 , and C_Y represents the parasitic capacitance of the node. Since the output impedance of the BJT is

inversely proportional to the bias current, ideal stability at the rated bandwidth requires a sufficiently large bias current.

2.4. Noise

The equivalent input noise current $\overline{I_{n,in}^2}$ of the TIA can be derived by first converting the open-circuit output noise voltage of the operational amplifier into the amplifier's equivalent input noise voltage $\overline{V_{n,A}^2}$ and equivalent input noise current $\overline{I_{n,A}^2}$ via the amplifier's voltage gain and transimpedance gain, respectively. Finally, the total equivalent input noise current $\overline{I_{n,in}^2}$ of the TIA is obtained by scaling through the TIA's transimpedance gain, i.e., R_F .

Noise is a metric that follows the barrel effect; components contributing a small proportion to the total noise should not be the focus of practical design. It is observed that the output noise of the emitter follower formed by Q_3 and Q_4 is referred to the input through the gain of the common-emitter stage, resulting in negligible noise contribution from these two transistors.

Given the signal characteristics of the TIA, the input signal current operates in the current sink mode: the current signal generated by optical illumination on the APD is either present or absent, with no negative current component. Thus, the downward swing at node Y is nearly useless. For this reason, the design employs the largest feasible degeneration resistor R_{E1} to mitigate the impact of Q_2 on noise performance. As a result, only Q_1 and the feedback resistor R_F serve as the primary noise sources.

Figure 3 presents the noise model of the BJT, where $\overline{I_b^2} = 2qI_b$ denotes the shot noise of the emitter junction, $\overline{V_b^2} = 4kTrb$ represents the thermal noise of the base series resistance, and $\overline{I_c^2} = 2qI_c$ indicates the shot noise of the collector junction. By referring $\overline{I_c^2}$ to the input port using the transconductance g_m and current gain β of Q_1 , we obtain the total equivalent input noise voltage and equivalent input noise current of the operational amplifier (i.e., Q_1):

$$\overline{V_{n,A}^2} = 4kTrb + \frac{2qI_c}{g_{m1}^2} \quad (5)$$

$$\overline{I_{n,A}^2} = 2qI_b + \frac{2qI_c}{\beta_1^2} \quad (6)$$

The total input noise current of the TIA is given by

$$\overline{I_{n,in}^2} = \frac{4kT}{R_F} + \frac{4kTrb + \frac{2qI_c}{g_{m1}^2}}{R_F^2} + 2qI_b + \frac{2qI_c}{\beta^2} \quad (7)$$

This reveals a trade-off between noise and stability. Ideal noise performance requires minimizing the shot noise of the emitter junction, which demands a sufficiently small bias current of Q_1 .

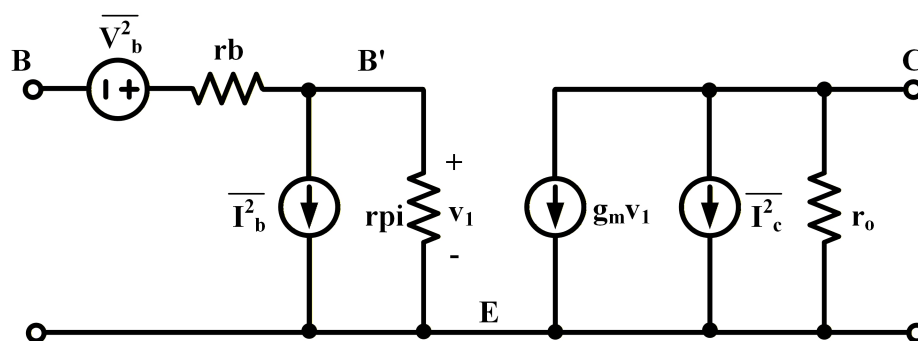


Figure 3. The noise model of the BJT.

3. Fast Recovery Circuit Design

The proposed recovery circuit is implemented by embedding protection devices, including Schottky diode D_1 , Q_7 , and Q_8 , and protection resistor R_P into the core TIA circuit. The TIA circuit with the added protection scheme is illustrated in Figure 4.

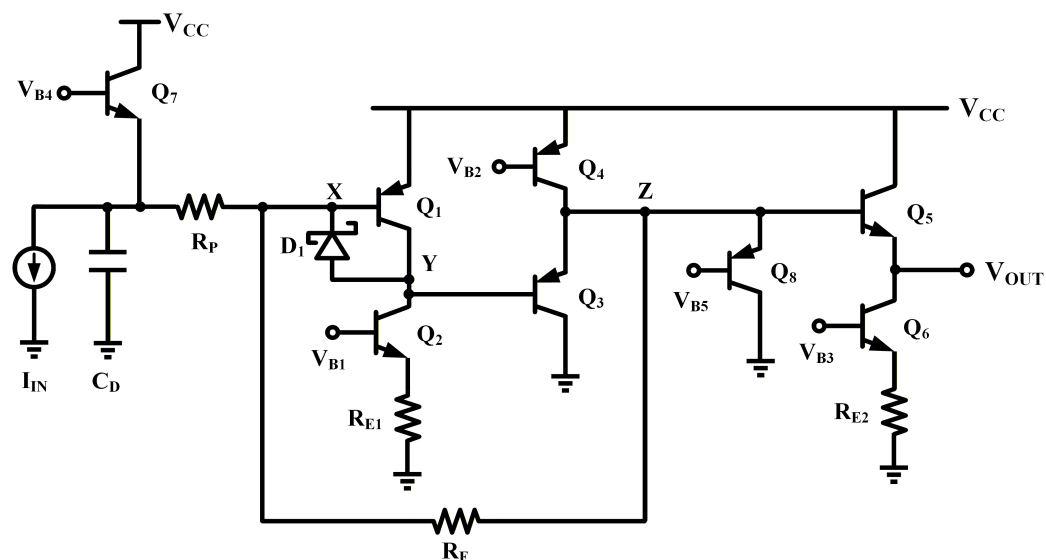


Figure 4. Schematic diagram of the TIA core circuit with added fast recovery circuit.

The working principle of the proposed protection circuit is as follows: When the input current slightly exceeds the linear input range of the circuit under the condition of mild overload, the overload signal makes the potential of node Z rise to a value where $V_Z - V_{B5}$ is higher than the emitter junction forward voltage V_{EB8} of transistor Q_8 . Then, Q_8 is turned on, which clamps the potential V_Z of node Z near $V_{B5} + V_{EB8}$. In this case, the circuit will not output an excessive voltage signal to cause the overload of the subsequent circuit.

A further increase in the potential of node Y causes the emitter follower Q_3 to turn off. Eventually, the deep negative feedback of the amplifier induced by the feedback resistor R_F disappears, and the characteristics of virtual short and virtual open at node X are lost. The circuit is converted into an open-loop common-emitter amplifier consisting of Q_1 . During this process, most of the overload current is supplied by the emitter junction of Q_1 . When the overload signal disappears, the quiescent operating points of node Y and node Z are recovered by Q_1 and Q_4 , which do not enter the saturation region.

Refer to Equation (8). When the input current $I_{OVERLOAD1}$ exceeds the linear input range of the TIA, the potential of node Y rises, and the potential of node X decreases, which makes the Schottky diode D_1 start to conduct. At this time, the overload current is provided by the collector junction of Q_1 .

$$V_{ZQ} + I_{OVERLOAD1} \cdot R_F = V_{B5} + V_{EB8} \quad (8)$$

$$V_{CC} - V_{EB1} - I_{OVERLOAD2} \cdot R_P = V_{B4} - V_{BE7} \quad (9)$$

Refer to Equation (9). When the input current $I_{OVERLOAD2}$ falls into the range of 10 mA to 100 mA, the voltage drop formed by the overload current across the protection resistor R_P causes the emitter potential of Q_7 to decrease. Q_7 enters the active region and starts to divert more input current to the positive power supply. When the overload signal disappears, the quiescent operating points of node Y and node Z are also recovered by Q_1 and Q_4 , which do not enter the saturation region.

Key considerations for the above design: (1) The resistance value of the protection resistor R_P and the junction capacitance of the Schottky diode D_1 will degrade the circuit bandwidth to a certain extent. R_P also contributes additional noise to the circuit. However, an excessively small R_P requires Q_1 with sufficient current capability to provide the required current for turning on Q_7 , which may exceed the maximum sustainable current of Q_1 . (2) The device area of Q_7 should be sufficiently large to provide a current output capability of 100 mA. Accordingly, V_{B4} must be able to supply a maximum current of 1 mA to ensure the normal operation of Q_7 , with a certain response speed to guarantee the fast recovery performance of the circuit. (3) The quiescent operating point V_{ZQ} of node Z is almost affected by the process, voltage, and temperature (PVT) variations of all devices. The expression of V_{ZQ} is given by Equation (10). It can be observed that the emitter junction voltage drop of Q_1 , the current gain β of Q_1 , and the resistance value of R_F all vary with temperature. The process corner deviation of Q_1 alters the β value of Q_1 , thereby affecting the magnitude of the base current I_{B1} . The resistance value of R_F itself has a tolerance of $\pm 20\%$ under different process corners, and the supply voltage directly impacts the value of V_{ZQ} .

$$V_{ZQ} = V_{CC} - V_{EB1} - I_{B1}R_F \quad (10)$$

The output swing of the TIA is determined by the magnitude of $V_{B5} + V_{EB8} - V_{ZQ}$. To prevent the clamping effect of transistor Q_5 from making the TIA output swing too small under certain PVT conditions and losing the clamping function under other PVT conditions, which would cause overload of the subsequent circuit, the bias voltage V_{B5} requires a unique design to track PVT variations. Figure 5 illustrates the generation scheme of bias voltages V_{B4} and V_{B5} .

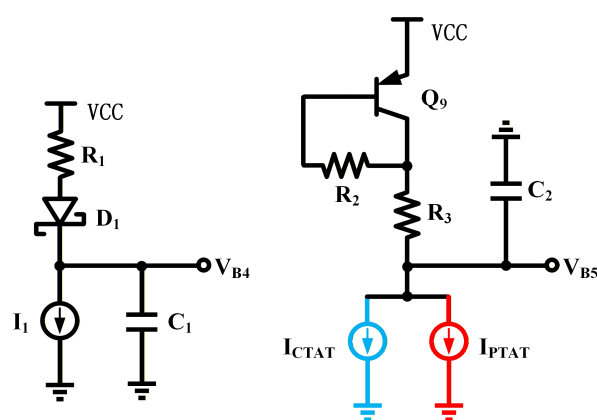


Figure 5. Generation method of bias voltages V_{B4} and V_{B5} .

In the figure above, V_{B4} is generated by the voltage drop of current I_1 across resistor R_1 and diode D_1 . Capacitor C_1 is set to 30 pF to ensure the stability of node V_{B4} under a transient overload of 100 mA. The expression of V_{B5} is given by Equation (11).

$$V_{B5} \approx V_{CC} - V_{EB9} - I_{B9}R_2 - (I_{PTAT} + I_{CTAT})R_3 \quad (11)$$

From the above equation, it can be concluded that by using the same devices as those in the amplifier circuit and adjusting the magnitudes of the positive and negative temperature coefficient currents as well as the resistance values of R_2 and R_3 , approximately consistent swing characteristics can be obtained under different PVT conditions.

4. Ambient Light Cancellation Circuit Design

Figure 6 illustrates the implementation principle of the ambient light cancellation function. The circuit employs an error amplifier to compare the output of the transimpedance amplifier (TIA) with the reference voltage V_{REF} , and the resulting output voltage drives the PMOS transistor M_1 to generate a reverse compensation current I_{COMP} for offsetting the quiescent current I_{DC} . Specifically, the ambient light cancellation loop incorporates an integrator low-pass filter R_1C_1 to achieve low-pass characteristics, which enables the separation of the slowly varying quiescent current I_{DC} from the fast echo signal current I_{SIG} . The reference voltage V_{REF} is derived from a dummy-TIA (the same as Figure 4), which replicates the topology of another TIA circuit but operates without input signals. Excellent process voltage temperature (PVT) characteristics of V_{REF} can be achieved through layout matching.

Figure 7 presents the detailed implementation of the error amplifier. A simple folded cascode architecture is adopted. To match the input voltage range of transistor M_1 , a single-stage emitter follower composed of Q_9 is introduced to shift the quiescent operating point upward by an emitter-base voltage drop V_{EB9} .

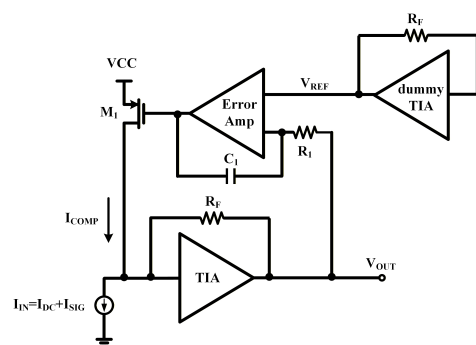


Figure 6. Principle of ambient light cancellation circuit.

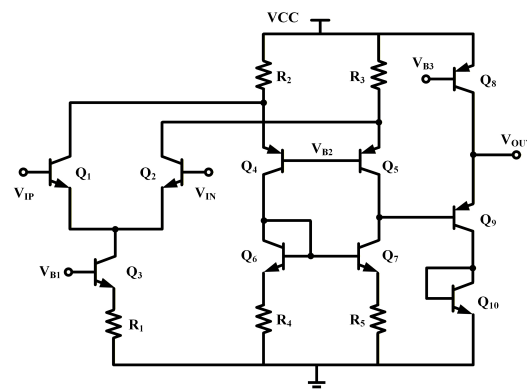


Figure 7. Circuit structure of the error amplifier.

The gain of the amplifier in Figure 7 is given by

$$A \approx g_{m1}[(R_3 \parallel r_{be5})g_{m5}r_{o5} \parallel (R_5 \parallel r_{be7})g_{m7}r_{o7}] \quad (12)$$

We can calculate the low-frequency cutoff of the loop using feedback theory. Assuming the transfer function of the transimpedance amplifier is given by the following equation, where ω_1 denotes the dominant pole (i.e., the -3 dB bandwidth) of the TIA stage,

$$R_T = \frac{V_{OUT}}{I_{IN}} = R_F \frac{1}{1 + \frac{s}{\omega_0}} \quad (13)$$

The transfer function of the feedback network formed by the error amplifier is given in (14), where ω_2 is the pole formed by R_1 , C_1 , and the Miller effect, with $\omega_2 = \frac{1}{R_1 \times C_1 \times A}$:

$$g_{m_{FB}} = \frac{I_{COMP}}{V_{OUT}} = A \times g_{m1} \frac{1}{1 + \frac{s}{\omega_2}} \quad (14)$$

$$\frac{V_{OUT}}{I_{IN}} = \frac{R_T}{1 + g_{m_{FB}} \times R_T} \cdot \frac{\left(1 + \frac{s}{\omega_2}\right) R_F}{\left(1 + \frac{s}{\omega_1}\right) \left(1 + \frac{s}{\omega_2}\right) + R_F \times A \times g_{m1}} \quad (15)$$

Solving for the dominant pole p_1 from the denominator of the above equation gives the low-frequency cutoff of the ALC loop:

$$p_1 = \frac{R_F \times A \times g_{m1} \times \omega_2}{2\pi} \quad (16)$$

In Equation (16), it can be seen that to achieve a sufficiently low low-frequency cutoff for the ALC loop, a larger time constant formed by R_1 and C_1 is required.

5. Post-Layout Simulation Results

This design is implemented based on a 180 nm SiGe process. Figure 8 presents the layout of the proposed design. Figures 9 and 10 illustrate the transient simulation waveform and AC simulation waveform of the core TIA circuit respectively, under the conditions of 3.3-V supply voltage, typical typical (TT) process corner, and different temperatures. A pulse excitation with an amplitude of 50 μ A is applied in the transient simulation to mimic the actual signal. The results demonstrate that the proposed design achieves a transimpedance gain of nearly 10 k Ω and a bandwidth of 421 MHz.

Figure 11 presents the noise performance simulation results under the conditions of 3.3-V supply voltage, typical typical (TT) process corner, and different temperatures of the proposed design. The simulation results show that the equivalent input noise current integrated from 1 Hz to 250 MHz is 73.6 nA_{rms}. The equivalent input noise current spectral density scaled by the 10 k Ω transimpedance gain and bandwidth is 4.65 pA/ $\sqrt{\text{Hz}}$.

Figure 12 illustrates the output of the transimpedance amplifier under the overload current with an amplitude of 100 mA and a half pulse width of 6 ns under different PVT conditions. The three PVT configurations are as follows: (i) Supply voltage is 3.15-V; temperature is 125 °C; and the process corners of resistors, capacitors, NPN transistors and PNP transistors are set as slow. (ii) Supply voltage is 3.3-V; temperature is 25 °C; and the process corners of resistors, capacitors, NPN transistors, and PNP transistors are set as typical. (iii) Supply voltage is 3.45-V; temperature is −40 °C; and the process corners of resistors, capacitors, NPN transistors, and PNP transistors are set as fast. Under the typical process corner condition, the pulse broadening induced by severe overload is controlled to 2.6 ns, and the recovery time for the output to recover to 1% of the quiescent value after the overload disappears is 8.7 ns.

Figure 13 shows the AC simulation waveform of the TIA output with the ALC loop under a DC bias current (I_{DC}) of 100 μ A under the conditions of 3.3-V supply voltage, typical typical (TT) process corner, and different temperatures. The simulation results demonstrate that the low-frequency cut-off frequency of the ALC loop is approximately 321 kHz. Meanwhile, the maximum quiescent current that can be eliminated by the ALC loop is mainly determined by the device size of transistor M_1 in Figure 6, which can be flexibly configured according to practical application scenarios.

Figures 14–17 illustrate the Monte Carlo simulations of the gain, bandwidth, overload recovery time, and low-frequency cutoff frequency under mismatch and process variations, respectively.

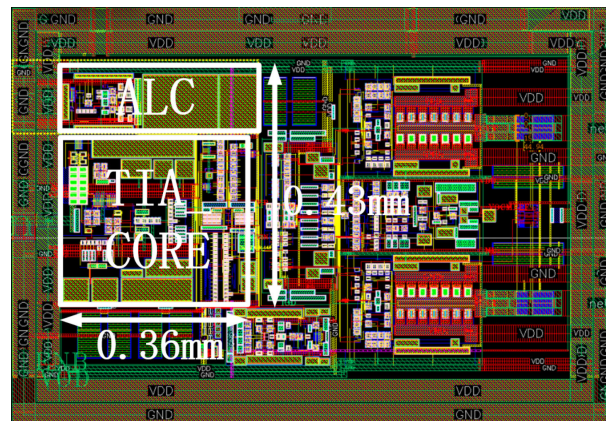


Figure 8. Layout of the proposed TIA.

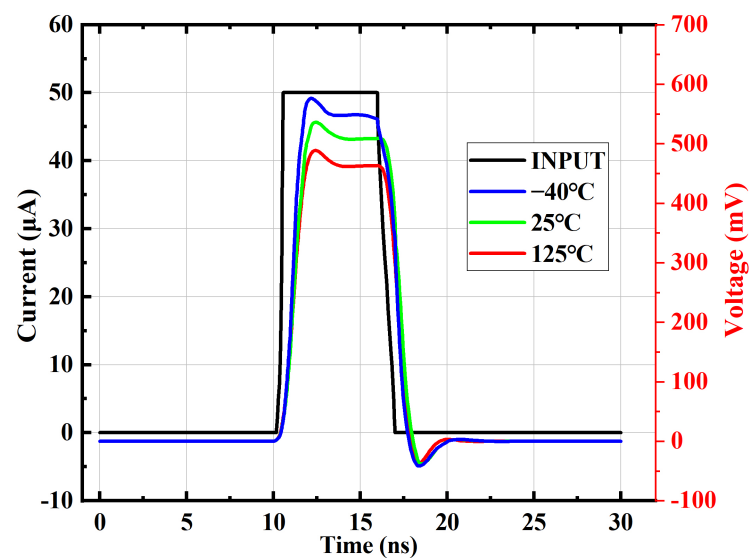


Figure 9. Transient response of the TIA core circuit across varying temperatures.

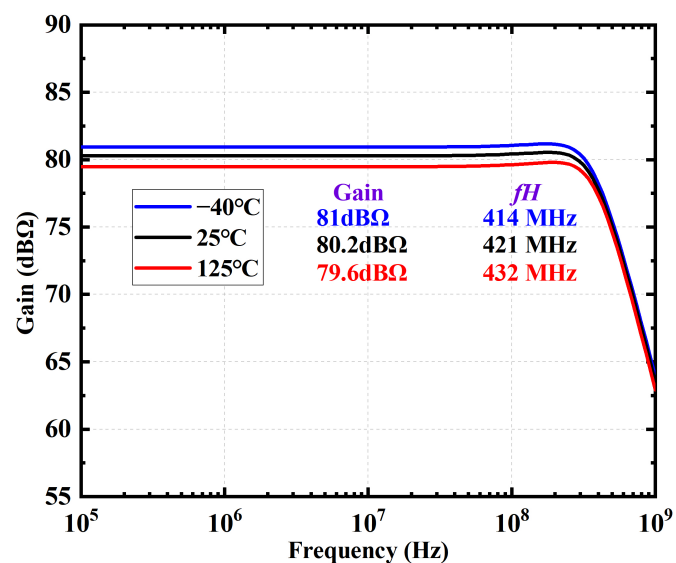


Figure 10. Simulated AC response of the TIA core circuit across varying temperatures.

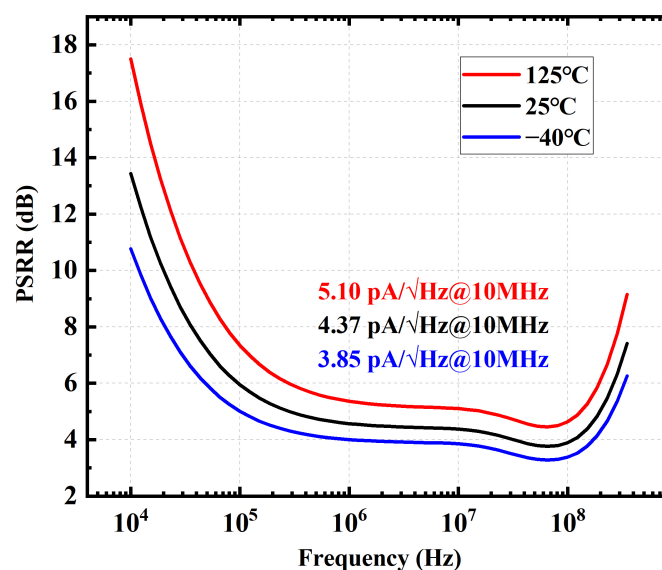


Figure 11. Input-referred noise current power spectral density of the TIA under varying temperature conditions.

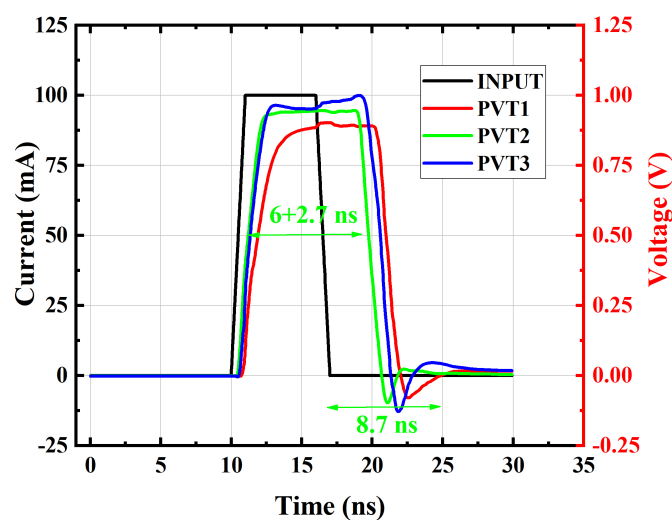


Figure 12. Output of the transimpedance amplifier under a 100 mA overload current under different PVT conditions.

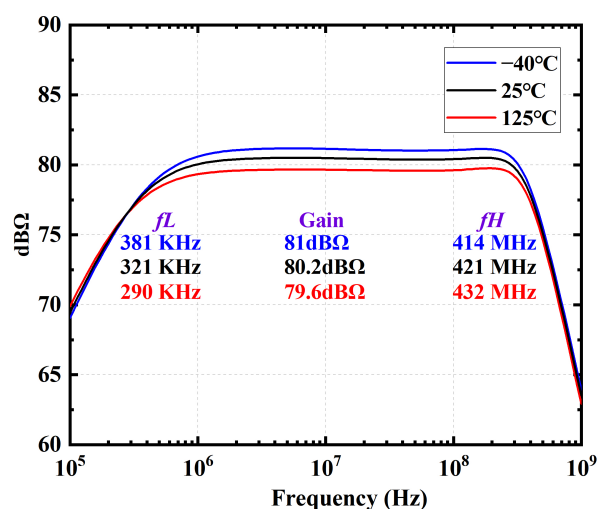


Figure 13. Simulated AC response curves of the TIA output with the ALC loop enabled under varying temperature conditions.

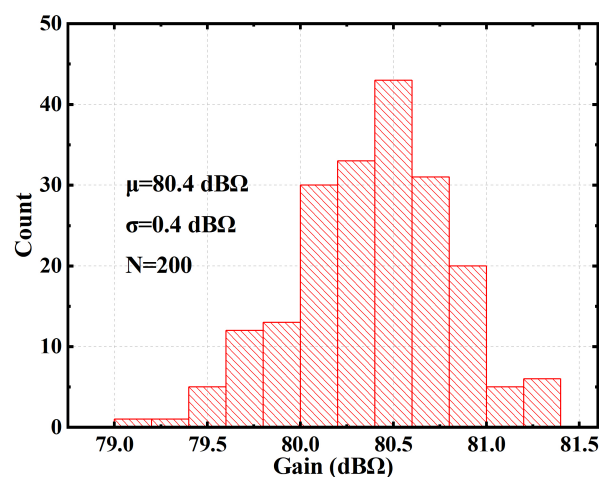


Figure 14. Histogram of gain from Monte Carlo simulations, accounting for process variations and device mismatch.

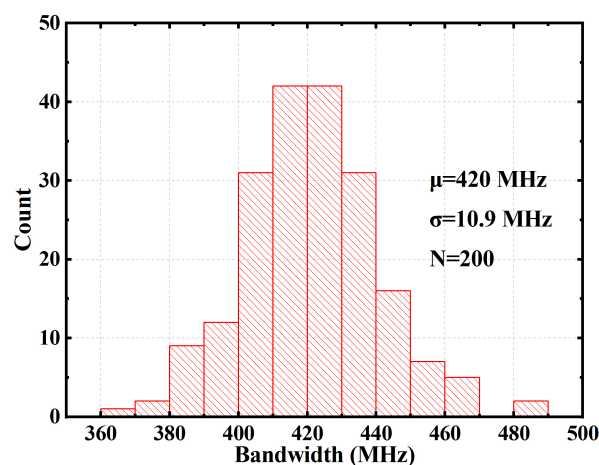


Figure 15. Histogram of bandwidth from Monte Carlo simulations, accounting for process variations and device mismatch.

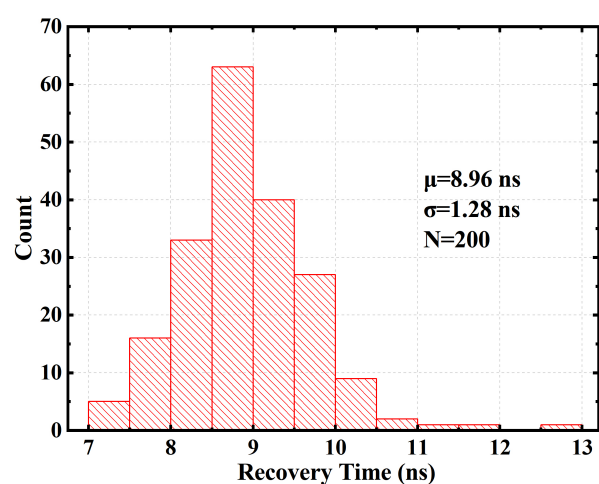


Figure 16. Histogram of recovery time from Monte Carlo simulations, accounting for process variations and device mismatch.

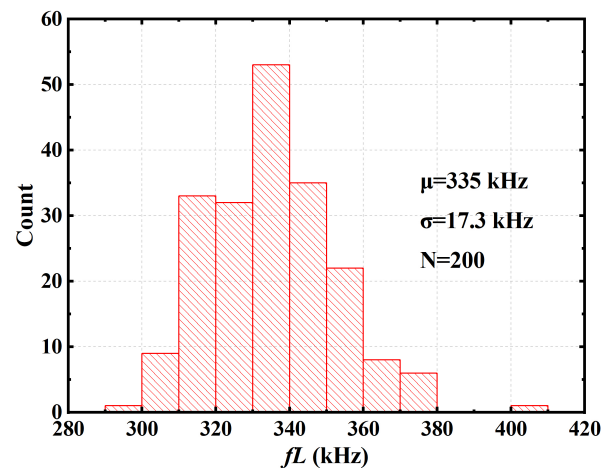


Figure 17. Histogram of low-frequency cutoff frequency f_L from Monte Carlo simulations, accounting for process variations and device mismatch.

Table 1 summarizes the performance metrics of this study and compares them with previous research. The table demonstrates the exceptional fast recovery performance and superior ambient light rejection capability of this work. The fast recovery time under heavy-load conditions outperforms that of two mainstream commercial products [19,20]. It also achieves reasonable performance in other aspects, meeting the stringent requirements of automotive LiDAR scenarios.

Table 1. Performance comparison of this circuit with other circuits.

Specification	LTC6560 [19] Commercial	LMH32404 [20] Commercial	Ref. [8]	Ref. [9]	Ref. [10]	This Work
Technology	—	—	0.11 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm SiGe
APD Capacitance (pF)	2	1	1	1.5	2	1
Active Area (mm^2)	—	—	0.023	0.012	0.35	0.15
Power Dissipation (mW)	90	92.4	41	29.4	8	46.2
Bandwidth (MHz)	220	350	300	260	110	421
Transimpedance Gain ($\text{k}\Omega$)	74	20	100	50	100	10
Input-Referred Noise ($\text{pA}/\sqrt{\text{Hz}}$)	4.8	3.54	3.67	3.3	2.21	4.7
Ambient Light Rejection (kHz)	—	400	—	—	—	321
Max. Ambient Light Range (mA)	—	2.5	—	—	—	3
Fast Recovery Time (ns)	10@10mA	12@100mA	—	—	—	8.7@100mA
Pulse Broadening (ns)	—	5@100mA	—	—	—	2.7@100mA

6. Conclusions

This paper proposes a high-performance TIA for automotive dToF LiDAR, addressing ambient light interference and slow overload recovery. Integrating an adaptive ALC loop, it eliminates up to 3 mA background current (321 kHz low-frequency cutoff) without AC coupling capacitors. A multi-stage clamping-current transfer mechanism enables an 8.7 ns recovery time and 2.7 ns pulse broadening under 100 mA overload. Implemented in 0.18- μm SiGe BiCMOS, the TIA features 0.15 mm^2 area, 80 $\text{dB}\Omega$ gain, 421 MHz bandwidth, and 4.7 $\text{pA}/\sqrt{\text{Hz}}$ input-referred noise, meeting automotive-grade (-40°C to

125 °C) requirements. It offers a reliable analog front-end solution for autonomous driving LiDAR systems.

Compared with traditional TIAs, the proposed design has two core strengths: the ALC architecture breaks the voltage swing limit of conventional DC servo loops and cancels large ambient light-induced offset currents that traditional schemes cannot handle, and its hierarchical overload handling mechanism solves the trade-off between recovery speed and signal integrity in traditional clamp circuits, which usually have slow recovery or severe pulse distortion. These innovations make the proposed TIA more suitable for the complex and dynamic working conditions of automotive LiDAR, unlike traditional designs that only focus on single indicators, such as low noise or bandwidth, but ignore scenario-specific bottlenecks. Although the proposed design performs well, it still has room for further optimization, and future research will closely follow the practical application needs of automotive scenarios: optimizing the TIA's fast standby recovery capability to adapt to the frequent power-on/off of on-board LiDAR, exploring circuit architectures with a better bandwidth-power trade-off while maintaining nanosecond-level fast recovery, studying the feasibility of realizing the fast recovery mechanism with a pure CMOS process, further improving the noise performance without degrading fast recovery and bandwidth, and developing adaptive Automatic Gain Control (AGC) schemes to break through integration bottlenecks caused by LiDAR's extremely small duty cycle. Overall, the proposed circuit theory and design method offer a new approach for the development of automotive LiDAR TIAs, and the continuous improvement in this design is expected to promote the progress of high-performance, low-power, and cost-effective environmental perception systems for autonomous driving.

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Abbreviations

The following abbreviations are used in this manuscript:

TIA	Transimpedance Amplifier.
LiDAR	Light Detection and Ranging.
APD	Avalanche Photodiode.
dToF	direct Time of Flight.
ALC	Ambient Light Cancellation.
FDA	Fully Differential Amplifier.
ADC	Analog-to-Digital Converter.
DSP	Digital Signal Processor.
FPGA	Field Programmable Gate Array.
PVT	Process, Voltage, Temperature.
BJT	Bipolar Junction Transistor.
PMOS	P-type Metal-Oxide-Semiconductor.
ICTAT	Current Proportional to Absolute Temperature.
IPTAT	Current Inversely Proportional to Absolute Temperature.

VLSI	Very Large Scale Integration.
SNR	Signal-to-Noise Ratio.
RMS	Root Mean Square.

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