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Article

A Novel Low-Voltage-Based Methodology for Short-Circuit Withstand Time Screening of Commercial 4H-SiC MOSFETs

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Abstract

With the rapid advancement of silicon carbide technology, device reliability has emerged as a critical concern for high-performance power electronics applications. Among various reliability challenges, the limited short-circuit withstand time (SCWT) of SiC MOSFETs, coupled with significant device-to-device variation, poses a serious risk, as it can lead to catastrophic field failures. In addition, established short-circuit screening technique utilizes high-voltage and high-stress condition that may degrade the long-term reliability of otherwise good devices. Hence, this work proposes a novel short-circuit screening methodology employing lower voltages and verifies it using commercial 1.2 kV 4H-SiC MOSFETs. The proposed approach can remove devices with lower SCWT while minimizing electrical and thermal overstress during screening. The results indicate that the proposed low-voltage screening technique offers a safe, repeatable, and reliable alternative to conventional short-circuit screening method, making it well suited for practical manufacturing, leading to system-level reliability enhancement in SiC-based power electronics applications.

Keywords: SiC MOSFET; short-circuit withstand time screening; low voltage; non-destructive method; short-circuit ruggedness

1. Introduction

Short-circuit withstand time (SCWT) is a critical reliability benchmark for power semiconductor devices, as insufficient short-circuit (SC) ruggedness can result in catastrophic failures during operation [1]. With the rapid adoption of silicon carbide (SiC) technology, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) have increasingly replaced conventional silicon IGBTs in high-performance power electronics systems. This transition is driven by the superior material properties of 4H-SiC, including its wide bandgap, high thermal conductivity, and high critical electric field. These characteristics enable higher switching frequencies, increased power density, and improved efficiency [2]. These advantages are particularly attractive in industrial, automotive, and traction applications such as electric vehicle (EV) power converters and traction inverters where reliability and long-term ruggedness are of paramount importance.

Despite these benefits, the SC robustness of commercial 4H-SiC MOSFETs remains a major reliability concern. The inherently smaller chip area and higher power density of SiC devices result in severe thermal stress, leading to rapid thermal runaway, accompanied by

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gate oxide degradation and eventual gate failure, thereby severely limiting the SCWT of the device [3–6].

Significant research efforts have been directed toward improving device-level short-circuit reliability [7–14] and detailed investigations have been carried out to understand short-circuit failure mechanisms under different gate and drain voltage conditions for both planar and trench MOSFETs [4,5,15–28]. Nevertheless, commercially available state-of-the-art SiC MOSFETs typically exhibit SCWTs in the range of 2-7 μs, which further degrade at elevated voltages and temperatures [26]. In addition, considerable device-to-device variation in SCWT, often approaching 1 μs even within a small batch of devices, has been reported [29]. This variability is primarily attributed to the minor process-induced differences in device structure during fabrication. The combination of limited SCWT, large device-to-device variability, and the high-frequency switching capability of SiC MOSFETs poses serious challenges for protection circuit design. As highlighted in prior studies, the fast switching speed of SiC devices necessitates enhanced noise suppression, which often compromises the response time of SC protection circuits [30], thereby increases system-level vulnerability.

To address these challenges, it is essential to screen commercial SiC MOSFETs for short-circuit capability and selectively eliminate devices with inferior SCWT before deployment without compromising the reliability of robust devices. The conventional high-voltage short-circuit screening approach known as Peak Transient Drain Current Methodology (PTDM) [29] suffers from several limitations, although effective in specific cases. This method applies high drain voltage for a short period of time, which may reduce device lifetime and adversely affect the long-term reliability of otherwise healthy devices. Moreover, the reported technique is limited to planar MOSFET structure and is prone to false rejection, thereby reducing manufacturing yield.

In this work, a novel low-voltage SCWT screening methodology for commercial 1.2 kV 4H-SiC MOSFETs is proposed and experimentally validated using both planar and trench gate devices. The proposed approach, termed Low-Voltage Short-Circuit Energy Evaluation (LVSCEE), utilizes controlled low-voltage stress to accurately differentiate devices with lower SCWT from reliable ones while minimizing degradation of the screened devices. Unlike high-voltage screening technique, the proposed method significantly reduces electrical and thermal overstress, enabling safe and repeatable screening, applicable to both planar and trench commercial SiC MOSFETs. Furthermore, key electrical parameters are extracted and analyzed before and after screening to assess potential performance degradation. The results demonstrate that the proposed methodology achieves consistent SCWT screening with negligible impact on device characteristics, making it a practical and reliable solution for improving system-level robustness in SiC power electronics applications.

2. Experimental Methodology

2.1. Device Details

Commercial 1.2 kV SiC MOSFETs with planar gate and reinforced double-trench gate structures from Vendor F and Vendor G2, respectively, were utilized in this study. The typical device structures are shown in Figure 1. The device parameters are presented in Table 1. Before SC measurement, each device underwent typical electrical characterizations using a Keysight B1506A Power Device Analyzer (Keysight Technologies, Colorado Springs, CO, USA) to obtain threshold voltage (V_{th}) and on-resistance (R_{on}). V_{th} of these devices were extracted using the linear extrapolation method [31] at drain-to-source voltage (V_{ds}) of 100 mV, whereas R_{on} was calculated at gate-to-source voltage (V_{gs}) of 20 V and V_{ds} = 1.5 V.

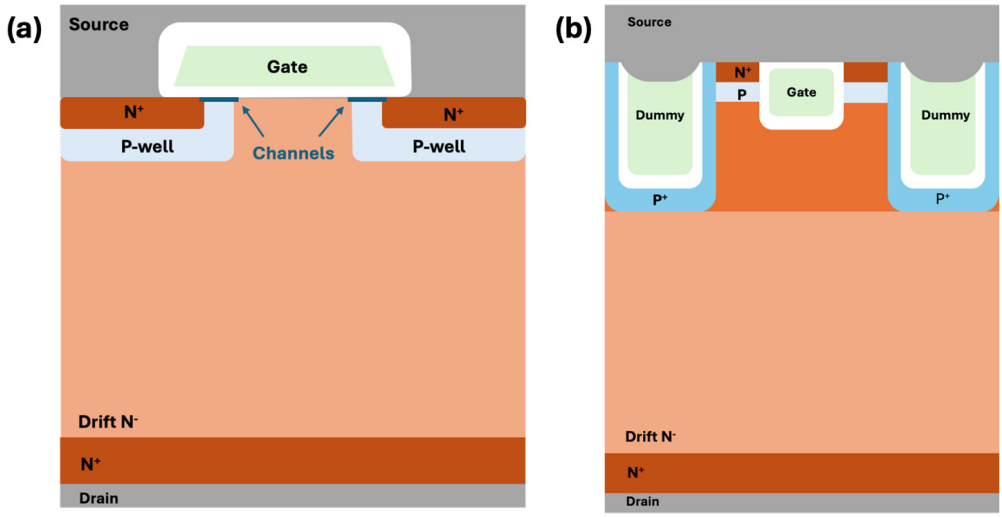

Figure 1. Cross-sectional view of a typical (**a**) planar and (**b**) reinforced double-trench MOSFET.

Table 1. 1.2 kV Commercial devices details.

Vendor	Vendor F	Vendor G2
Device Type	Planar	Reinforced Double-Trench
Rated Voltage (kV)	1.2	1.2
Rated Current (A)	7.6	26
Typical Threshold Voltage (V)	2.5	2.8
Typical On-Resistance (mΩ)	350	62
Number of Devices Tested	18	25

2.2. Short-Circuit Evaluation

SC evaluation of commercial 4H-SiC MOSFETs was carried out using a typical SC setup, as shown in Figure 2 [29]. The setup contained three 100 µF thick film capacitors to stabilize the DC source voltage, along with a 1 µF decoupling capacitor with low ESL (equivalent serial inductance) and ESR (equivalent serial resistance), guaranteeing high frequency switching conditions. A 10 Ω gate resistor was used to ensure controlled turn-on and turn-off of the device under test (DUT). Drain-to-source transient current during SC evaluation (I_{ds}) was measured using a 10 mV/A sensitive PEM CWT3 Rogowski coil with a rated peak current of 600 A. For enhanced safety of the setup, 5 kΩ current-limiting resistors along with 66 kΩ bleeding resistors were provided. The SC measurements were carried out at varying V_{ds} = 200 V, 400 V, 600 V, and 800 V under V_{gs} = 20 V. Depending on the condition, the gate turn-on pulse width was varied to ensure minimum heating effect. To evaluate the SCWT of the DUT, V_{gs} = 20 V and V_{ds} = 800 V condition was selected where the starting pulse was kept at 0.5 µs, which was then increased by a step of 0.1 µs until failure was observed. Sufficient cooling time was provided in between two consecutive pulses to guarantee minimum heating effect. The time of failure (or the pulse width) was termed as the SCWT of the DUT. The setup was kept unchanged throughout the experiments to ensure consistent results.

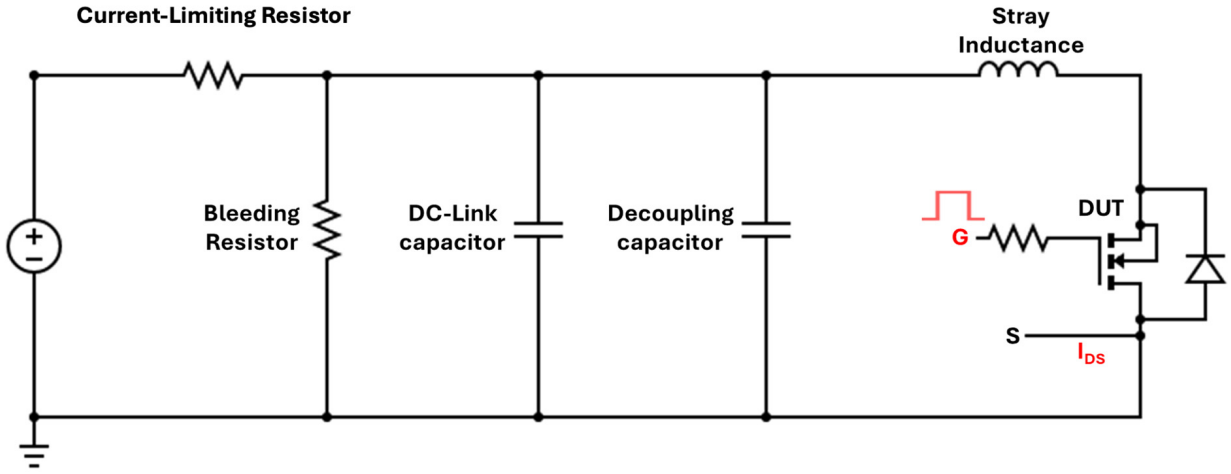

Figure 2. Topology of a typical short-circuit experiment setup.

3. Low-Voltage Short-Circuit Energy Evaluation (LVSCEE)

3.1. Variation in SCWT

1.2 kV 4H-SiC MOSFETs from Vendor F and Vendor G2 underwent SCWT measurement at V_{gs} = 20 V and V_{ds} = 800 V, and the results are shown in Figure 3. DUTs were carefully selected from same batch and lot to ensure consistency among devices. The results show a 0.6 µs SCWT variation for both vendors.

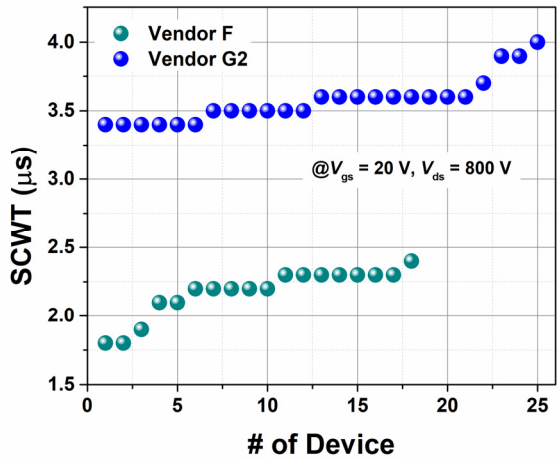

Figure 3. SCWT variation of devices from Vendor F and Vendor G2.

3.2. Peak Transient Drain Current Methodology and False Rejection Rate

$$P_{TDM} = \frac{I_{peak}}{slope} \tag{1}$$

$$slope = \frac{\left(I_{peak} - I_{min}\right)}{\left(t_{screen} - t_{peak}\right)} \tag{2}$$

where I_{peak}, I_{min}, t_{screen}, and t_{peak} are peak drain current, turn-off drain current at t_{screen}, screening pulse width, and time at which drain current achieves I_{peak}, respectively.

The high-voltage PTDM [29] has been proposed to selectively screen out devices with lower SCWT without damaging reliable devices. First, a SCWT screening parameter P_{TDM} is calibrated using Equations (1) and (2) with a preliminary set of devices. This is performed by measuring the SCWT of the preliminary set at V_{ds} = 800 V and V_{gs} = 20 V while the gate pulse duration t_{screen} is incremented in 0.1 µs steps until the device fails. Depending

on the minimum SCWT requirement, a permissible range of P_{TDM} can be established for devices from the same vendor and production lot. Once the P_{TDM} range is defined, only a single pulse of t_{screen} duration is needed to remove devices with inferior SCWT, without destroying reliable ones.

The variation in P_{TDM} is influenced by several device design and process parameters, such as die area, die volume, channel design, active area design, gate oxide thickness and quality, interface defect state density, doping profile, temperature diffusion process, etc. [32–34]. Consequently, both the manufacturers and the end users must experimentally determine P_{TDM} ranges for different vendors and process flows. However, a major concern of PTDM is the possibility of incorrectly rejecting reliable devices during the screening process, as illustrated in Figure 4 for Vendor F devices. This phenomenon is referred to as false rejection.

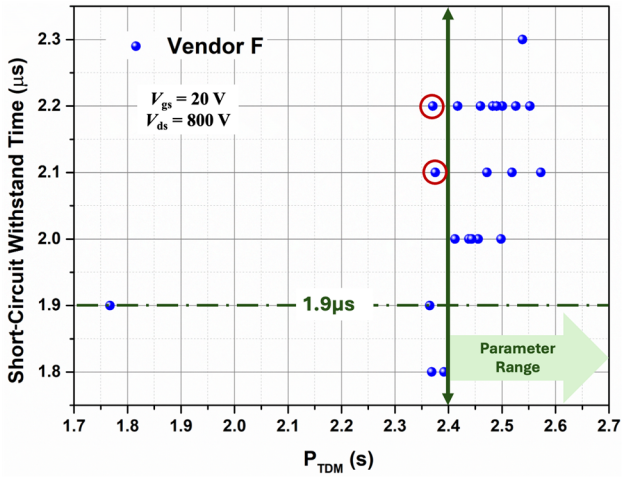

Figure 4. P_{TDM} distribution of Vendor F devices. The red circles indicate devices that will be falsely rejected while screened using PTDM.

The false rejection rate (*FRR*) can be defined as follows:

$$FRR = \left(\frac{Number\ of\ reliable\ devices\ falsely\ screened\ out}{Total\ number\ of\ devices} \right) \times 100\% \quad (3)$$

Using this definition, an *FRR* of 8.69% is observed for Vendor F devices (number of devices tested are 23) at $P_{TDM} \geq 2.4$ s. Such a level of false rejection is undesirable, as it adversely affects device yield and overall manufacturing efficiency.

3.3. Proposed LVSCEE Method

Fundamentally, the proposed LVSCEE method is based on the SC energy during different applied V_{ds} under a particular gate pulse width (t_{pulse}). Mathematically, SC energy at a particular pulse (E_{pulse}) can be defined as follows:

$$E_{pulse} = \int_0^{t_{pulse}} V_{ds} I_{ds} dt \quad (4)$$

During the event of SC, the DUT experiences lattice heating [26], which eventually causes the failure of the device. This effect of heating is directly correlated to the transient energy E_{pulse} at each time frame. Hence, a correlation between E_{pulse} and SCWT can be established. The proposed LVSCEE method is graphically shown in Figure 5.

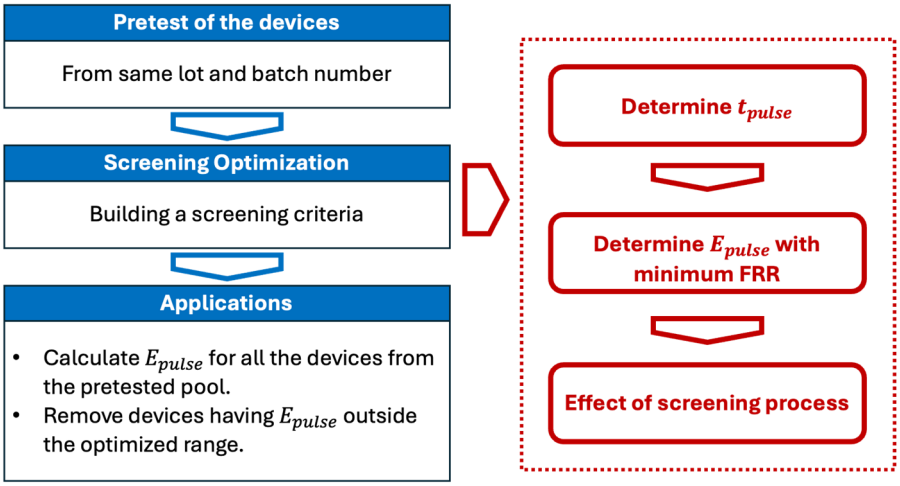

Figure 5. Novel LVSCEE methodology along with SC screening energy (E_{pulse}) optimization process.

For successful screening, the key factors include determining the appropriate E_{pulse} under a certain V_{ds} and pulse width (t_{pulse}) as well as setting the minimum SCWT threshold to effectively screen out weaker devices, while maintaining an extremely low false rejection rate. Furthermore, the effect of the screening on the devices needs to be examined using static characteristics and interface defect analysis pre- and post-screening to ensure no degradation. Upon establishing the E_{pulse} window needed for the reliable devices, this methodology can be used in thousands of devices just by applying a low-voltage single pulse to remove the weaker devices without damaging the reliable ones. Moreover, as this methodology relies solely on the dissipation energy under a given V_{ds} and t_{pulse}, it enables the applicability of this technique irrespective of screening or operating voltage level, and cross-voltage correlation can be established.

3.3.1. Drain Current Behaviour Under Different Drain Voltages

The first part of this work aims to understand the behaviour of the drain current under different applied drain voltages. Figure 6 shows the I_{ds} vs. transient time characteristics of a representative Vendor F device under t_{pulse} = 1.5 µs for V_{ds} = 200 V, 400 V, 600 V, and 800 V. It can be clearly seen that under a fixed t_{pulse}, with the increase in V_{ds} level from 200 V to 800 V, the peak drain current ($I_{\text{ds,peak}}$) enhances significantly, indicating more heat generation.

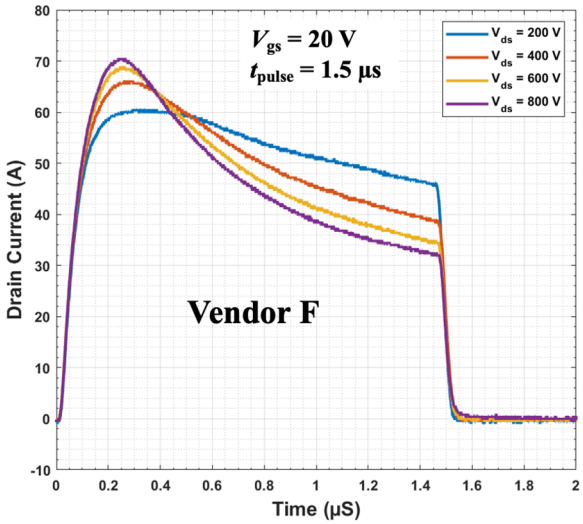

Figure 6. Drain current behaviour of a representative Vendor F device under V_{ds} = 200 V, 400 V, 600 V, and 800 V at t_{pulse} = 1.5 µs.

3.3.2. Determining Screening Pulse Energy, Pulse Width, and SC Screening

Using Equation (4), the screening pulse energy (E_{pulse}) under different V_{ds} and t_{pulse} = 1.5 µs was calculated and is shown in Figure 7 for the Vendor F devices. SCWT at different drain voltage levels is also plotted in Figure 7. It is evident that as V_{ds} increases, E_{pulse} under the same t_{pulse} increases and SCWT decreases. Under V_{ds} = 400 V, the representative device can withstand ~9 µs, after which SC occurs.

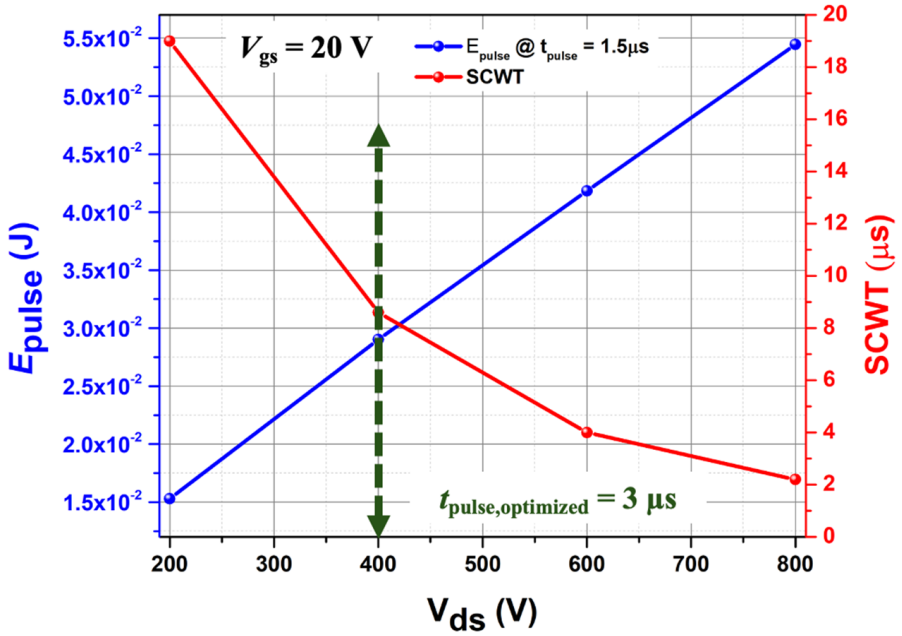

Figure 7. E_{pulse} and SCWT of Vendor F devices under different V_{ds}.

Another critical aspect of effective short-circuit screening is the optimization of the t_{pulse} to minimize FRR. Figure 8 illustrates the SCWT measured at V_{ds} = 800 V as a function of E_{pulse} calculated at V_{ds} = 400 V for different t_{pulse} values using Vendor F devices. The pulses are varied from 2.5 µs to 4.0 µs in steps of 0.5 µs. It can be clearly seen that, under t_{pulse} = 3.0 µs (Figure 8b) and t_{pulse} = 3.5 µs (Figure 8c), no device was falsely rejected.

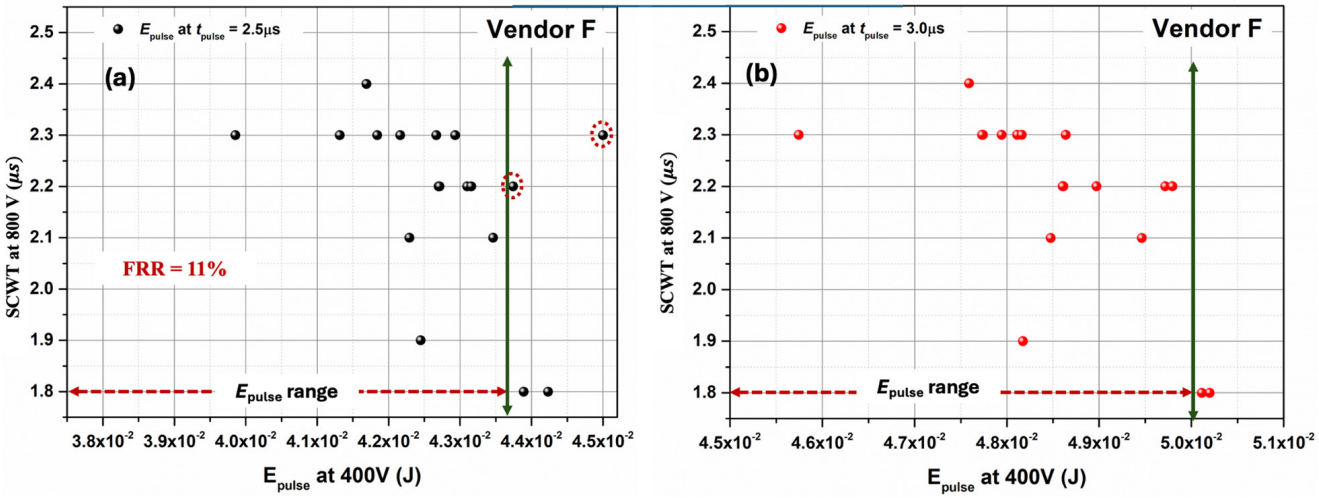

Figure 8. *Cont.*

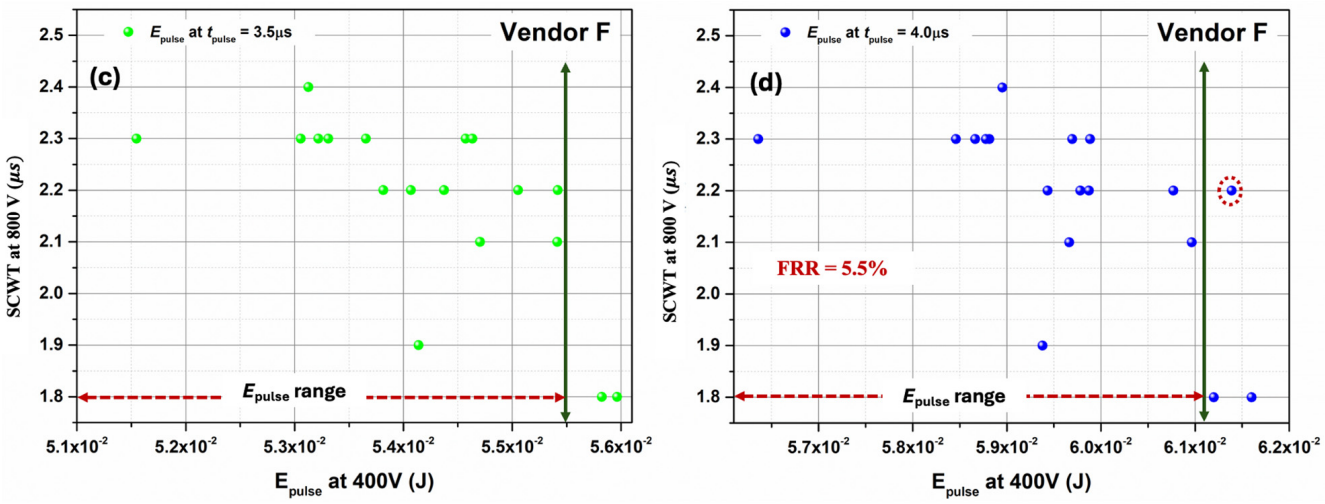

Figure 8. Screening pulse optimization for Vendor F devices under different pulse widths of (**a**) t_{pulse} = 2.5 µs, (**b**) t_{pulse} = 3.0 µs, (**c**) t_{pulse} = 3.5 µs, and (**d**) t_{pulse} = 4.0 µs to achieve minimum false rejection. Red arrow indicates allowable E_{pulse} range to achieve SCWT ≥ 1.8 µs under V_{ds} = 800 V. Devices that are falsely rejected are highlighted by red circles. For t_{pulse} of 3.0 µs and 3.5 µs, no device has been falsely rejected.

To further assess the impact of screening conditions on devices' thermal integrity, additional electro-thermal simulations were performed using LTspice to estimate the junction temperature (T_j) of a typical Vendor F device under t_{pulse} corresponding to an extremely low FRR. T_j has been evaluated using a Cauer thermal network model [35], as shown in Figure 9a. This model utilizes an equivalent RC network, where the input is the instantaneous power dissipation ($V_{ds} \times I_{ds}$) as a function of transient time. The equivalent RC parameters are listed in Table 2.

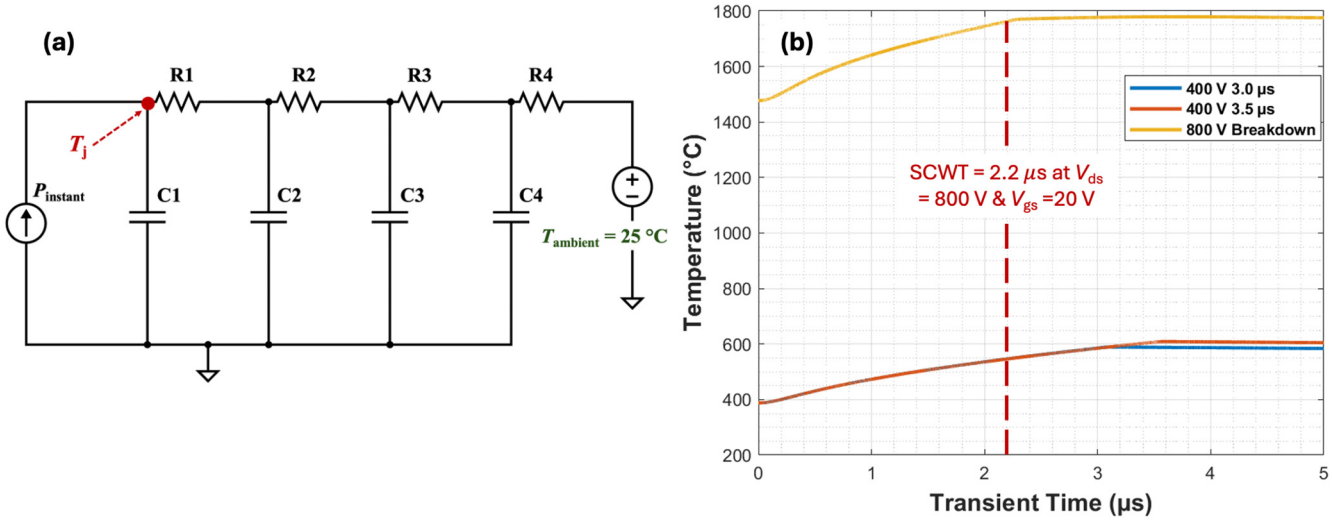

Figure 9. (**a**) Cauer thermal network model; (**b**) LTspice simulation result of a typical Vendor F device. The red dashed line shows the SCWT of the simulated device under V_{ds} = 800 V.

The simulation result (Figure 9b) indicates that, under the optimized conditions (V_{ds} = 400 V, t_{pulse} = 3 µs, and 3.5 µs), maximum junction temperature ($T_{j,max}$) remains below one-third of the value observed during convention SCWT measurement at V_{ds} = 800 V. Based on this analysis, in this work, we considered V_{ds} = 400 V with optimized pulse width ($t_{pulse,optimized}$) of 3 µs for screening of Vendor F devices, to assure no thermal damage occurs while maintaining reliable screening output.

Table 2. RC parameter values of Cauer thermal network model.

Parameter	Values
R1	406 mΩ
R2	1.088 Ω
R3	481 mΩ
R4	341 mΩ
C1	238 µF
C2	1.15 mF
C3	5.86 mF
C4	90.1 mF

Figure 10a shows the SCWT as a function of optimized E_{pulse} at $t_{pulse,optimized}$ = 3.0 µs for Vendor F devices. Although the E_{pulse} is calculated at a lower drain voltage level of 400 V, to maintain consistency, SCWT is determined at V_{ds} = 800 V for the same devices. It is apparent that to remove devices with SCWT lower than or equal to 1.8 µs at V_{ds} = 800 V, E_{pulse} should be less than 0.05 J. Similar analysis was performed on Vendor G2 devices, considering $t_{pulse,optimized}$ = 5.0 µs at V_{ds} = 400 V, and is shown in Figure 10b. To successfully remove devices with SCWT less than or equal to 3.4 µs at V_{ds} = 800 V, E_{pulse} should be less than 0.24 J.

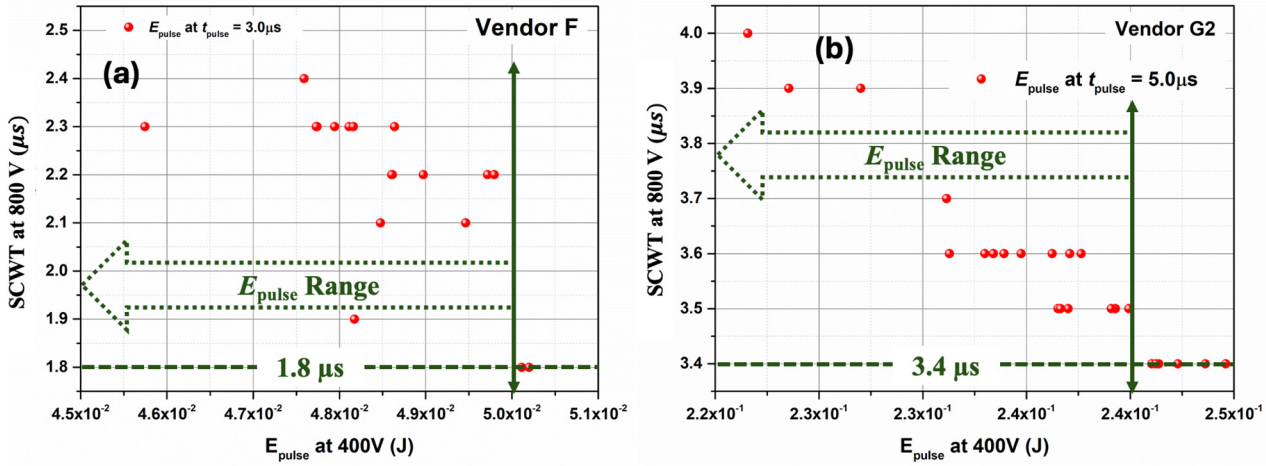

Figure 10. SCWT as a function of E_{pulse} for (**a**) Vendor F and (**b**) Vendor G2 devices. Ranges of E_{pulse} for SCWT ≥ 1.8 µs and SCWT ≥ 3.4 µs for Vendor F and Vendor G2 devices, respectively, are shown using green arrows.

It is evident that devices with lower E_{pulse} indicate lower heat generation and hence lower thermal effect, leading to higher SCWT. The t_{pulse} and V_{ds} need to be optimized for different vendors to ensure optimal screening. The analysis further shows that this methodology is independent of device design parameters or fabrication process flow and can be implemented easily without any prior device knowledge.

3.3.3. Effect of Short-Circuit Screening Process

The effect of the LVSCEE method on the devices' characteristics was studied by measuring and comparing V_{th}, R_{on}, and gate leakage current (I_{gss}) on a batch of devices from each vendor before and after applying the E_{pulse}. The V_{th} of these devices was extracted using the linear extrapolation method [31] at V_{ds} = 100 mV, whereas the R_{on} was calculated at V_{gs} = 20 V and V_{ds} = 1.5 V. I_{gss} is measured at V_{gs} = 30 V. The results are consolidated in Table 3. All results are representative in nature.

Table 3. Key electrical parameters variations pre- and post-screening.

Vendor	Threshold Voltage (V)		On-Resistance (mΩ)		Gate Leakage Current (nA)	
	Pretest	Post-Screening	Pretest	Post-Screening	Pretest	Post-Screening
F	6.11	6.09	313.9	300.01	25.8	25.6
G2	6.03	6	51.96	51.68	4201.71	4201.89

Moreover, the effect of screening on the interface is determined by utilizing the subthreshold method [36] at room temperature. The mathematical model of this technique is briefly discussed below.

The drain current at subthreshold region is defined as

$$I_{ds} = I_0 e^{\frac{qV_{gs}}{nkT}} \left(1 - e^{\frac{qV_{ds}}{kT}}\right) \tag{5}$$

where the ideality factor n is given as

$$n = \frac{q}{2.3kT} \left(\frac{\partial log I_{DS}}{\partial V_{gs}}\right)^{-1} = 1 + \frac{C_D + C_{it}}{C_{ox}} \tag{6}$$

where C_D is depletion capacitance, C_{ox} is oxide capacitance, and C_{it} is the interface trap capacitance per unit area.

The energy-dependent interface trap density is given as

$$D_{it}(\varphi_s) = \frac{C_{it}}{q} \tag{7}$$

and the energy distribution of the trap level $(E_{cs} - E_T)$

$$E_{cs} - E_T = \frac{E_g}{2} - q\left(\varphi_F - \frac{2.3kT}{q} \log\left[\frac{I_{DS}(2\varphi_F)}{I_{DS}(\varphi_s)}\right]\right) \tag{8}$$

where surface potential (φ_s) is in the range $\varphi_F < \varphi_s < 2\varphi_F$ and φ_F is the Fermi potential.

Using Equations (7) and (8), $D_{it}(\varphi_s)$ of the representative devices from Vendor F and Vendor G2 were extracted before and after applying screening pulse, and the results are shown in Figure 11. It can be clearly seen that no significant degradation occurred due to the screening, and hence this methodology can be safely applied to remove devices with lower SCWT from a batch of devices without harming the reliable ones.

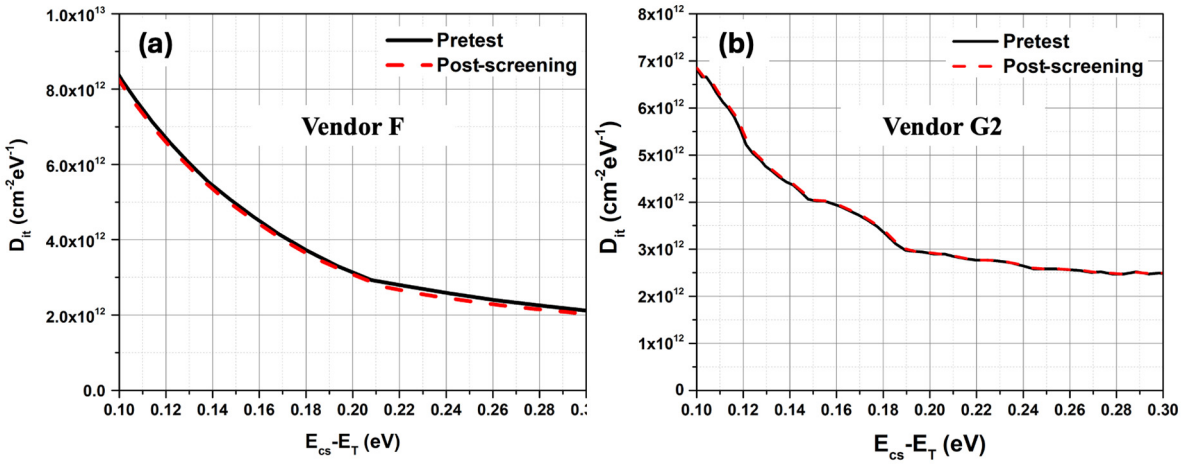

Figure 11. D_{it} profile extracted at room temperature for (**a**) Vendor F and (**b**) Vendor G2 representative devices pre- and post-screening.

4. Conclusions

This paper presents a novel low-voltage short-circuit screening methodology, termed as LVSCEE, aimed to address the reliability challenges associated with poor SCWT and large device-to-device variability in commercial 1.2 kV 4H-SiC MOSFETs. Unlike the conventional high-voltage Peak Transient Drain Current Methodology, the proposed approach utilizes a lower screening voltage, and thus significantly reduces electrical and thermal overstress during screening. This minimizes the risk of latent damage and long-term reliability degradation. Experimental validation on both planar and trench gate SiC MOSFETs confirms that the LVSCEE method effectively removes devices with inferior SCWT while preserving the electrical integrity of robust devices. The analysis of key electrical parameters before and after screening indicates negligible performance degradation, highlighting the suitability of the proposed technique for practical manufacturing and qualification environments.

Overall, the LVSCEE methodology provides a reliable, repeatable, and structure-independent solution for SCWT screening of SiC MOSFETs. By enabling early elimination of weak devices without compromising healthy ones, the proposed approach contributes to enhanced system-level robustness and increased reliability of next-generation SiC-based power electronics applications.

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Abbreviations

The following abbreviations are used in this manuscript:

SC	Short Circuit
SCWT	Short-Circuit Withstand Time
PTDM	Peak Transient Drain Current Methodology
LVSCEE	Low-Voltage Short-Circuit Energy Evaluation
DUT	Device Under Test
FRR	False Rejection Rate

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