electronics

MDPI

Article

The FPGA-Based Control System for High-Speed SRM Drive with a C-Dump Converter

Daniel Rataj [1,*], Krzysztof Tomczewski [1] and Andrzej Tomczewski [2]

[1] Faculty of Electrical Engineering, Automatic Control and Computer Science, Opole University of Technology, 45-758 Opole, Poland; k.tomczewski@po.edu.pl
[2] Institute of Electrical Engineering and Electronics, Faculty of Control, Robotics and Electrical Engineering, Poznan University of Technology, Piotrowo 3A, 60-965 Poznan, Poland; andrzej.tomczewski@put.poznan.pl
* Correspondence: d.rataj@po.edu.pl

Abstract

This article focuses on power supply control issues in high-speed switched reluctance motors (SRMs). The primary scientific objective of this study was to determine whether and to what extent, the controller itself imposes limitations on SRM drive operation at very high rotational speeds, and to identify the maximum achievable speed range resulting from these limitations. Unlike most existing studies, which focus mainly on motor or power electronics constraints, this work explicitly analyses the dynamic limitations introduced by the control system architecture. An analysis of the essential controller functionalities required for implementing the SRM drive control algorithm with a C-dump converter was performed. The control system, composed of specialised hardware modules operating concurrently, was implemented in an field-programmable gate array (FPGA) device. Simulation and experimental investigations were conducted to evaluate signal propagation delays within the FPGA and their impact on the motor control process. Key functional modules contributing to the maximum signal propagation delays were identified, enabling a direct determination of the maximum motor speed at which correct power supply operation can be ensured. Furthermore, delays introduced by the power electronic components were characterized for the developed test controller, allowing a comprehensive assessment of both control and hardware-induced speed limitations. The research concluded that the FPGA-based controller introduces no significant limitations to the drive's maximum speed. The maximum speed is limited by the mechanical constraints of the rotor and the inertia of the phase windings. Furthermore, expanding the controller with additional functionality does not significantly slow down the control algorithm's execution.

Keywords: switched reluctance motor (SRM); switched reluctance drive; field-programmable gate array (FPGA); C-dump converter; high-speed drive

Check for updates

Academic Editors: Spyridon Nikolaidis and Alexander Barkalov

Received: 4 December 2025
Revised: 14 January 2026
Accepted: 25 January 2026
Published: 28 January 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

1. Introduction

High-speed drives are essential in diverse fields, ranging from industrial manufacturing (milling machines, lathes) to laboratory equipment, such as centrifuges. In medical applications, these systems are employed in the separation of blood samples and other biological fluids. Low-power variants are widely applied in portable power tools, including drills, engravers, grinders, and saws. Furthermore, significant applications are found in the aviation and automotive industries, where very high rotational speeds are required for turbochargers, aircraft windshield wipers, and starter motors [1–10]. These drives are also

used in household appliances, such as vacuum cleaners, to reduce their size and acoustic noise [11]. In the textile industry, they are primarily applied for spindle actuation [1,12,13].

Several types of electric motors are employed in high-speed drives systems, including permanent magnet motors, hysteresis motors and SRMs [2,3,14]. Permanent magnet motors, most commonly implemented as BLDC motors, can achieve very high rotational speeds with an appropriate design consideration. The challenge with this type of motor lies in the mounting of the magnets, which are subjected to very high centrifugal forces in the rotors. Nevertheless, due to their high power density, they are dominant in drives for small flying objects such as drones [2,15]. For larger drives and higher speeds, it is often necessary to mount the magnets in channels inside the rotor.

Hysteresis motors are much more resistant to damage resulting from high rotational speeds. A key advantage of hysteresis motors is their low acoustic noise emissions. Nevertheless, their disadvantages include significant rotor heating and low torque at low speeds, which significantly limits their applicability in many practical applications [16–20].

Switched reluctance motors do not exhibit these specific disadvantages [21–23]. They feature a robust rotor made of laminated electrical steel, offering high durability and relatively high efficiency [24,25]. Their main drawback is the high vibration and noise levels resulting from the pulsed power supply and the salient-pole rotor design. These effects can be mitigated through advanced control strategies [21,22,25–29].

SRMs require specialised converters that switch the phase supply voltage depending on the rotor angular position [23,24,30]. To achieve correct operation, it is necessary to make the supply voltage and the angular ranges of the phase supply dependent on the motor's operating point. At high speeds, precise control of the phase supply, and in particular the determination of rotor position and speed, requires the controller to execute multiple complex functions with very low latency. Therefore, the controller must ensure very high algorithm execution speed [30–32]. Expanding the control algorithm with additional functionalities, such as vibration and noise reduction, and calculating the drive's mathematical model, in the case of microcontrollers, leads to longer control cycles.

A significant portion of a microcontroller's control algorithm is implemented in interrupt handling routines. As drive speed and control accuracy increase, the percentage of processor time required to perform basic functions increases. Compared to typical low-speed drive systems, the interrupt generation frequency can increase by over a hundred-fold. Therefore, in high-speed, adjustable-speed drives, the time required to execute interrupt handling routines increases proportionally with the speed. In microprocessor controllers, ultra-high speed capabilities are typically achieved at the expense of control precision. In such cases, any additional expansion of the control algorithm can slow down the execution of the control algorithm.

For this reason, a good alternative to the control program may be the implementation of the control algorithm in the form of specialized hardware structures that operate concurrently. In such systems, adding new functionalities does not degrade performance, provided that the execution time remains within the maximum delay of existing modules. Field-programmable gate arrays (FPGAs) provide such capabilities [20,33–38]. The concurrent architecture ensures that execution speed and temporal determinism remain largely independent of the number of implemented tasks.

The scientific objective of this paper is to determine whether, and to what extent, the controller architecture itself introduces limitations on SRM drive operation at high rotational speeds, and to identify the maximum achievable speed range resulting from these hardware-induced constraints.

2. Properties of Switched Reluctance Motors

Due to the simple rotor structure, made as a stack of sheets, switched reluctance motors are characterised by high mechanical strength and resistance to centrifugal forces. In this respect, they are similar to hysteresis motors [18,19]. Nevertheless, due to the method of obtaining electromagnetic torque, their rotors possess salient rotor teeth, which introduce a clear dependence of magnetic reluctance on the rotor angle.

The electromagnetic torque of this type of motor is proportional to the difference between the maximum and minimum values of magnetic reluctance. When a phase is supplied with power within a specific angular range, the rotor tends to achieve the position of minimum magnetic reluctance. To maintain continuous motion, the supply voltage to a phase can be switched off before this position is reached, while simultaneously switching on the supply voltage to the next phase. It is also possible to specify an angular range that positions the rotor in the position of minimum magnetic reluctance [14,23,30].

This enables these motors to achieve their rated torque when they are operated at low speeds and during positioning. In this speed range, it is necessary to limit the current or reduce the supply voltage. The phase is therefore supplied as a series of pulses. In practical operation, this occurs between zero and the rated speed. Above the rated speed, when supplied with the rated voltage, the phases are often supplied with single pulses, and the speed depends on the commutation angles [21–24,39–41].

A further increase in rotational speed can be achieved by increasing the supply voltage of the motor phases. Particularly important in this case is the increase in voltage at the initial stage of the phase supply cycle and the return of energy from the windings, after the phase supply is switched off, to a higher voltage source. This accelerates the rise and fall of phase currents. As a result, the average current value is increased in the angular range where the electromagnetic torque is positive. Conversely, this limits the time of phase current flow in the angular range where the electromagnetic torque is negative.

Therefore, a number of different converter topologies have been developed to power SRM motors [23,24]. SRMs have mechanical characteristics similar to those of series motors, but their properties can be adjusted over a wide range by changing the commutation angles. The electronic converter, acting as an electronic sparkless commutator, must enable the appropriate selection of the phase supply angle ranges to the motor operating point [21,25,26,42].

The efficiency of SRM motors is slightly lower than that of BLDC motors, but they do not contain rare-earth magnets. It should also be noted that the mechanical strength of BLDC motor rotors is lower than that of SRM motors. Therefore, for very high speeds, complex rotor designs are required in permanent magnet motors, and the magnets are mounted below the rotor surface.

Unlike the converters that power BLDC motors, to achieve correct operation of an SRM motor, it is necessary to adjust the commutation angles according to the desired operating point. For high-speed drives, the controller must decode very quickly the position, measure currents and instantaneous speed, and control the signals that activate the phase power supply.

The main goal of this work was to analyse the feasibility of implementing an SRM control system based on a programmable logic device. Using this type of system eliminates the need for sequentially executed microcontroller programs, where the introduction of any additional functionality slows down the control algorithm.

Programmable logic devices enable the implementation of a controller as specialised logic circuits in which various controller functionalities operate concurrently, and significantly faster than in a microprocessor-based software implementation. With this controller structure, only the basic control path modules are critical to the controller's speed. The re-

maining modules operate concurrently and therefore do not affect the maximum execution speed of the algorithm.

Due to the hardware implementation of the functional modules of the main control path, the delays introduced by the controller are relatively small compared to those observed in microprocessor controllers. This work determined the maximum theoretical drive speed at which the controller can operate correctly, with high commutation angle resolution.

This study aimed to determine the maximum theoretical operating speed of the drive at which the controller can function correctly while maintaining high angular position measurement resolution of the rotor. For this purpose, a functional analysis of the control system was performed, and the key modules and signal paths having the greatest impact on the execution speed of the control algorithm were identified. Simulation and experimental investigations were conducted to determine the delays introduced by these modules, and the maximum delay introduced by the primary signal path was established. Based on these results, the maximum theoretical rotational speed at which the control system is capable of executing the control algorithm was determined.

3. Functional Analysis of the SRM Control System

Proper relationship between commutation angles and rotational speed enables optimisation of drive performance at specific operating points, for example, to maximise efficiency or minimise acoustic noise [43]. In SRM drives, the operating points corresponding to maximum power, maximum efficiency, and minimum torque ripple generally differ. Therefore, achieving both high efficiency and high output power requires a compromise and careful optimisation of control parameters. Reducing electromagnetic torque ripple and the associated acoustic noise typically requires shaping of phase current waveforms through supply voltage modulation. Consequently, multipulse voltage excitation is often applied; however, this approach increases commutation losses. Furthermore, operation at high rotational speeds with multipulse excitation requires accurate determination of control parameters.

The angular range of phase excitation is defined by the resolution of the rotor position measurement. Various sensor-based and sensorless techniques can be employed to estimate rotor position. Sensorless methods rely on indirect measurements, such as phase inductance variation with rotor position, and are generally less accurate than sensor-based approaches. In practical SRM drives, incremental encoders are most commonly used. These can be mounted externally on the motor shaft or integrated directly into the motor housing. At high rotational speeds, integrated encoders are preferable due to potential alignment issues associated with external sensors. Higher encoder resolution enables more precise adjustment of phase excitation angles. Encoder signals are also used for instantaneous speed estimation, which is required for closed-loop control.

Accurate determination of rotor position is a key challenge in SRM drives. The required phase excitation angle range depends on the number of motor phases. For a typical two-phase SRM, a minimum conduction interval of 90 degrees (electrical) is required to ensure continuous torque production. For three-phase and four-phase machines, this interval decreases to approximately 30 and 15 degrees, respectively. When using a standard encoder with a resolution of 360 pulses per revolution, the angular resolution becomes progressively coarser for motors with a higher number of phases. Improved accuracy can be achieved by applying advanced position estimation techniques or higher-resolution sensors.

Another important aspect is voltage regulation within the phase excitation interval. When PWM is applied, the number of voltage pulses per conduction cycle decreases as speed increases. At high speeds, single-pulse operation is commonly used. However,

additional voltage modulation may still be required to minimise torque ripple. Therefore, the PWM switching frequency should be sufficiently high to generate multiple supply voltage pulses within the excitation interval, enabling accurate shaping of the phase current waveform.

Appropriate phase current measurement frequency is also essential. The rate of current rise depends on the instantaneous phase inductance and reaches its maximum when the rotor and stator teeth are fully unaligned. The sampling frequency must, therefore, ensure a sufficiently fast controller response to prevent current overshoot beyond permissible limits. Additional protection can be implemented at the hardware level by directly coupling transistor drivers with current sensors, allowing rapid overcurrent response independent of the controller.

For C-dump converter topologies, measurement of the capacitor voltage is also required. High sampling speeds are necessary to maintain the voltage within predefined limits, which depend on the rotational speed. Based on the measured voltage, switching devices are controlled to limit the maximum voltage during capacitor charging and the minimum voltage during discharge. The voltage variation rate is determined by the phase current magnitude and the capacitance.

4. Structure of a Controller Based on an FPGA Programmable Logic Device

The presented drive system consists of an FPGA-based control module, a driver module, a power transistor module, and a power supply. Depending on the converter topology, the output transistors can operate in various configurations. The simplest and most commonly used solution is the asymmetric H-bridge converter. For high-speed operation, more advanced converter topologies, such as C-dump or multilevel converters, can be employed [24,31,44–47]. However, these configurations require more sophisticated control algorithms, including the control of additional switching devices and the measurement of extra parameters affecting the control process.

Multilevel converters are generally more expensive due to the large number of power transistors they require. A more cost-effective alternative is the C-dump converter. In this topology, the C-dump capacitor acts as a dynamic energy buffer, whose voltage can be adjusted by the control system according to the motor operating conditions.

To achieve high rotational speeds, the converter configuration shown in Figure 1 is applied. In addition to regulating the supply voltage from zero to its rated value and adjusting the commutation angles, this topology allows the voltage to be boosted to expand the drive's power and speed range. The C-dump capacitor is charged using energy recovered from the phase windings after phase excitation is switched off. Increasing the voltage, particularly during the initial excitation interval, enables approximately a threefold increase in speed while maintaining the rated output power. A detailed description of this system is provided in [48].

The driver module incorporates signal conditioning circuits and measurement units. For an asymmetric H-bridge converter, the measured quantities include phase currents and supply current. In C-dump converter configurations, additional measurements of the C-dump capacitor voltage are necessary.

The power supply system provides the voltages needed to power the motor, drivers, sensors, and control system. The motor power supply subsystem consists of a rectifier and filter capacitors. In drives with regenerative braking capability, it also includes a feedback circuit that returns energy to the supply source. Furthermore, the power supply delivers regulated voltages to the controller in accordance with component requirements.

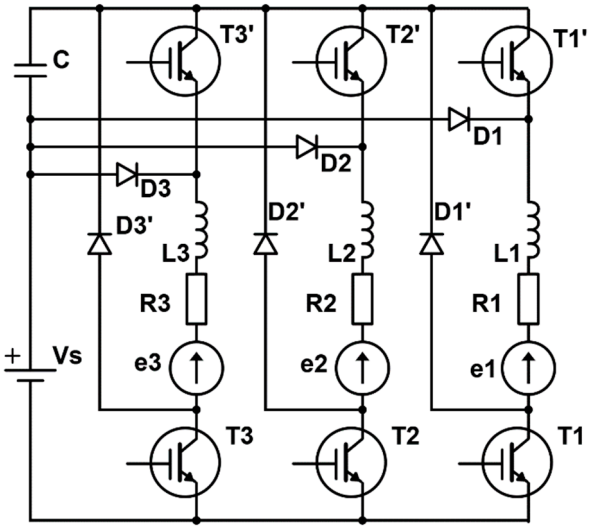


Figure 1. C-dump converter schematic for a three-phase SRM drive with the C-dump capacitor connected in series with the supply V_s.

In the proposed system, the controller is implemented using an FPGA device. To minimize processing delays at high rotational speeds, parallel hardware structures are used instead of sequential microcontroller-based software control. The controller functionality can be divided into two main groups: time-critical modules directly involved in the control process and auxiliary modules that do not influence real-time operation, such as user interface and communication modules. The resulting block diagram, derived from the functional analysis, is shown in Figure 2.

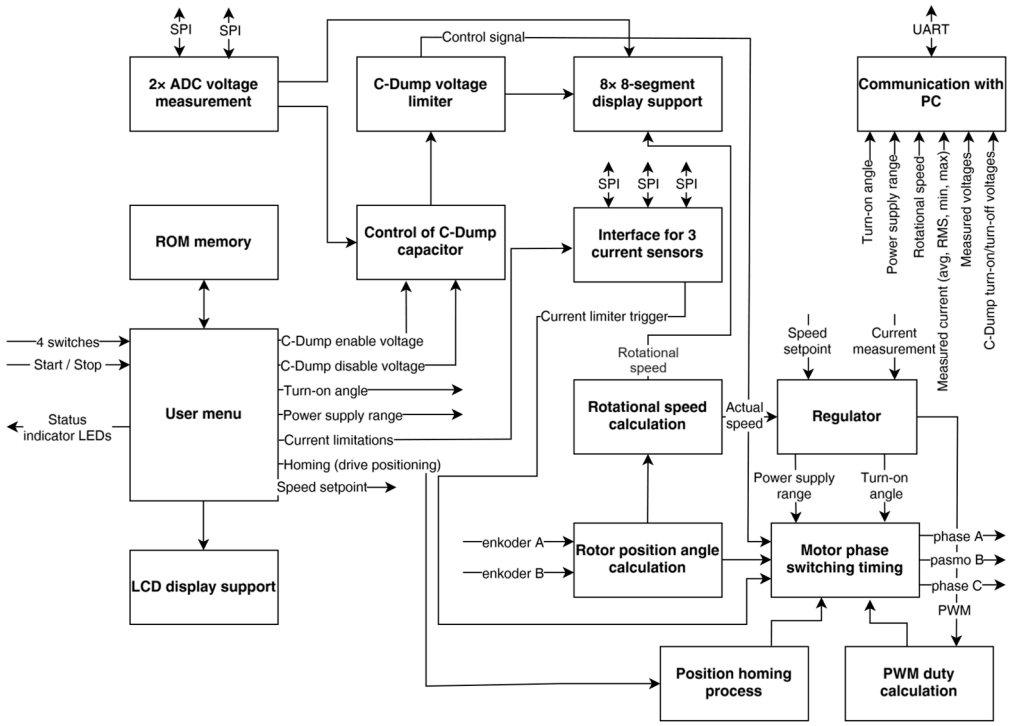


Figure 2. Block diagram presenting the functional structure of the controller.

The controller comprises the following main functional modules: a rotor angular position estimation module, a phase sequence decoder, current and voltage measurement modules, a speed estimation module, a PWM generator module with current limiting, and a control module. Depending on the applied control strategy, additional modules

may be incorporated, such as a mathematical model computation unit. All core modules must execute their functions within each drive control cycle, as any excessive latency may degrade system performance or destabilize the control process.

4.1. PWM Generator Module

PWM is applied to regulate the supply voltage to the motor phases. The PWM signal frequency is set to 20 kHz. Therefore, the voltage update period is 50 µs or an integer multiple of this value. The PWM generator is implemented using a counter clocked by a prescaler and digital comparator. The module features a 16-bit input port for the duty-cycle signal and a single-bit output port generating the PWM signal. The designed architecture provides a PWM resolution of 1000 discrete levels.

An additional input is included for the current limiting circuit. The PWM output signal is connected to an AND gate, the other input of which receives the inverted signal from the current limiting module. When the phase current exceeds the predefined threshold, the second input of the gate is forced low, thereby blocking the PWM pulses.

Synthesis results indicate a maximum PWM rising-edge delay of less than 5 ns relative to changes in the input control signal. This delay is mainly caused by the prescaler and the reduced clock frequency of the generator. Experimental measurements with the module connected to the FPGA I/O ports revealed a total propagation delay of 20.6 ns, as shown in Figure 3.



Figure 3. Measured input current limit flag (magenta) and output PWM waveforms (green).

The module has a two-bit incremental encoder input port and an 11-bit output port for the rotor angular position value. The module operates synchronously to a 10 ns system clock. On the synchronization pulse edge, the module checks for a change in encoder state, then determines the direction of rotation and updates the position counter.

The resulting rotor angular position value is transmitted via the output port. Detection of all state changes occurs in both channels at 360-pulse/rev and the system can detect

rotor position changes every 0.25 degrees. The delay time of the output signals relative to the input signals obtained during synthesis is 10 ns.

Experimental measurements, including the FPGA I/O port delays, revealed a total delay of 15 ns, as shown in Figure 4.

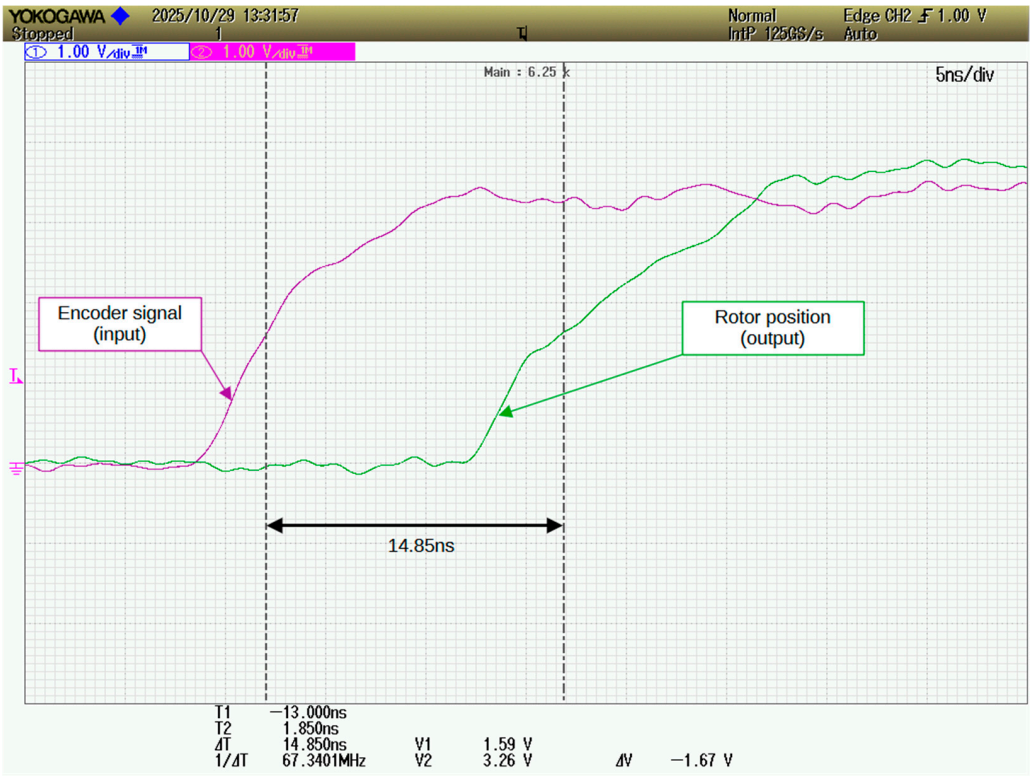


Figure 4. Measured output signal waveforms (green) after a rising edge of one encoder channel (magenta).

Assuming a rotor position detection frequency of half the system clock frequency (50 MHz) and a measurement resolution of 0.25 degrees, the module can theoretically operate at speeds exceeding 2.5 million rpm. Therefore, this module does not impose a limit on the maximum speed of the drive.

4.2. Instantaneous Speed Measurement Module

This module is implemented as a process within the rotation angle determination module and has a two-bit encoder signal input. The measurement is synchronised with the PWM signal period. The output of this module is a 16-bit port. The module counts the number of state changes of both encoder channels within 1 ms.

Theoretically, speed can be measured in a range from approximately 40 rpm to over 2.7 million rpm. The instantaneous speed signal is utilized by the controller module and can also be used, for example, to adjust calculations in the drive's mathematical model, depending on the control strategy. Since the instantaneous speed value is not used in the user interface, it is expressed directly as the number of encoder pulses per millisecond. This module does not restrict the controller's maximum operating speed.

4.3. Average Speed Measurement Module

The average speed measurement module processes output from the instantaneous speed measurement module by averaging the results over 256 measurements cycles. The display module then converts this value into rpm. This module does not affect the operation of the control chain. The average speed value is used in the user interface module only

to inform the operator of the current motor speed. Delays resulting from this module's operation are irrelevant to the control process.

4.4. Current Measurement Module

Infineon TLI4970 Hall-effect sensors with a serial SPI interface are used for current sensing. The measurement is performed with 13-bit resolution, and results are read as a 16-bit values. The sensor updates its output at a maximum frequency of 80 kHz. The phase current measurement module consists of three independent SPI interfaces clocked at 3 MHz.

The total time from the start of processing to the delivery of the measured values to the controller corresponds to the SPI transmission time, as the values are written to output buffers immediately upon completion of the transfer. Synthesis results indicate an output signal delay of 8 ns relative to the end of the SPI transmission. Experimental measurements showed a delay of approximately 5.9 ns, as shown in Figure 5. The maximum total time required to obtain a result, from the start of conversion to the end of transmission to the controller, is approximately 18 µs.



Figure 5. Delay in the current measurement path, from the edge of the CS signal of the SPI bus (green) to the end of transmission signal and averaging of the measurement results (magenta).

4.5. Voltage Measurement Module

An LEM LV-25P Hall effect sensor was used to measure the capacitor voltage. The sensor's output is digitized using a 12-bit ADCS7476 converter with an SPI interface. The measurement result, provided as a 16-bit value, is transmitted to a dedicated SPI interface in the FPGA at a clock frequency of 3 MHz. The 16-bit transmission cycle takes 5.3 µs. The delay of the voltage output signal on the 12-bit port relative to the end-of-transmission edge is shown in Figure 6, where the measured delay is approximately 8.4 ns. The maximum measurement frequency of this converter is 10 MHz. Therefore, the maximum delay in this module is approximately 5.4 µs.



Figure 6. Delay measurement in the voltage measurement module from the rising edge of the SPI bus CS signal (green) to the end of transmission and the results averaging signal (magenta).

4.6. Capacitor Voltage Control Module

The capacitor voltage control module manages the charging and discharging processes of the C-dump capacitor. This module utilizes setpoints for the minimum and maximum voltage values at which capacitor charging is enabled or disabled. These voltages depend on the speed. At speeds below the rated speed, the capacitor voltage is maintained near zero. At high speeds, it assumes values consistent with those calculated in the simulation program. These voltage values are supplied from the regulator module.

4.7. Controller Module

The controller is implemented as a dual-mode discrete PID structure using specialized hardware logic. The controller inputs receive the speed setpoint from the user interface and the actual speed from the instantaneous speed measurement module. The output signal below the rated speed is the duty cycle of the PWM signal of the phase supply voltage. Within this range, the commutation angle values can also be changed according to predefined dependencies.

Once the rated voltage is reached, the speed is regulated by a second PID regulator that sets the commutation angles. In the case of the C-dump converter, the capacitor charge and discharge voltages are also varied within this range, allowing for a wider speed control range. The capacitor charge and discharge voltage values are determined based on predefined dependencies on the rotational speed.

By implementing the regulator elements as specialised hardware structures, the delays introduced by the regulator were significantly reduced. The delays introduced by the regulators, obtained during module synthesis are 1.2 µs. The regulator is clocked according to the instantaneous speed calculation period, so the delay in the regulator does not adversely affect the drive's operation.

4.8. Output Decoder Module

The output decoder module operates based on the instantaneous rotor angular position, the output signals from the PWM generator module, controlled by the output of the first controller, and the phase power supply angular ranges obtained from the output of the second controller. In the case of the C-dump converter, the minimum and maximum capacitor voltage values are also used. This module is designed as an asynchronous decoder. Depending on the input signals, it controls the operation of the drivers that switch the transistors powering the motor phases. Delays in this module result from the signal propagation time through the structure and are 2.0 ns, according to the module's synthesis results. Measurement results for this module, after it was connected to the FPGA ports, are shown in Figure 7. The measurements indicate a propagation delay of 2.4 ns.

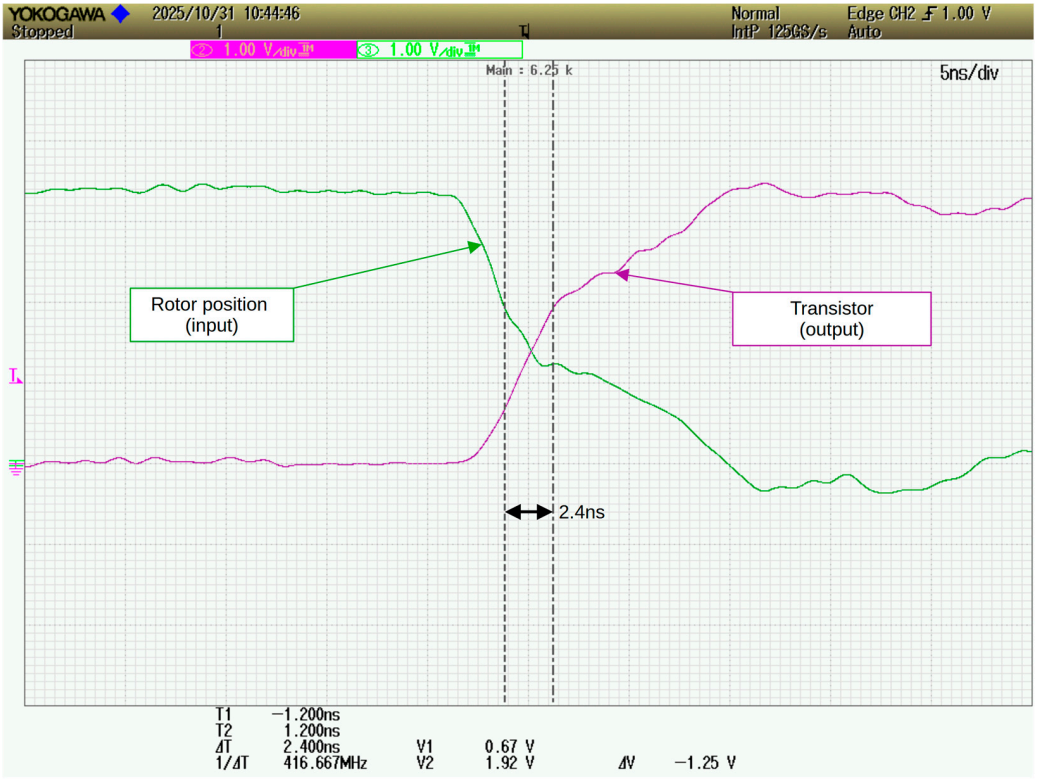


Figure 7. Delays of the signal changing the state of the output transistor after changing the rotor position—angular position signal (green) and output signal (magenta).

4.9. Interface

The user interface consists of a serial menu module and a display control module. The display module comprises a configuration section, activated when the controller is powered on, which sets the operating mode, and a section that allows viewing of selected parameters during controller operation. The module displays current control parameter values, such as speed, phase currents, supply current, voltages, and commutation angles. It uses parameter values measured in the control path modules. To edit drive operating parameters, a four-button serial menu is provided, allowing functions to be selected and then edited. After configuring the parameters, two dedicated buttons are used to control the motor: one for starting and one for stopping the drive. This module has no direct impact on the controller's operating speed because it operates fully concurrently.

4.10. Controller Synthesis

The controller was synthesised according to the block diagram shown in Figure 8.

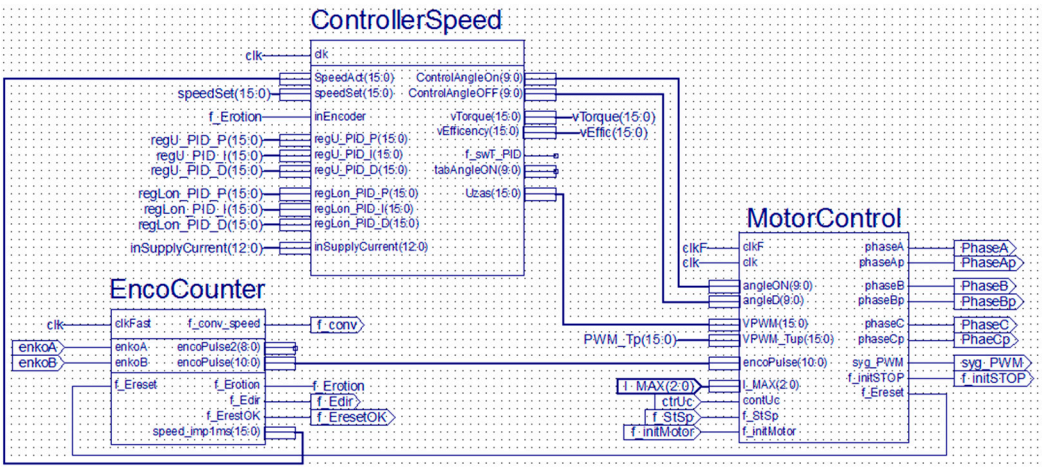


Figure 8. Functional diagram of the main signal path directly influencing the maximum speed of the drive.

Functional modules were developed based on an analysis of the system's operation. After testing the individual modules, the controller was synthesised. The most significant delays introduced by the control system originate from signal propagation paths between the encoder input and the outputs that controlling the phase supply transistors as the rotor angle changes. Another limitation is imposed by the PWM voltage period, which limits the controller's operating speed.

The maximum delay associated with signal propagation through the system from the encoder input to the outputs that control the motor phase power supply was determined during controller synthesis to be 15.6 ns. The measurement results of the output signal delays relative to the encoder signals are shown in Figure 9. This represents the fundamental limitation on the maximum speed at which the controller can operate.

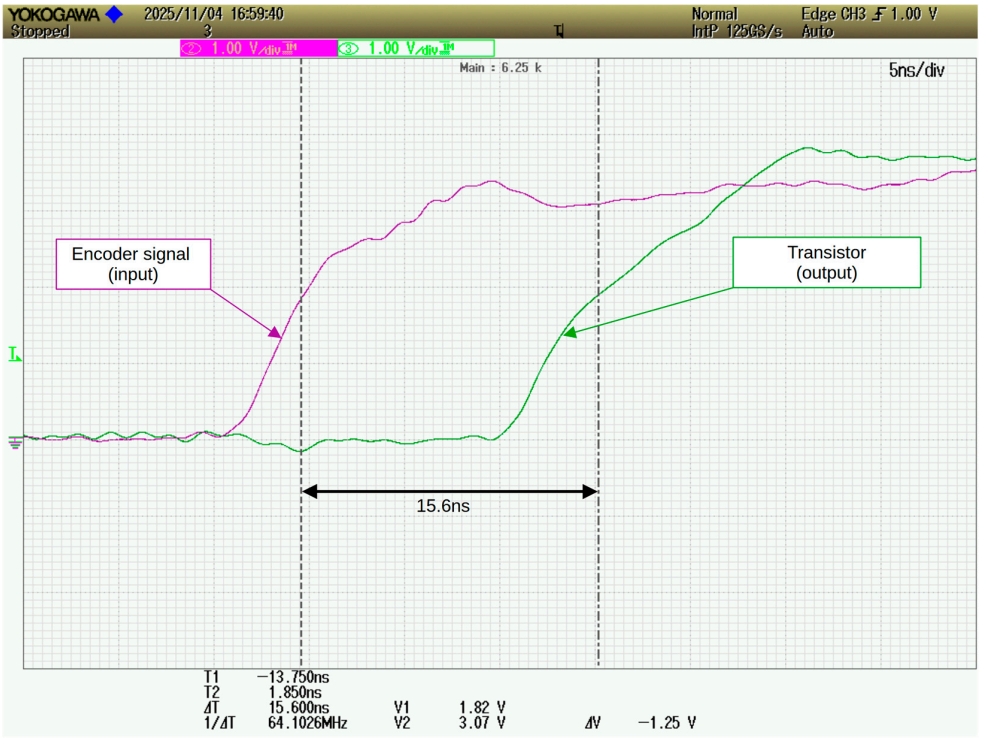


Figure 9. Delay time in the main signal path of the controller (input signal from the encoder—magenta, output signal controlling the transistor—green).

Since the encoder signal changes state 1440 times per rotor revolution, the minimum theoretical duration of a full revolution is 23 µs. Consequently, the controller can operate correctly, without reducing the angular position measurement resolution, at speeds of up to 2.5 million rpm. The maximum drive speed is primarily limited by the remaining drive components. Other modules, such as the PID controller, may operate at a lower update frequency.

The second critical element is the current limiting circuit. The total delay from the start of current measurement to PWM signal blocking is 45 µs. During this time, the current should not exceed the permissible value. Phase currents in high-speed motors increase rapidly due to the low inductance of the windings in these machines, as well as the increased supply voltage. Permissible delays in the current limiting circuit can only be determined for a specific motor and the power supply topology used. If the delays are excessive, it may be necessary to replace the current sensors.

Figure 10 presents the input and output propagation delays of individual controller modules as well as the delay of the critical signal path. The values were obtained from experimental measurements and synthesis results.

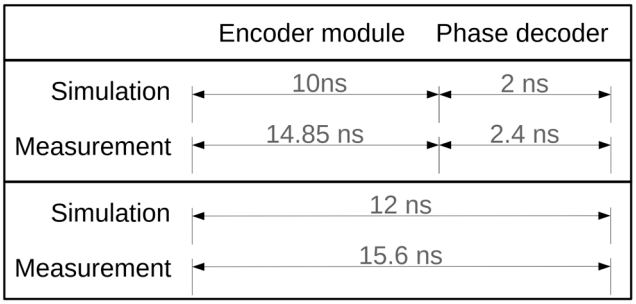


Figure 10. Input and output propagation delays of individual controller modules and the critical signal path, obtained from experimental measurements and synthesis results.

5. Peripheral Elements

The controller's operation was tested in a drive with a maximum rotational speed of 12,000 rpm. Therefore, typical actuators, such as drivers and IGBT transistors, were used. According to the manufacturer's specifications and the adopted algorithm and resolution of the rotor angular position measurement in the drive used for testing the developed controller, the maximum drive speed is significantly lower than the maximum controller speed. To increase the drive's rotational speed, faster transistor drivers can be employed.

In the tested drive system, a C-dump converter was used. The circuit employs IRGP4640DPbF IGBT transistors, for which the maximum turn-on and turn-off times are 53 ns and 115 ns, respectively (at 25 °C). The transistors are driven by IR2104 gate drivers, characterised by maximum propagation delays of 160 ns for the rising edge and 150 ns for the falling edge, along with maximum rise and fall times of 100 ns and 50 ns, respectively. The total maximum switching delay of the transistors relative to the control signals at the FPGA outputs is therefore 263 ns for turn-on and 365 ns for turn-off. This delay can be considered constant and independent of the rotational speed.

The accuracy of determining commutation angles, current limiting, and other controller modules was verified for a drive with a 750 W three-phase SRM motor. For this motor, the angular range of the phase feed was assumed to be constant at 30 degrees. The relationship between commutation angles and rotational speed was determined using a simulation program in the Matlab Simulink (2024b) environment [48].

The calculated dependencies of capacitor charging voltages and commutation angles were implemented in the controller as arrays, whose elements are interpolated using spline

functions. The tests demonstrated the correct operation of the voltage regulator, current limiting circuit, capacitor charging circuit, and phase power supply angle range determination.

As part of the testing of the commutation angle controller, phase current waveforms were measured for various commutation angle values. The obtained results were compared with the drive simulation results and are presented in Figures 11–13. In all cases, similar current waveforms were obtained, characteristic of different phase power supply angle ranges.

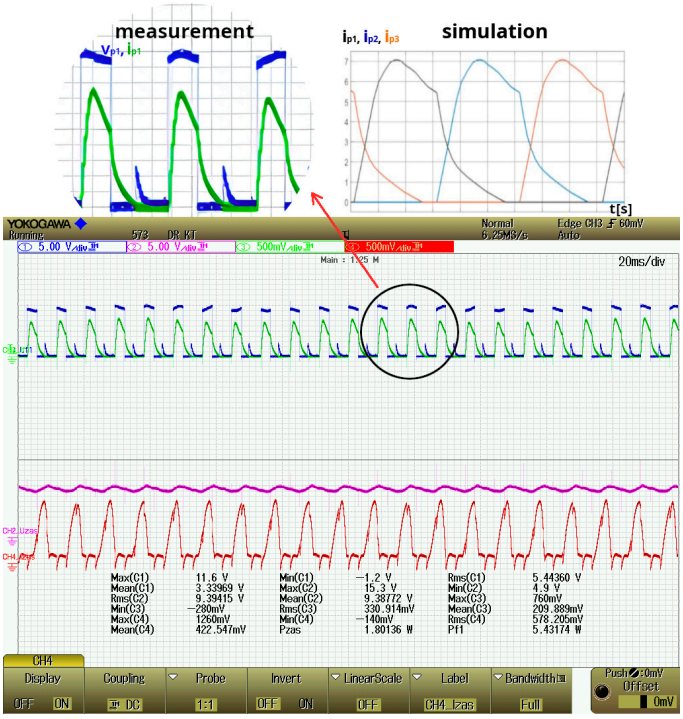


Figure 11. Phase current measurement (green i_{p1}) and simulation results ($\alpha_{off} = -17$ degrees, $\Delta\alpha = 30$ degrees).

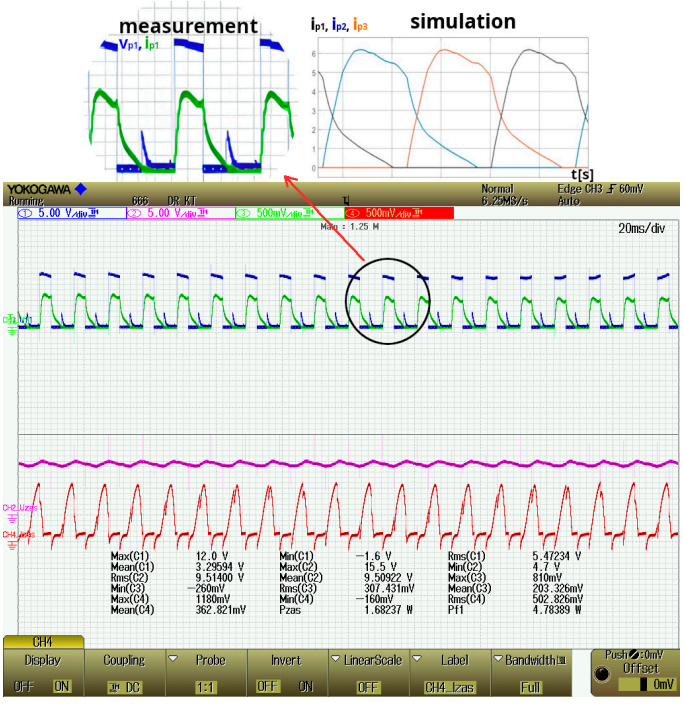


Figure 12. Phase current measurement and simulation results ($\alpha_{off} = -13$ degrees, $\Delta\alpha = 30$ degrees).

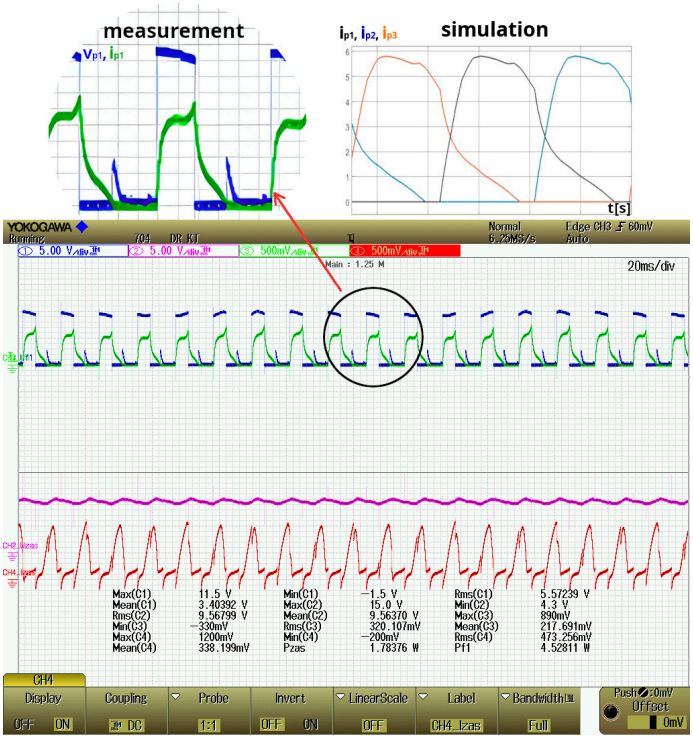


Figure 13. Phase current measurement and simulation results ($\alpha_{off} = -11$ degrees, $\Delta\alpha = 30$ degrees).

Measurements and calculations were made with the supply voltage reduced to 130 V and a load of 2.5 Nm.

6. Summary

As part of the research, an SRM motor controller based on an FPGA programmable logic device was developed. The project was designed for a drive with a C-dump converter, but after adaptation the controller can be used with SRM drives employing various types of converters.

A controller for C-dump converters is more complex than those for typical SRM drive systems. Additionally, it must control the charging and discharging process of the C-dump capacitor. Similarly to the process of determining the control signals for the transistors powering the phase windings, the control of the capacitor charging and discharging process must be implemented with high priority. While the process of controlling the phase power supply based on encoder signals is clocked by the edges of these signals, the capacitor voltage measurement process must be performed continuously. This means that the measurement results must be analysed immediately after the measurement is completed. In a microcontroller-based system, this limits the maximum execution speed of the control algorithm. Thanks to the use of an FPGA, the implementation of this functionality has little impact on the maximum speed, as it is implemented fully concurrently.

As part of the research, a functional analysis of the control system was performed. The signal delays introduced by the functional modules essential for high-speed control were analysed. As a result, the maximum delay introduced by the programmable logic device-based controller was determined and verified experimentally, thus directly addressing the scientific objective of this study.

By developing the controller as a concurrent hardware structure instead of a microcontroller program, the maximum signal propagation time through the system was limited to 15.6 ns. Within this time, all functions necessary for proper drive operation are executed. The tests were performed using a Spartan 7 FPGA clocked at 100 MHz. These results con-

firm that the proposed control architecture does not impose significant dynamic limitations on high-speed SRM operation.

Other modules, such as the user interface or serial interface, do not affect the speed of the control algorithm because they operate concurrently. Further expansion of the controller also does not significantly affect its speed, as long as the execution time of new functionalities does not exceed the maximum propagation time of the control signals through the system, as additional modules can be implemented concurrently. For example, it is possible to change the regulator type, implement the mathematical model of the drive, etc., without affecting the speed control range.

The main factor limiting the controller's maximum operating speed is the path for determining the phase power supply angle ranges, from the incremental encoder inputs to the transistor control outputs. This path also includes PWM voltage regulation, commutation angle regulation, phase current measurement, and the current limiting circuit, which, however, operate at a slower cycle. The achieved delay of 15.6 ns indicates that the controller can theoretically perform basic functions correctly at motor speeds up to 2.5 million rpm, meaning that the controller itself is not the speed-limiting factor. The measured total delay is smaller than the sum of the delays of the individual control path modules because it accounts for only a single connection between the control path and the FPGA output ports.

Nevertheless, when considering the transistor commutation times, in order to limit errors to the assumed rotor angular position resolution of 0.25 degrees, the maximum drive speed should be limited to 110 k rpm. For higher speeds, faster power electronic components may be required.

Additional functionality that significantly slows down microprocessor controllers, such as the measurement and analysis of the charge state of the C-dump capacitor, does not affect the maximum speed of the control algorithm implementation in the case of the FPGA controller.

If there are more complex calculations, the controller can be expanded with a microcontroller cooperating with the FPGA or the microcontroller can be implemented within the FPGA, to perform selected algorithm functions that are difficult to realise as hardware structures. The main advantage of the proposed FPGA-based solution remains the implementation of the control algorithm as specialised hardware modules operating concurrently.

Author Contributions: Conceptualization, D.R. and K.T.; methodology, K.T. and A.T.; software, D.R.; validation, D.R.; formal analysis, D.R.; investigation, D.R.; resources, D.R.; data curation, D.R.; writing—original draft preparation, D.R., K.T. and A.T.; writing—review and editing, K.T. and A.T.; visualization, D.R.; supervision, D.R.; project administration, K.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog-to-digital converter
α_{off}	Turn-off angle
BLDC	Brushless direct current (motor)
C	Capacitance

CS	Chip select signal
D_k, D_k'	Diode in the *k*-th phase branch
e_k	Electromotive force of phase k
FPGA	Field-programmable gate array
IGBT	Insulated gate bipolar transistor
L_k	Inductance of k-th phase winding
LCD	Liquid crystal display
PID	Proportional–integral–derivative
PWM	Pulse-width modulation
$\Delta\alpha$	Conduction angle range between turn-on and turn-off angles
R_k	Resistance of the k-th phase winding
ROM	Read-only memory
SPI	Serial peripheral interface
SRM	Switched reluctance motor
T_k, T_k'	Transistor in the k-th phase branch
UART	Universal asynchronous receiver-transmitter
V_s	Supply voltage

References

1. Kuss, H.; Wichert, T.; Szymanski, B. Design of a High-Speed Switched Reluctance Motor for Spindle Drive. In Proceedings of the Compatibility in Power Electronics (CPE 2007), Gdańsk, Poland, 29 May–1 June 2007; pp. 1–5. [CrossRef]
2. Araújo, R.E.; Camacho, J.R. (Eds.) *Modelling and Control of Switched Reluctance Machines*; IntechOpen: London, UK, 2020. [CrossRef]
3. Mahmoud, I.; Khedher, A. Special Use of Switched Reluctance Motors for Industrial Applications: Design and Electromagnetic Performance Evaluation. *WSEAS Trans. Syst.* **2025**, *24*, 472–485. [CrossRef]
4. Mecrow, B.C.; Jack, A.G. Efficiency Trends in Electric Machines and Drives. *Energy Policy* **2008**, *36*, 4336–4341. [CrossRef]
5. Bateman, C.J.; Mecrow, B.C.; Clothier, A.C.; Acarnley, P.P.; Tufftnell, N.D. Sensorless Operation of an Ultra-High-Speed Switched Reluctance Machine. *IEEE Trans. Ind. Appl.* **2010**, *46*, 2329–2337. [CrossRef]
6. Watkins, S.J.; Winward, E. Modelling and Control of an Ultra-High-Speed Switched Reluctance Machine. In Proceedings of the 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, UK, 19–21 April 2016; pp. 1–6. [CrossRef]
7. Kocan, S.; Rafajdus, P.; Bastovansky, R.; Lenhard, R.; Stano, M. Design and Optimization of a High-Speed Switched Reluctance Motor. *Energies* **2021**, *14*, 6733. [CrossRef]
8. El-Shahat, A.; Hunter, A.; Rahman, M.; Wu, Y. Ultra-High Speed Switched Reluctance Motor–Generator for Turbocharger Applications. *Energy Procedia* **2019**, *162*, 359–368. [CrossRef]
9. Aiso, K.; Akatsu, K. Performance Comparison of High-Speed Motors for Electric Vehicle. *World Electr. Veh. J.* **2022**, *13*, 57. [CrossRef]
10. Masoudi, K.; Feyzi, M.R.; Masoudi, A. Reduction of Vibration and Acoustic Noise in the Switched Reluctance Motor by Using New Improved Stator Yoke Shape. In Proceedings of the 21st Iranian Conference on Electrical Engineering (ICEE), Mashhad, Iran, 14–16 May 2013; pp. 1–4. [CrossRef]
11. Mukhopadhyay, S.; Mansani, S.; Sekaran, S. Advanced Speed Control Strategies for Switched Reluctance Motors: A Comprehensive Review. In Proceedings of the IEEE Silchar Subsection Conference (SILCON 2024), Agartala, India, 15–17 November 2024; pp. 1–6. [CrossRef]
12. Szymanski, J.; Kuss, H.; Wichert, T.; Kompa, K. Switched Reluctance Motor in Textile Machine Drive. In Proceedings of the IEEE Power Electronics Specialists Conference (PESC), Rhodes, Greece, 15–19 June 2008; pp. 2115–2117. [CrossRef]
13. Tang, Y.; He, Y.; Wang, F.; Kennel, R. Voltage-Sourced Converter Fed High-Speed Switched Reluctance Motor Drive System with Energy Feedback and Near-Unity Power Factor. *IEEE Trans. Ind. Electron.* **2022**, *69*, 3460–3470. [CrossRef]
14. Husain, I. *Electric and Hybrid Vehicles: Design Fundamentals*, 3rd ed.; CRC Press: Boca Raton, FL, USA, 2021. [CrossRef]
15. Ozer, K.; Yilmaz, M. Design and Analysis of a High Power Density Brushless DC Motor for a Multi-Rotor Unmanned Aircraft. In Proceedings of the 2021 12th International Conference on Electrical and Electronics Engineering (ELECO), Bursa, Turkey, 25–27 November 2021; pp. 378–382. [CrossRef]
16. Gao, B.; Cheng, Y.; Zhao, T.; Sun, H.; Cui, S. A Review on Analysis Methods and Research Status of Hysteresis Motor. *Energies* **2023**, *16*, 5715. [CrossRef]
17. Jagieła, M.; Garbiec, T.; Kowol, M. Design of High-Speed Hybrid Hysteresis Motor Rotor Using Finite Element Model and Decision Process. *IEEE Trans. Magn.* **2014**, *50*, 7021304. [CrossRef]

18. Li, S.; Xu, Q.; Wang, Q. Research on Global Temperature Rise Characteristics of Hysteresis Motor Based on Dynamic Loss Model. In *Proceedings of the 17th Annual Conference of China Electrotechnical Society; Lecture Notes in Electrical Engineering*; Springer: Singapore, 2022; pp. 27–37. [CrossRef]
19. Cai, Y.; El-Faouri, F.S.; Saikawa, N.; Chiba, A.; Yoshizaki, S. Magnetostriction Vibration and Acoustic Noise in Motor Stator Cores. *IEEE Trans. Ind. Appl.* **2024**, *60*, 6066–6078. [CrossRef]
20. Pawar, J.D.; Nikose, M.D. Control of Torque Ripple and Rotor Position for SRM (8/6-4 Phases) Using an Optimization-Based Model Predictive Torque Control. *Adv. Control Appl. Eng. Ind. Syst.* **2025**, *7*, e242. [CrossRef]
21. Xu, J.; Liu, Z.S. Optimum Design and Research of Switched Reluctance Motor for Electric Vehicle Based on Motor-CAD. *J. Phys. Conf. Ser.* **2023**, *2631*, 012009. [CrossRef]
22. Sial, M.R.; Sharma, O.; Dash, S. Integrated Modelling, Simulation, and Experimental Analysis of Multi-Algorithm Torque Ripple Reduction in Switched Reluctance Motor Drives. *Proc. Indian Natl. Sci. Acad.* **2025**, 1–28. [CrossRef]
23. Ehsani, M.; Fahimi, B. Switched Reluctance Motor Drives. In *Wiley Encyclopedia of Electrical and Electronics Engineering*; Webster, J.G., Ed.; Wiley: New York, NY, USA, 1999. [CrossRef]
24. Ma, B.; Liu, T.; Chen, C.; Shen, T.; Feng, W. Design and implementation of a sensorless switched reluctance drive system. In Proceedings of the Second International Conference on Power Electronics and Drive Systems, Singapore, 26–29 May 1997; Volume 1, pp. 174–180. [CrossRef]
25. Juarez-Leon, F.; Emery, N.; Bilgin, B. Acoustic Noise Reduction in an 8/6 Switched Reluctance Machine Using Structural Design. *Energies* **2023**, *16*, 3282. [CrossRef]
26. Reis, R.R.; Kimpara, M.L.M.; Galotto, L.; Pinto, J.O.P. Genetic Algorithm-Based Commutation Angle Control for Torque Ripple Mitigation in Switched Reluctance Motor Drives. *IEEE Access* **2023**, *11*, 97331–97339. [CrossRef]
27. Peng, S.; Yang, Y.; Li, R. Torque Ripple Suppression and Efficiency Optimization Methods for Switched Reluctance Motors. In Proceedings of the IEEE International Conference on Energy Internet (ICEI), Zhuhai, China, 1–3 November 2024; pp. 310–315. [CrossRef]
28. Asati, R.; Bankar, D.S.; Nehete, A.L. Torque Ripple Assessment of Converter Topologies for Switched Reluctance Motor. In Proceedings of the IEEE 3rd International Conference on Electrical Power and Energy Systems (ICEPES), Bhopal, India, 21–22 June 2024; pp. 1–6. [CrossRef]
29. Chaple, M.D.; Deotale, N.T.; Deotale, N.T. Torque Ripple Minimization in an 8/6 Switched Reluctance Motor Drive: Optimization Using the AZOA Method. *Aust. J. Electr. Electron. Eng.* **2024**, *22*, 27–44. [CrossRef]
30. Grbo, Z.; Vukosavić, S.N.; Levi, E. A Novel Power Inverter for Switched Reluctance Motor Drives. *Facta Univ. Ser. Electron. Energ.* **2005**, *18*, 453–465. [CrossRef]
31. Ismael, D.M.; Atyia, T.H. Comparative Evaluation of Speed Control Techniques for Switched Reluctance Motors in Industrial Applications. *Eng. Res. Express* **2024**, *6*, 032304. [CrossRef]
32. Dufour, C.; Cense, S.; Bélanger, J. FPGA-Based Switched Reluctance Motor Drive and DC–DC Converter Models for High-Bandwidth HIL Real-Time Simulator. In Proceedings of the 2013 15th European Conference on Power Electronics and Applications (EPE 2013), Lille, France, 2–6 September 2013; pp. 1–8. [CrossRef]
33. Saravanan, P.; Arumugam, R.; Kumaran, M.S. FPGA-Based Speed Control of SRM with Optimized Switching Angles by Self Tuning. *Circuits Syst.* **2016**, *7*, 1530–1545. [CrossRef]
34. Gorbounov, Y. FPGA-Based Generalized Switched Reluctance Motor Controller. *J. Eng. Res. Technol.* **2014**, *1*, 45–51.
35. Kandhasamy, S. Machine learning based SRM control using FPGAs for torque ripple minimization. In Proceedings of the 2020 International Conference on Artificial Intelligence in Information and Communication (ICAIIC), Fukuoka, Japan, 19–21 February 2020; pp. 675–680. [CrossRef]
36. Vijayan, S.; Paramasivam, S. Intelligent Speed Controller for a Switched Reluctance Motor Drive Using FPGA. *Int. J. Intell. Syst. Technol. Appl.* **2009**, *7*, 414–429. [CrossRef]
37. Babu, A.C.; Ashok, S.; Sandeep, J. FPGA-Based Speed Controller for 8/6 Switched Reluctance Motor Using Hysteresis Controller. In Proceedings of the 2019 2nd International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT), Kannur, India, 5–6 July 2019; Volume 1, pp. 962–966. [CrossRef]
38. Weiss, C.P.; Klein-Hessling, A.; De Doncker, R.W. Discussion on Control Structure Modifications Using an FPGA for Predictive DITC in Switched Reluctance Machines Regarding LUT Resolution. In Proceedings of the 2016 19th International Conference on Electrical Machines and Systems (ICEMS), Chiba, Japan, 13–16 November 2016; pp. 1–6.
39. Li, H.; Wei, Q.; Zhang, L.; Li, N. Suppression of torque ripple in switched reluctance motors which is based on synchronization technology. *EAI Endorsed Trans. Energy Web* **2024**, *11*. [CrossRef]
40. Fernando, W.U.N.; Barnes, M.; Marjanovic, O. Excitation Control and Voltage Regulation of Switched Reluctance Generators above Base Speed Operation. In Proceedings of the IEEE Vehicle Power and Propulsion Conference, Chicago, IL, USA, 6–9 September 2011; pp. 1–6. [CrossRef]

41. Diao, H.; Xia, H. Simulation and optimization for position servo control system of switched reluctance motor. *J. Phys. Conf. Ser.* **2023**, *2469*, 012018. [CrossRef]
42. Korkosz, M.; Bogusz, P.; Prokop, J. Complex Performance Analysis and Comparative Study of Very High-Speed Switched Reluctance Motors. *IEEE Trans. Magn.* **2019**, *55*, 8204714. [CrossRef]
43. Xiao, Y.; Pei, E.; Shi, L.; Peng, K.; Liu, W. Research on SRM Control Strategy for Looms Based on Multi-Algorithm Fusion. *J. Intell. Fuzzy Syst.* **2024**, *46*, 7933–7957. [CrossRef]
44. Lee, T.-W.; Yoon, Y.-H.; Kim, Y.-C.; Lee, B.-K.; Won, C.-Y. Control of C-Dump Converters Fed Switched Reluctance Motor on an Automotive Application. *Electr. Power Syst. Res.* **2007**, *77*, 804–812. [CrossRef]
45. Badhoutiya, A.; Yadav, K. Switched Reluctance Motor with C-Dump Converter. In Proceedings of the 2022 6th International Conference on Computing, Communication, Control and Automation (ICCUBEA), Pune, India, 18–20 August 2022; pp. 1–6. [CrossRef]
46. Gaafar, M.A.; Orabi, M.; Chen, H.; Dardeer, M. Fault-Tolerant Multilevel Converter for Multiphase Switched Reluctance Motor Drives Based on q+2 Converter. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA, 16–20 March 2025; pp. 906–911. [CrossRef]
47. Malekpour, H.; Rashidi, A.; Saghaian Nejad, S.M.; Lee, D.-H. Multi-Level Voltage High Fault-Tolerance Modular SRM Converter with Simultaneous Charge and Discharge Capability for HEV. *IEEE Access* **2025**, *13*, 127447–127461. [CrossRef]
48. Tomczewski, K.; Wróbel, K.; Rataj, D. The Influence of the C-Dump Converter on the Parameters of a Mains-Supplied Three-Phase SRM Drive. *Energies* **2025**, *18*, 5400. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.