

Article

Is GaN the Enabler of High-Power-Density Converters? An Overview of the Technology, Devices, Circuits, and Applications

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Abstract

The growing demand for electric vehicles, renewable energy systems, and portable electronics has led to the widespread adoption of power conversion systems. Although advanced structures like the superjunction *MOSFET* have prolonged the viability of silicon in power applications, maintaining its dominance through cost efficiency, *Si*-based technology is ultimately constrained by its intrinsic limitations in critical electric fields. To address these constraints, research into wide bandgap semiconductors aims to minimize system footprint while maximizing efficiency. This study reviews the semiconductor landscape, demonstrating why Gallium Nitride (*GaN*) has emerged as the most promising technology for next-generation power applications. With a critical electric field of 3.75 MV/cm ($12.5\times$ higher than *Si*), *GaN* facilitates power devices with lower conduction loss and higher frequency capability when compared to their *Si* counterpart. Furthermore, this paper surveys the *GaN* ecosystem, ranging from device modeling and packaging to monolithic ICs and switching converter implementations based on discrete transistors. While existing literature primarily focuses on discrete devices, this work addresses the critical gap regarding *GaN* monolithic integration. It synthesizes key challenges and achievements in the design of *GaN* integrated circuits, providing a comprehensive review that spans semiconductor technology, monolithic circuit architectures, and system-level applications. Reported data demonstrate monolithic stages reaching 30 m Ω and 25 MHz, exceeding *Si* performance limits. Additionally, the study reports on high-density hybrid implementations, such as a space-grade POL converter achieving 123.3 kW/L with 90.9% efficiency.

Keywords: circuit; converter; gallium; nitride; GaN; HEMT; monolithic; overview; wide-bandgap; survey



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1. Introduction

Power electronics (PE) has become one of the leading fields in engineering, driven by the ongoing digitization and electrification of modern infrastructure. Power conversion systems (PCS) are found in a wide range of applications, including server farms [1], electric vehicles [2], portable devices, household appliances, and renewable energy systems [3]. The growth of this field is fueled by the demand for higher energy efficiency, reduced system size, and the emergence of new technologies and topologies, such as those discussed in [4,5].

To illustrate the widespread use of power conversion systems, Figure 1 presents the architecture of a fully electric vehicle (EV). In this type of vehicle, two batteries are

used: a high-voltage (HV) battery that powers the traction motors, and a low-voltage (LV) battery from which various lower-voltage power buses are derived. The system includes an onboard battery charger (OBC) that enables external charging of the HV battery by converting the grid's AC voltage into the required HV DC voltage. The LV battery is charged from the HV battery via a DC-DC converter.

As shown in Figure 1, multiple vehicle subsystems are powered from the LV voltage rail. These include body electronics (BE), infotainment systems (INFO), and Advanced Driver Assistance Systems (ADAS). Each of these subsystems may use the LV supply bus to generate its specific required voltages. The electric traction motor is driven by an inverter that converts HV DC power into a three-phase AC voltage. This power architecture clearly demonstrates that numerous power conversions are necessary within such a complex system, with the majority being implemented using various topologies of switching converters (SC).

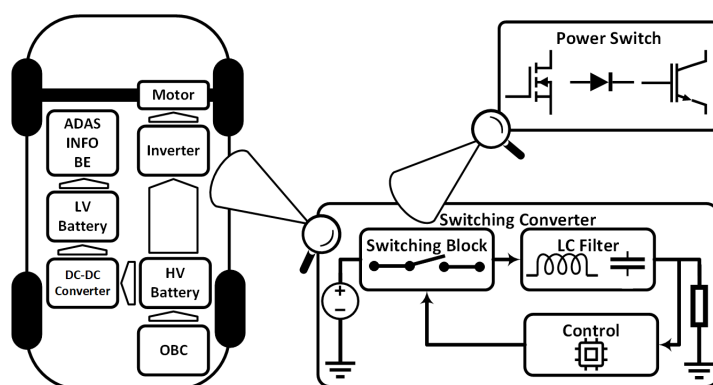


Figure 1. Representation of the abstraction hierarchy for power applications, from system level to semiconductor device level [6]. License Number 6167541103265.

The lower right side of Figure 1 shows a block diagram of a switching converter (SC). Its main functional components are the control circuit, the switching block (SB), and the output LC filter composed of reactive elements [7]. Among these, the switching block has the most significant impact on the system's overall efficiency. At its core is the power switch (PS), whose primary role is to control the flow of power through the reactive components. It operates in cycles, alternating between on and off states, driven by square-wave pulse signals generated by the control circuit.

An ideal PS turns on and off instantaneously, exhibits zero resistance when conducting, and blocks any voltage when turned off. In practice, however, PS devices are implemented using semiconductors that introduce several non-idealities, such as conduction resistance (R_{on}), finite switching time, limited drain-to-source breakdown voltage (BV), and, in the case of diodes, a non-zero forward voltage drop [7]. These deviations from ideal behavior result in power losses within the PCS, reducing overall efficiency. Additionally, limitations such as low BV and slow switching speed can restrict the range of applications for a given semiconductor device [8].

Most PSs are implemented using silicon (Si) devices due to their low cost and technological maturity. Si devices have advanced to the point where they can approach, or even surpass, the theoretical R_{on} and BV limits imposed by the material's physical properties as presented in [9], through structures such as the IGBT or superjunction MOSFET [10]. At present, the primary commercial competitors for the PS role are Silicon Carbide (SiC) and Gallium Nitride (GaN), both of which are wide bandgap (WBG) semiconductors. Their physical properties translate into higher theoretical material limits, allowing devices to reach higher BVs and lower R_{on} in the same, or even smaller, device area, whereas many advanced Si structures can approach similar performance only at the cost of significantly

larger area [11]. When compared with SiC, GaN transistors allow for higher switching frequencies, primarily driven by their lower parasitic capacitances [12]. The resulting reduction in passive component size contributes to a higher SC power density [13,14], supporting GaN's growing adoption in portable electronic devices [15,16] as well as in PCS for electric and hybrid vehicles [17] and data-centers [18].

Although multiple overviews and surveys on GaN technology have been published, they typically focus on device design, technology-specific effects, or targeted applications. With the emergence of GaN monolithic integrated circuits, a gap remains in the consolidated discussion of the key achievements and challenges associated with this topic. The scope of this paper is to introduce the challenges in the design of GaN integrated circuits by synthesizing the major advances that have enabled monolithic integration in GaN technology and its resulting benefits, as well as by examining the technology-specific characteristics that impact circuit design. Specifically, this work extends [6] and focuses on three main subjects related to GaN technology: (i) devices, including semiconductor technology, device structures, simulation models, and packaging; (ii) monolithic circuits, covering analog and digital design, power stages, and integrated SCs; and (iii) applications, spanning various application domains and PCS implemented with discrete transistors.

Several semiconducting materials are presented and compared, including Si, GaAs, SiC, and ultra-wide bandgap (UWBG) materials such as Aluminum Nitride (AlN) and β -Gallium Oxide (β -Ga₂O₃). While surveys on WBG technologies have been published [11], this work expands the existing literature by incorporating the physical properties of UWBG semiconductors, as they are expected to play a key role in the future of power electronics [19]. GaN is explored in detail by describing the evolution of the typical power device structure and synthesizing the performance data of various reported power transistors, emphasizing key advantages such as higher BVs in smaller device areas and improved current conduction enabled by $\approx 1.5\times$ higher electron mobility compared to Si [20]. Additionally, aspects related to the SPICE simulation model and packaging with high thermal efficiency and low parasitic elements are outlined.

Digital circuits represented through different logic gates families [21–24] and analog circuits, such as amplifiers [25] and comparators [26], are discussed while accounting for technological limitations, such as the absence of complementary devices and significant device parameter variations. Despite these challenges, monolithically integrated circuits, including power stages and integrated SCs, have been developed. GaN power stages can exhibit R_{on} values as low as 30 m Ω [27] and higher operating frequencies [27,28] compared to Si CMOS implementations [29]. For SCs, despite the technological constraints, control loops have been successfully implemented, enabling system efficiencies exceeding 95% [26,30,31].

A report of performance improvements offered by GaN transistors over their Si counterparts [32] applied to boost converters and a comparative analysis of Si, SiC and GaN devices used in buck converters [33] are used to support that WBG semiconductors are key enablers of the high efficiency and high power density required by emerging power conversion applications. A synthesis of multiple PCS that target fields such as high-performance computing in space [34], aircraft electrification [35] and EVs [36] is presented. These SCs achieve high power densities (e.g., this hybrid point-of-load (POL) [34] converter reaching 123.3 kW/L) and high power efficiencies (e.g., this three-level flying capacitor multilevel (FCML) converter [36] achieving 98.9%).

The remainder of this paper is organized as follows: Section 2 presents several semiconductor technologies in the context of power applications, emphasizing the physical characteristics that make them suitable for this field. Section 3 focuses on GaN technology, detailing the types of devices fabricated in this process, the simulation model developed

for the lateral device, and packaging solutions for emerging technologies. In Section 4, GaN monolithic circuit design is explored, addressing both digital and analog design challenges and summarizing the performance of various power circuits. Section 5 outlines the efficiency gains offered by GaN devices and synthesizes the application areas they have enabled, supported by representative design examples. In Section 6, the authors' forecast for the development of GaN technology is presented. Finally, Section 7 concludes the paper.

2. Semiconductor Technologies for Power Conversion Applications

The application's power rating and switching frequency dictate the choice of semiconductor device [8], as illustrated in Figure 2. For high power applications, Si thyristors are commonly used. In the medium- to high-power range, insulated-gate bipolar transistors (IGBTs) were traditionally the preferred choice. However, with the advent of SiC MOSFETs, the two technologies are now in competition. SiC MOSFETs offer several advantages, including an intrinsic body diode, whereas IGBTs require an external freewheeling diode on the printed circuit board (PCB) or integrated at the package level. Additionally, SiC devices support higher switching frequencies than IGBTs [37]. For low- to medium-power SCs, Si MOSFETs compete with both SiC MOSFETs and GaN High Electron Mobility Transistors (HEMTs). These wide-bandgap devices offer superior performance in terms of voltage-blocking capabilities and switching speed, typically in smaller packages. SiC MOSFETs are favored for their higher BV and thermal conductivity, while GaN HEMTs are preferred for their fast switching capabilities [38].

While several semiconductors are under active research for power electronics, GaN and SiC have already been adopted across a wide range of applications. The technology readiness map from 2023 presented in [39] projects the market shares of SiC and GaN by 2027. According to this forecast, SiC devices are expected to capture approximately 82% of the automotive and transportation market, whereas GaN devices are projected to reach 48% of the consumer electronics market and 31% of the telecommunications market. This distribution is driven by the widespread use of SiC in EV drivetrains and onboard chargers, while GaN has already achieved a dominant position in applications such as USB fast chargers.

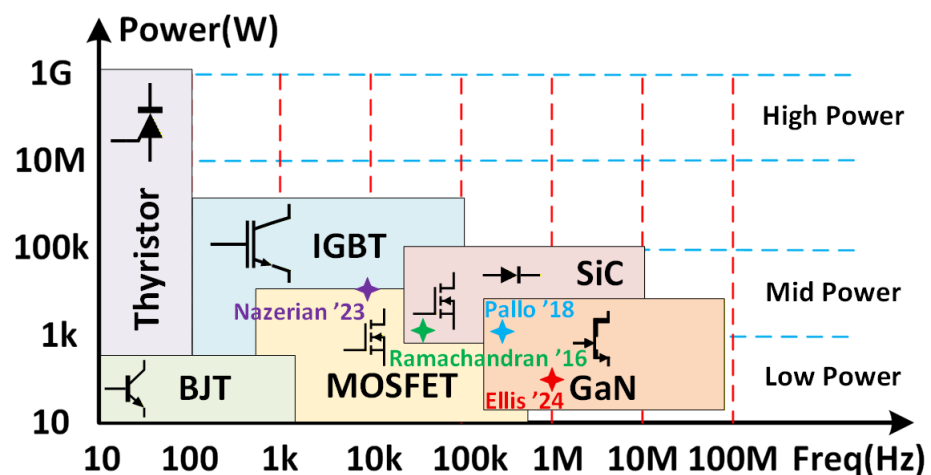


Figure 2. Power devices distribution across different power levels and switching frequencies [6]. Comparison based on power and frequency of power device applications from literature by: Ellis'24 [34], Pallo'18 [35], Nazerian'23 [36], and Ramachandran'16 [40]. License Number 6167541103265.

The feasibility of using emerging WBG semiconductors as PSs stems from their superior physical properties. These materials offer higher critical electric fields, wider bandgaps, greater thermal conductivity, and improved electron mobility. A summary of the physical

characteristics of various semiconductor materials is presented in Table 1 [41–45] with key parameters including band gap (E_g), dielectric constant (ϵ_r), carrier mobility (μ_n), critical electric field (E_c), electron saturation velocity (v_s), and thermal conductivity (k).

GaAs offers a higher μ_n of $8.500 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ compared to Si's $1.350 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$, making it a preferred material for high-frequency applications such as optical switches and RF devices [41]. However, its low k of $0.5 \frac{\text{W}}{\text{cm}\cdot\text{K}}$ limits its suitability for power applications. SiC, by contrast, is well-suited for high-power and high-voltage applications due to its $\approx 10\times$ higher thermal conductivity compared to GaAs and about $8\times$ higher E_c than Si. It also serves as a suitable substrate for GaN devices [41]. GaN surpasses all the aforementioned materials in terms of E_g and E_c , while also exhibiting higher electron mobility than both Si and SiC. As a result, GaN based devices are widely adopted alongside SiC devices in commercial PCS due to their technological maturity and performance [46].

For future power devices, UWBG materials such as AlN, $\beta - \text{Ga}_2\text{O}_3$, and diamond are currently under research [19,42–45]. As shown in Table 1, $\beta - \text{Ga}_2\text{O}_3$ offers promising characteristics compared to GaN, including an $\approx 2.1\times$ higher E_c and $\approx 1.4\times$ higher E_g , which could enable devices with even higher BVs in the future. AlN stands out with the highest E_c of $15.9 \frac{\text{MV}}{\text{cm}}$ among the listed materials, along with a high k of $3.21 \frac{\text{W}}{\text{cm}\cdot\text{K}}$, surpassed only by SiC and diamond. Among all presented semiconductors, diamond exhibits the best properties, with a $\approx 3.5\times$ higher μ_n , $\approx 2.7\times$ higher E_c , and about $\approx 18.7\times$ higher k compared to GaN.

Due to its higher μ_n , E_g and E_c compared to Si and SiC; while still being a mature technology unlike UWBG semiconductors, GaN is a strong candidate for implementing PSs. Its material properties allow the fabrication of devices that match or surpass the performance of their Si counterparts while occupying a smaller die area. The reduced device area lowers parasitic capacitances, enabling operation at higher switching frequencies. In turn, this capability supports significant increases in PCS power density, making GaN particularly suited for portable devices, as well as SCs for electric and hybrid vehicles and server farms. For these reasons, GaN technology was selected as the primary focus of this work.

Table 1. Physical properties for mature and research-grade semiconductors.

Material	E_g (eV)	ϵ_r	μ_n $\left(\frac{\text{cm}^2}{\text{V}\cdot\text{s}}\right)$	E_c $\left(\frac{\text{MV}}{\text{cm}}\right)$	v_s $\left(\frac{\text{cm}}{\text{s}}\right)$	k $\left(\frac{\text{W}}{\text{cm}\cdot\text{K}}\right)$
Si	1.12	11.7	1350	0.3	$1 \cdot 10^7$	1.5
GaAs	1.42	12.9	8500	0.4	$2 \cdot 10^7$	0.5
4H-SiC	3.23	9.66	900	2.5	$1.9 \cdot 10^7$	4.9
GaN	3.39	8.9	1265 *	3.75	$2.5 \cdot 10^7$	1.3
$\beta - \text{Ga}_2\text{O}_3$	4.9	10	300	8	$1.5 \cdot 10^7$	0.23 **
Diamond	5.47	5.7	4500	10	$2 \cdot 10^7$	24
AlN	6.1	8.5	500	15.9	$2 \cdot 10^7$	3.21

Notes: * $1265 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ in bulk, $2000 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ in 2DEG. ** 0.23 for [010] and 0.13 for [100].

3. GaN Technology

This chapter provides insight into the development of the standard GaN transistor structure and compares various lateral and vertical device implementations. It also covers specific aspects such as the simulation model proposed as the industry standard for this transistor and the packaging methods commonly used for these power devices.

3.1. GaN Devices

The first GaN transistors utilized a lateral Metal-Insulator-Semiconductor High Electron Mobility Transistor (MIS-HEMT) structure, as shown in Figure 3a. In this implementation, a dielectric layer is inserted between the gate and the two-dimensional electron gas (2DEG) formed at the GaN-AlGa_N heterojunction, resulting in a depletion-mode (d-mode) device. In such devices, the channel conducts by default, and electron flow can only be interrupted by applying a negative gate voltage, which repels charge carriers from the channel. Although these transistors offered performance advantages over their Si counterparts, their normally on behavior was considered unsuitable for PE applications due to safety and control concerns. An early commercial solution to this limitation was the GaN-Si cascode structure, which combined a low-voltage Si MOSFET with a high-voltage GaN d-mode HEMT to create a normally off, enhancement-mode (e-mode) configuration [32]. This approach also allowed for the integration of features such as gate driving and protection circuitry within the Si circuit [47].

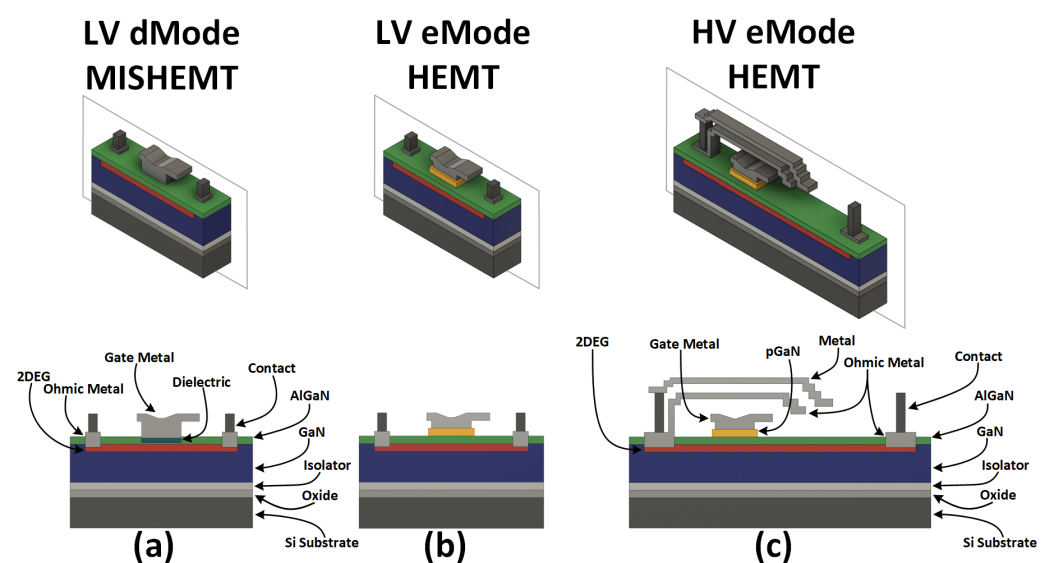


Figure 3. GaN Devices 3D Representations and Cross-sections: (a) MIS-HEMT (b) LV pGa_N gate HEMT (c) HV pGa_N gate HEMT (The figure is an extension of the representation from [48]).

To eliminate the need for additional components, various device-level modifications have been explored to create e-mode HEMTs. The most widely adopted solution is shown in Figure 3b, where a p-doped GaN layer is introduced beneath the gate. This forms a reverse-biased Schottky junction, which creates a depletion region that suppresses the 2DEG channel under zero gate bias, thereby achieving normally off behavior. To reach BVs in the range of 200 V to 650 V, a HV variant of the device is employed, as depicted in Figure 3c. In this version, the drain region is extended, and field plates are added to redistribute the electric field away from the gate. Another approach to developing devices that leverage the advantages of GaN semiconducting material while exhibiting higher BVs, currents, and reliability than HEMTs is the use of vertical structures such as [49,50].

The p-GaN gate HEMT exhibits a maximum gate breakdown voltage of approximately 7 V, while the recommended gate voltage for achieving low R_{on} is approximately 6 V. These values leave only a narrow operating margin. As a result, parasitic elements in the gate loop can lead to voltage overshoots, requiring additional PCB-level protection components such as clamps or series gate resistors. To mitigate time-dependent gate breakdown (TDGB), structural enhancements to the device have been proposed in [51], increasing the gate breakdown voltage from 10.5 V to 12.7 V at 25 °C and from 11.4 V to 13.4 V at 150 °C.

While the vertical architectures from [49,50] have successfully demonstrated breakdown voltages exceeding 1.2 kV in compact footprints, they rely on expensive native GaN substrates, which are typically limited to 100 mm diameter wafers. In contrast, utilizing Si substrates for 1.2 kV-rated power switches requires the growth of technologically challenging thick epitaxial layers [52], significantly complicating the fabrication process [53]. To address these manufacturing and cost constraints, industrial research has revisited the GaN–Si cascode topology as a practical interim solution [54,55]. Notably, reference [54] presents a 1.7 kV cascode transistor based on this approach, which has been qualified for automotive and industrial applications and offers a cost-effective alternative to SiC technology.

An initial obstacle that hindered the widespread adoption of GaN devices was the difficulty of growing large GaN crystals suitable for wafer production [41]. The high cost associated with native GaN substrates led to the use of alternative materials such as Si, sapphire, and SiC. Among these, Si is the most cost-effective option, SiC offers improved thermal conductivity at a higher cost, and sapphire is typically used in RF and optoelectronic applications of GaN devices. Recently, a technological breakthrough enabled the production of 300 mm wafers, a development that is expected to reduce GaN device prices in the long term [56].

To mitigate the crystal lattice and thermal expansion coefficient mismatch between the foreign substrates and the GaN/AlGaIn layers, a buffer layer is grown between these regions. For clarity, the buffer layer was omitted in Figure 3. An example of a step-graded AlGaIn buffer fabrication is shown in [57]. This approach aims to suppress carrier injection into the buffer, which can otherwise lead to punch-through at high blocking voltages. Further improvements in thermal and electrical performance can be achieved by doping the buffer layer with iron or carbon. Such doping increases buffer resistivity, thereby reducing carrier injection [57], and mitigates self-heating effects, which in turn limits drain current degradation caused by low heat dissipation [58].

A milestone in GaN device development is the realization of the dual-gate bidirectional switch (BDS) [59]. This device operates in four modes: it blocks current when both gates are unbiased, functions as a switch when both gates are biased, and acts as a rectifier when only one gate is biased (true for either gate). BDSs are especially useful in SCs such as matrix converters, an AC-AC converter topology that eliminates the need for a DC-link capacitor. Traditionally, the switches in these topologies are implemented using two anti-series connected devices, such as MOSFETs or IGBTs. The GaN BDS offers advantages such as reduced cost, area, and R_{on} , by utilizing a shared drift region. This innovation has already reached commercial availability [60].

Table 2 synthesizes multiple reported lateral and vertical devices. This GaN fin FET [50] offers $\approx 24\times$ more current conduction per area and $81\times$ lower on-resistance compared to the Current Aperture Vertical Electron Transistor (CAVET) reported in [49], while also reducing production cost by eliminating the need for epitaxial regrowth. The transistor reported in [52] exhibits the highest BV among the lateral devices but also an undesirably low threshold voltage of 0.64 V and $\approx 11\times$ higher R_{on} than the other works presented. Both Refs. [61,62] HEMTs have very low R_{on} values of $0.62\text{ m}\Omega \cdot \text{cm}^2$ and $0.8\text{ m}\Omega \cdot \text{cm}^2$, respectively. The device in [61] has the advantage of a high BV of 1000 V but suffers from low current conduction. In contrast, the device presented in [62] has a BV of 420 V and boasts the highest current conduction among the HEMTs, reaching 0.86 A/mm. Although [49] has demonstrated the possibility of co-integrating HEMTs and CAVETs, the lateral device structure is still preferred for GaN monolithic circuit design.

Table 2. Lateral and Vertical GaN Devices Comparison [6]. License Number 6167541103265.

Param. \ Work	[50] (V)	[49] (V)	[52] (L)	[61] (L)	[62] (L)
Type	Fin	CAVET	HEMT	HEMT	MIS-HEMT
Substrate	GaN	GaN	Si	SiC	SiC
Threshold [V]	1	−2.8	0.64	1.8	3
$R_{ON} \cdot A$ [$\text{m}\Omega \cdot \text{cm}^2$]	0.2	16.2	9	0.62	0.8
V_{BR} [V]	1200	201	1200	1000	420
I_{DS} [*]	25	1.08	0.18	0.35	0.86

Notes: L—Lateral, V—Vertical, * kA/cm^2 for V, A/mm for L.

In the case of commercial GaN transistors, performance is evaluated not only by current capability, maximum blocking voltage and R_{on} , but also by the parasitic capacitances (C_{iss} , C_{oss} , C_{rss}) and gate charge. For example, this 60 V GaN device [63] rated for 99 A, exhibits a C_{iss} of 1450 pF, C_{oss} of 700 pF and C_{rss} of 17 pF, while achieving an R_{on} of 1.3 m Ω at a gate voltage of 5 V. When compared to this Si MOSFET from the same manufacturer with the same voltage rating [64], the initial impression may suggest superior performance, as the Si device supports a higher current of 120 A and achieves a lower R_{on} of 1.1 m Ω . However, this resistance is obtained at a gate voltage of 10 V, and the device exhibits larger parasitic capacitances: $6\times$ higher for C_{iss} , $\approx 2\times$ higher for C_{oss} and $\approx 3.5\times$ higher for C_{rss} . These increased capacitances, together with the higher gate drive voltage requirement, lead to increased switching and driver losses and limit operation at high switching frequencies. A further advantage of the GaN device in this comparison is its smaller PCB footprint, occupying approximately half the area of the Si MOSFET.

Additionally, owing to the high bond strength of the material, GaN transistors exhibit promising characteristics for aerospace applications [65]. Because high energy is required to create lattice displacements, GaN is considered inherently radiation hardened; however, this property also depends on device design and material quality. The primary radiation effects observed in semiconductor devices include total ionizing dose (TID), displacement damage, and single-event effects (SEEs) [66]. In the case of p-GaN gate devices, threshold voltage shifts due to TID have been reported to be negligible after exposure to a total gamma dose of 1 Mrad (Si) [67]. Furthermore, due to the absence of a gate oxide, GaN HEMTs are expected to exhibit high immunity to TID effects. In [68], the displacement damage effects for a p-AlGaIn gate device were investigated. Since many satellites and space stations operate in low Earth orbit, where protons are the dominant source of radiation, the device was irradiated with protons at an energy of 5 MeV. Following irradiation, the device R_{on} increased from 1.89 m Ω to 5.29 m Ω , while the drain current was reduced by 50%. After thermal annealing at 400 °C, the device characteristics exhibited partial recovery. SEEs are of particular concern in power systems due to their potential to cause device degradation or catastrophic failure. SEEs occur when a high-energy radiation particle strikes a device, generating a track of electron-hole pairs that can induce transient disturbances, permanent parametric shifts, or instantaneous failure. In [69,70], commercial GaN transistors were subjected to irradiation, and their electrical characteristics were evaluated following SEE exposure. In both studies, high breakdown-voltage devices exhibited increased gate and drain leakage currents after irradiation. By contrast, the 40 V device reported in [69] showed lower charge amplification compared to the 100 V and 200 V devices, and no SEE-induced failure was observed for this device. While GaN technology

is still under active investigation for space applications, it shows potential, as evidenced by the release of radiation-hardened GaN products specifically targeting this domain [71,72].

3.2. GaN HEMT Model

Due to the structure of GaN transistors and the material-specific properties of GaN technology, standard SPICE models are inadequate for accurately capturing device behavior. The authors of [73] highlight key differences between MOSFET and HEMT devices, including significantly different transfer characteristics and a threshold voltage that exhibits weak temperature dependence in GaN HEMTs. To better reproduce the characteristics of HEMTs in circuit simulations, two main modeling approaches can be identified: a top-down approach, in which the device behavior is characterized and represented using implementations built from available SPICE devices or look-up tables, and a bottom-up approach, in which a physics-based compact model is developed.

In [74], the GaN transistor modeling using standard SPICE devices was investigated for a synchronous Buck converter. Although the simulated efficiency matched the measured results with an error of approximately 1%, this approach does not account for device-specific physical effects that can influence efficiency under practical operating conditions. Furthermore, empirical models based on fitting parameters or table-based representations become unreliable when extrapolated beyond the measured bias range.

To overcome these limitations, two industry-standard physics based models have been proposed: the Advanced SPICE Model for GaN HEMTs (ASM-HEMT), which is based on surface-potential calculations [75], and the MIT Virtual Source GaN-HEMT (MVSG) model, which is based on charge-based formulations [76].

In [75], HEMT-specific features incorporated in the ASM-HEMT model, such as access region resistance and field plates, are described. Its accuracy was validated by comparing simulation results with measured data for both RF and power devices. The same model was applied in [77] to a GaN–Si cascode PS, where it accurately reproduces device capacitance behavior while accounting for the effects of field plates.

The MVSG model presented in [78] employs a charge-based approach that simplifies the model formulation compared to ASM-HEMT, while maintaining numerical robustness. Its equivalent circuit is shown in Figure 4. The schematic illustrates five distinct regions of the device: the intrinsic transistor region under the gate, two field plate regions on the drain side that enhance the BV, and two access regions at the ends of the channel, modeled as implicit gate (gate voltage is V_{IG} on the schematic) transistors. The superimposed components in blue represent the modeled elements that define the device behavior. These components, implemented in Verilog-A, include: resistors modeling contact resistance; C_{GS} and C_{GD} modeling the gate-source and gate-drain capacitances; and $C_{GS,FP1}$, $C_{GD,FP1}$, $C_{GS,FP2}$, and $C_{GD,FP2}$ modeling the capacitances between each field plate and the source or drain.

This model accounts for phenomena such as access-region depletion, dynamic thermal behavior, and charge-trapping effects. Its accuracy was validated through simulations of an HV Buck SC and an RF power amplifier. In the Buck converter case, the model accurately predicted the slew rate of the half-bridge switching node, demonstrating its effectiveness in capturing transient behavior. Further enhancements to the MVSG model have been proposed to include the behavior of the Schottky p-GaN gate. The validity and accuracy of this extension were confirmed through comparisons with experimental data and TCAD simulations [79].

Although the charge trapping effect has been incorporated into various modeling approaches, its accurate measurement remains challenging, as it depends on factors such as blocking voltage, pulse duration, and temperature. This phenomenon leads to a dy-

dynamic R_{on} , which manifests as a temporary increase in conduction resistance following the blocking of a high drain voltage. An on-wafer double-pulse test method for this purpose is proposed in [80]. The ability to characterize devices before dicing is a valuable and time-saving feature, enabling faster design iterations during device development. In [81], device characterization and SPICE modeling methodologies for charge trapping are presented. Although the proposed approach relies on fitted parameters, the model that includes the dynamic R_{on} effect exhibits a maximum error of 22.4%, whereas the model without this feature shows an error of 86.9% when comparing simulated and measured R_{on} values.

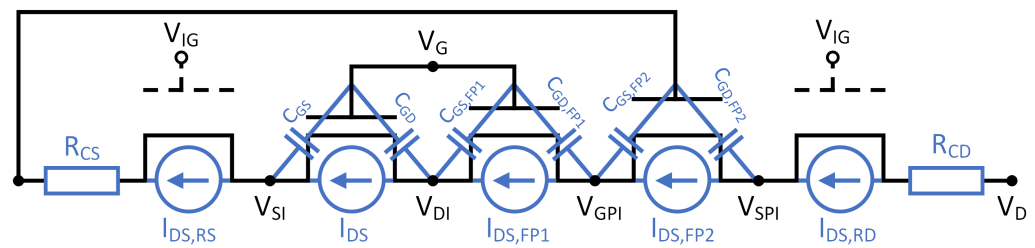


Figure 4. HEMT MVSG Model Equivalent Circuit.

3.3. GaN Packaging

The power losses in a PCS are converted into heat, which must be effectively dissipated to ensure reliable operation. As the temperature rises, the R_{on} of power transistors increases, leading to even greater power losses. Additionally, excessive temperatures can cause irreversible damage to the device, making thermal management a critical aspect of PCS design. While WBG devices deliver superior performance in smaller die areas, this miniaturization inherently limits heat dissipation. These thermal challenges are further intensified by the demand for higher system power densities and reduced PCB footprints, necessitating cooling solutions that do not compromise miniaturization.

To meet these requirements, chip-scale (CS) packages have been adopted for GaN devices [82]. This packaging style improves the package-to-die size ratio, reducing overall packaging costs, which helps compensate for the higher material costs of GaN, and enhances thermal performance by eliminating additional thermal impedances introduced by traditional package methods.

In [83], the thermal performance of commercial chip-scale GaN power transistors was compared to that of Si power MOSFETs housed in various packages. To ensure a fair comparison between the two technologies, Buck converters were developed using each device. When comparing a GaN HEMT to a MOSFET in a CanPAK package, both operating without additional cooling and under a 30 A load, the GaN-based system demonstrated a 35% reduction in power losses at a switching frequency of 300 kHz, and a 40% reduction at 400 kHz. When equipped with a heatsink, the SC using GaN achieves an output current of 30 A while operating at 100 °C, whereas its Si counterpart is limited to 20 A under the same thermal conditions. As a result, the GaN-based system delivers 50% higher output power at the same temperature.

Another advantage of CS packaging is the reduction in parasitic resistance and inductance. Thanks to the lateral structure of GaN HEMTs, there is no need for leadframes or bond wires to bring the drain, source, and gate terminals to the same plane. In contrast, Si power transistors typically use vertical structures, which place the drain and source on opposite sides of the die, requiring such interconnections. The reduced parasitic resistance helps further decrease R_{on} , while the lower parasitic inductance enables higher switching frequencies with minimized voltage ringing. Reduced ringing, particularly on the gate signal, is crucial, as excessive oscillation can damage the gate terminal [84].

While CS packaging improves the electrical performance of the device, it also presents disadvantages related to thermal management, as the limited area available for heat dissipation can lead to increased thermal stress. High operating currents may induce mechanical strain in solder bumps or even cause chip damage. For flip-chip packages, the influence of solder bump material and packaging method has been investigated through simulation in [85]. The results show that, due to its smaller size, the CS package experiences higher mechanical stress compared to a die directly attached to a copper substrate. Two solder bump materials, copper and aluminum, were evaluated, with aluminum exhibiting lower package stress under repeated temperature cycling. These simulation results are supported by measurements reported in [86], where a switching converter exhibits reduced efficiency at high load currents when employing a flip-chip packaged GaN IC.

Ongoing research focuses on advancing packaging methods for emerging semiconductor technologies. In [87], the authors propose replacing traditional bond wires with copper clips and sintered copper paste to improve thermal and electrical performance. Meanwhile, [88] explores embedding the GaN die directly into the PCB and positioning the decoupling capacitor as close as possible to the die, significantly reducing parasitic inductance. These findings highlight that advanced packaging techniques are essential for emerging power semiconductor technologies to minimize parasitic elements and enhance thermal conductivity. Despite its disadvantages, chip-scale packaging is currently the most prevalent solution, as it enhances performance by reducing thermal impedance and parasitic elements. This is achieved through the use of redistribution layers combined with solder bumps or copper pillars, which lower parasitic resistance and inductance while also providing an additional path for heat dissipation.

4. GaN Monolithic Integrated Circuits

The high switching frequencies targeted by GaN devices pose a challenge due to the parasitic inductances inherent in the packaging, bond wires and PCB traces. Such phenomena can induce voltage ringing on the gate of GaN power transistors, potentially leading to destructive overshoot. To address this issue, the first approach was to package GaN HEMTs with Si gate drivers to minimize parasitics. To further reduce these inductances, monolithic integration of the control circuits and power transistor has emerged as a solution [20]. This chapter presents the adopted digital and analog design techniques used in this technology and reports and compares the performances of multiple GaN monolithic circuits.

4.1. Digital Design

The initial step in developing GaN ICs involves designing suitable digital circuits. Since commercial technologies lack a p-type GaN device, primarily due to the added fabrication complexity and the $50 \div 100$ times lower transconductance [20], alternative logic families have been developed to overcome this limitation. These logic families primarily differ in their implementation of the pull-up (PU) network. The main types of logic families used in GaN ICs are presented in Figure 5 and respecting the notation from the figure they are described as follows: (a) Resistor-Transistor Logic (RTL): In this family, the load is a resistor [21], (b) Direct-Coupled FET Logic (DCFL): Here, the PU is a d-mode GaN device [22], (c) Pseudo-Complementary FET Logic (PCFL): In this family, the load is an e-mode device controlled by a signal complementary to the input, resembling a push-pull stage [23], (d1) Bootstrapped (BS) Logic: This logic family uses an enhancement-mode device as the PU, with its gate bootstrapped through a diode and a capacitor [24]. Due to its complementary control, the PCFL family has the lowest power consumption, while the BS family exhibits better noise margins with smaller devices when compared to DCFL [24]. Additionally, the enhancements to the BS logic family proposed in [89] are illustrated in

Figure 5(d2), and consist of the addition of a PD device and a resistor (highlighted in blue), which effectively reduce static current. However, this modification results in a slower rise time.

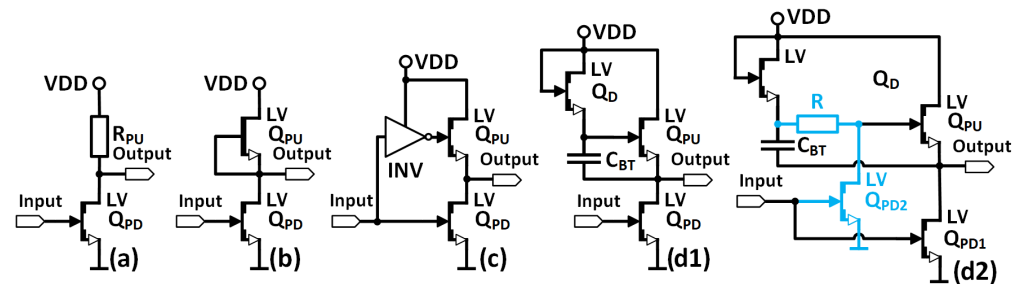


Figure 5. GaN Logic Inverter Families: (a) RTL, (b) DCFL, (c) PCFL, and (d1,d2) BS.

Even though the complementary GaN device demonstrates inferior performance compared to its n-type counterpart, novel approaches for its utilization have been proposed, such as in [90]. In this work, the complementary device is employed to block leakage current paths and reduce static power consumption. Moreover, the use of this hybrid topology leads to improvements in both fan-out and propagation delay.

When considered in the context of digital design in other IC technologies, commercially available GaN processes lead to logic families that resemble earlier solutions developed in Si NMOS/PMOS, Si BJT, or GaAs technologies. For example, processes that provide only e-mode devices may employ RTL style loads, BS loads, switched e-mode devices as dynamic loads, or biased e-mode devices operating in the linear or saturation region as active loads. In processes that include both e-mode and d-mode devices, DCFL can be implemented, which corresponds to ratioed logic in NMOS or PMOS technologies. Furthermore, when Schottky diodes are available, logic gates analogous to bipolar diode–transistor logic (DTL) or GaAs-style logic families can be realized [91–93].

4.2. Analog Design

Power stages and switching regulators often incorporate protection circuits, such as overtemperature, overcurrent, and overvoltage protection, which are typically implemented using analog blocks. Furthermore, as demonstrated in [26,30,31], control loops in SCs are also realized using analog techniques.

One challenge in GaN analog design stems from the absence of p-type devices. The lack of complementary transistors imposes several constraints: it necessitates the use of resistors as loads, limits current mirrors to sinking-only configurations, and restricts the input common-mode range of differential pairs. Given the p-type current mirrors unavailability, large-area resistors are used as loads when designing GaN-based amplifiers. As shown in [25], with only 20 dB per amplification stage, multiple stages of differential amplification are required to achieve a gain of 60 dB. A similar cascading approach is used in the comparator of the Buck converter presented in [26], where two amplifier stages are employed to attain a gain of 31 dB.

The common-mode limitation of e-mode n-type-only GaN technologies comes from the high positive threshold voltage of the devices. As a result, input signals below this threshold require level shifting. Two solutions have been proposed: in [26], diode-connected HEMTs are used in the comparator to shift the input voltage levels, whereas in [30], a switched-capacitor technique is employed for level shifting.

Crystal defects in GaN degrade device matching, imposing an additional constraint on analog design. In [20], the matching performance of various fundamental analog building blocks was evaluated. A resistive divider demonstrated a mismatch standard deviation of

$\sigma = 0.76\%$ between its resistors and an absolute resistance variation of $\sigma = 10.9\%$ across the wafer. These resistors are implemented using 2DEG channels formed from HEMTs without gates. However, due to back-gating effects in the upper device, its resistance is consistently higher than that of the lower device. Threshold voltage measurements reported in [32] show that standard HEMT structures exhibit a variation of $\sigma = 229$ mV, whereas structures with a modified gate reduce this variation to $\sigma = 63$ mV. These mismatches significantly impact analog circuits, especially differential pairs, resulting in input-referred offsets as high as ± 200 mV.

A solution to mismatches in current mirrors is the use of source degeneration, as resistors are expected to exhibit less variation compared to HEMTs due to the absence of the layers required to form the p-GaN gate [20]. This approach has been implemented in the level shifter of the power stage described in [94], although no data is reported regarding the accuracy of current matching. To address mismatch in differential stages, auto-zeroing and chopping techniques can be applied, as demonstrated in the comparator from [95], which successfully reduces the input offset from 112 mV to 1.2 mV.

Another physical effect observed in GaN e-mode HEMTs that can affect analog performance is positive bias temperature instability (PBTI), which manifests as a shift in the threshold voltage following positive gate-bias stress [96]. This effect results in hysteresis in the device transfer characteristics. Its impact has been investigated in the context of a comparator in [97], where it caused a shift in the input voltage at which the output transitions from logic high to logic low.

Similarly to digital design, analog circuit design in GaN technologies largely borrows from earlier approaches developed for NMOS and GaAs processes. For instance, the input stage of the GaN comparator presented in [98] resembles the architecture used in the GaAs comparator reported in [99]. A key difference between the two implementations is that the GaN circuit uses a resistor to bias the differential pair, whereas the GaAs design employs a depletion-mode device as a tail current source. A similar trend can be observed in operational amplifier design: although more complex, the GaN implementation reported in [100] adopts circuit techniques analogous to those used in earlier NMOS designs such as [101]. To date, experimental analog circuits based on truly complementary GaN devices have not been reported.

4.3. Power Circuits

To overcome the limitations imposed by parasitic inductance on the switching frequency of GaN transistors, monolithic integration of the driver and the PSs on a single die has been adopted, resulting in a power stage circuit. Various research implementations of such circuits are enabled by one or more of the previously discussed logic families. For example, the GaN half-bridge circuit in [94] employs a combination of RTL and PCFL, while the design in [21] exclusively uses RTL gates. Additionally, the commercial GaN IC presented in [102] is based on the BS logic gates family.

The characteristics of multiple power stages are summarized in Table 3. The IC detailed in [29] exhibits the slowest switching frequency and the highest R_{on} , serving as a reference Si power stage. The multi-die approach from [103], which combines Si control with GaN PSs, stands out among the listed circuits by achieving the lowest R_{on} at 4.4 m Ω , the highest drain current of 35 A, and the second-highest switching frequency of 10 MHz.

The power stage presented in [27] integrates switches with an R_{on} of 30 m Ω , the second-lowest value in the table, and supports a high switching frequency of 25 MHz. The design utilizes the modified BS logic gate family shown in Figure 5(d2) to enhance PU speed and reduce static power consumption. While it results in higher power consumption at lower frequencies, it achieves lower power consumption in the 25–30 MHz range com-

pared to a commercial Si driver. It also features a level shifter with high common-mode transient immunity, as well as an adaptive PD switch that prevents signal loss during freewheeling. The circuit presented in [104] employs a segmented, binary-weighted driver to control the voltage slopes of the gate and drain terminals. This approach effectively reduces gate voltage oscillations, thereby preventing the potential damage of this terminal. The power stage presented in [28] exhibits the highest dynamic power loss, due to its RTL driver implementation. Although this work does not propose a complex design, it compares the circuit's performance with simulation results based on the MVSG model for the HV device, showing a maximum error of 21.2% in the t_{ON} switching time parameter. In [94], a novel protection method for the high-side latch in the level shifter is proposed. The drivers are implemented using RTL gates that control two push-pull stages in a PCFL configuration, reducing power consumption in the stages with higher output current capability. Two different supply voltages are used to configure the resistance of the PU devices and mitigate voltage overshoots at the gates of the PSs. The commercial circuit in [102] employs the BS logic family and is the only GaN power stage that integrates a bootstrap switch for the high-side driver; all other implementations use an external diode. It supports a maximum operating current of 40 mA at 3 MHz, while the BS power stage from [27] achieves a current consumption of 20 mA at 5 MHz. The circuit also includes an undervoltage lockout block that enables operation only when the supply voltage exceeds a specified threshold.

Table 3. Integrated power stage circuits comparison

Param.	Work						
	[27]	[104]	[28]	[94,105]	[102]	[29]	[103]
V_{DD} [V]	5	12 ⁽¹⁾	6	6 ⁽²⁾	12	24 ⁽⁴⁾	5
Freq [MHz]	25	5	10	6.25	3	1.2	10
Area [mm ²]	2	-	4.75	6.6	10.2	-	-
Logic Family	BS	RTL	RTL	RTL, PCFL	BS	CMOS	CMOS
R_{HS} [mΩ]	30	80	-	500	14.5 ⁽³⁾	100	4.4
R_{LS} [mΩ]	30	80	67	500	14.5 ⁽³⁾	100	4.4
I_{DS} [A]	1.5	3	10	-	15	9	35
V_{DSMax} [V]	25	200	100	650	60	28	90
P_{Static} [mW]	100	-	-	-	21	60 ⁽⁵⁾	22.5
$P_{Dynamic}$ [mW@MHz]	≈200@25	-	2070@10	132@30	40@3	-	75@0.5

Notes: ⁽¹⁾ V_{DDLs} is 6.8 V and V_{DDHS} is 12 V. ⁽²⁾ V_{dd} is 6 V and V_{dd+} is 11 V. ⁽³⁾ In the previous datasheet version the value was 8.5 mΩ. ⁽⁴⁾ The voltage is internally regulated down to 5 V. ⁽⁵⁾ The type of power consumption isn't specified. Static power is assumed.

Another promising type of power circuit for GaN monolithic integration is the switching regulator, which is a system that incorporates a power stage and a control loop. Multiple Buck SCs have been reported [26,30,31].

The circuit presented in [30] is realized in an e-mode 650 V GaN technology, occupies an area of 2.1 mm² and achieves an efficiency of 95.6% for an input of 85 V. The control loop operates in boundary conduction mode. It integrates a zero voltage detector (ZVD) and reads the output current through a shunt resistor. When the switching node reaches zero volts, the driver control signal is set high, and when the current reaches a peak value

determined by an external voltage reference, the signal is set low. This way, the average current is set by the reference voltage.

A GaN buck converter for server POL applications is proposed in [31]. It is designed in a 200 V GaN-on-SOI technology, and for a load of 3 A and a switching frequency of 250 kHz, it achieves an efficiency of 84.3% when stepping down from 48 V to 1 V. The integrated feedback loop employs voltage mode control.

In this work [26], a SC fabricated in a 650 V GaN technology is presented. The circuit converts from 400 V to 48 V, occupies an area of 16.25 mm², and achieves an efficiency of 93.1%. A peak efficiency of 95.5% is reached when stepping down from 250 V to 125 V. The converter employs a constant-on-time (COT) control method and integrates a ZVD, which enables soft switching of the low-side transistor. Using this circuit, a 5.5% efficiency improvement is reported compared to operation with the ZVD disabled. The minimum on and off times of the control loop are trimmed using 5-bit and 3-bit resolution, respectively, through adjustment of a binary-weighted capacitor bank. The power stage can operate at frequencies up to 3.5 MHz, but the COT controller is capable of generating control signals only up to 1.7 MHz.

5. GaN Power Converters Evaluation

This section presents a synthesis of reported efficiency improvements in PCS driven by replacing Si devices with GaN HEMTs, complemented by a review of SCs architectures designed to maximize power density using this technology.

In [32], the authors evaluate the performance improvements offered by GaN transistors over their Si counterparts in Boost converters, considering both non-synchronous and synchronous topologies. While the Si-based non-synchronous converter reaches a peak efficiency of 98.2% at 500 kHz, the GaN implementation demonstrates superior performance, achieving 98.5% peak efficiency and maintaining a flatter efficiency curve at heavier loads. Similarly, in the synchronous Boost topology operating at 100 kHz, the synchronous Boost converter with Si switches was limited to 2.4 kW output due to thermal constraints, peaking at 97% efficiency. The GaN-based equivalent, however, delivered 37.5% more power and maintained 99% efficiency across a 1.4 kW to 2.9 kW load range.

The comprehensive comparative analysis presented in [33] evaluates Si, SiC, and GaN implementations within a synchronous Buck converter topology, operating with an input range of 140–240 V and a 48 V output. The goal was to identify the optimal device technology for maximizing both efficiency and power density. Three configurations were analyzed: Si MOSFET and diode, SiC JFET with SiC Schottky diode, and GaN transistor paired with SiC Schottky diode. The results show that, across the full input voltage range, the hybrid GaN-transistor/SiC-Schottky implementation achieved the highest performance, with peak efficiencies of $\approx 97\%$ at 100 kHz and $\approx 96\%$ at 200 kHz. It was closely followed by the SiC-JFET/SiC-Schottky combination, which reached about $\approx 96.5\%$ and $\approx 96\%$ at the same frequencies. In contrast, the Si-based implementation achieved only around $\approx 90\%$ efficiency at 100 kHz and dropped to $\approx 82\%$ at 200 kHz.

Synthesizing the findings from the aforementioned studies [32,33], it confirms that GaN and other WBG semiconductors are key enablers for attaining the high efficiency and power density demanded by emerging power conversion applications. Multiple SC implementations using discrete GaN devices that meet these demands are synthesized in Table 4. These systems target applications such as power delivery systems for high performance computing in space [34], aircraft electrification [35] and EVs [36]. Moreover, these PCSs are represented in Figure 2 as a function of output power and switching frequency, placing them within the broader context of the power semiconductor landscape.

In [34], the authors present a high conversion rate POL converter developed for space applications, enabled by GaN's inherent radiation hardening. The design can output a maximum of 50 A at $\approx 86\%$ efficiency while keeping a steady temperature of 58°C under forced air cooling. The reported peak system efficiency is 90.1%.

The inverter developed in [35] targets aircraft electrification. A FCML topology was selected to reduce both power loss and system weight. Through this architecture, although the switching frequency is 120 kHz, the effective ripple frequency at the inductor input reaches 960 kHz, allowing the use of two 10 μH inductors that occupy less PCB area. The system achieves the second-highest power density among the surveyed works at 35.3 kW/L, while reaching a peak efficiency of 98.6%.

The isolated bidirectional converter presented in [40] achieves a peak efficiency of 98.8% in both buck and boost modes. To further improve system efficiency, the authors designed custom wound inductors and a transformer for the prototype. Although the converter height is not reported, preventing a precise power-density calculation, the prototype delivers 1.7 kW of power while occupying a PCB footprint of $14.3\text{ cm} \times 7.7\text{ cm}$.

An FCML topology is also employed in the DC–DC SC presented in [36] for EV applications. Similarly to the FCML inverter in [35], this architecture results in the inductor input being switched at twice the fundamental switching frequency, enabling a reduction in inductor size. This converter exhibits the highest inductor size and lowest power density, with a value of 16.54 kW/L, but has a high output power target of 10 kW, while also having the highest input and output voltages from the selected papers.

Table 4. Power Converters Comparison

Param.	Work			
	[34]	[35]	[40]	[36]
V_{In} [V]	48	1k	130	650–800
V_{Out} [V]	1	353 RMS	52	350–450
I_{Out} [A]	50	40	32	-
P_{Out} [W]	50	9.7 k	1.7 k	10 k
Freq [Hz]	1M	120 k	50 k	40 k
Peak Efficiency [%]	90.1	98.6	98.8	98.9
Power Density [kW/L]	123.3	35.3	-	16.54
Topology	HSCC POL ⁽¹⁾	FCML Inverter	Iso FB Bidi ⁽²⁾	3L FCML ⁽³⁾
L [μH]	$2 \times 78\text{ nH}$	$2 \times 10\text{ }\mu\text{H}$	10.2 μH	110 μH
Switch	EPC2070 EPC2216 EPC2066	EPC2034	EPC2010C	V22C65S1A

Notes: ⁽¹⁾ HSCC—Hybrid Switched Capacitor Converter, POL—Point-of-Load. ⁽²⁾ 3L FCML—Three-Level Flying Capacitor Multilevel. ⁽³⁾ Iso FB Bidi—Isolated Full-Bridge Bidirectional.

Beyond the already mentioned applications, GaN-based converters are now used in satellites, augmented-reality systems, and robotics [32]. A common thread across these fields is the need for small footprint and energy-efficient power conversion: portability implies battery operation and strict space and thermal constraints, as in robotics

and drones [106], while satellites require compact electronic systems with radiation tolerance [107].

Driven by the inherent advantages of monolithic integration discussed in Section 4, together with the demonstrated superiority of discrete GaN transistors over their Si counterparts highlighted in this section, single chip GaN power integrated systems represent an important milestone in the evolution of the technology, with commercial products already available [102,108].

6. Discussions

The author's forecast for the development of GaN technology is outlined in the following paragraphs. In the case of discrete devices, the advancement of 300 mm GaN wafers is expected to enable the fabrication of vertical devices capable of withstanding BVs exceeding 1200 V. These devices will compete with IGBTs and SiC-based components, positioning GaN technology within the mid- to high-power range of the power semiconductor spectrum.

For IC technologies, GaN-based solutions are anticipated to incorporate a broader variety of devices, including fuse elements, which would allow on-chip parameter calibration directly within the power stage, eliminating the need for external Si-based circuitry. Device structures will be optimized for both cost and electrical performance, with particular attention to parameter variation and manufacturing yield. Furthermore, as reported by Intel in [109], hybrid integration of Si and GaN is feasible, suggesting that growing HEMT power devices directly on a Si driver could become a practical approach.

At present, monolithic GaN power stages have gained traction in portable applications such as chargers, drones, and robots. However, wider adoption is anticipated in data center servers and in hybrid or fully electric vehicles, particularly for DC-DC converters between the system's HV and LV batteries. Upon the commercial release of devices with a BV of 1200 V, GaN is expected to be adopted in traction inverters and OBCs as well.

Due to the small form factor of GaN devices and the benefit of enabling smaller reactive components, we can expect to see a rise in compact system-in-package (SiP) designs. Regarding packaging, CS packages are widely used across semiconductor technologies due to their low cost, small footprint, reduced parasitics, and good thermal conduction. Thermal performance can be enhanced by adding thermal pads that facilitate the attachment of heat sinks. A potential implementation has been investigated in [110], where the backside of the die is removed to allow filling with a high thermal conductivity material, such as copper. A similar approach was investigated in [111], where backside copper filling resulted in a temperature reduction of 22 °C. This reduction mitigated self-heating effects and led to a 26% improvement in the transconductance of the HEMT. This technique could be applied to both SiPs mounted on PCBs and chips employing CS packaging.

7. Conclusions

This paper presented the need for efficient, high-power-density PCS. It showed that, while Si is currently used across a wide range of power applications, its performance is fundamentally limited by its physical properties. As alternatives, several semiconductor technologies were discussed, including WBG and UWB materials, with a focus on GaN. By reviewing key advancements in GaN technology, spanning fabrication processes, device design, compact modeling, packaging, circuit implementation, and converter architectures, this work demonstrated its suitability for next-generation power electronics. Through its high switching frequency, small footprint, and low R_{on} , GaN technology has been shown to meet the demands for high efficiency and power density in applications such as portable chargers, electric vehicles, and satellites. This was supported by reported performance examples, such as a monolithically integrated GaN buck converter achieving 95.4% peak

efficiency when stepping down from 250 V to 150 V, and a synchronous boost converter using discrete GaN transistors, which delivered 37.5% more power while maintaining 99% efficiency. GaN devices have also enabled switching regulators for fields such as high-performance computing in space and aircraft electrification, and have improved the feasibility and cost-effectiveness of topologies like the matrix converter. Thus, GaN power devices, through their superior physical properties, have surpassed Si in low- to mid-power applications. With continued technological advancements, GaN could compete with SiC in the mid- to high-power range and approach its theoretical limits, eventually to be surpassed by emerging UWBG materials.

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Abbreviations

The following abbreviations are used in this manuscript:

ADAS	Advanced Driver Assistance Systems
AlN	Aluminum Nitride
BDS	Bidirectional Switch
BE	Body Electronics
BS	Bootstrapped
BV	Breakdown Voltage
CAVET	Current Aperture Vertical Electron Transistor
COT	Constant-On-Time
CS	Chip-scale
DCFL	Direct-Coupled FET Logic
DTL	Diode-Transistor Logic
EV	Electric Vehicle
FCML	Flying Capacitor Multilevel
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMTs	High Electron Mobility Transistors
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
INFO	Infotainment
LV	Low Voltage
MIS-HEMT	Metal-Insulator-Semiconductor HEMT
MVSG	MIT Virtual Source GaN-HEMT
OBC	Onboard Battery Charger
PCB	Printed Circuit Board

PCFL	Pseudo-Complementary FET Logic
PCS	Power Conversion System
PD	Pull-Down
PE	Power electronics
POL	Point-Of-Load
PS	Power Switch
PU	Pull-Up
RTL	Resistor-Transistor Logic
RF	Radio Frequency
SC	Switching Converter
SB	Switching Block
SEE	Single-event Effect
Si	Silicone
SiC	Silicone Carbide
SiP	System in Package
TID	Total Ionizing Dose
UWBG	Ultra Wide Bandgap
WBG	Wide Bandgap
ZVD	Zero Voltage Detector

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