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Analysis and Phase Selection of a Three-Inductor Interleaved Parallel Converter with a Scalable Voltage Multiplier

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Abstract

High-step-up interleaved converters are usually phase-shifted to cancel the sum of their inductor currents. In the three-inductor converter studied here, one inductor reaches the source through a series switch, so the source current is not that sum. This paper analyzes the converter with a scalable voltage multiplier of N cells. It derives the gain $(2N + D)/(1 - D)$ for duty ratio D, the device-stress and current-sharing laws, a phase-displacement rule that minimizes the AC RMS current at the source terminal, and gain and boundary laws for mixed continuous and discontinuous conduction. A charge-transfer-aware loss model and a sampled-data current/voltage controller are evaluated at six 400 V operating points. All results are numerical and are cross-checked in PLECS and two independent solvers. At 15 V and 100 kHz, reducing the phase displacement from 180° to 72° lowers the source AC RMS current by 4.75% and doubles the ripple of the two continuously connected branches. Estimated efficiency is 85.7–93.6%. The controller is locally stable at every evaluated point, including ±20% inductance and capacitance changes, and the analysis identifies the multiplier resonance that sets its margins at 24 V input. Source-current quality, component stress, and control stability must, therefore, be assessed separately, and at the physical source terminal. Analytical and numerical study of source-current phase selection, scalable voltage gain, discontinuous-conduction boundaries, device losses, and sampled control in an interleaved parallel converter.

Keywords: DC–DC conversion; interleaved converter; voltage multiplier; phase selection; discontinuous conduction; sampled-data control

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1. Introduction

Photovoltaic modules, batteries, and fuel cells deliver tens of volts, whereas DC distribution buses and inverter DC links operate near 400 V. The interface converter must, therefore, provide a gain of roughly 15–35 at input currents of tens of amperes. A conventional boost converter reaches such gains only at extreme duty ratio, where conduction loss, diode reverse recovery, and switch voltage stress become limiting. Several families of nonisolated high-step-up converters address this limit. Voltage-multiplier cells extend the gain of nonisolated DC–DC converters while distributing device blocking voltage [1–4]. Switched-inductor networks [5,6] and coupled-inductor converters [7–12] add gain through the magnetic elements, at the cost of leakage-energy management. Differential-output and hybrid structures combine these mechanisms [13–15]. Interleaved branches distribute the input current [16,17], and interleaving is now routinely combined with multiplier cells or coupled inductors [18–22]. Charge-transfer models connect multiplier loading to capacitance and resistance [23].

Table 1 compares the present converter with interleaved high-gain converters published between 2024 and 2026. The entries for the cited converters are the values reported by their authors for hardware prototypes under their own test conditions. The entries for this work are numerical. The present converter uses no coupled inductor, its gain is scaled by the cell count N, and its switch stress is $V_o/(2N + D)$. It uses a third switch with a floating driver, and its source current contains the gated current of one branch, which is the subject of this paper.

Table 1. Comparison with interleaved high-gain converters published in 2024–2026. S, D, and C are switch, diode, and capacitor counts; L is an uncoupled inductor and CI a coupled inductor; n is the turns ratio; FL is full load; n.q. means not quantified in the source.

Converter	Gain V_o/V_{in}	S	Magnetics	D	C	Switch Stress	Reported Operating Point	Efficiency (%)	Input-Current Ripple
[18]	$3/(1-D)$ [a]	2	2 L	3	3	$V_o/3$	25 V to 159 V, about 150 W, 50 kHz	97 at 150 W	Reduced by interleaving, n.q.
[19]	$5/(1-D)$ [a]	2	2 L	5	5	55 V at 270.5 V	25 V to 270.5 V, 50 kHz	96 peak	About 0.3 A on 4.22 A
[20]	$(3n+2)/(1-D)$	2	2 CI (three windings)	8	7	$V_o/(3n+2)$	36 V to 400 V, 1 kW	90.4 FL, 97.4 peak	3.6 A
[21]	$(3n+2)/(1-D)$	2	2 CI	5	5	$V_o/(3n+2)$	36 V to 400 V, 1 kW	92.0 FL, 95.7 peak	About 3 A
[22]	$(2n+4)/(1-D)$	2	2 CI	4	4	$V_o/(2n+4)$	28–33 V to 400 V, 400 W	97.2 FL, 97.4 peak	Reduced by interleaving, n.q.
This work	$(2N+D)/(1-D)$	3	3 L	$2N+1$	$2N+1$	$V_o/(2N+D)$	12–24 V to 400 V, 400–800 W (numerical)	85.7–93.6 (calculated)	10.5 A peak-to-peak and 3.62 A AC RMS on 43.1 A [b]

[a] For $D \geq 0.5$. [b] Table 2 operating point with $N = 2$ and $\delta = 0.5$.

Table 2. Baseline circuit parameters. Section 5 defines the separate engineering loss reference.

Quantity	Value
$V_{in}, D, \delta, f_s, R$	15 V, 0.8, 0.5, 100 kHz, 200 Ω
L_1, L_2, L_3	100 µH each
C_1, C_2, C_3, C_4, C_o	10 µF each, 100 µF
Capacitor ESR	1 mΩ each
Switch channel resistance, diode threshold	Zero
Diode series resistance	$r_{D4} = 10$ mΩ, others zero

In a two-phase interleaved boost stage, such as the scalable family of [17], both inductors are permanently connected to the source. The source current is then the sum of the inductor currents, and a 180° displacement minimizes its ripple. The present converter differs in three respects. A third inductor reaches the source through a series switch, the load is returned to a negative rail, and the gain numerator contains the duty ratio. In consequence, ripple cancellation depends on the observation port. The series switch disconnects one inductor from the source during every cycle. Continuous inductor current, therefore, produces a discontinuous source contribution, and 180° is no longer the displacement that minimizes the source ripple.

Recent phase-selection studies optimize multiphase ripple through a pre-learning process [24] or derive an analytical phase shift that minimizes output-capacitor RMS current in asymmetric two-input boost converters [25]. Three differences separate the present analysis from these studies. First, the circuit contains a gated branch, so the optimized quantity is the AC RMS current at the physical source terminal. Optimizing the sum of the two continuously connected branches addresses a different current port. Second, the constrained optimum is obtained in closed form. Third, the conduction-mode analysis

extends to mixed operation, in which the three branches leave continuous conduction at different loads.

Regulation of such a converter must tolerate source, load, and component variation. Robust nonlinear controllers are one response. A disturbance-tailored super-twisting scheme, for example, improves disturbance rejection and DC-link voltage regulation in neutral-point-clamped converters under unbalanced grids [26]. At the system level, uncertainty-aware scheduling based on robust optimization manages hydrogen-powered vehicles and renewable units in coupled microgrid–transportation networks [27]. Such scheduling moves the operating point of every interface converter over a wide range. The present paper retains linear sampled-data compensators because they permit exact local analysis of the switched circuit, and it quantifies their margins under parameter perturbation in Section 6.

Figure 1 places the converter between a low-voltage PV or battery source and a 400 V differential DC bus. The evaluated input levels are 12, 18, and 24 V, with 400 and 800 W output cases. Local DC–DC interfaces draw power across p and n to supply DC loads. An optional standalone inverter supplies AC loads. The controller senses $v_o = v_p - v_n$ and $i_\Sigma = i_2 + i_3$, then sets common duty d at the selected phase displacement.

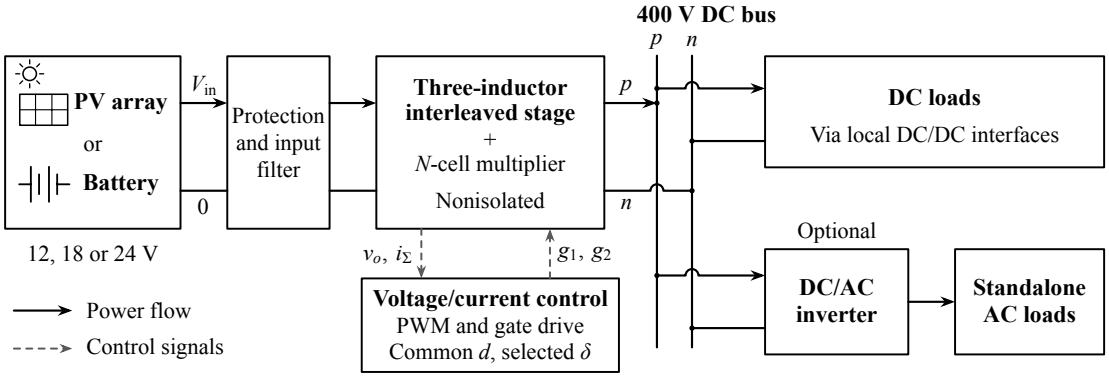


Figure 1. Application of the converter as a unidirectional interface from a low-voltage PV or battery source to a 400 V differential DC bus. The sources are alternatives. Local DC–DC interfaces and an optional standalone inverter supply DC and AC loads. Solid arrows denote power flow, while dashed arrows denote feedback and gate commands. Input reference 0 and output return n are distinct. The controller uses $v_o = v_p - v_n$ and $i_\Sigma = i_2 + i_3$.

This study provides five circuit-specific results:

- An explicit N-cell extension with gain, current-sharing, and blocking-voltage laws, together with the dependence of stress, loss, and capacitor current on N at a fixed 400 V output.
- A phase-selection rule separating source RMS reduction, upper-pair ripple, and unequal-inductance slope cancellation, with its sensitivity to load, input voltage, and inductance tolerance.
- Mixed-conduction gain laws and successive discontinuous-conduction boundaries, checked at several duty ratios and inductances.
- Charge-transfer-aware loss calculations and a sampled controller evaluated at six 400 V operating points, including its margins under component perturbation.
- Verification of the steady-state results in PLECS and in an independent piecewise-linear switching simulator, which also supplies start-up, load-step, and input-step waveforms.

All results in this paper are analytical or numerical. The evidence comprises analytical derivations and three switching-circuit simulations of the same circuit: an event-driven solver based on diode complementarity, a fixed-step piecewise-linear simulator, and PLECS

(Section 7). Efficiency estimates use disclosed device-loss assumptions. Controller margins refer to the evaluated CCM operating points. Table A1 in Appendix A lists the principal symbols.

2. Topology and CCM Gain

2.1. Connections and Operating Sequence

Figure 2 defines the baseline and extended circuits. Both panels use one device notation. D_1 and C_1 form the return branch, $D_2, \dots, D_{2N}$ and $C_2, \dots, C_{2N}$ form the ladder, and D_o and C_o are the output diode and capacitor. The load voltage is $v_o = v_p - v_n$, with a negative output return n distinct from source ground. Let $T_s = 1/f_s$, $s = t/T_s$, $q = 1-D$, and δ denote normalized phase delay. The commands are

$$g_1(s) = \mathbf{1}_{\{0 \le \{s\} < D\}}, \qquad g_2(s) = g_1(s-\delta), \qquad \tfrac{1}{2} < D < 1, \quad q \le \delta \le D. \tag{1}$$

Q_1, Q_2 receive g_1, and Q_3 receives g_2. The sequence $(1,1), (1,0), (1,1), (0,1)$ has normalized durations $\delta - q, q, D - \delta, q$. The single-OFF intervals are denoted $\mathcal{A}$ and $\mathcal{B}$, and both-ON intervals are denoted $\mathcal{O}$.

The two inequalities in (1) have one purpose. Q_3 is OFF for $s \in [\delta - q, \delta)$, and Q_1, Q_2 are OFF for $s \in [D, 1)$. These windows are disjoint if and only if $q \le \delta \le D$, and such a δ exists only for $D \ge \frac{1}{2}$. Inside this domain at least one of the legs b and c is clamped to source ground at every instant. The ladder is then charged alternately from the two legs, and the clamp relations used in (4)–(9) and in Sections 3–6 hold. The region $D > \frac{1}{2}$ is also the region of practical interest, because (5) gives $M_N > 4N + 1$ there, which is a gain above 9 for $N = 2$.

The constraints are, therefore, the validity domain of the analyzed sequence, and they are also a practical operating limit. For δ outside the range both legs are OFF during part of the period. The currents i_2 and i_3 then return through the load and C_1 and no longer through a grounded leg, and the clamp relations fail. The piecewise-linear simulator of Section 7, which prescribes no conduction sequence, quantifies the effect for Table 2. At $D = 0.8$ the output is 359.5 V at $\delta = 0.2$, on the edge of the domain. It falls to 322.2 V at $\delta = 0.15$ and to 209.6 V at $\delta = 0.10$, where both legs are OFF for 5% and 10% of the period, and the upper-branch currents become unequal (16.0 and 12.2 A at $\delta = 0.15$). PLECS gives 322.1 and 209.6 V for the same two cases (Section 7.1). A controller should, therefore, enforce (1) at all times, including start-up. Section 7.4 gives a start-up sequence that keeps $D > \frac{1}{2}$.

For $N = 2$, capacitor states are $v_1 = -v_n$, $v_2 = v_x - v_c$, $v_3 = v_y - v_b$, and $v_4 = v_z - v_x$. The state vector and physical input current are

$$\mathbf{x} = [i_1, i_2, i_3, v_1, v_2, v_3, v_4, v_{C_o}]^{\mathsf{T}}, \tag{2}$$

$$i_{\text{in}} = g_1 i_1 + i_2 + i_3. \tag{3}$$

States exclude capacitor ESR drops. Terminal v_o includes output-capacitor ESR. Figure 3 resolves the additional diode events under finite capacitance, and Figure 4 shows the conducting paths of the resulting six subintervals on the circuit diagram.

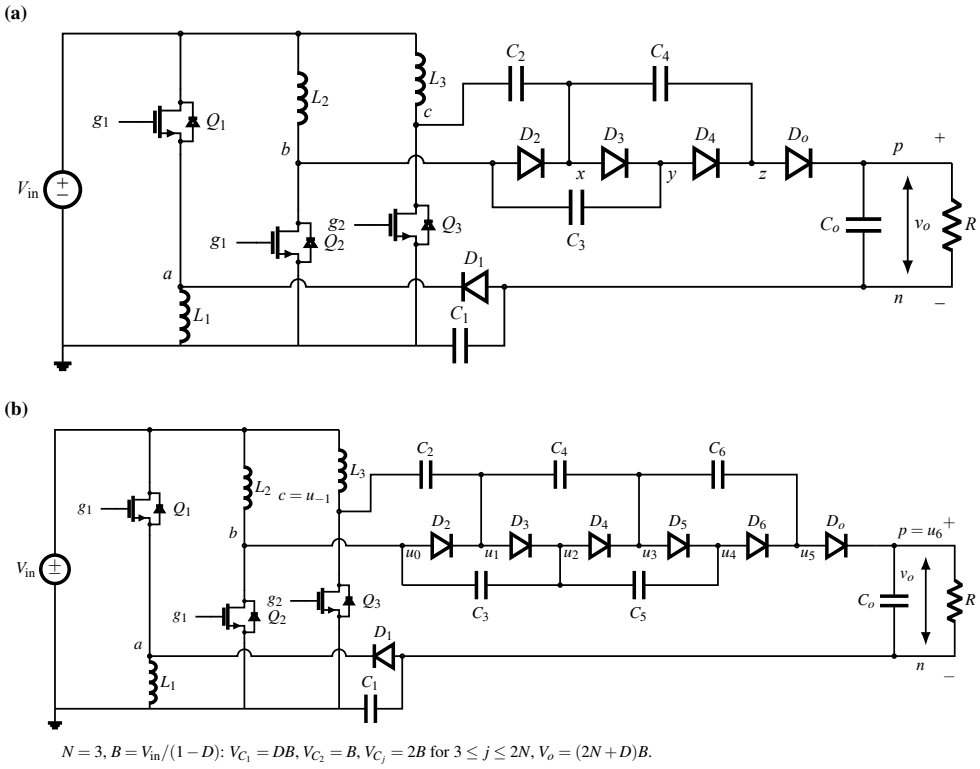


Figure 2. Converter connections. (**a**) Baseline $N = 2$. The load spans positive rail p and negative rail n. (**b**) $N = 3$ extension. Each added cell contains two diodes and two capacitors. Diodes and capacitors carry the same names in both panels: D_1, C_1 in the return branch, D_2 to D_{2N} and C_2 to C_{2N} in the ladder, and D_o, C_o at the output. Ladder nodes are $u_0 = b$, $u_{-1} = c$, and $u_{2N} = p$, so x, y, z in (**a**) are u_1, u_2, u_3. Bridges indicate unconnected wire crossings. Capacitor ESR is included in the numerical model.

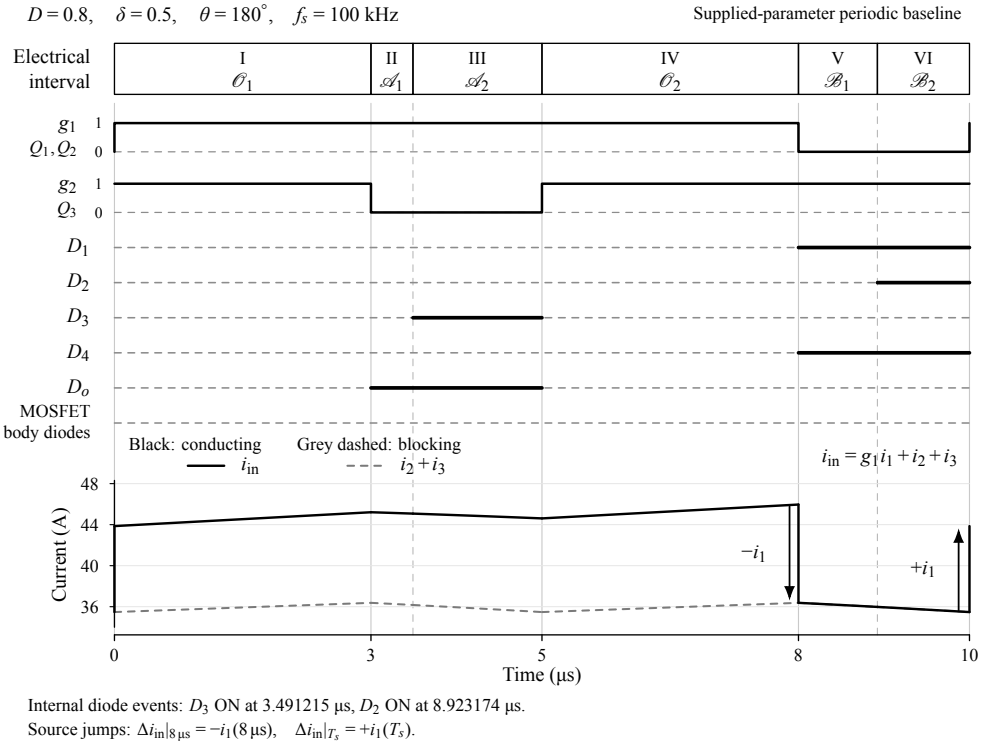


Figure 3. Nominal conduction sequence for Table 2. Five configurations occupy six chronological subintervals. D_3 begins conduction at 3.4912 µs and D_2 at 8.9232 µs without gate changes. The g_1 edges connect or disconnect i_1 at the source. Figure 4 gives the corresponding current paths.

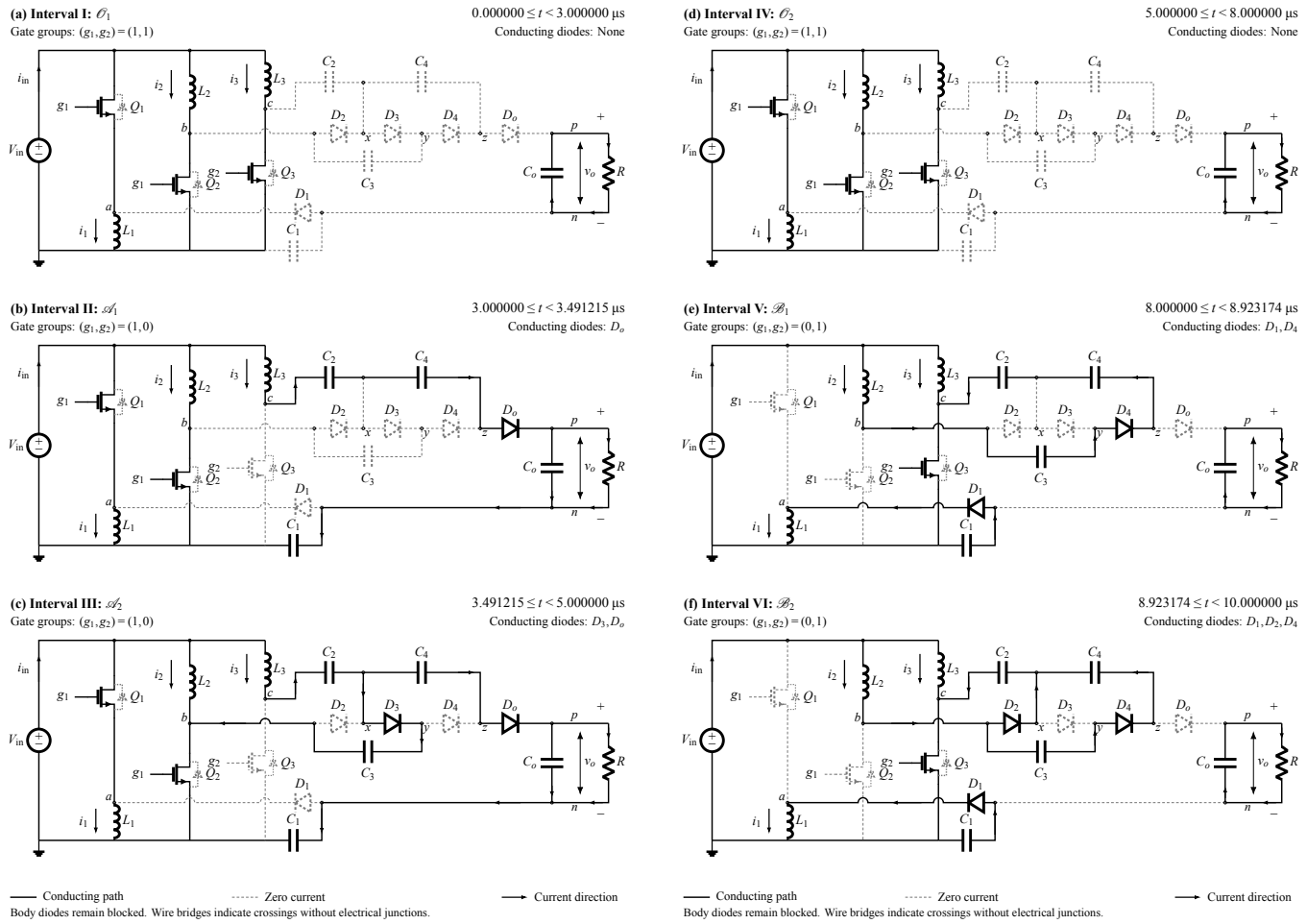


Figure 4. Operating states of the $N = 2$ converter for Table 2, drawn on the circuit diagram. Solid lines carry current and dotted lines are idle. (**a**,**d**) O: all switches ON, the three inductors charge from the source, and C_o supplies the load. (**b**) $\mathcal{A}_1$: Q_3 OFF, i_3 discharges C_2 and C_4 into the output through D_o and returns through C_1. (**c**) $\mathcal{A}_2$: D_3 also conducts and part of i_3 charges C_3. (**e**) $\mathcal{B}_1$: Q_1, Q_2 OFF, i_1 charges C_1 through D_1, and i_2 moves charge from C_3 to C_4 and C_2 through D_4. (**f**) $\mathcal{B}_2$: D_2 also conducts and i_2 charges C_2 directly. The source current contains i_1 only in (**a**–**d**).

The six states follow from the switch commands and from two internal diode commutations. In O all three switches conduct, every diode blocks, and each inductor current rises with slope V_{in}/L_k. In $\mathcal{A}$ only Q_3 is OFF. The current i_3 first flows through C_2, C_4, and D_o to the output rail p and returns to ground through the load and C_1. When the voltage across D_3 reaches zero, D_3 turns on and the remaining interval also recharges C_3 through the grounded leg b. In $\mathcal{B}$ the switches Q_1 and Q_2 are OFF. Q_1 disconnects i_1 from the source, and i_1 circulates through D_1 and charges the return capacitor C_1, which sets v_n. The current i_2 first transfers charge from C_3 to C_4 and C_2 through D_4 and the grounded leg c. D_2 then turns on and charges C_2 directly.

2.2. Voltage and Charge Balance

With $B = V_{\text{in}}/q$, inductor volt-second balance and diode clamps give

$$V_1 = DB, \qquad V_2 = B, \qquad V_3 = V_4 = 2B, \qquad M_2 = \frac{V_o}{V_{\text{in}}} = \frac{4 + D}{q}. \tag{4}$$

For integer $N \ge 1$, define $u_{-1} = c$, $u_0 = b$, and $u_{2N} = p$. The ladder diodes are $D_{k+1} : u_{k-1} \to u_k$ for $k = 1, \ldots, 2N - 1$, the output diode is $D_o : u_{2N-1} \to u_{2N}$, and the pump capacitors have

$v_{C_{j+1}} = v_{u_j} - v_{u_{j-2}}$ for $j = 1, \ldots, 2N-1$. The return branch retains $D_1 : n \to a$ and $v_{C_1} = -v_n$. At $N = 2$ these definitions reproduce Figure 2a. Alternating diode clamps yield

$$\begin{aligned} V_p = 2NB, \quad V_n = -DB, \quad M_N = \frac{2N+D}{q}, \\ V_{C_1} = DB, \quad V_{C_2} = B, \quad V_{C_j} = 2B \ (3 \le j \le 2N). \end{aligned} \tag{5}$$

The graph contains three switches, three inductors, and $2N+1$ external diodes and capacitors each. Ideal repetitive blocking voltages are

$$V_{Q_k} = V_{D_1} = V_{D_o} = B, \qquad V_{D_j} = 2B \quad (2 \le j \le 2N). \tag{6}$$

Capacitor charge balance gives mean diode current I_o and leading triangular-CCM branch means

$$I_1 = \frac{I_o}{q}, \qquad I_2 = I_3 = \frac{NI_o}{q}, \qquad I_{\text{in}} = DI_1 + I_2 + I_3 = M_N I_o. \tag{7}$$

For $\Delta_k = V_{\text{in}} D/(L_k f_s)$, the first CCM boundary follows from $I_k = \Delta_k/2$:

$$R_{\text{CCM}} = \frac{2f_s(2N+D)}{Dq^2} \min(L_1, NL_2, NL_3). \tag{8}$$

Successive boundaries require the mixed-mode gain in Section 4. Under monotonic transfer, capacitor charge balance gives

$$\Delta V_{C_k} \simeq \frac{[N - \lfloor (k-1)/2 \rfloor] I_o}{C_k f_s} \quad (2 \le k \le 2N), \qquad \Delta V_{C_o} \simeq \frac{DI_o}{C_o f_s}. \tag{9}$$

Both expressions are peak-to-peak ripples of the capacitor state, excluding the ESR drop. The first pump capacitor C_2 transfers NI_oT_s per cycle. Its RMS rating, therefore, requires a separate current calculation.

At a fixed output target,

$$D_N^* = \frac{V_o^* - 2NV_{\text{in}}}{V_o^* + V_{\text{in}}}, \qquad B^* = \frac{V_o^* + V_{\text{in}}}{2N+1}. \tag{10}$$

The analyzed sequence requires $V_o^*/V_{\text{in}} > 4N+1$. Additional cells reduce duty and blocking voltage while increasing component count and transfer paths. Section 5.4 quantifies this trade-off with the nonideal model.

3. Phase Selection and Unequal Inductances

3.1. Source-Current RMS Objective

For equal inductances, define $\Delta = V_{\text{in}} D/(Lf_s)$ and the periodic unit-ripple waveform

$$h(s) = \begin{cases} -1/2 + s/D, & 0 \le s < D, \\ 1/2 - (s-D)/q, & D \le s < 1. \end{cases} \tag{11}$$

Then $i_{1,2} = I_{1,2} + \Delta h(s)$ and $i_3 = I_3 + \Delta h(s-\delta)$. Integrating $(i_{\text{in}} - I_{\text{in}})^2$ over one period gives, for $x = \delta - 1/2$,

$$\begin{aligned} I_{\text{in,ac}}^2 = Dq I_1^2 + \frac{2I_1 \Delta q}{D} x + \Delta^2 \left[F_0(D) + \frac{2x^2}{D^2} \right], \\ F_0(D) = \frac{5D^3 + 2D^2 - 6D + 2}{12D^2}. \end{aligned} \tag{12}$$

The positive curvature yields a unique constrained minimum,

$$\frac{\mathrm{d}^2 I_{\mathrm{in,ac}}^2}{\mathrm{d}\delta^2} = \frac{4\Delta^2}{D^2} > 0, \qquad \delta^*_{\mathrm{RMS}} = \max\left(q, \frac{1}{2} - \frac{I_1 D q}{2\Delta}\right). \tag{13}$$

At the nominal point, $\Delta = 1.2$ A and $I_1 = 9$ A give $\delta^* = 0.2$. Finite-capacitance calculations reduce source AC RMS from 3.61735 to 3.44544 A, or 4.75%, relative to $\delta = 0.5$. Upper-pair ripple increases from 0.90 to 1.80 A, and source peak current increases by 0.45 A (Figure 5a,b).

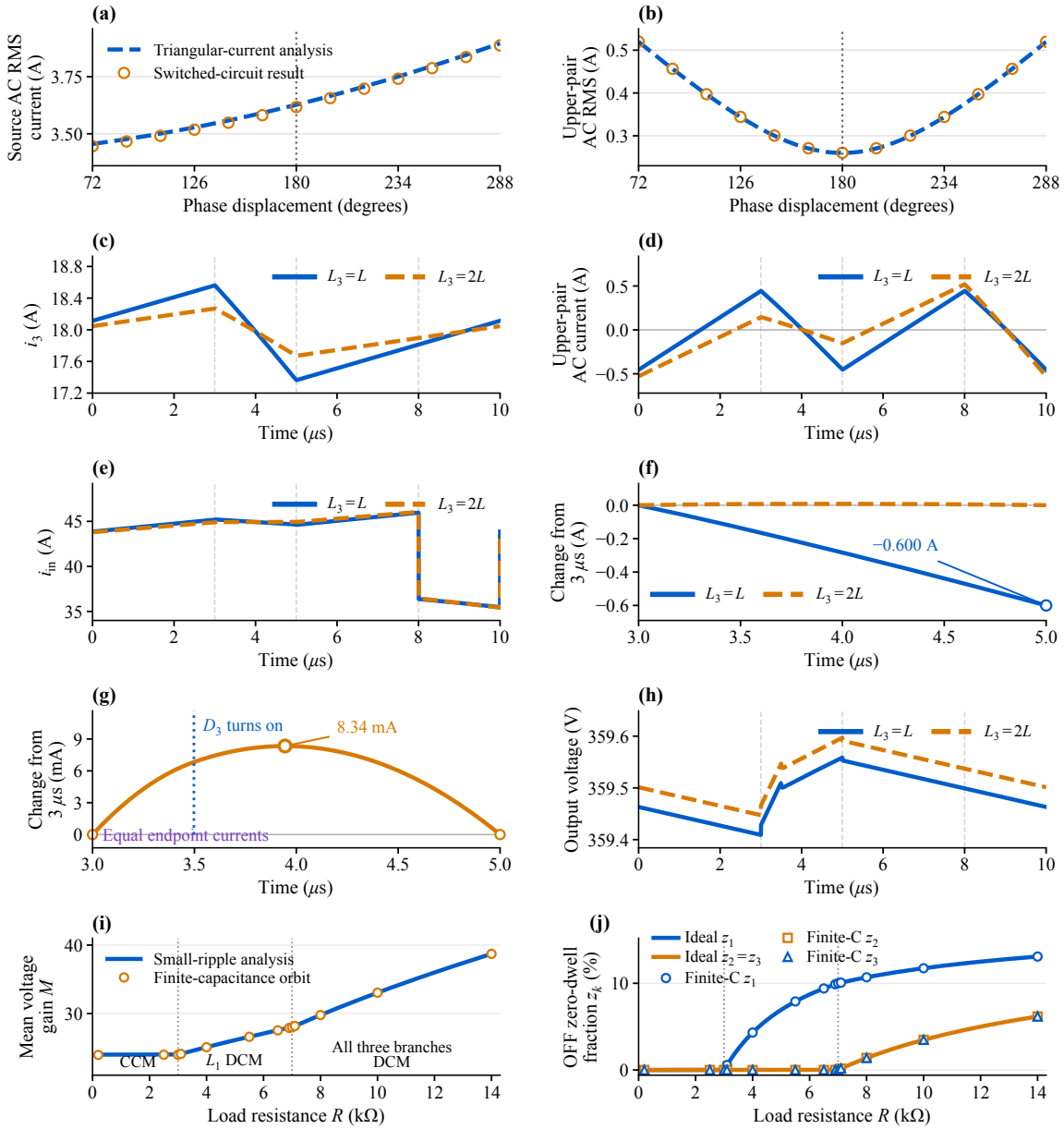


Figure 5. Phase, inductance, and DCM comparison at 15 V, $D = 0.8$, 100 kHz, and $N = 2$. (**a**,**b**) Source and upper-pair AC RMS at $R = 200\ \Omega$ and $L_k = 100$ µH. (**c**–**h**) $L_3 = L$ versus $2L$ for $L_1 = L_2 = L = 100$ µH, $R = 200\ \Omega$, and $\delta = 0.5$: third-inductor current, upper-pair AC current, source current, interval change, enlarged residual, and output voltage. The ideal slope in $\mathcal{A}$ is zero for $L_3 = 2L$, and finite capacitance leaves the 8.338 mA residual shown in (**g**) over $\mathcal{A} = [3, 5]$ µs. (**i**,**j**) Gain and OFF zero-dwell fractions versus load with equal inductances. Dotted lines mark the 3 and 7 kΩ boundaries. Curves and markers in (**a**,**b**,**i**,**j**) denote analytical and finite-capacitance results.

The practical significance of this reduction is as follows. It lowers the ESR heating of the input capacitor by 9.28% and the capacitance needed for a given ripple by 6%, as quantified below. The fundamental component of the source current, which dominates what remains behind an input filter, falls by 8.7%, from 2.394 to 2.185 A RMS. The costs are a doubled upper-pair ripple, which matters only if i_Σ is sampled without cycle averaging, and a source peak current that is 1.0% higher. The inductor, switch, and diode currents are unchanged, so the rule changes neither the component stress inside the converter nor its efficiency (Section 7). The rule requires no hardware and, therefore, improves source-current quality at no cost.

3.2. Sensitivity to Load, Input Voltage, and Inductance Tolerance

Substituting $I_1 = M_N V_{\text{in}}/(Rq)$ and $\Delta = V_{\text{in}} D/(Lf_s)$ into (13) gives

$$\delta^*_{\text{RMS}} = \max\left(q,\ \frac{1}{2} - \frac{M_N L f_s}{2R}\right). \tag{14}$$

At a fixed duty ratio the optimum is independent of the input voltage and depends on the load through Lf_s/R only. At a fixed output voltage it depends on the input voltage through $M_N = V_o^*/V_{\text{in}}$, which is the guarded rule used in Section 7. The optimum is interior for $R > M_N L f_s/(2D-1)$, which is 400 Ω at the nominal point, and it is clamped at $\delta = q$ for heavier loads.

Table 3 tests (14) against the piecewise-linear simulator at five loads, with a timing guard of 0.01 on the clamp. The rule coincides with the numerically located optimum at every load, both where it is clamped and where it is interior. The reduction of source AC RMS relative to $\delta = 0.5$ is 2.7% at 100 Ω, peaks at 6.1% near the load where the clamp is released, and falls to 3.2% at 1600 Ω. Lighter loads also need a smaller displacement from 180°, so the upper-pair ripple penalty falls from a factor of 1.97 to 1.25. Over the 400 V envelope of Section 7, where the input voltage varies from 12 to 24 V, the reduction is 2.26–9.01% and increases with input voltage.

Table 3. Phase selection against load at $V_{\text{in}} = 15$ V, $D = 0.8$, and $L_k = 100$ µH (piecewise-linear simulator, Table 2). The rule is (13) with a 0.01 timing guard. The numerical optimum is the minimum of the simulated curve.

R (Ω)	Rule δ	Numerical Optimum	AC RMS at $\delta = 0.5$ (A)	AC RMS at Rule (A)	Reduction (%)	Upper-Pair Ripple Ratio	Peak Change (A)
100	0.210	0.210	7.1872	6.9934	2.70	1.97	0.43
200	0.210	0.210	3.6173	3.4494	4.64	1.97	0.43
400	0.210	0.210	1.8495	1.7367	6.10	1.97	0.43
800	0.350	0.350	1.0009	0.9490	5.19	1.50	0.22
1600	0.425	0.425	0.6299	0.6095	3.24	1.25	0.11

Table 4 applies the rule computed from the nominal inductance to circuits whose inductances deviate by ±20%. A deviation of L_1 or L_2 moves the true optimum by at most 0.017 in δ (6°), and a deviation of L_3 does not move it. Because the variance (12) is quadratic in δ with a flat minimum, the nominal rule stays within 0.07% of the optimal source AC RMS in every case. The benefit itself changes with the tolerance, between 3.8% and 5.8% at 200 Ω and between 4.2% and 7.5% at 800 Ω. The rule is, therefore, robust to inductance tolerance.

Table 4. Phase selection under inductance tolerance at $V_{in} = 15$ V and $D = 0.8$. The rule value of δ is computed from the nominal 100 µH and applied to the perturbed circuit. Reductions are relative to $\delta = 0.5$ on the same circuit. The penalty is the excess source AC RMS of the rule over the numerical optimum.

R (Ω)	Inductances	Rule δ	Numerical Optimum	Reduction at Rule (%)	Reduction at Optimum (%)	Penalty (%)
200	Nominal	0.210	0.210	4.64	4.64	0.00
200	L_1 −20%	0.210	0.210	4.43	4.43	0.00
200	L_3 +20%	0.210	0.210	3.85	3.85	0.00
200	L_3 −20%	0.210	0.210	5.85	5.85	0.00
800	Nominal	0.350	0.350	5.19	5.19	0.00
800	L_1 +20%	0.350	0.336	5.84	5.88	0.04
800	L_1 −20%	0.350	0.367	4.26	4.33	0.07
800	L_2 +20%	0.350	0.336	5.87	5.92	0.05
800	L_2 −20%	0.350	0.367	4.22	4.28	0.07
800	L_3 +20%	0.350	0.350	4.22	4.22	0.00
800	L_3 −20%	0.350	0.350	6.64	6.64	0.00
800	L_2 +20%, L_3 −20%	0.350	0.336	7.47	7.52	0.06

3.3. Input Capacitor and Source Impedance

With constant upstream current, an input capacitor carries $I_{in} - i_{in}$. Its ESR loss and capacitance requirement follow

$$P_{C_{in}} = r_{C_{in}} I_{in,ac}^2, \qquad C_{in} \geq \frac{\max Q - \min Q}{\Delta V_{in}}, \qquad Q(t) = \int_0^t [I_{in} - i_{in}(\tau)]\, d\tau. \tag{15}$$

The nominal phase change reduces constant-ESR heating by 9.28%. Ideal charge excursion falls from 14.4 to 13.5 µC, giving 96 and 90 µF for 0.15 V ripple. These quantities support filter sizing. Filter volume and EMI performance additionally depend on harmonic attenuation, damping, and component ratings.

Equation (15) assumes a constant upstream current, which is the limit of a large source inductance, and it neglects the capacitor ESR. The input stage of Figure 1 is not ideal in either respect. Table 5, therefore, adds a source resistance of 5 mΩ, a series inductance L_s, and a 100 µF capacitor with 5 mΩ ESR to the piecewise-linear simulation. Three effects appear. First, the terminal-voltage ripple is 194–202 mV at $\delta = 0.5$, whereas the capacitance-only estimate $\Delta Q/C_{in}$ is 144 mV. The difference is the ESR step $r_{C_{in}} \Delta i_{in} \approx 5$ mΩ × 10.3 A, which must be added to (15). Second, the ripple that reaches the source depends on the resonance $f_0 = 1/(2\pi\sqrt{L_s C_{in}})$. For $L_s = 5$, 1, and 0.2 µH the source-side AC RMS is 0.4%, 1.9%, and 10% of the converter input value, of the order of $(f_0/f_s)^2$ while $f_0 \ll f_s$. A stiff low-inductance source, therefore, receives a substantial part of the ripple, and a resonance near f_s would require damping. Third, the phase rule remains effective behind the filter. The source-side AC RMS at $\delta = 0.2$ is 8.5% lower than at $\delta = 0.5$ for every L_s, in line with the 8.7% reduction of the fundamental. The source resistance also lowers the terminal voltage by 0.21 V and the output by 5.1 V at fixed duty.

Table 5. Source-side quantities with a nonideal source at the Table 2 point: source resistance 5 mΩ, series inductance L_s, and a 100 µF input capacitor with 5 mΩ ESR. f_0 is the resonance of L_s with the capacitor.

δ	Source Network	f_0 (kHz)	Converter Input AC RMS (A)	Source-Side AC RMS (A)	Source-Side Peak-to-Peak (A)	Terminal Ripple (mV, Peak-to-Peak)
0.5	Stiff source, no capacitor		3.617	3.617	10.484	0
	L_s = 0.2 µH	35.6	3.567	0.366	1.074	202.4
	L_s = 1 µH	15.9	3.567	0.066	0.194	195.0
	L_s = 5 µH	7.1	3.567	0.013	0.038	193.6
0.2	Stiff source, no capacitor		3.445	3.445	10.484	0
	L_s = 0.2 µH	35.6	3.398	0.335	0.987	193.4
	L_s = 1 µH	15.9	3.398	0.061	0.179	186.1
	L_s = 5 µH	7.1	3.398	0.012	0.035	184.7

3.4. Local Slope Cancellation

Between gate edges, unequal inductances give

$$\frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} = V_{\mathrm{in}} \begin{cases} L_1^{-1} + L_2^{-1} + L_3^{-1}, & \mathcal{O}, \\ L_1^{-1} + L_2^{-1} - D/(qL_3), & \mathcal{A}, \\ -D/(qL_2) + L_3^{-1}, & \mathcal{B}. \end{cases} \tag{16}$$

Cancellation in $\mathcal{A}$ requires

$$\begin{aligned} L_3 &= \frac{D}{q}\frac{L_1 L_2}{L_1 + L_2}, \\ D_{\mathrm{flat}} &= \frac{(L_1 + L_2)^2}{(L_1 + L_2)^2 + L_1 L_2} \geq \frac{4}{5} \quad \text{if } L_3 = L_1 + L_2. \end{aligned} \tag{17}$$

Thus, $L_1 = L_2 = L$, $L_3 = 2L$ cancels the ideal slope at $D = 0.8$. The cancellation is the cause of the reduction: with equal inductances the source current changes by 0.600 A over $\mathcal{A}$, and with $L_3 = 2L$ the ideal change is zero. Finite capacitance is what remains. The capacitor-voltage ripple makes the inductor voltages vary within the interval, which leaves a residual excursion of 8.338 mA. Complete-period source ripple instead increases from 10.48420 to 10.63515 A at $\delta = 0.5$. Gate-induced current steps persist, so local cancellation does not establish global ripple reduction (Figure 5c–h).

The unequal design has three practical benefits. The source current is flat for $qT_s = 2$ µs in every period, so a source-current sample taken in $\mathcal{A}$ is insensitive to the sampling instant. The ripple of i_3 halves, from 1.2 to 0.6 A, which lowers the core and AC winding loss of L_3. The margin of the third branch to its extinction boundary doubles through (8). Against these stand the following costs. L_3 stores twice the energy, 32.3 against 16.1 mJ. Over the complete period the source ripple is 1.44% larger, the source AC RMS 0.29% larger (3.6277 against 3.6173 A), and the fundamental 0.9% larger. The phase rule becomes less effective, because $\delta = 0.2$ then reduces the source AC RMS by 2.3% and no longer by 4.75%. Local slope cancellation, therefore, provides a locally flat source current and is distinct from a reduction of the complete-period ripple, a distinction that the conventional sum-of-currents view does not make.

4. DCM Gain and Boundary Laws

DCM requires a positive-duration zero-current dwell during an OFF command. The following closed forms assume ideal devices, small capacitor ripple, $D > 1/2$, and $q \leq \delta \leq D$. Set $(w_1, w_2, w_3) = (1, N, N)$, the ratio of each branch mean current to I_o/q in (7), and $\Delta_k = V_{\mathrm{in}} D/(L_k f_s)$. The current-touch threshold and all-CCM candidate boundary are

$$I_{t,k} = \frac{\Delta_k q}{2w_k},$$
$$R^{\mathrm{CCM}}_{\mathrm{crit},k} = \frac{2w_k L_k f_s (2N + D)}{Dq^2}, \qquad L^{\mathrm{CCM}}_{\mathrm{crit},k} = \frac{RDq^2}{2w_k f_s (2N + D)}. \tag{18}$$

Only the smallest candidate determines the first transition. For a discontinuous branch, triangular OFF-current charge balance gives

$$\frac{1}{2}\Delta_k \lambda_k = w_k I_o, \qquad z_k = q - \lambda_k > 0, \qquad I_k = \frac{\Delta_k (D + \lambda_k)}{2}, \tag{19}$$

where λ_k and z_k are normalized transfer and zero-dwell durations.

Let $\chi_k = 1$ denote DCM and $\chi_k = 0$ denote CCM. Substituting $I_o = MV_{\mathrm{in}}/R$ into the capacitor-charge and volt-second balances yields

$$\Gamma_{\boldsymbol{\chi}} = (1 - \chi_1)\frac{D}{q} + N\left[\frac{2 - \chi_2 - \chi_3}{q} + \chi_2 + \chi_3\right],$$
$$\kappa_{\boldsymbol{\chi}} = \frac{D^2}{2f_s}\sum_{k=1}^{3}\frac{\chi_k}{L_k}, \tag{20}$$
$$M_{\boldsymbol{\chi}} = \frac{\Gamma_{\boldsymbol{\chi}} + \sqrt{\Gamma^2_{\boldsymbol{\chi}} + 4\kappa_{\boldsymbol{\chi}} R}}{2}.$$

Admissibility requires $I_o < I_{t,k}$ for each discontinuous branch and $I_o > I_{t,k}$ for each continuous branch. Equality identifies a shared boundary. Full DCM gives

$$M_{\mathrm{DCM}} = N + \sqrt{N^2 + \frac{D^2 R}{2f_s}\sum_{k=1}^{3}\frac{1}{L_k}}. \tag{21}$$

For a continuous branch approaching extinction in pattern $\boldsymbol{\chi}$, define $H_k = 2w_k L_k f_s/(Dq)$. Substituting $R = H_k M$ gives the subsequent boundary

$$R^{\boldsymbol{\chi}}_{\mathrm{crit},k} = H_k(\Gamma_{\boldsymbol{\chi}} + \kappa_{\boldsymbol{\chi}} H_k), \qquad L_{\mathrm{crit},k} = \frac{RDq}{2w_k f_s M_{\boldsymbol{\chi}}}. \tag{22}$$

The other branches must satisfy their admissibility inequalities. Adjacent admissible gains coincide at equality.

For $N = 2$, $D = 0.8$, $L_k = 100$ µH, and $f_s = 100$ kHz,

$$M(R) = \begin{cases} 24, & R \le 3000, \\ 10 + \sqrt{100 + 0.032R}, & 3000 < R < 7000, \\ 2 + \sqrt{4 + 0.096R}, & R \ge 7000, \end{cases} \qquad [R] = \Omega. \tag{23}$$

The upper-branch boundary follows the mixed-mode solution at 7 kΩ. Applying the all-CCM formula beyond the first extinction incorrectly predicts 6 kΩ.

Figure 5i,j compares the analytical gain and zero-dwell fractions with finite-capacitance solutions, and Figure 6 shows the waveforms at 4 and 10 kΩ.

Finite-capacitance continuation follows the periodic orbit through each preceding extinction. The resulting boundary brackets are 2997.42–2997.44 Ω for L_1, 6992.15–6992.17 Ω for L_3, and 6993.03–6993.05 Ω for L_2. Diode complementarity resolves the intervening charge-transfer paths [28]. At extinction, inductor currents and stored capacitor voltages remain continuous. Released branch nodes satisfy $v_{Lk} = 0$ until the next ON command. Branchwise dwells need not overlap. Event-time sensitivities remain necessary for closed-loop stability analysis.

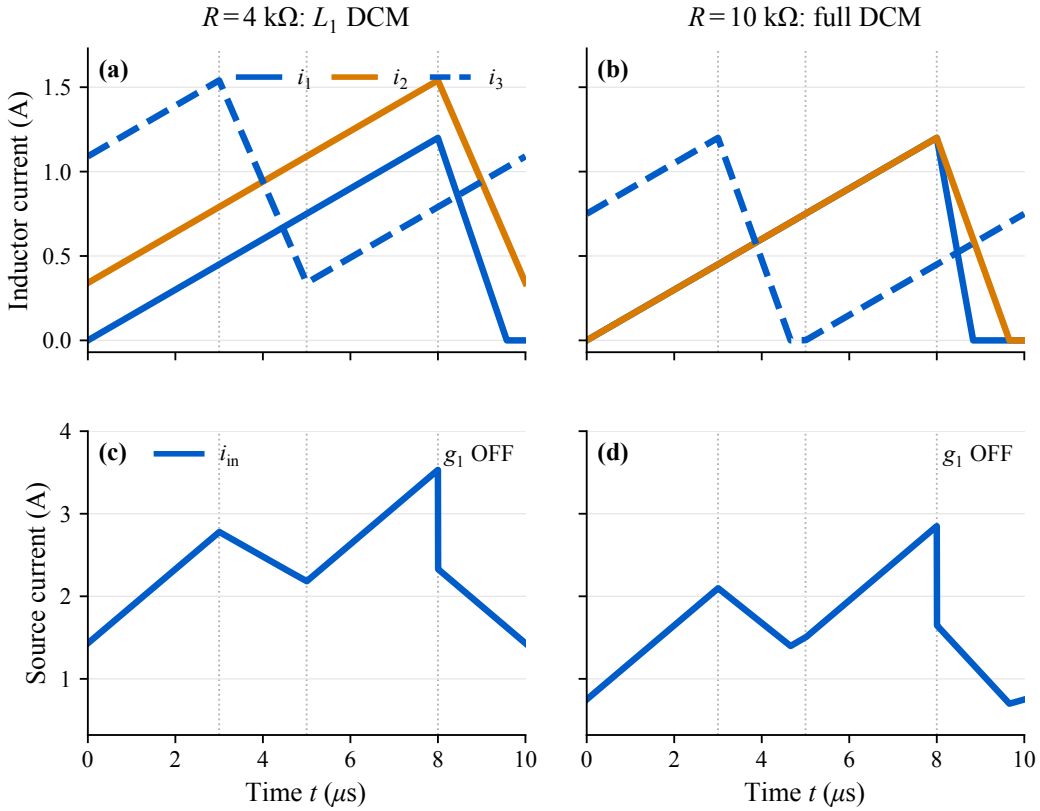


Figure 6. Finite-capacitance DCM waveforms. (**a**) Inductor currents and (**c**) source current at 4 kΩ, where only L_1 has a zero dwell. (**b**) Inductor currents and (**d**) source current at 10 kΩ, where all three branches have zero dwells. Mean outputs are 376.360 and 495.716 V, respectively. Dotted lines mark gate edges. Source current retains the gated i_1 contribution.

Table 6 repeats the boundary test at other duty ratios and inductances. It uses the piecewise-linear simulator of Section 7, which contains no conduction-mode logic, so a zero-current dwell arises only from the device model. Each boundary is located by computing the valley current of the branch at 97.5% and 99.2% of the predicted resistance, with any preceding branch already discontinuous, and extrapolating it to zero. The simulated boundaries lie between 0.01% and 0.37% below the closed forms. The deviation grows as the duty ratio falls and as the inductance falls, that is, with the load current at the boundary and, therefore, with the capacitor-voltage ripple that the closed forms neglect. The case $L_1 = 300$ μH reverses the extinction order. The upper pair extinguishes first at 6 kΩ, and L_1 follows at 12 kΩ in the mixed pattern, as (22) predicts. For unequal upper inductances ($D = 0.7$, $L_3 = 150$ μH) the three boundaries are distinct, and the simulated values follow the predicted sequence within 0.20%. At 21 loads spread over the continuous, mixed, and fully discontinuous regions of these circuits, the gain law (20) agrees with the simulated gain within 0.17%.

Table 6. Extinction boundaries at $V_{in} = 15$ V, $f_s = 100$ kHz, and $N = 2$ for several duty ratios and inductances. The analytical values follow (18) for the first extinction and (22) for the next. The simulated values are from the piecewise-linear simulator with the capacitances of Table 2.

D	L_1, L_2, L_3 (µH)	Branch	Preceding Pattern	Analytical (Ω)	Simulated (Ω)	Deviation (%)
0.8	100, 100, 100	L_1	all CCM	3000.0	2997.7	−0.08
0.8	100, 100, 100	L_2, L_3	mixed	7000.0	6994.0	−0.09
0.7	100, 100, 100	L_1	all CCM	1492.1	1489.5	−0.17
0.7	100, 100, 100	L_2, L_3	mixed	3428.6	3421.4	−0.21
0.6	100, 100, 100	L_1	all CCM	958.3	955.6	−0.28
0.6	100, 100, 100	L_2, L_3	mixed	2166.7	2158.7	−0.37
0.8	50, 50, 50	L_1	all CCM	1500.0	1497.5	−0.17
0.8	50, 50, 50	L_2, L_3	mixed	3500.0	3493.2	−0.20
0.8	200, 200, 200	L_1	all CCM	6000.0	5998.3	−0.03
0.8	200, 200, 200	L_2, L_3	mixed	14000.0	13997.2	−0.02
0.8	300, 100, 100	L_2, L_3	all CCM	6000.0	5995.4	−0.08
0.8	300, 100, 100	L_1	mixed	12000.0	11999.2	−0.01
0.7	100, 100, 150	L_1	all CCM	1492.1	1489.7	−0.16
0.7	100, 100, 150	L_2	mixed	3428.6	3421.7	−0.20
0.7	100, 100, 150	L_3	mixed	6476.2	6466.5	−0.15

5. Device Stress and Loss Model

5.1. Current Paths and Ratings

With $h_A = 1 - g_2$, $h_B = 1 - g_1$, and output-diode current ι_{2N}, the switch currents are

$$\begin{aligned} i_{Q_1} &= g_1 i_1, \\ i_{Q_2} &= g_1 i_2 + h_A (i_3 - \iota_{2N}), \\ i_{Q_3} &= g_2 i_3 + h_B i_2, \\ I^2_{Q_3,\mathrm{rms}} &= \langle g_2 i_3^2 \rangle + \langle h_B i_2^2 \rangle + 2\langle g_2 h_B i_2 i_3 \rangle. \end{aligned} \tag{24}$$

The cross term carries the product $g_2 h_B$, because i_{Q_3} contains i_3 only while Q_3 conducts. Under (1) the interval $h_B = 1$ lies inside $g_2 = 1$, so $g_2 h_B = h_B$ and no reported value changes. The squared terms are unaffected because $g_2^2 = g_2$ and $h_B^2 = h_B$. All RMS ratings use the complete current paths. Omitting the transfer terms understates Q_3 channel loss by 30.7% in guarded-phase case A. The first pump capacitor has $i_{C_2} = h_B i_2 - h_A i_3$. Across the twelve evaluated phase/operating states, Q_3 reaches 35.115 A RMS and 63.369 A peak, and C_2 reaches 15.825 A RMS. Each external diode carries mean current I_o, with $I_{d,\mathrm{rms}} \geq I_o / \sqrt{\rho_d}$ for conduction fraction $\rho_d \leq q$.

Repetitive MOSFET and ladder-diode blocking maxima are 89.912 and 171.909 V. Select voltage ratings above $V_{\mathrm{orb}} + V_{\mathrm{unc}} + L_\sigma |\mathrm{d}i/\mathrm{d}t|$. Here, V_{orb} (V) is the largest repetitive blocking voltage on the computed periodic orbit, which already contains the finite-capacitance excursion. V_{unc} (V) is the allowance for input-voltage, duty, and component tolerance. L_σ (H) is the stray inductance of the commutation loop extracted from the layout, and $|\mathrm{d}i/\mathrm{d}t|$ (A/s) is the current slew rate at turn-off, so that the last term is the commutation overshoot. Current ratings require the corresponding safe-operating-area and thermal checks [29].

5.2. Conduction, Commutation, and Magnetic Losses

The conduction calculation uses temperature-dependent device parameters [30]:

$$
\begin{aligned}
P_{\mathrm{cond}} &= \sum_{s} R_{\mathrm{DS},s}(T) I^2_{Q_s,\mathrm{rms}} + \sum_{d} [V_{F,d}(T) I_o + r_d(T) I^2_{d,\mathrm{rms}}] \\
&\quad + \sum_{k} R_{W,k}(T) I^2_{k,\mathrm{rms}} + \sum_{c} r_c I^2_{c,\mathrm{rms}}, \\
R(T) &= R_{25}[1 + \alpha_R (T - 25)].
\end{aligned} \tag{25}
$$

The reference imposes $T = 75\,^{\circ}\mathrm{C}$, $\alpha_{\mathrm{DS}} = 0.006/^{\circ}\mathrm{C}$, and $\alpha_W = 0.00393/^{\circ}\mathrm{C}$. Table 7 specifies the remaining assumptions.

These assumptions are representative of commercial parts. The 20 mΩ channel resistance equals the maximum on-resistance of a 150 V silicon MOSFET of the class required by the 89.9 V blocking maximum (16 mΩ typical, 20 mΩ maximum, 214 pF typical output capacitance, 31 nC maximum gate charge) [31]. The assumed 300 pF and 80 nC are, therefore, conservative for that part. The 0.85 V threshold lies between the maximum forward voltages of a 200 V, 10 A Schottky rectifier at 10 A, which are 0.9 V at 25 °C and 0.8 V at 125 °C [32]. Two design notes follow. The ladder diodes block up to 171.9 V, so a 200 V rectifier leaves only 14% for V_{unc} and overshoot, and a 250–300 V device with a higher forward voltage may be needed. The Q_3 current in case A, 35.1 A RMS and 63.4 A peak, calls for paralleled devices or a lower-resistance part. The sensitivity analysis later in this section brackets both situations. The winding resistance and the core-loss surrogate are assumptions for a 100 µH inductor and are not tied to a specific component.

Table 7. Nonideal-reference assumptions per device or winding unless identified as totals. Core-loss coefficients define a current-ripple surrogate.

Parameter	Value
$R_{\mathrm{DS},25}$, $R_{W,25}$, capacitor ESR	20, 15, 1 mΩ
V_F, r_d	0.85 V, 10 mΩ
$t_{\mathrm{on}} = t_{\mathrm{off}}$, $C_{\mathrm{oss,er}}$, Q_{rr}	20 ns, 300 pF, 50 nC
Q_g, V_{drv}, P_{aux} (total)	80 nC, 10 V, 0.50 W
P_0, f_0, Δi_0	1.5 W, 100 kHz, 1.2 A
α, β, $\Delta R_{\mathrm{ac},0}$	1.5, 2.5, 20 mΩ

For positive one-sided commutation values, overlap, capacitance, and recovery energies give

$$
\begin{aligned}
E_{\mathrm{ov},s} &= \tfrac{1}{2}(V^-_{s,\mathrm{on}} I^+_{s,\mathrm{on}} t_{\mathrm{on}} + V^+_{s,\mathrm{off}} I^-_{s,\mathrm{off}} t_{\mathrm{off}}), \\
E_{\mathrm{oss}}(V) &= \int_0^V v C_{\mathrm{oss}}(v)\, \mathrm{d}v, \\
P_{\mathrm{sw}} &= f_s \left[\sum_{s} E_{\mathrm{ov},s} + \sum_{e \in \mathcal{H}_Q} [\Delta E_{\mathrm{oss},e}]_+ + \sum_{d \in \mathcal{H}_D} V_{R,d} Q_{\mathrm{rr},d} \right].
\end{aligned} \tag{26}
$$

Here, $V^-_{s,\mathrm{on}}$ and $I^+_{s,\mathrm{on}}$ are the switch voltage just before and the switch current just after turn-on, $V^+_{s,\mathrm{off}}$ and $I^-_{s,\mathrm{off}}$ are the corresponding turn-off values, and $V_{R,d}$ is the reverse voltage applied to diode d after a hard commutation. The sets $\mathcal{H}_Q$, $\mathcal{H}_D$ contain hard commutations, $[z]_+ = \max(z, 0)$, and $\Delta E_{\mathrm{oss}} = E_{\mathrm{oss}}(V^-) - E_{\mathrm{oss}}(V^+)$. The reference uses $E_{\mathrm{oss}} = C_{\mathrm{oss,er}} V^2/2$ and assigns no recovery charge to natural current-zero turn-off [33,34]. Characterized switching energies replace overlapping terms to avoid double counting.

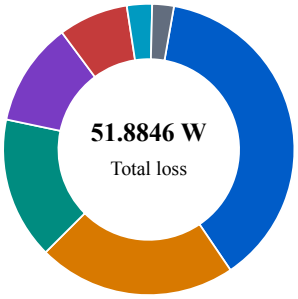
For magnetic flux density $\mathcal{B}$, the generalized Steinmetz model and excess winding loss are [35–37]

$$
\begin{aligned}
P_{\mathrm{core},k} &= \frac{V_{e,k} k_{i,k}}{T_s} (\Delta \mathcal{B}_k)^{\beta_k - \alpha_k} \int_0^{T_s} |\dot{\mathcal{B}}_k|^{\alpha_k}\, \mathrm{d}t, \\
P_{W,\mathrm{ac}} &= \sum_{k,h \geq 1} [R_{\mathrm{ac},k}(h f_s) - R_{W,k}] I^2_{k,h}.
\end{aligned} \tag{27}
$$

Here, $V_{e,k}$ (m^3) is the effective core volume of inductor k, $k_{i,k}$ is its generalized-Steinmetz coefficient, α_k and β_k are the Steinmetz frequency and flux-density exponents, $\Delta\mathcal{B}_k$ (T) is the peak-to-peak flux density, n_w is the number of winding turns, and A_e (m^2) is the effective core cross-section, so that $\dot{\mathcal{B}} = v_L/(n_w A_e)$. $R_{\mathrm{ac},k}(hf_s)$ (Ω) is the winding resistance at harmonic h, and $I_{k,h}$ is the RMS current of that harmonic. Without specified core geometry, the numerical reference substitutes $P_0 \sum_k (f_s/f_0)^{\alpha} (\Delta i_k/\Delta i_0)^{\beta}$ and $\Delta R_{\mathrm{ac},0}\sqrt{f_s/f_0}\sum_k I^2_{k,\mathrm{ac,rms}}$, where P_0 is the core loss of one inductor at the reference frequency f_0 and reference ripple Δi_0, Δi_k is the peak-to-peak ripple of i_k, and $\Delta R_{\mathrm{ac},0}$ is the excess winding resistance at f_0 (Table 7). Gate demand is $P_{\mathrm{gate}} = f_s \sum_s Q_{g,s} V_{\mathrm{drv},s}$.

$$P_{\mathrm{add}} = P_{\mathrm{sw}} + P_{\mathrm{core}} + P_{W,\mathrm{ac}} + P_{\mathrm{gate}} + P_{\mathrm{aux}},$$
$$\eta_{\mathrm{eng}} = \frac{\langle v_o^2\rangle/R}{P_{\mathrm{in,cond}} + P_{\mathrm{add}}}, \qquad \zeta_\lambda = \frac{100 P_\lambda}{\sum_\lambda P_\lambda}. \tag{28}$$

Here, $P_{\mathrm{in,cond}}$ is the source power of the conduction-loss orbit, P_λ is the loss of mechanism λ, and ζ_λ is its percentage share. Conduction losses determine the periodic orbit. Additional losses are evaluated from its waveforms and events, are added to the source power, and do not alter the orbit or the output voltage. Figure 7 gives the nominal 51.8846 W loss estimate. Duty is solved separately for each 400 V case in Table 8, giving 85.73–93.63% estimated efficiency.



Loss mechanism	Power (W)	Share (%)
MOSFET channel	19.5813	37.740
DC winding	11.4194	22.009
Diode forward threshold	7.1483	13.777
Diode dynamic resistance	1.0396	2.004
Switching overlap	5.9825	11.530
Core surrogate	4.0157	7.740
Recovery cells	1.4523	2.799
Output capacitance	0.2471	0.476
Capacitor ESR	0.2520	0.486
Gate networks	0.2400	0.463
AC winding increment	0.0066	0.013
Auxiliary supply	0.5000	0.964

Figure 7. Nominal loss distribution at $V_{\mathrm{in}} = 15$ V, $D = 0.8$, $\delta = 0.5$, $f_s = 100$ kHz, $R = 200\ \Omega$, and imposed 75 °C. Conduction contributes 39.4405 W and additional terms 12.4442 W. The output is 336.3895 V and 565.7896 W, giving 91.60% estimated efficiency. Percentages use total loss. The output is lower than the 359.488 V of the ideal-device circuit of Table 2 because this figure uses the conduction parameters of Table 7. Section 5.3 resolves the difference.

Table 9 gives the influence of temperature and of the main parasitic parameters. Between 25 and 125 °C the estimate falls by 1.93 percentage points and the output voltage by 7.2 V at fixed duty, because the channel and winding resistances rise by 60% and 39%. Channel resistance is the dominant parameter. Doubling it costs 2.86 points, which also indicates the effect of series layout resistance: each milliohm added to all three switch paths costs about 0.11 points. Overlap time, recovery charge, and core loss move the estimate by 0.4–1.3 points across the ranges shown. Commutation-loop inductance, capacitor ESL, and inductor winding capacitance are layout-dependent. They add overshoot to the blocking voltages through $L_\sigma|di/dt|$ and are covered by the voltage margin of the selected devices. The efficiency values are estimates under the stated assumptions.

Table 8. Calculated 400 V operating envelope at $f_s = 100$ kHz and $\delta = 0.5$, using Table 7.

Case	V_{in} (V)	P_o (W)	D	Loss (W)	η (%)
A	12	800	0.872205	133.197	85.727
B	18	800	0.797655	70.653	91.885
C	24	800	0.728227	54.389	93.634
D	12	400	0.863580	39.360	91.041
E	18	400	0.792188	28.301	93.392
F	24	400	0.724069	27.501	93.567

Table 9. Sensitivity of the nominal estimate ($V_{in} = 15$ V, $D = 0.8$, $\delta = 0.5$, $R = 200\ \Omega$) to temperature and loss parameters. One parameter is changed at a time from Table 7. Temperature is imposed on the channel and winding resistances and is not solved from the losses.

Scenario	V_o (V)	Total Loss (W)	η (%)
Reference, 75 °C	336.39	51.88	91.60
25 °C	340.02	46.36	92.58
125 °C	332.84	57.16	90.65
R_{DS} halved/doubled	341.98/325.75	43.32/67.33	93.10/88.74
R_W halved/doubled	339.63/330.09	46.97/61.14	92.47/89.91
Overlap time 10/40 ns	336.39	48.89/57.87	92.05/90.72
Q_{rr} 0/100 nC	336.39	50.43/53.34	91.82/91.39
Core reference 0.5/3 W	336.39	49.21/55.90	92.00/91.01

5.3. Effect of Conduction Loss on the Voltage Gain

The charge balances that give $I_{in} = M_N I_o$ in (7) are topological, so they survive conduction loss as long as the conduction sequence is unchanged. Power balance on the conduction-loss orbit, $V_{in} I_{in} = V_o I_o + P_{cond}$, then gives

$$V_o \simeq M_N V_{in} - \sum_{\lambda} \frac{P_\lambda}{I_o}, \qquad \frac{P_{V_F}}{I_o} = (2N+1)V_F, \tag{29}$$

where the sum runs over the conduction mechanisms. Each mechanism lowers the output by its loss divided by the load current. The diode-threshold term is exact because every external diode carries mean current I_o. Table 10 applies (29) to the nominal point, where $I_o = 1.6819$ A. The five terms sum to 23.45 V, against a simulated drop of 23.61 V from the ideal law. The 0.16 V remainder is the finite-ripple correction of the charge relations. Channel resistance accounts for one half of the drop and winding resistance for 29%. Introducing one mechanism at a time into the ideal-device circuit gives slightly larger individual drops, which sum to 23.84 V, because the branch currents are higher before the other drops are present. The additional losses of (26) and (27) are drawn from the source and do not enter (29). The 23.10 V difference between Figure 7 and the 359.488 V of the ideal-device circuit of Table 2 is, therefore, entirely the conduction drop of Table 7.

Table 10. Composition of the output-voltage drop at $V_{in} = 15$ V, $D = 0.8$, $\delta = 0.5$, $R = 200\ \Omega$, and $N = 2$. The attribution column is P_λ / I_o on the full nonideal orbit. The last column introduces one mechanism alone into the Table 2 circuit.

Step or Mechanism	V_o (V)	P_λ / I_o (V)	Drop Alone (V)
Ideal law (5)	360.000		
Finite capacitance, ESR, r_{D4} (Table 2)	359.488		0.512
MOSFET channel, 26.0 mΩ at 75 °C		11.642	12.009
Winding, 17.9 mΩ at 75 °C		6.790	7.101

Table 10. *Cont.*

Step or Mechanism	V_o (V)	P_λ/I_o (V)	Drop Alone (V)
Diode threshold, 5 × 0.85 V		4.250	4.246
Diode slope resistance, 10 mΩ		0.618	0.485
Capacitor ESR, 1 mΩ		0.150	
All mechanisms (Table 7)	336.389	23.450	

5.4. Scaling with the Cell Count

Table 11 extends the stress and loss evaluation to $N = 1, \ldots, 5$ at a fixed 400 V output from 18 V. Duty is solved for each N with the nonideal model, and every device keeps the parameters of Table 7 and the capacitances of Table 2. Four trends follow. First, the switch blocking voltage falls from 142 V at $N = 1$ to 56 V at $N = 5$, and the largest diode reverse voltage falls from 280 to 99 V. The finite-capacitance maxima exceed the ideal value B^* of (10) increasingly with N, because C_2 transfers NI_oT_s per cycle through a fixed 10 µF. Second, the capacitor-current requirement grows. The RMS current of C_2 rises from 8.1 to 21.7 A, and the sum of the RMS currents of C_1 to C_{2N} rises from 16 to 140 A. Third, conduction loss rises with N, from 41 to 94 W at 800 W, because $2N + 1$ diodes conduct the load current and the upper-branch current NI_o/q grows as the duty falls. The additional losses fall from 25.5 to 8.1 W with the lower blocking voltage and inductor ripple. Fourth, the estimated efficiency is, therefore, highest at $N = 1$ for 800 W (92.32%) and at $N = 2$ for 400 W (93.39%), and it decreases for larger N. The source AC RMS current falls monotonically with N. The comparison holds the device parameters fixed. A lower blocking voltage permits devices with lower channel resistance, so the efficiency penalty of large N is an upper estimate. The baseline $N = 2$ places the switch stress below 90 V, which admits 150 V devices, at the cost of 0.44 points relative to $N = 1$ at 800 W.

Table 11. Effect of the cell count at $V_{\text{in}} = 18$ V, $V_o = 400$ V, $f_s = 100$ kHz, and $\delta = 0.5$, from the piecewise-linear simulator with Table 7. Voltages are maxima over the period. I_{C_2} is the largest capacitor RMS current, and ΣI_C sums the RMS currents of C_1 to C_{2N}. Rows up to ΣI_C refer to 800 W.

Quantity	$N = 1$	$N = 2$	$N = 3$	$N = 4$	$N = 5$
Diodes + capacitors	3 + 3	5 + 5	7 + 7	9 + 9	11 + 11
Duty D	0.8769	0.7977	0.7211	0.6471	0.5756
Ideal B^* (V)	139.3	83.6	59.7	46.4	38.0
Switch blocking voltage (V)	142.4	88.1	67.5	58.8	56.4
Diode reverse voltage (V)	279.9	168.9	125.7	106.0	98.6
Q_3 RMS/peak current (A)	18.1/33.1	23.4/40.0	26.8/43.3	29.6/45.4	31.9/47.1
I_{C_2} (A RMS)	8.06	12.58	16.07	19.05	21.71
ΣI_C (A RMS)	16.1	35.3	62.3	97.9	139.5
Source AC RMS (A)	5.38	4.00	3.23	2.70	2.31
Conduction loss, 800 W (W)	41.04	53.18	66.58	80.21	93.80
Additional loss, 800 W (W)	25.51	17.47	13.09	10.18	8.09
η, 800 W (%)	92.32	91.88	90.94	89.85	88.70
η, 400 W (%)	93.01	93.39	93.25	92.87	92.38

6. Sampled-Data Model and Control

The N-cell converter has $2N+4$ energy states, giving eight states for $N = 2$. Composing the affine conducting-mode flows with diode-event sensitivities yields the linearized period map [38]:

$$\begin{aligned} \hat{\boldsymbol{x}}[k+1] &= \mathbf{A}_d\hat{\boldsymbol{x}}[k] + \mathbf{B}_d\hat{\boldsymbol{u}}[k], \\ \hat{\boldsymbol{y}}[k] &= \mathbf{C}_d\hat{\boldsymbol{x}}[k] + \mathbf{D}_d\hat{\boldsymbol{u}}[k]. \end{aligned} \tag{30}$$

Inputs are $\boldsymbol{u} = [d_{g1}, d_{g2}, V_{\text{in}}, 1/R, \delta]^{\mathsf{T}}$. Outputs include terminal voltage and $i_\Sigma = i_2 + i_3$, averaged over each completed switching period. Capacitor ESR and finite-capacitance

commutation times are retained. Numerical matrices and extraction routines accompany the source.

For common duty, $\boldsymbol{b}_d = \mathbf{B}_d(:,1) + \mathbf{B}_d(:,2)$. Let $\boldsymbol{c}_j$ be the selected row of $\mathbf{C}_d$ and d_{jd} the corresponding summed feedthrough. Then

$$G_{jd}(z) = \boldsymbol{c}_j(z\mathbf{I} - \mathbf{A}_d)^{-1}\boldsymbol{b}_d + d_{jd}, \qquad j \in \{v, i\}. \tag{31}$$

Replacing $\boldsymbol{b}_d, d_{jd}$ with the relevant input column gives line, load, and phase sensitivities. At B, $G_{vd}(1) = 1887.905$ V/duty and $G_{vV_{\text{in}}}(1) = 22.44585$ V/V. The nonminimum-phase voltage zero constrains outer-loop bandwidth.

The outer voltage regulator commands i_Σ^*, and the inner average-current regulator commands common duty. Both use the bilinear mapping $s = (2/T_s)(1 - z^{-1})/(1 + z^{-1})$ [39,40]:

$$C_i(s) = 0.010\frac{1 + 2\pi(150)/s}{1 + s/[2\pi(10000)]}, \qquad C_v(s) = \frac{1 + 2\pi(20)/s}{1 + s/[2\pi(500)]}. \tag{32}$$

Their units are duty/A and A/V. Phase is fixed at $\delta = 0.5$ for the design; the guarded analytical phase is evaluated below. A register applies each command in the next period, giving

$$K_i = z^{-1}C_i, \qquad L_i = K_iG_{id}, \qquad L_v = C_v\frac{K_iG_{vd}}{1 + L_i}, \qquad G_{vr} = \frac{L_v}{1 + L_v}. \tag{33}$$

The plant already includes frame holding and output averaging. At B, current- and voltage-loop crossovers are 2576.6 and 72.29 Hz.

Figure 8a–f shows representative sampled responses.

Identical gains stabilize the six CCM points in Table 8. Minimum inner/outer phase margins are 63.66°/68.71°, and minimum gain margins are 15.62/12.60 dB. The largest evaluated closed-loop spectral radius is 0.999055. These results establish local stability for the stated CCM envelope.

6.1. Slowest Mode and Numerical Accuracy

A mode with multiplier λ decays with time constant $\tau = -T_s/\ln|\lambda|$. At $f_s = 100$ kHz every mode slower than 1 ms has $|\lambda| > 0.990$, so the distance of ρ from unity measures a time constant and is not a stability margin by itself. The value 0.999055 belongs to case C. It is the complex pair $0.99613 \pm \mathrm{j}\,0.07644$, a 1.22 kHz oscillatory mode whose envelope decays with $\tau = 10.58$ ms and damping ratio 0.012. Table 12 lists the slowest mode of each case. Case A is governed by a real 5.8 ms mode. The other cases are governed by lightly damped pairs between 0.6 and 1.2 kHz with envelope time constants of 5.3–10.6 ms. These pairs are the resonance between the multiplier capacitors and the inductors. With the loops open the same resonance decays in 3.6 ms at case C ($\rho = 0.99722$). Closing the loops, therefore, lowers its damping, and this resonance sets the slowest closed-loop time constant. The 24.75 ms recovery to 0.1 V reported in Section 7 for case B is consistent with its 7.1 ms modes acting on a 1.44 V excursion.

The numerical uncertainty of ρ is far below its distance from unity. The state Jacobian is variational and agrees with an independent finite-difference Jacobian. Halving or doubling the finite-difference steps of the input matrices changes ρ at case C by less than 6×10^{-12}, against $1 - \rho = 9.45 \times 10^{-4}$.

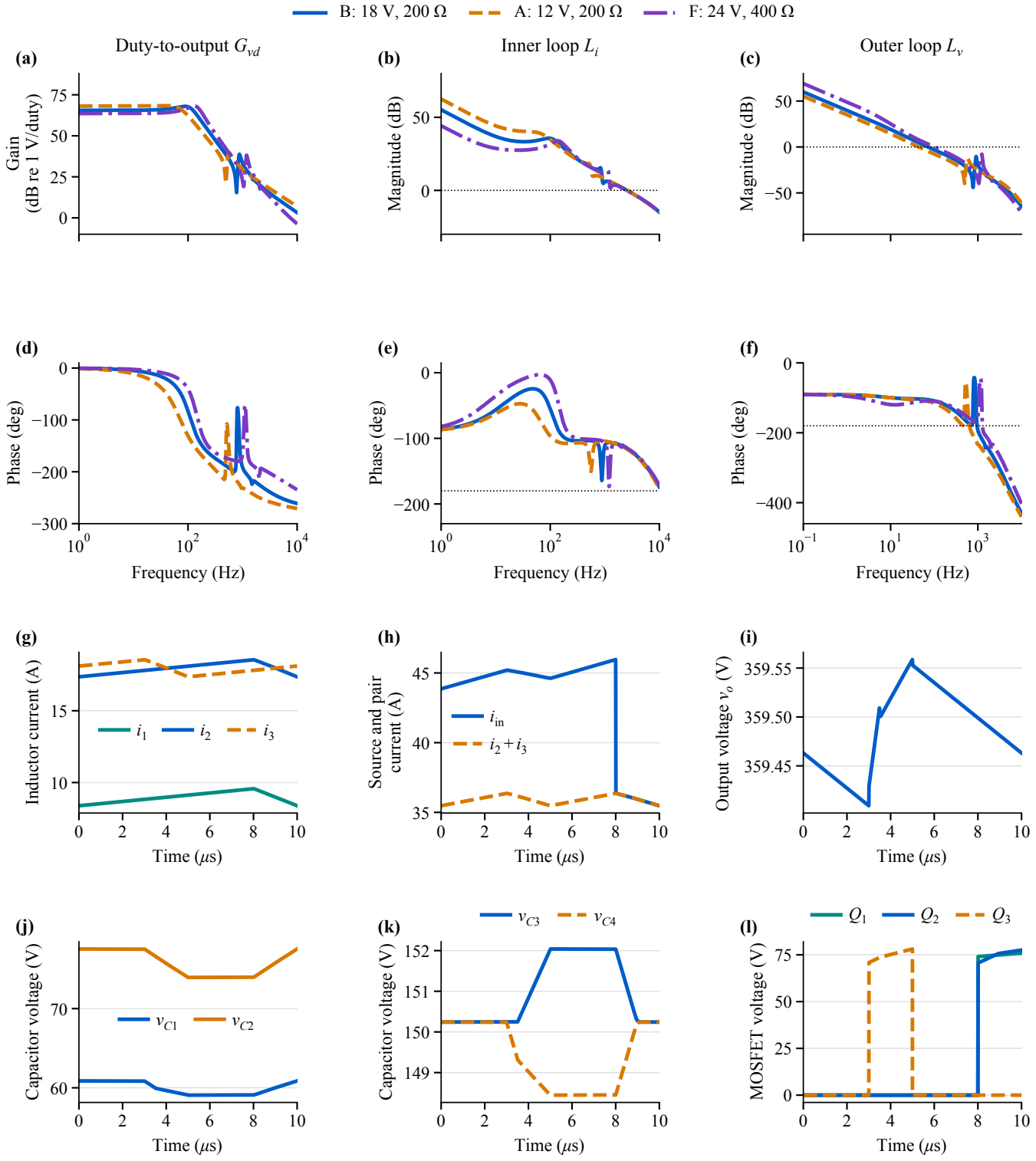


Figure 8. Sampled responses and nominal periodic waveforms. (**a**–**c**) Magnitudes and (**d**–**f**) phases of G_{vd}, L_i, and L_v for cases A, B, and F. The model retains eight energy states, diode-event sensitivities, cycle averaging, and next-period duty application. Margins cover all six cases and crossings below the 50 kHz Nyquist frequency. (**g**–**l**) One period under Table 2: inductor currents, source and upper-pair currents, output voltage, capacitor voltages in (**j**,**k**), and switch blocking voltages. The gated L_1 branch produces source-current steps.

Table 12. Slowest closed-loop mode of each case at $\delta = 0.5$, with envelope time constant $\tau = -T_s/\ln|\lambda|$, and the time constant of the slowest open-loop mode.

Case	V_{in} (V)	P_o (W)	ρ	Slowest Mode	τ (ms)	Open-Loop τ (ms)
A	12	800	0.998271	real	5.78	4.31
B	18	800	0.998599	0.91 kHz pair	7.13	3.97
C	24	800	0.999055	1.22 kHz pair	10.58	3.59
D	12	400	0.998102	0.62 kHz pair	5.26	4.28
E	18	400	0.998540	0.94 kHz pair	6.85	3.95
F	24	400	0.999014	1.24 kHz pair	10.14	3.57

6.2. Margins at the Guarded Analytical Phase and Under Parameter Perturbation

The linearization was repeated at the guarded analytical phase δ_c of Section 7, which lies between 0.138 and 0.292 for the six cases. The compensators were not retuned. The minimum inner/outer phase margins become 65.39°/68.75° and the minimum gain margins 17.23/12.72 dB, and the largest spectral radius is 0.999058. The phase displacement, therefore, has no adverse effect on the local margins. The inner-loop margins are 1–2° and 1.0–1.6 dB larger than at $\delta = 0.5$.

Table 13 gives the worst margins over the six cases when the circuit is perturbed and the duty is re-solved for 400 V. All 72 perturbed operating points remain locally stable. Lower inductance reduces the inner phase margin to 58.8°, and the other single perturbations leave phase margins above 63°. The lowest margins occur at 24 V input (cases C and F). With inductance 20% high and capacitance 20% low, the multiplier resonance near 1.24 kHz adds gain crossovers. The phase margins are then 18.7° and 25.4°, the modulus margins 0.22 and 0.23, and the slowest mode has $\tau = 60$ ms. At 25 °C the lower resistive damping lets the inner loop gain cross −180° twice near 1.2 kHz while it exceeds unity. The loop is then stable, with $\rho = 0.99944$ and a lower gain margin of 5.2–10.2 dB. The fixed compensators are, therefore, stable over the full perturbation set. Larger margins at the 24 V corner can be obtained by damping the multiplier resonance, for example with a notch in C_i or a damping network across C_2, or by a lower current-loop bandwidth.

Table 13. Worst local margins over cases A–F under parameter perturbation at $\delta = 0.5$, with the duty re-solved for 400 V and the compensators of (32) unchanged. L scales the three inductances and C all five capacitances. PM and GM are phase and gain margins of the inner (i) and outer (v) loops, $\min|1 + L|$ is the modulus margin, and τ is the slowest envelope time constant with its case.

Perturbation	PM_i (°)	GM_i (dB)	PM_v (°)	GM_v (dB)	$\min\|1+L_i\|$	$\min\|1+L_v\|$	ρ	τ (ms)
Nominal	63.7	15.6	68.7	12.6	0.58	0.70	0.99905	10.6 (C)
L −20%	58.9	13.7	69.2	16.8	0.67	0.81	0.99864	7.4 (C)
L +20%	66.8	17.2	68.2	8.3	0.38	0.51	0.99952	20.9 (C)
C −20%	63.7	15.6	69.7	9.0	0.39	0.57	0.99935	15.4 (C)
C +20%	63.7	15.6	66.5	15.2	0.72	0.76	0.99885	8.7 (C)
L −20%, C −20%	58.9	13.7	70.2	14.1	0.62	0.76	0.99871	7.8 (C)
L −20%, C +20%	58.8	13.7	66.9	18.9	0.67	0.84	0.99855	6.9 (C)
L +20%, C +20%	66.8	17.2	66.2	11.6	0.54	0.64	0.99931	14.4 (C)
L +20%, C −20%	18.7	17.2 [a]	25.4	3.3	0.22	0.23	0.99983	60.5 (C)
Capacitor ESR ×10	63.6	15.6	68.7	13.2	0.61	0.72	0.99897	9.7 (C)
25 °C	63.3	15.6 [a]	68.9	9.9	0.40	0.57	0.99944	18.0 (C)
125 °C	64.0	15.6	68.6	14.4	0.72	0.76	0.99867	7.5 (C)

[a] Conditionally stable: the inner loop gain also crosses −180° twice near 1.2 kHz while above unity (cases C and F). The listed GM is the margin against a gain increase.

At a transverse DCM extinction, physical states remain continuous while the variational state changes through [41]

$$\mathbf{S}_k = \mathbf{I} + \frac{(\boldsymbol{f}^+ - \boldsymbol{f}^-)\boldsymbol{e}_k^{\mathsf{T}}}{f_k^-}, \qquad f_k^- \neq 0. \tag{34}$$

Here, $\boldsymbol{f}^{-}$,$\boldsymbol{f}^{+}$ are the pre- and post-event vector fields, and $\boldsymbol{e}_k$ selects the extinguishing current. Asynchronous extinctions require ordered event and zero-current dwell maps. Their closed-loop Jacobian must satisfy $\rho(\mathbf{J}_{\mathrm{cl}}) < 1$. State continuity alone does not establish stability across a conduction boundary. The reported margins certify the six CCM points. The sampled model and its margins do not apply once a branch enters DCM. Section 7.4, therefore, examines a transition into mixed conduction by switching simulation.

7. Results and Validation

7.1. Simulation Methods and Their Agreement

Every result in this section is numerical. Three simulators are used: two solvers written for this work, which share no code, and the commercial simulator PLECS.

The first is the event-driven solver used throughout Sections 2–6. It propagates each circuit configuration to the next gate or diode event with ideal diodes that satisfy complementarity conditions. Shooting enforces periodic states, and interval quadrature evaluates mean and RMS quantities. Across 23 baseline cases, the largest power-balance residual is 5.14×10^{-8} W. These calculations use the extracted circuit parameters in Table 2.

The second is a piecewise-linear switching simulator written for this revision. Every MOSFET channel, body diode, and diode is a two-state resistor, with on-resistance and threshold when conducting and 10 MΩ when blocking. This is the device model of circuit simulators of the PLECS and SPICE class. No conduction sequence is prescribed. Each device changes state when its own current or voltage changes sign. Between state changes the linear network is advanced with the matrix exponential on a 5 ns grid, and a step is split at every gate edge and at every detected commutation. The simulator accepts any gate pattern, any stage count, discontinuous conduction, a source impedance, and a controller executed once per period. Ideal devices are represented by 10 μΩ.

Table 14 compares the two simulators. For the ideal-device circuit all quantities agree within 0.002%. For the loss model of Section 5 the output voltage, both loss totals, and the efficiency estimate agree within 0.001%, and the six 400 V cases of Table 8 are reproduced within 0.6 mV, 1 mW, and 0.001 points. The piecewise-linear results do not change in the digits shown when the step is 2 or 10 ns. This agreement confirms the numerical solutions.

Table 14. Agreement of the two independent simulators. The piecewise-linear results use a 5 ns step; steps of 2 and 10 ns give the same digits.

Quantity	Event-Driven	Piecewise-Linear	Difference (%)
Table 2 parameters			
Output voltage (V)	359.488	359.482	−0.001
Mean source current (A)	43.118	43.118	−0.001
Source AC RMS (A)	3.6174	3.6173	−0.001
Source peak-to-peak (A)	10.484	10.484	−0.001
Source peak (A)	45.960	45.960	−0.001
Terminal ripple, peak-to-peak (mV)	149.45	149.45	−0.001
Capacitor-state ripple, peak-to-peak (mV)	143.79	143.79	0.001
Table 7 parameters, $V_{\mathrm{in}} = 15$ V, $D = 0.8$			
Output voltage (V)	336.390	336.389	<0.001
Conduction loss (W)	39.440	39.441	0.001
Additional loss (W)	12.444	12.444	<0.001
Estimated efficiency (%)	91.600	91.599	−0.001
Six 400 V cases at the duty of Table 8			
Output voltage, largest deviation from 400 V			0.0006 V
Total loss, largest difference			0.001 W
Estimated efficiency, largest difference			0.001 points

The third simulator is PLECS Standalone 4.7.5. The supplied circuit file (File S1 in the Supplementary Materials) was parameterized, probes were connected to output ports, and the simulations were driven from MATLAB over the PLECS remote interface. Table 15 compares PLECS with the reference values. For the ideal-device circuit the output voltage, source current, and both ripple quantities agree within 0.002%, and the source AC RMS values within 0.05%. PLECS also reproduces the 4.75% reduction of source AC RMS at $\delta = 0.2$ (4.746%), the 8.338 mA residual excursion with $L_3 = 2L$, the mixed-conduction gain at 4 kΩ, and the loss of output voltage outside the gate domain of (1). Figure 9 shows the PLECS model, and Figure 10 overlays its waveforms on those of the piecewise-linear simulator. The inductor currents of the two simulators differ by less than 0.2 mA RMS over a period, in continuous conduction and with one branch discontinuous. With the conduction parameters of Table 7, PLECS gives 336.390 V at the nominal point and the six 400 V cases within 0.4 mV. Two further sweeps are not listed in the table. The source AC RMS values of Table 3 are reproduced within 0.17% at all five loads, at $\delta = 0.5$ and at the rule value. The output voltage for duty ratios from 0.55 to 0.90 agrees with the piecewise-linear simulator within 0.009%. In PLECS the first branch is discontinuous at 3.1 kΩ and continuous at 2.9 kΩ, which brackets the predicted 3.0 kΩ boundary.

Two settings of the PLECS runs are noted. Cases C to F use the duty rounded to four decimals, which gives the PLECS pulse generators a common time base, and the reference values were computed at the same duties. Five runs use 0.1 mΩ switch and diode resistances in place of ideal devices for numerical robustness; these are marked in Table 15 where they appear. The three simulators, thus, give one consistent set of results for the same component models.

Table 15. PLECS results against the reference values of this paper. The reference is the event-driven solver where it reports the quantity and the piecewise-linear simulator otherwise. PLECS used the variable-step solver with a relative tolerance of 10^{-6} and 1–1.5 s of simulated time for the ideal-device circuit.

Quantity	Reference	PLECS	Difference (%)
Table 2 parameters, $\delta = 0.5$ unless stated			
Output voltage (V)	359.488	359.488	<0.001
Mean source current (A)	43.118	43.119	0.001
Source AC RMS (A)	3.6174	3.6188	0.038
Source peak-to-peak (A)	10.484	10.484	0.002
Terminal ripple, peak-to-peak (mV)	149.45	149.45	0.001
Capacitor-state ripple, peak-to-peak (mV)	143.79	143.79	0.002
Source AC RMS at $\delta = 0.2$ (A)	3.4454	3.4470	0.047
Output voltage with $L_3 = 2L$ (V)	359.526	359.526	<0.001
Residual excursion in $\mathcal{A}$ with $L_3 = 2L$ (mA)	8.338	8.338	−0.006
Gain at $R = 4$ kΩ (one branch discontinuous)	25.0907	25.0907	<0.001
Gain at $R = 10$ kΩ (all discontinuous) [a]	33.0477	33.0546	0.021
Output at $D = 0.8$, $\delta = 0.15$ (V)	322.2	322.1	−0.017
Output at $D = 0.8$, $\delta = 0.10$ (V)	209.6	209.6	0.023
Table 7 conduction parameters			
Output voltage, 15 V, $D = 0.8$ (V)	336.390	336.390	<0.001
Conduction loss, 15 V, $D = 0.8$ (W)	39.44	39.43	−0.021
Q_3 RMS current, 15 V, $D = 0.8$ (A)	19.895	19.895	0.002
Six 400 V cases: largest output-voltage difference			0.4 mV
Six 400 V cases: largest conduction-loss difference			0.13 W

[a] PLECS run with 0.1 mΩ switch and diode resistances, because the ideal-device circuit stopped with a switching error.

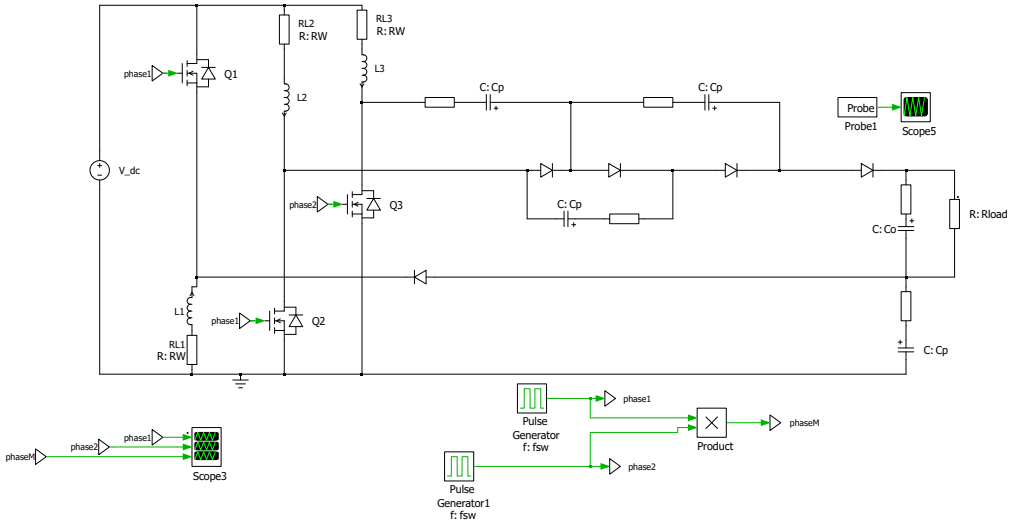


Figure 9. PLECS model used for Table 15, as exported from PLECS. The switches Q_1 and Q_2 share the gate signal `phase1`, and Q_3 is driven by `phase2`, which is displaced by δ. The resistors `RL1`–`RL3` are the winding resistances of the loss model, and the unlabeled resistors are the capacitor ESRs. Green arrows are control-signal connections, and black lines are electrical connections.

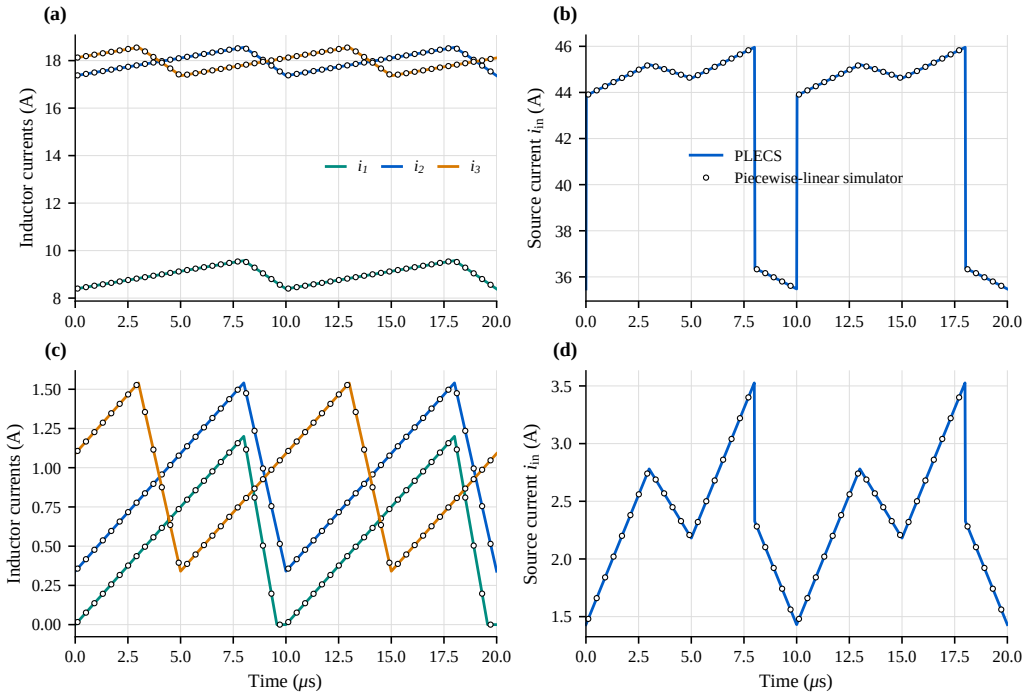


Figure 10. Steady-state waveforms from PLECS (lines) and from the piecewise-linear simulator (circles) for the parameters of Table 2. (**a**,**b**) Inductor currents and source current at $R = 200\ \Omega$, with all branches in continuous conduction. (**c**,**d**) The same quantities at $R = 4\ \mathrm{k}\Omega$, where the L_1 branch is discontinuous.

7.2. Steady-State Performance

Figures 8g–l and 11a–d show the converged periodic waveforms. The positive and negative output rails average 299.561 and −59.927 V. Their differential voltage is 359.488 V, within 0.143% of ideal CCM. Table 16 reports two distinct output-ripple quantities, both peak-to-peak. The capacitor-state ripple is the excursion of the internal voltage of C_o and is the quantity predicted by (9). The terminal ripple is the excursion of $v_o = v_p - v_n$ at the load. It adds the step produced by the 1 mΩ ESR of C_o when the output-diode current

commutates, which raises the ripple from 143.79 to 149.45 mV. At the same input, duty, frequency, and resistance, $N = 1, 2, 3$ produce 209.893, 359.488, and 508.652 V.

Table 16. Nominal performance at 15 V, $D = 0.8$, 100 kHz, $R = 200\ \Omega$, and $\delta = 0.5$ with the ideal devices of Table 2. All ripple entries are peak-to-peak values. The ideal column has zero ESR.

Quantity	Ideal CCM	Finite Capacitance
Output voltage (V)	360.000	359.488
Output power (W)	648.000	646.157
Mean source current (A)	43.200	43.118
Source AC RMS (A)	3.627	3.617
Source peak-to-peak ripple (A)	10.500	10.484
Output-capacitor state ripple, excluding ESR (mV, peak-to-peak)	144.00	143.79
Load-terminal ripple, including ESR (mV, peak-to-peak)	144.00	149.45

Energy conservation requires

$$p_{\text{in}} = p_o + p_{\text{diss}} + \frac{\mathrm{d}W}{\mathrm{d}t}, \qquad W = \frac{1}{2}\sum_k L_k i_k^2 + \frac{1}{2}\sum_c C_c v_c^2. \tag{35}$$

Periodic averaging gives $P_{\text{in}} = P_o + P_{\text{diss}}$. The baseline supplies 646.7697 W, comprising 646.1571 W output and 0.61256 W dissipation. Section 5 adds the nonideal engineering loss budget.

7.3. Application Envelope and Load Response

Table 8 evaluates 400 V operation at 12, 18, and 24 V inputs with 400 and 800 W loads. The guarded rule $\delta_c = \text{clip}_{[q+0.01, D-0.01]}[1/2 - V_o^* L f_s/(2RV_{\text{in}})]$ retains 100 ns between gate commands. Re-solving duty at each phase preserves output power and reduces source AC RMS by 2.26–9.01%. Estimated efficiency changes by less than 0.007 percentage points. The small efficiency change has a direct explanation. A phase displacement shifts the waveform of the third branch in time and leaves the waveform of every inductor current, the mean current of every diode, and the commutation voltages unchanged. Winding, diode, switching, and core losses are, therefore, unchanged. The only internal change is the overlap of i_3 with the transferred current $h_B i_2$ in Q_3, which raises the channel loss by 0.02–0.06 W and lowers the estimate by 0.005–0.006 points. The reduction of source AC RMS acts outside this budget, in the input capacitor and the source. With a 5 mΩ input-capacitor ESR, for example, the heating in case B falls from 80 to 73 mW. Phase selection is, thus, a measure of source-current quality and capacitor stress and is not an efficiency measure. The 12 V, 800 W case requires 933.197 W source power, or 77.766 A mean current. PV or battery operation requires matching source power and current capability, a floating driver for Q_1, and separation of the negative output return from input ground [42–44].

Figure 11e–h applies a 5% conductance increase to the local sampled model at 18 V input and 400 V output. The initial load increment is 40 W. The predicted dip is 1.436 V, with recovery within 0.1 V after 24.75 ms.

7.4. Closed-Loop Switching Simulations

The piecewise-linear simulator was run in closed loop with the conduction parameters of Table 7 and $N = 2$. The controller of Section 6 is executed once per switching period on the cycle means of v_o and i_Σ, and its command is applied in the next period. The duty is limited to $[0.51, 0.93]$, so that (1) holds throughout, and the current reference to $[0, 120]$ A, with conditional integration as anti-windup. The simulation uses ideal PWM timing and ideal sensing. Figures 12 and 13 show the results.

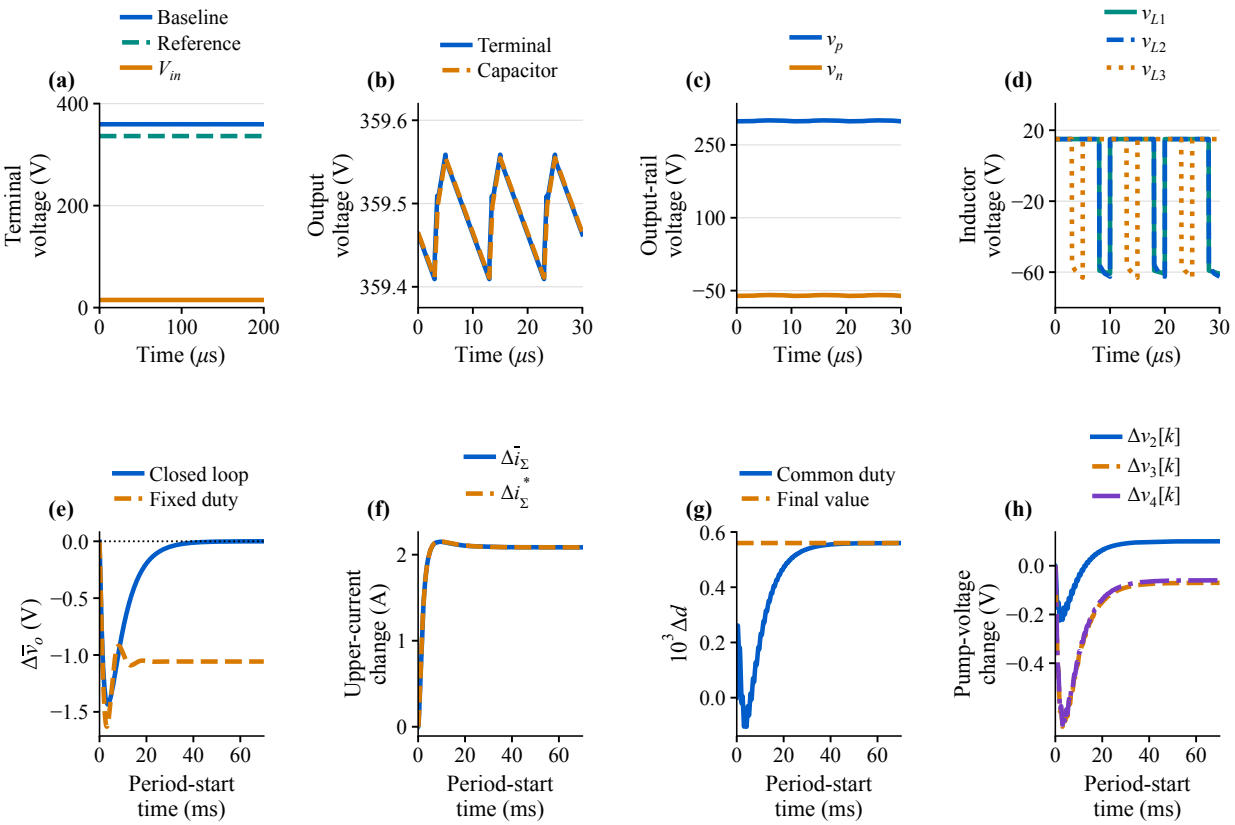


Figure 11. Steady operation and local load response. (**a**–**d**) $V_{\text{in}} = 15$ V, $D = 0.8$, $f_s = 100$ kHz, $R = 200\ \Omega$, and $\delta = 0.5$: output voltage over repeated periods, terminal and capacitor-state ripple, output rails, and inductor voltages. Panel (**a**) compares baseline and nonideal-reference outputs. Panels (**b**–**d**) use baseline parameters. (**e**–**h**) Local sampled response at 18 V input, 400 V output, $R = 200\ \Omega$, and $\delta = 0.5$ to a +5% conductance step: output-voltage deviation, upper-current deviation and reference, duty deviation, and pump-voltage deviations. Compensators follow Section 6. The linear response excludes switching ripple.

Agreement with the sampled model: For the 5% conductance step of case B the switching simulation gives a dip of 1.431 V at 3.54 ms and recovery within 0.1 V after 24.95 ms. The sampled linear model predicts 1.436 V at 3.54 ms and 24.75 ms (Figure 12a,b). The nonlinear switched circuit, thus, confirms the local model.

Operation at the selected phase: The same test was repeated with the phase scheduled in every period from the sensed current, $\delta_c[k] = \text{clip}_{[q+0.01, D-0.01]}[1/2 - \bar{\imath}_\Sigma qLf_s/(4NV_{\text{in}})]$, which is (13) with $I_1 = \bar{\imath}_\Sigma/(2N)$. The phase settles at 0.212. The response is indistinguishable from that at $\delta = 0.5$: the dip is 1.431 V and the recovery time 24.96 ms. The large load steps below also give the same excursions with the scheduled phase.

Start-up: The start-up sequence keeps $D > \frac{1}{2}$. The duty is held at or above 0.51 and the input voltage is ramped, as an input soft-start or precharge stage does. From zero state with $R = 200\ \Omega$, the input rises to 18 V in 10 ms and the reference to 400 V in 30 ms (Figure 12c,d). While the duty is at its lower limit the output follows the input and reaches 166 V, with inductor currents below 10.8 A and a source current below 26.1 A. The controller raises the duty from 11.6 ms onward. The output overshoots by 4.10 V (1.0%) and stays within 1% from 7.1 ms after the end of the ramp. The largest inductor current is 32.2 A, the largest source current 79.9 A, and the largest switch voltage 89.2 V, against 88.2 V in the final steady state. The input ramp limits the inrush current: without it, enabling the gates at $D = 0.51$ on the full 18 V gives a 73 A inductor-current peak.

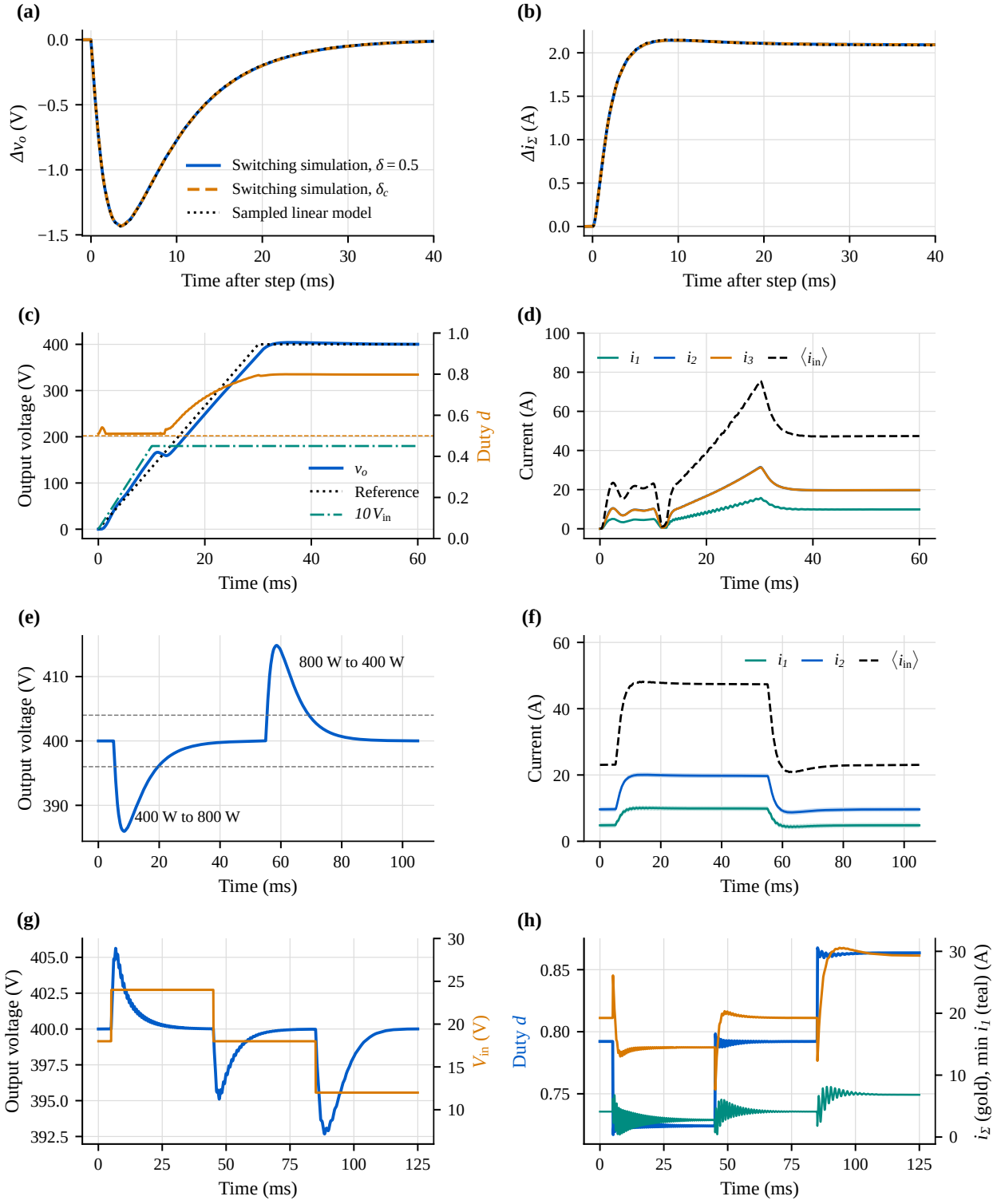


Figure 12. Closed -loop switching simulations with Table 7 parameters, $N = 2$, and $V_o^* = 400$ V. Lines are cycle means and shaded bands are the extrema within each period. (**a**,**b**) 5% conductance step at 18 V and 800 W: deviations of v_o and i_Σ at $\delta = 0.5$, at the scheduled phase δ_c, and from the sampled linear model. (**c**,**d**) Start-up at $R = 200\ \Omega$ with a 10 ms input-voltage ramp to 18 V, a 30 ms reference ramp, and the duty held above 0.5: output (blue), reference (dotted), ten times the input voltage (dash-dotted), and duty (orange), and inductor and mean source currents (i_2 lies beneath i_3). The dashed orange line marks $d = 0.5$. (**e**,**f**) Load steps 400 to 800 W and back at 18 V, with the ±1% band. (**g**,**h**) Input steps 18, 24, 18, and 12 V at 400 W: output (blue) and input voltage (orange), and duty (blue), i_Σ (gold), and the valley of i_1 (teal).

Load steps: A step from 400 to 800 W produces a dip of 14.05 V (3.5%), and the reverse step an overshoot of 14.84 V (3.7%). The output returns within 1% after 14.6 and 14.2 ms and within 0.1 V after 41.0 and 36.6 ms (Figure 12e,f). All three branches stay in continuous conduction. Figure 13a,b shows the inductor currents and the output voltage across the step instant at switching resolution.

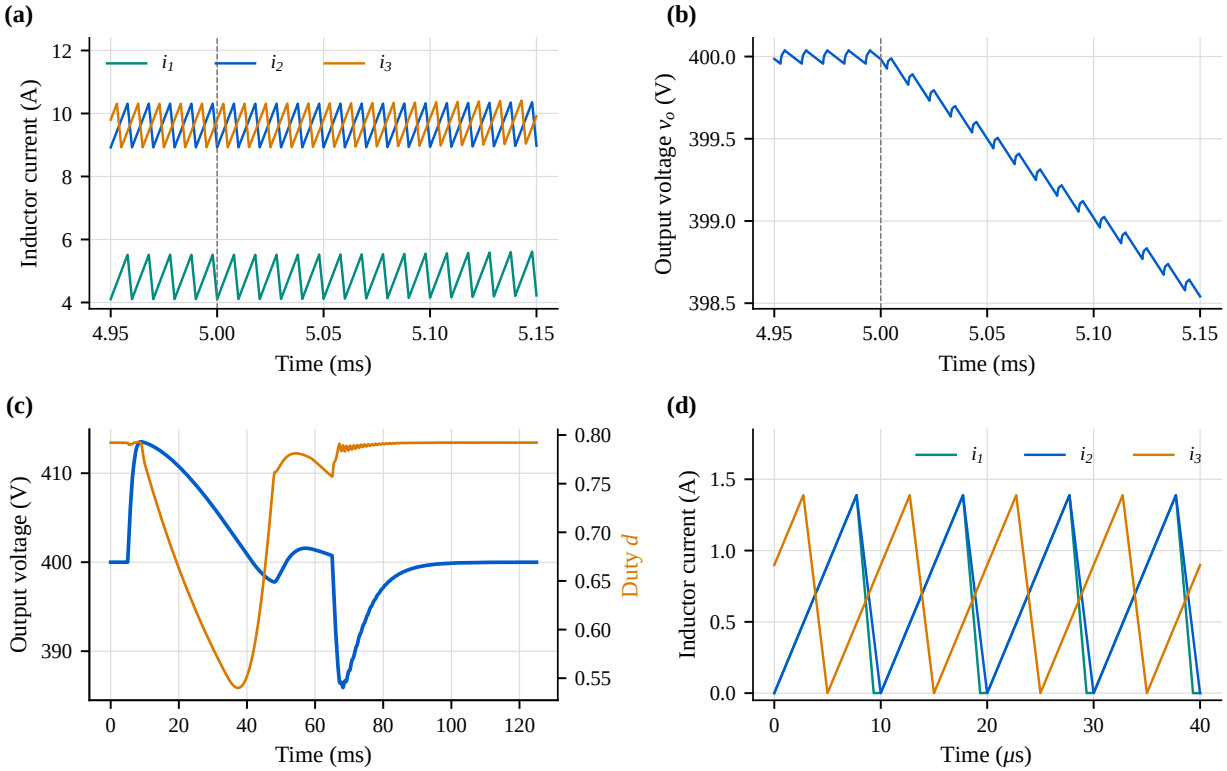


Figure 13. Switching-resolution waveforms and the light-load transition. (**a**,**b**) Inductor currents and output voltage across the 400 to 800 W load step of Figure 12e, applied at 5.00 ms (dashed line). (**c**) Output voltage (blue) and duty (orange) for load steps 400 to 40 W at 5 ms and back at 65 ms. (**d**) Inductor currents over four periods at 40 W, where all three branches are discontinuous.

Input-voltage steps: At 400 W, steps of 18 to 24 V, 24 to 18 V, and 18 to 12 V give excursions of +5.63, −4.89, and −7.33 V and return within 1% after 3.6, 3.7, and 10.4 ms (Figure 12g,h). Each step excites the lightly damped mode of Table 12, at 1.2, 1.0, and 0.6 kHz for the three steps. It is visible in the duty and in the valley of i_1 and decays in 15–20 ms. At 24 V the valley of i_1 is 0.39 A, so the branch remains in continuous conduction.

Light load and discontinuous conduction: A step from 400 to 40 W ($R = 4\,\mathrm{k}\Omega$) takes all three branches into discontinuous conduction (Figure 13c,d). The output rises by 13.5 V (3.4%), the current reference saturates at its lower limit, and the output returns within 1% after 29.3 ms. Thereafter the output stays within the ±1% band, between 397.8 and 403.6 V, while the duty varies between 0.54 and 0.78. The switch voltage reaches 122.6 V, because the capacitor voltages redistribute when the duty falls at a regulated output, and this value sets the device rating for light-load operation. On return to 400 W the dip is 14.1 V and the output is within 1% after 12.9 ms. The compensators designed for continuous conduction, therefore, hold the output within 1% in discontinuous conduction. Mode-dependent gains or a minimum load would smooth the duty further.

Worst perturbed corner: At 24 V, 800 W, inductances 20% high, and capacitances 20% low, the 5% step gives a 1.19 V dip followed by a 1.245 kHz oscillation whose envelope decays with a 63 ms time constant. The linear analysis of Section 6.2 predicts 1.241 kHz and 60.5 ms. The oscillation amplitude is 6 mV on the output for this small step.

7.5. Design Surfaces

Figures 14 and 15 summarize twelve parameter surfaces. Inadmissible CCM and duty regions are masked. Connections between integer stage counts provide visual interpolation only. Efficiency and loss surfaces use 81 nonideal periodic solutions. Input-capacitance sizing assumes $\delta = 0.5$, constant upstream current, and zero ESR/ESL.

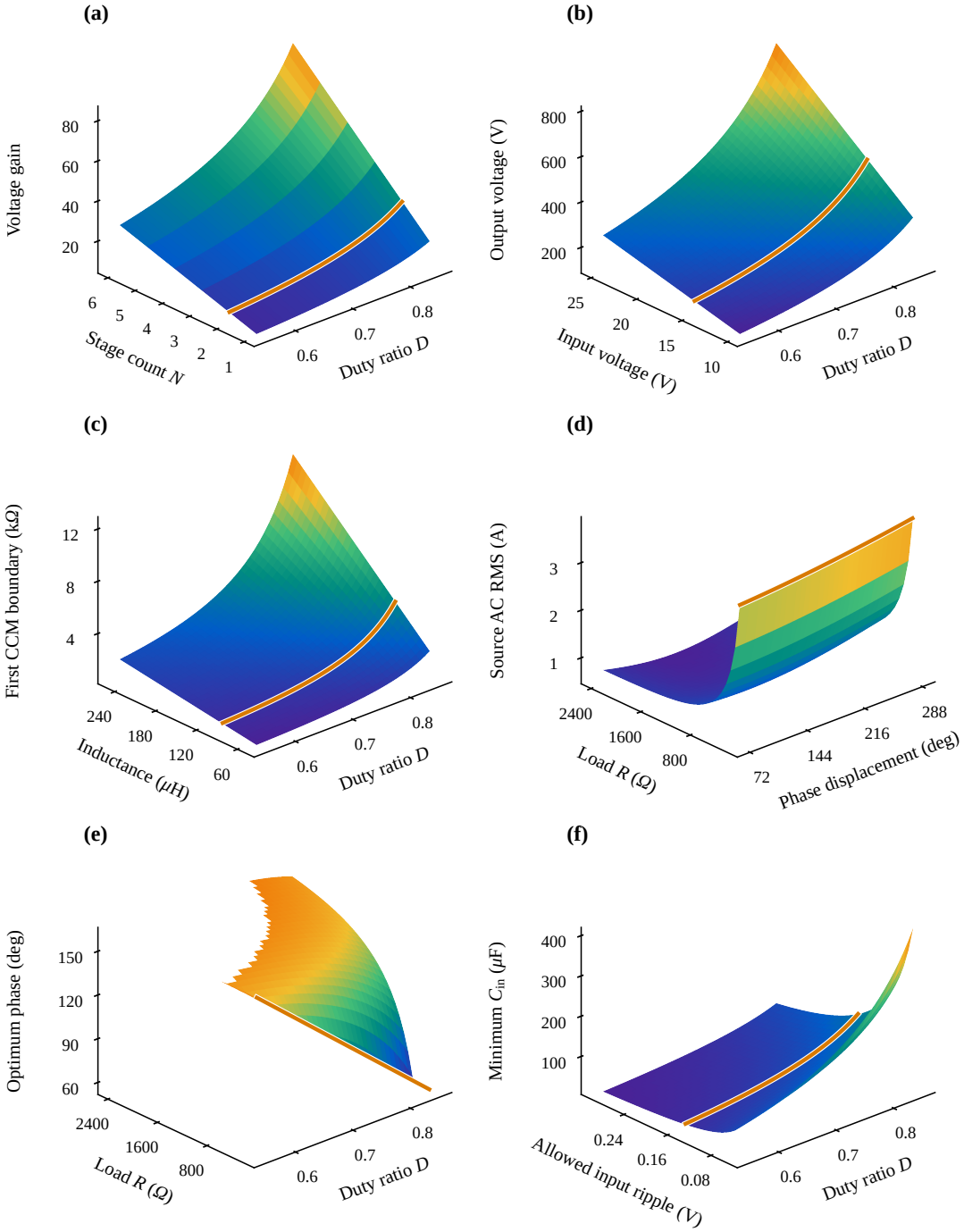


Figure 14. Analytical design surfaces. (**a**) Gain versus duty and stage count. (**b**) Output voltage versus duty and input. (**c**) First CCM boundary versus duty and inductance. (**d**) Source AC RMS versus phase and load. (**e**) Optimum phase versus duty and load. (**f**) Input capacitance versus duty and allowed ripple. Unvaried parameters are 15 V, $D = 0.8$, $\delta = 0.5$, 100 µH, 100 kHz, $N = 2$, and 200 Ω. Surface color encodes the vertical-axis value. Amber curves mark the sections at these reference values.

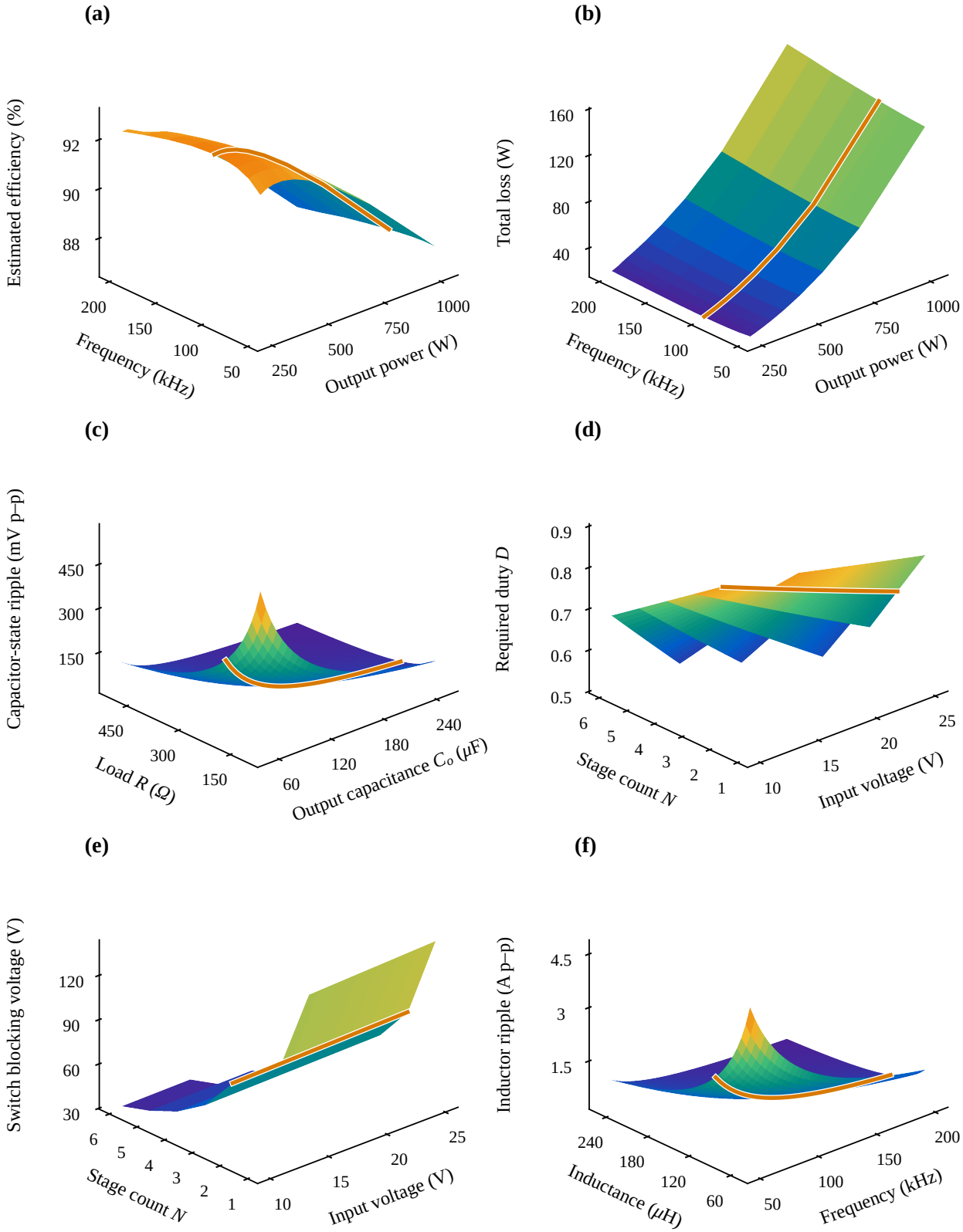


Figure 15. Loss and component-design surfaces. (**a**,**b**) Estimated efficiency and loss versus output power and frequency under Table 7. (**c**) Capacitor-state output ripple versus capacitance and load. (**d**,**e**) Duty and switch voltage versus input and stage count for 400 V output. (**f**) Inductor ripple versus frequency and inductance. Unvaried parameters follow Figure 14. Surface color encodes the vertical-axis value. Amber curves mark reference sections.

8. Conclusions

This paper analyzed a three-inductor interleaved converter with a scalable voltage multiplier in which one inductor reaches the source through a series switch. The conclusions are stated in three groups.

Analytical contributions: The physical input current determines phase selection in this three-inductor converter. The derived gain is $(2N + D)/(1 - D)$, with switch stress $V_o/(2N + D)$ and explicit current-sharing and capacitor-ripple laws for N cells. The source AC RMS current has a closed-form constrained minimum in the phase displacement. A slope-cancellation condition exists for unequal inductances. Mixed-mode laws identify successive current-extinction boundaries, and conduction loss lowers the output by each loss divided by the load current.

Numerically demonstrated performance: At the nominal point, 72° displacement reduces source AC RMS by 4.75% relative to 180°, while doubling upper-pair ripple. The reduction is 2.3–9.0% over the 400 V envelope and leaves the efficiency estimate unchanged, so it improves source-current quality and capacitor stress at no hardware cost. With $L_3 = 2L$ the ideal source-current slope in one interval is zero, and finite capacitance leaves a residual excursion of 8.34 mA. Charge-transfer-aware loss estimates span 85.73–93.63% across six 400 V cases. The common sampled controller achieves minimum current- and voltage-loop phase margins of 63.66° and 68.71° at those CCM points. PLECS and a second, independent switching simulator reproduce the steady-state results within 0.05%. The second simulator also reproduces the local load response within 0.4% and shows regulated start-up, 400–800 W load steps with 3.7% excursion, and 12–24 V input steps with 1.8% excursion.

Future work: The controller is locally stable at all 72 perturbed operating points, and the analysis identifies the 0.6–1.2 kHz multiplier resonance as the mode that sets its margins. Damping this resonance, mode-dependent gains for discontinuous conduction, and experimental verification on a hardware prototype are the planned extensions. These results provide separate design criteria for source-current quality, device stress, and local control stability.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronics15235604/s1, File S1: PLECS models of the converter with ideal devices (`Interleaved_R1_base.plecs`) and with the conduction parameters of the loss model (`Interleaved_R1_losses.plecs`), and the MATLAB script that runs the PLECS simulations of Section 7 (`run_plecs_experiments.m`) with its helper function for the PLECS remote interface (`plecs_rpc.m`).

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Data Availability Statement: The data and scripts supporting the reported results are available from the author on request.

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Conflicts of Interest: The author declares no conflicts of interest.

Appendix A. Principal Symbols

Table A1. Principal symbols. Uppercase currents and voltages are period means, and lowercase quantities are instantaneous.

Symbol	Meaning	Unit
V_{in}, $v_o = v_p - v_n$, V_o^*	Input voltage, differential output voltage, output reference	V
v_p, v_n	Positive and negative output-rail potentials relative to source ground	V
N	Number of voltage-doubling cells	–
D, $q = 1 - D$, d	Steady duty ratio, its complement, commanded duty	–
δ, δ^*_{RMS}, δ_c	Normalized phase delay of g_2, its RMS-optimal value, guarded value	–
f_s, T_s, $s = t/T_s$	Switching frequency, period, normalized time	Hz, s, –
g_1, g_2; $h_A = 1 - g_2$, $h_B = 1 - g_1$	Gate commands of Q_1, Q_2 and of Q_3; their complements	–
$\mathcal{O}$, $\mathcal{A}$, $\mathcal{B}$	Both-ON interval, Q_3-OFF interval, Q_1, Q_2-OFF interval	–
$B = V_{\text{in}}/q$, B^*	Base clamp voltage, its value at a fixed output	V
M_N	Ideal CCM voltage gain $(2N + D)/q$	–
L_k, i_k, I_k	Inductance, current, and mean current of branch $k = 1, 2, 3$	H, A, A
$\Delta_k = V_{\text{in}} D/(L_k f_s)$	Peak-to-peak inductor-current ripple	A
i_{in}, I_{in}, $I_{\text{in,ac}}$	Source current $g_1 i_1 + i_2 + i_3$, its mean, its AC RMS value	A
$i_\Sigma = i_2 + i_3$	Upper-pair current sensed by the controller	A
I_o, R	Load current, load resistance	A, Ω
Q_1–Q_3	MOSFETs: series switch of L_1, and legs b and c	–
D_1; D_2–D_{2N}; D_o	Return diode; ladder diodes; output diode	–
C_1; C_2–C_{2N}; C_o; C_{in}	Return, pump, output, and input capacitors	F
v_k, V_{C_k}, ΔV_{C_k}	Capacitor state voltage, its mean, its peak-to-peak ripple	V
u_k	Ladder nodes, with $u_{-1} = c$, $u_0 = b$, $u_{2N} = p$	–
w_k	Branch weight $(1, N, N)$ in the charge balance	–
χ_k, λ_k, z_k	DCM indicator, normalized transfer duration, zero-current dwell	–
$I_{\text{t},k}$, $R^{\boldsymbol{\chi}}_{\text{crit},k}$, $L_{\text{crit},k}$	Load current, load resistance, and inductance at extinction of branch k	A, Ω, H
$\Gamma_{\boldsymbol{\chi}}$, $\kappa_{\boldsymbol{\chi}}$, H_k	Coefficients of the mixed-mode gain and boundary laws	–, S, Ω
R_{DS}, R_W, r_d, r_c	Channel, winding, diode slope, and capacitor series resistances	Ω
V_F, Q_{rr}	Diode threshold voltage and recovery charge	V, C
t_{on}, t_{off}, $C_{\text{oss,er}}$	Overlap times and energy-related output capacitance	s, F
Q_g, V_{drv}, P_{aux}	Gate charge, driver voltage, auxiliary power	C, V, W
P_0, f_0, Δi_0, α, β	Core-loss surrogate: reference loss, frequency, ripple, exponents	W, Hz, A, –
$\Delta R_{\text{ac},0}$	Excess winding resistance at f_0	Ω
V_{orb}, V_{unc}, L_σ	Orbit blocking maximum, tolerance allowance, commutation-loop inductance	V, V, H
V_e, k_i, $k_{,k}$, n_w, A_e, $\mathcal{B}$	Core volume, Steinmetz coefficient, turns, core area, flux density	m^3, –, –, m^2, T
η_{eng}, ζ_λ	Estimated efficiency, loss share of mechanism λ	–, %
$\mathbf{A}_d$, $\mathbf{B}_d$, $\mathbf{C}_d$, $\mathbf{D}_d$	Matrices of the sampled-data model	–
G_{jd}, C_i, C_v, L_i, L_v	Plant transfer functions, compensators, loop gains	–
ρ, τ	Closed-loop spectral radius, envelope time constant $-T_s/\ln\rho$	–, s

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