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Article

A High-Efficiency Bipolar Pulse Generator Based on a Push–Pull Inverter for Tissue Welding

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Abstract

The push–pull inverter topology inherently incorporates a transformer, making it suitable for electrosurgical generators without requiring an additional transformer. However, conventional push–pull topologies exhibit limitations, including high switch stress and the absence of a dedicated path for releasing transformer leakage-inductance energy, which may increase switching losses at high frequencies. This paper presents a bipolar pulse generator based on a push–pull inverter topology, offering a new engineering approach for electrosurgical applications. The prototype achieves soft-switching operation over a load range of 30–1000 Ω, reducing design complexity, extending load adaptability, and improving system reliability while meeting the stringent pulse-width control requirements of bipolar electrosurgical applications. In addition, based on an equivalent-impedance model of tissue welding, the operating modes and soft-switching mechanisms of the push–pull inverter under different dynamic load conditions are analyzed, and strict constraints relating to dead time, load resistance, and circuit parameters are derived. A bipolar pulse-generator prototype operating at 400 kHz was developed to validate the theoretical analysis. Experimental results show a conversion efficiency of 86–94% over a dynamic load range of 25–250 Ω. At a moderate nominal load, the system maintains an efficiency above 93% over an output-power range of 4.92–183.69 W, achieving high-efficiency operation across a power range relevant to electrosurgical applications. While maintaining tissue-welding quality, the proposed system improves overall efficiency, demonstrating the feasibility and engineering value of the topology and control strategy for bipolar electrosurgical generators.

Keywords: bipolar pulse generator; tissue welding; push–pull inverter; zero-voltage switching; dead time; power electronics

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1. Introduction

High-frequency electrosurgical generators convert electrical energy into waveforms suited to cutting, coagulation, sealing, or tissue joining [1,2]. In bipolar tissue welding, two electrodes deliver energy locally while mechanical compression maintains tissue contact. Electrical heating and the resulting tissue changes are coupled to the applied waveform and contact conditions [3,4]. The pulse source must therefore be considered together with the intended welding process: a generator suitable for a megahertz cutting instrument does not

necessarily provide the same waveform or control variables needed for a lower-frequency bipolar welding system.

One engineering challenge is the changing electrical load. Tissue dielectric properties depend on frequency and composition [5], while welding introduces changes in temperature, hydration, and electrode contact. Zhu et al. studied the trend of impedance changes in pig small intestine tissue during tissue welding and analyzed the correlation between welding effect and tissue impedance changes [6]. Resistive loads remain useful for repeatable converter characterization, but the ability to commutate at a static load and the ability to form an ex vivo weld provide complementary evidence. Both are relevant when assessing a practical pulse generator.

Two-stage and reconfigurable electrosurgical supplies offer independently adjustable conversion and waveform-generation functions [7,8]. Reported inverter approaches include a full bridge with a multiresonant filter [9], dual-current-mode power regulation [10], a single-ended resonant plasma-scalpel driver [11], and a dual-frequency Class-EF inverter [12]. Silicon carbide (SiC) and gallium nitride (GaN) full bridges have also been investigated at 4 MHz [13,14]. These studies address different output waveforms and surgical functions. Their results establish useful design alternatives, while their differing frequencies, loads, and measurement boundaries limit direct numerical efficiency comparisons.

A transformer-coupled push–pull inverter offers a direct route to alternating-polarity excitation using two controlled switches. Existing soft-switching push–pull converters illustrate the possibilities of this circuit family [15,16]. For the present welding application, the design question is how to combine the two-switch structure, a step-up transformer, and a practical gate-drive arrangement with suitable commutation timing. Zero-voltage switching (ZVS) requires sufficient charge transfer before turn-on and continued low drain voltage until the gate arrives. Studies of resonant transitions and dead-time effects show why the available current, parasitic capacitance, and timing interval must be considered together [17–19].

This work develops a fixed-frequency 400 kHz clamped push–pull generator for bipolar tissue welding. The implementation combines transformer-coupled bipolar excitation using two controlled inverter switches with dead-time selection to extend the demonstrated resistive-load capability. Its evaluation covers a 33.3:1 resistance span at the 100 ns setting, additional light-load points at 200 ns, inverter efficiency measurements, and preliminary ex vivo porcine welding tests. A commutation and loss framework relates the observed timing dependence to turn-on, conduction, and dead-time losses; total inverter loss is reconstructed from the existing efficiency data. Section 2 presents the circuit, loss model, and evaluation methods, Section 3 reports the electrical and tissue results, and Section 4 discusses their engineering significance and scope. Section 5 summarizes the findings.

2. Materials and Methods

2.1. Generator Architecture and Operating Requirements

Figure 1 shows the buck-fed clamped push–pull architecture. The front-end buck stage sets the voltage supplied to the inverter, and the transformer provides voltage step-up and an isolated secondary output. In the following analysis, V_{in} denotes the inverter input voltage downstream of the buck converter. The prototype uses V_{in} = 30–50 V, a transformer ratio of 1:3, and a switching frequency of 400 kHz. The ideal secondary pulse amplitude is therefore 90–150 V before semiconductor drops, leakage effects, and commutation intervals are included. The operating settings are listed in Table 1.

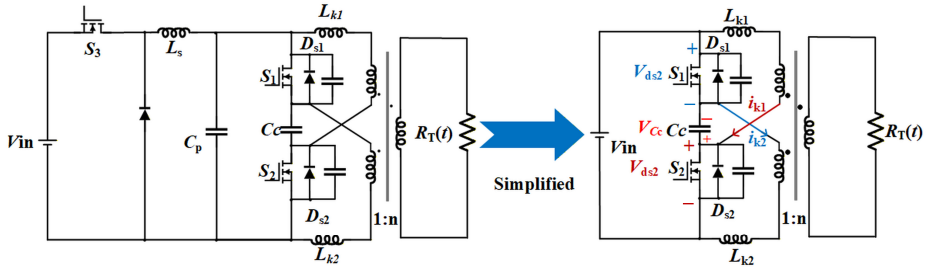


Figure 1. Buck-fed clamped push–pull architecture and simplified inverter model. The analysis defines V_{in} at the input of the inverter, downstream of the buck stage.

Table 1. Operating settings of the pulse generator.

Parameter	Setting
Inverter input voltage	30–50 V
Switching frequency	400 kHz
Transformer primary-to-secondary ratio	1:3
Nominal design power range	0–200 W
Number of pulses per burst	12
Nominal duty before dead time	0.5
Programmed dead time	100 ns; 200 ns in selected light-load tests

The electrode–tissue load is generally a time-dependent complex impedance. For circuit interpretation, R_T represents a resistive operating-point approximation rather than a complete model of the tissue. The positive and negative pulse sequences are set by the field-programmable gate array (FPGA). Input voltage determines the approximate pulse amplitude, while switching and burst timing determine the excitation duration. This separation allows waveform generation to be studied independently from the front-end conversion stage. Delivered energy remains load-dependent even when the pulse voltage is held approximately constant.

2.2. Switching Sequence and Commutation

The two principal intervals are shown in Figure 2. During power transfer, one switch conducts and the transformer applies a pulse to the secondary. During the inserted dead time, both gate commands are low and the available primary-side current redistributes charge among the switch output capacitances and other capacitances coupled to the commutating node. The complementary switch can turn on with a low drain voltage when its capacitance has discharged and the diode conduction maintains the clamp until channel conduction begins. Figure 3 gives the conceptual sequence; the traces are schematic rather than measured waveforms.

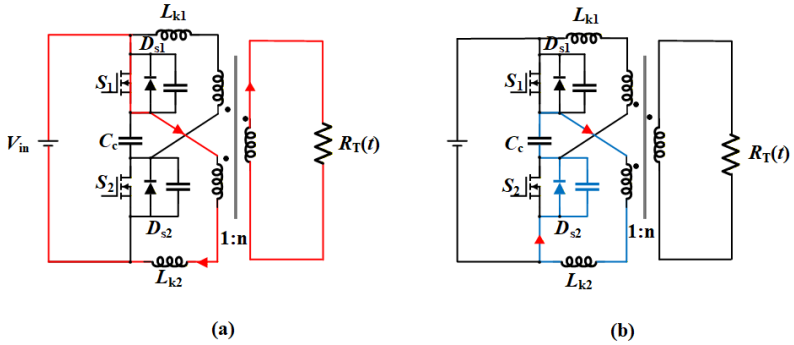


Figure 2. Equivalent circuits during (**a**) power transfer and (**b**) the dead-time commutation interval.

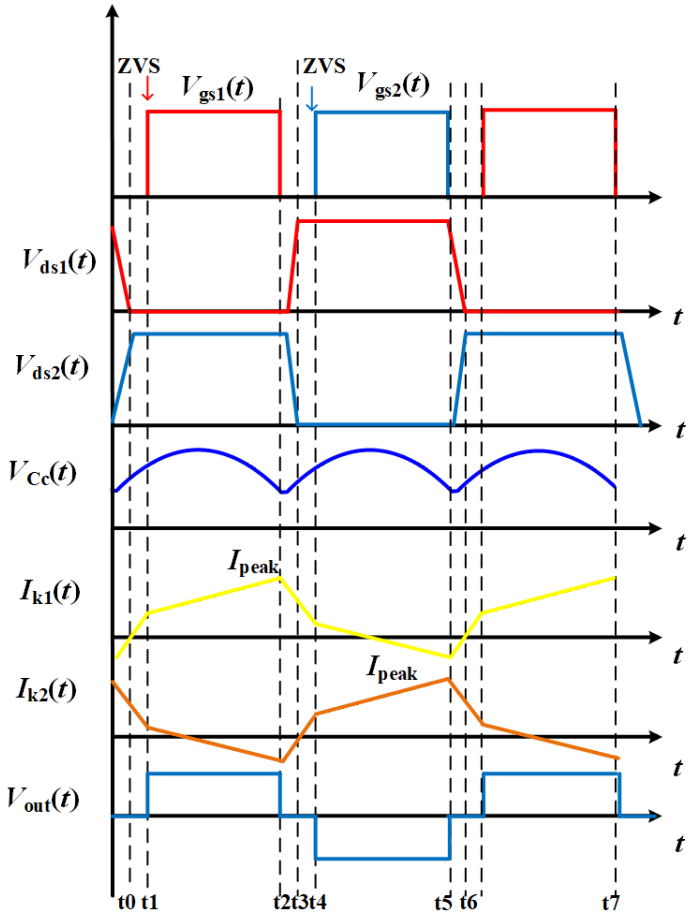


Figure 3. Conceptual gate, drain-voltage, clamp-voltage, primary-current, and output-voltage waveforms for zero-voltage switching (ZVS). The diagram illustrates the intended switching sequence and is not a measured waveform.

For an approximately complementary switch-voltage transition with $V_{sw} \approx 2V_{in}$, the required node charge may be written as

$$Q_{req} = Q_{oss,S1}(V_{sw}) + Q_{oss,S2}(V_{sw}) + C_{par}V_{sw}. \quad (1)$$

Here Q_{oss} is the voltage-dependent device output charge and C_{par} is additional capacitance referred to the same node. Output charge and stored output-capacitance energy have different definitions and cannot be interchanged [20]. If i_c denotes the net current available to discharge the incoming switch voltage, the first valid clamp crossing at T_{res} satisfies

$$\int_0^{T_{res}} i_c(\tau)d\tau = Q_{req},\ T_{res} \approx \frac{Q_{req}}{I_0}. \quad (2)$$

The second expression is a constant-current estimate using the initial available current I_0. It is useful for sensitivity analysis, while the actual current changes during a resonant transition. If diode-clamp conduction persists for t_z after the first crossing, the ideal turn-on interval is

$$T_{res} \le T_{dead} < T_{res} + t_z. \quad (3)$$

Thus, extending dead time can help an incomplete voltage transition, provided the low-voltage interval still persists when the gate arrives. A longer interval is not automatically preferable because current reversal can release the clamp and allow voltage rebound. Appendix A provides the reduced-order explanation and representative simulation waveforms. The analysis is used here to interpret timing behavior rather than to claim an independently calibrated boundary for the prototype.

2.3. Prototype and Gate Drive

The prototype uses an EP4CE10F17C8 FPGA (Intel Altera, San Jose, CA, USA) and Infineon IMW120R060M1H SiC metal–oxide–semiconductor field-effect transistors (MOSFETs, Infineon, Neubiberg, Germany). Figure 4 shows the gate-drive arrangement and prototype circuit board; nominal components are listed in Table 2. A UCC21520 (TI, Dallas, TX, USA) dual-channel isolated driver and isolated power modules provide separate drive returns for the two switches. The floating driver return follows the corresponding switch source. This arrangement accommodates the source-potential movement associated with the clamped primary circuit.

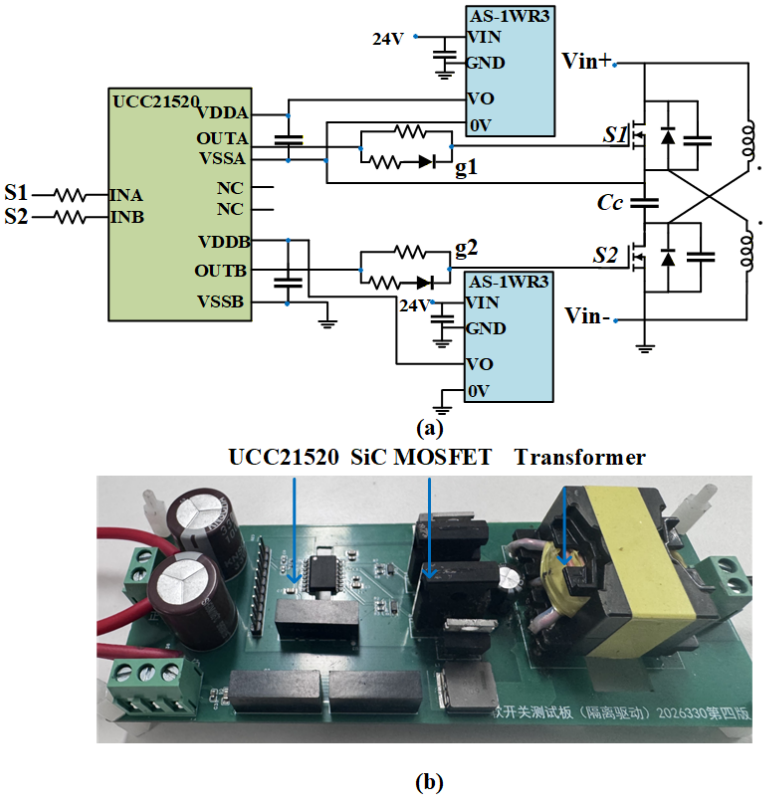


Figure 4. (**a**) Isolated gate-drive arrangement and (**b**) the inverter prototype circuit board.

Table 2. Nominal components and circuit parameters.

Component or Parameter	Nominal Specification
FPGA	EP4CE10F17C8
SiC MOSFET	IMW120R060M1H, 1200 V rating
Gate driver	UCC21520DWR
Isolated power module	Mornsun AS-1WR3 series
Primary-branch leakage inductance L_k	2.2 µH
Magnetizing inductance L_m	26 µH
Clamp capacitance C_c	10 µF
Transformer turns ratio	1:3

The inductance and clamp capacitance represent a compromise between commutation support and electrical stress. Increasing available magnetic current can shorten a charge-limited transition, but also increases circulating-current loss. The clamp capacitance should be large enough that its voltage changes only modestly within a switching transition. For a specified cumulative charge excursion ΔQ and allowable ripple ΔV_c, the first-order

sizing relation is $C_c \geq \Delta Q/\Delta V_c$. The values in Table 2 describe the implemented prototype; tolerance-qualified design limits are outside the present characterization.

2.4. Theoretical Power Loss Analysis

This section presents a theoretical framework for interpreting the inverter-stage loss mechanisms and the potential effect of ZVS on turn-on loss. Individual loss contributions have not been experimentally quantified.

$$P_{loss,pwr} = P_{cond} + P_{sw} + P_D + P_{mag} + P_{Cc} + P_{pcb}. \quad (4)$$

The terms represent MOSFET channel conduction, irreversible switching transitions, body-diode conduction, transformer loss, clamp-capacitor loss, and interconnection loss, respectively. Magnetic loss P_{mag} includes winding and core loss. All average currents and event counts below refer to the same T_w. For burst excitation, T_w includes the relevant inactive intervals; a burst duty factor must not be applied a second time to currents already averaged over this window.

2.4.1. Semiconductor Loss and the Dead-Time Tradeoff

With nearly constant junction temperature during the averaging window, channel-conduction loss can be approximated by

$$P_{cond} \approx \Sigma_{j=1,2} R_{on,j}\left(T_j, V_{gs,j}\right) I^2_{ch,j,rms}. \quad (5)$$

Here R_{on} is the drain–source on-state resistance and $I_{ch,j,rms}$ is the channel-current RMS value over T_w, with zero contribution outside the channel-conduction intervals. This definition already accounts for the alternating operation of the two switches. The current includes the load-related component, magnetizing current, and commutation circulation; replacing it with output current alone would omit part of the conduction loss. The selected device datasheet specifies a typical resistance of 60 mΩ at 18 V gate bias and 25 °C, increasing to 113 mΩ at 175 °C [21]. These are reference conditions, not measured prototype junction temperatures or gate settings.

For the N_j switching cycles of device j occurring within T_w, the average switching loss is represented by

$$P_{sw} = \frac{1}{T_w} \Sigma_{j=1,2} \Sigma_k \left(E_{on,jk} + E_{off,jk}\right). \quad (6)$$

The inner sum runs from k = 1 to N_j. E_{on} and E_{off} denote the irreversible transition energies for the actual operating voltage, current, temperature, and drive conditions. Recovery-related dissipation must be included once in a consistent transition-energy definition. ZVS reduces turn-on voltage–current overlap and the loss associated with residual drain voltage, but does not remove turn-off loss. A first-order overlap estimate is $E_{off} \approx V_{blk}|I_{off}|t_{ov}/2$ when one waveform changes approximately linearly while the other remains near its commutation value [22]. The effective overlap interval t_{ov} is distinct from the gate turn-off delay. The device datasheet switching energies were characterized at 800 V and 13 A and cannot be assigned directly to the much lower blocking voltages of this prototype [21].

The voltage-dependent energy stored in one output capacitance is

$$E_{oss}(V) = \int_0^V u C_{oss}(u) du. \quad (7)$$

This energy differs from VQ_{oss}. During soft commutation, capacitance energy can be exchanged with the inductive network rather than dissipated entirely at turn-on [20]. Therefore, full E_{oss} must not be added automatically for every ZVS event, or added again to

a switching-energy term that already includes the same dissipative contribution. Likewise, integrating terminal voltage and current over an incomplete transition can include a change in stored capacitive energy rather than irreversible heat alone.

During a diode-clamped interval, the conduction loss is

$$P_D = \frac{1}{T_w} \Sigma_{j=1,2} \int_{D_j} V_{F,j}\left(\left|i_{D,j}\right|, T_j\right) \left|i_{D,j}\right| dt. \quad (8)$$

D_j denotes the collection of body-diode conduction intervals of device j, excluding channel conduction. In the local approximation of Appendix A, the energy per interval is $E_D \approx V_F(I_3\, T_{fw} - aT_{fw}^2/2)$, for $0 \le T_{fw} < I_3/a$. Increasing dead time can complete the charge transfer and recover ZVS, but also extends diode conduction if the clamp persists. Increasing circulating current similarly improves commutation margin while increasing the RMS-current term in Equation (5). Thus, the appropriate dead time is the interval that completes commutation and reaches gate turn-on before clamp release, with acceptable current and diode losses.

2.4.2. Transformer and Clamp-Capacitor Loss

For a periodic evaluation waveform, winding copper loss can be expressed using its harmonic components as

$$P_{cu} = \Sigma_w \Sigma_{h\ge 0} R_{ac,w}\left(f_h, T_{winding}\right) I_{w,h,rms}^2. \quad (9)$$

The index w includes both primary branches and the secondary winding. R_{ac} includes frequency-dependent skin and proximity effects, and the h = 0 term uses DC resistance. For burst excitation, the harmonic frequencies f_h belong to the actual periodic burst waveform rather than only integer multiples of the 400 kHz carrier. The same RMS-current treatment captures circulating current that transfers no net load power.

The core flux density follows the internal magnetizing voltage v_m, after winding-resistance and leakage-inductance drops are excluded:

$$B(t) = B(0) + \frac{1}{N_p A_e} \int_0^t v_m(\tau) d\tau. \quad (10)$$

Here N_p is the turns count associated with the selected primary branch and A_e is the effective core cross-sectional area. For one closed flux loop of duration T, an improved generalized Steinmetz estimate is [23]

$$P_{core} \approx \frac{V_e k_i}{T} \int_0^T |dB/dt|^{\alpha} (\Delta B)^{\beta-\alpha} dt. \quad (11)$$

V_e is core volume, ΔB is the loop peak-to-peak flux swing, and k_i, α, and β are material- and temperature-dependent coefficients. Major and minor loops must be evaluated separately and combined by their energy contributions when the flux trajectory contains multiple loops. A sinusoidal core-loss value at 400 kHz alone does not characterize the bipolar burst waveform. Absolute transformer-loss prediction requires the core geometry, material coefficients, and winding AC resistances. The model is used here to identify the relevant dependencies, while measured efficiency constrains the aggregate loss.

The clamp capacitor carries commutation and circulating current. Its equivalent-series-resistance loss is

$$P_{Cc} = \Sigma_{h\ge 0} ESR_c(f_h, T_c)\, I_{Cc,h,rms}^2. \quad (12)$$

Increasing C_c reduces charge-induced voltage ripple, but does not by itself eliminate capacitor heating. Interconnection loss can be evaluated in the same way using the conductor

resistance and actual current spectrum. The inductances and capacitances responsible for ringing primarily exchange stored energy; their associated resistive and dielectric damping, rather than stored energy alone, contributes to average loss.

2.4.3. Gate Drive and the Measurement Boundary

For a unipolar gate drive without energy recovery, a first-order gate-charge estimate is $P_{\mathrm{gate}} \approx \Sigma_{\mathrm{j}} f_{\mathrm{e,j}}\, Q_{\mathrm{g,j}}\, \Delta V_{\mathrm{g,j}}$, where $f_{\mathrm{e,j}} = N_{\mathrm{j}}/T_{\mathrm{w}}$ is the actual cycle count per unit averaging time. Q_{g} must correspond to the relevant voltage swing and operating conditions. The auxiliary input power P_{aux} also includes driver quiescent consumption and isolated-supply conversion loss. If these circuits draw power within the measured inverter input boundary, the corresponding prediction is $P_{\mathrm{loss,bnd}} = P_{\mathrm{loss,pwr}} + P_{\mathrm{aux}}$; externally supplied auxiliary power is outside that boundary. The buck-stage loss is excluded in either case. This distinction prevents stage efficiency from being interpreted as complete generator efficiency.

2.5. Electrical and Tissue Evaluation

The test platform is shown in Figure 5. Electrical waveforms were acquired using a Rigol RP1025D differential voltage probe (RIGOL, Suzhou, China), a Cybertek HCP8030 current probe (Cybertek, Dongguan, China), and a Tektronix MSO44 oscilloscope (Tektronix, Beaverton, OR, USA). The probe uses CYBERTEK's Desk Fixture DF6800 (Cybertek, Dongguan, China) for timing alignment. Discrete resistors were used to obtain repeatable electrical operating points. The efficiency measurement boundary is the inverter input and output; it excludes the front-end buck converter. DC input power was obtained from an electronic multimeter measurement (RIGOL DM3058E, Jiangsu, China). Output active power was calculated offline in MATLAB (version,2025b) by numerically integrating the measured voltage–current product. With T_{w} denoting the output averaging window, the actual measurement window is 120 us:

$$P_{out} = \frac{1}{T_w}\int_0^{T_w} v_{out}(t) i_{out}(t) dt,\ \eta_{inv} = \frac{P_{out}}{P_{in,inv}}. \tag{13}$$

The measurement procedure combines calibrated probes with time-domain active-power evaluation to support measurement accuracy. Direct numerical integration of the measured voltage–current product accounts for the actual nonsinusoidal bipolar output waveform without an ideal pulse-shape approximation. The efficiency values are thus evaluated from measured power quantities at the defined inverter boundary.

For burst-mode excitation, the averaging window affects the interpretation of average power and should encompass the same input and output operating interval. Interpreting their difference as dissipated power also requires equal stored energy at the window boundaries, as in a periodic steady state; otherwise the difference includes net energy accumulation. The reported efficiency is a stage-level result. The available measurement documentation does not separately resolve auxiliary-drive power or provide a complete uncertainty budget; these points are considered in Section 4.

Ex vivo welding was performed on porcine small-intestine tissue. A ZQ-980A (Zhiqu Precision Instruments, Zhiqu, China) mechanical press applied a clamping force of 82.4 N through a hollow cylindrical electrode with an inner diameter of 5 mm and an outer diameter of 8 mm. Porcine small-intestinal tissue was purchased from a local market in shanghai, China, and used for the ex vivo tissue-welding experiments. The average size of the small intestine used in the experiment is 30cm. The inverter input voltage was set to 30, 40, or 50 V, with five burst-pressure measurements per voltage group and 15 welding procedures in total. Each welding procedure lasted 10 s and used a 400 kHz carrier frequency. The welded specimens were evaluated using a water-based burst-pressure test at an infusion flow rate

of 1 mL/min. The test was terminated upon the first observable water leakage from the tissue, and the corresponding pressure was recorded as the burst pressure. Individual measurements were summarized using the arithmetic mean and sample standard deviation (SD). The analysis was descriptive, and no statistically established optimal input voltage was inferred from these small groups.

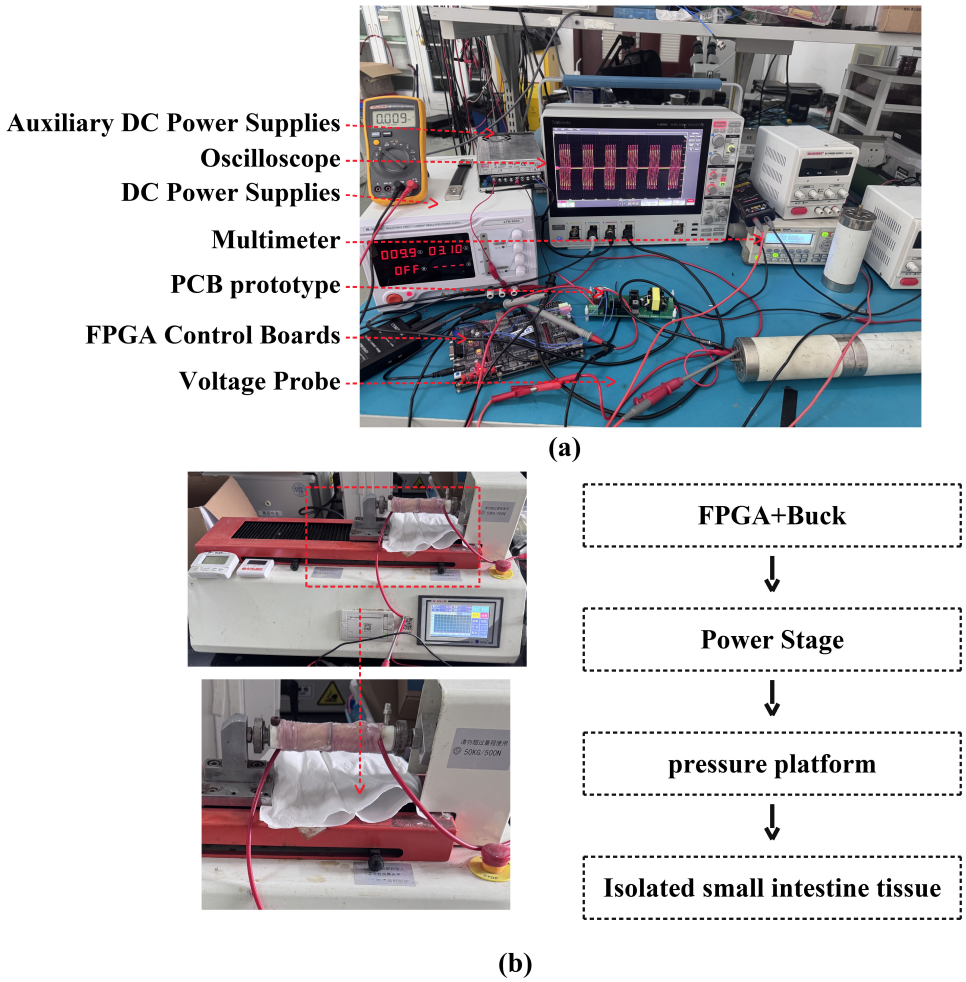


Figure 5. (**a**) Electrical evaluation platform and (**b**) the mechanical compression arrangement used for ex vivo small-intestine welding.

3. Results

3.1. Resistive-Load Switching and Dead-Time Dependence

Figure 6 presents lower-switch gate and drain voltage waveforms together with the output voltage at 30, 60, 90, 200, 500, and 1000 Ω. With a programmed dead time of 100 ns, the drain voltage reaches the low-voltage state before gate turn-on at all six illustrated operating points. The measurements demonstrate wide-resistive-load soft switching across a 33.3:1 resistance span while maintaining the 400 kHz operating frequency. The output waveform also shows load-dependent commutation and ringing, reflecting the interaction of the transformer, capacitances, and resistive termination.

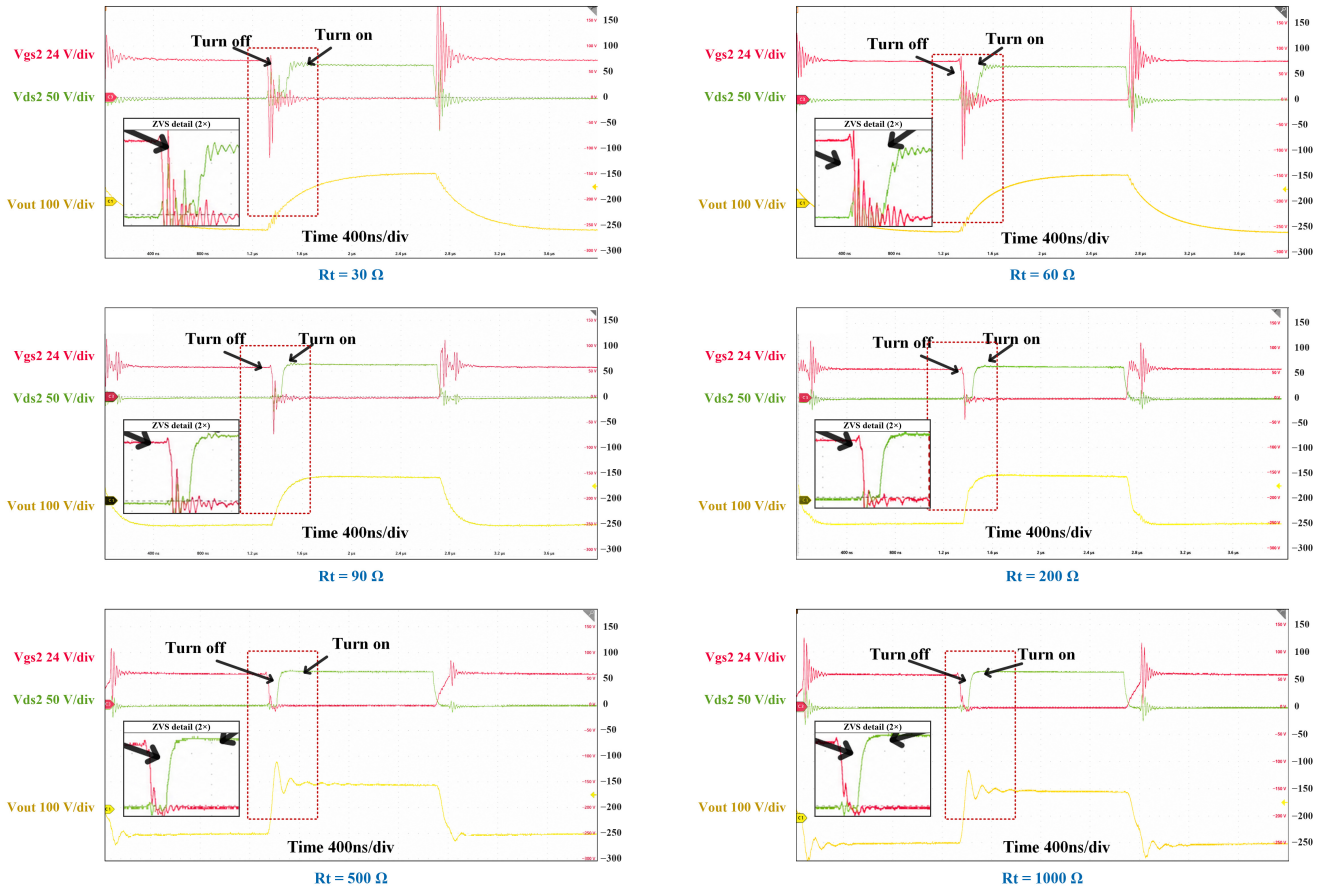


Figure 6. Measured lower-switch gate and drain voltage and inverter output voltage at the labeled resistive loads, with a programmed dead time of 100 ns. The six panels are distinct static operating points.

The light-load tests in Figure 7 make the timing dependence explicit. At V_{in} = 30 V and loads of 1200 and 1500 Ω, the 100 ns setting leaves an incomplete voltage transition at turn-on. Increasing the programmed dead time to 200 ns restores the illustrated low-voltage turn-on. The result is consistent with a longer transition when the available commutation current is reduced. These experiments use two manually selected dead-time settings; they establish the benefit of timing adjustment at those conditions rather than an online adaptive controller. The commutation behavior under dynamic load and ZVS throughout the entire welding cycle have not been validated yet.

Figure 8 compares the theoretical switch-voltage transition times at input voltages of 30, 40, and 50 V with experimental measurements obtained only at 30 V. For the experimental measurements, the end of the transition is defined as the instant at which the MOSFET drain–source voltage reaches 0 V. Both the theoretical and measured transition times increase with load resistance. At a fixed load resistance, the model predicts a shorter transition time as the input voltage increases. At 1000 Ω, the predicted transition times are approximately 39.9, 37.0, and 35.0 ns at 30, 40, and 50 V, respectively, whereas the measured value at 30 V is 51 ns. At this operating point, the prediction underestimates the measured value by 11.1 ns, or approximately 21.8% relative to the measurement.

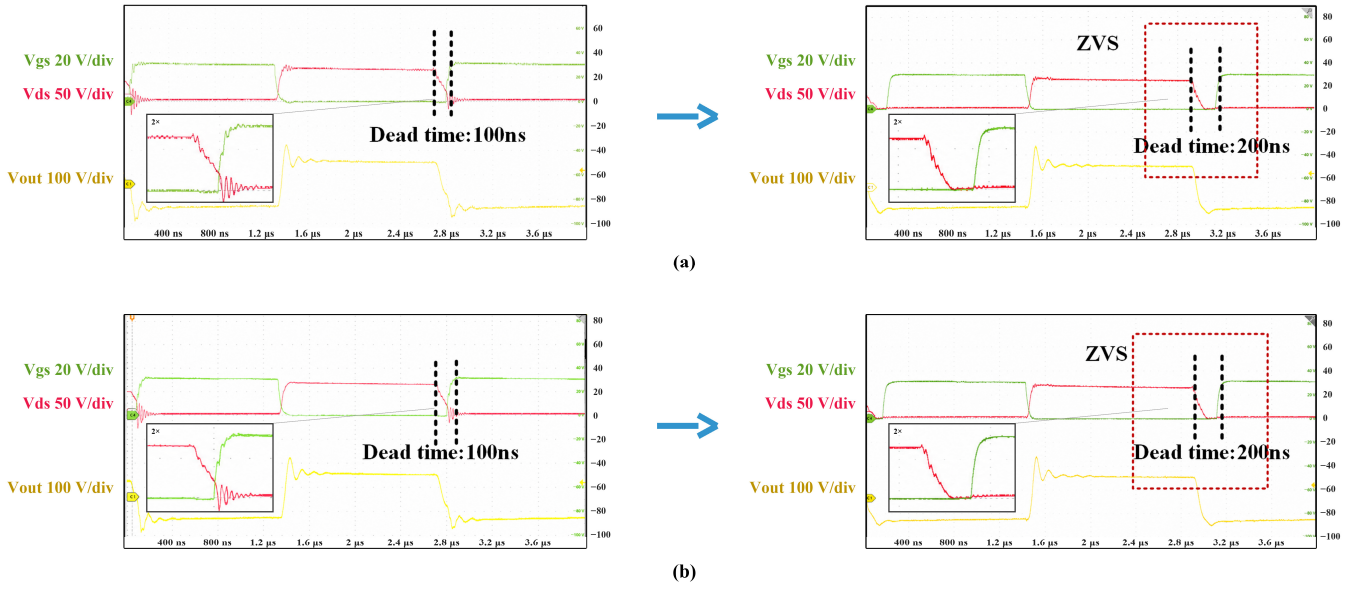


Figure 7. Comparison of the 100 ns and 200 ns dead-time settings at V_{in} = 30 V: (**a**) 1200 Ω and (**b**) 1500 Ω. The longer setting restores the illustrated ZVS behavior at these two light-load points.

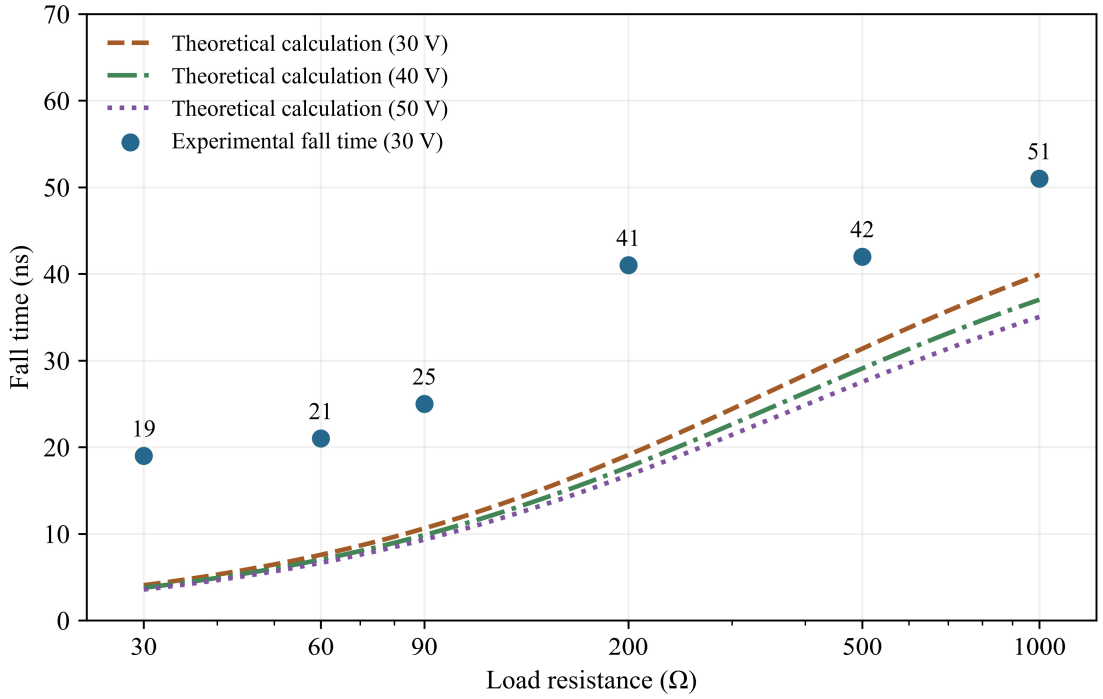


Figure 8. Predicted and measured drain–source voltage transition times of the upper MOSFET versus load resistance. Predictions are shown for input voltages of 30, 40, and 50 V; measurements are available only at 30 V.

Although the model captures the observed load-dependent trend at 30 V, its predictions are systematically lower than the measured values. This discrepancy may arise from the approximation of the commutation current and uncertainties in the aggregate parasitic capacitance. Probe loading and differences between the assumed device characteristics and actual operating conditions, including temperature, may also contribute. Further calibration is therefore needed to improve prediction accuracy. The calculations use a PCB-related parasitic capacitance of approximately 46 pF extracted from simulation, MOSFET output-charge characteristics derived from the Infineon datasheet, and a transformer

equivalent capacitance of approximately 240 pF. The resulting curves should be interpreted as approximate transition-time predictions rather than fully validated ZVS boundaries.

3.2. Inverter Efficiency

Figure 9 summarizes inverter efficiency in a fixed-load power sweep and at discrete load settings.

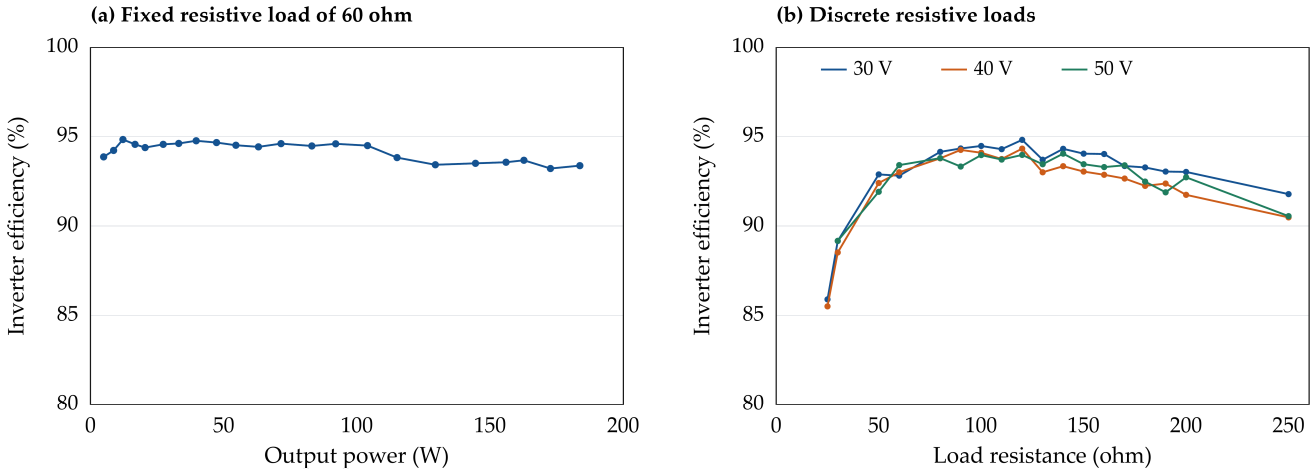


Figure 9. Inverter input-to-output efficiency: (**a**) power sweep with a 60 Ω resistive load; (**b**) discrete load measurements at the indicated inverter input voltages. The buck stage is outside the measurement boundary.

Figure 9a shows inverter efficiency measured with a 60 Ω resistive load. The 22 measured points span 4.922–183.687 W and 93.21–94.83% efficiency. The highest sampled efficiency is 94.83% at 12.169 W. Efficiency remains above 93% at the plotted points, covering low-power operation and output power approaching the nominal 200 W rating. This result demonstrates efficient inverter-stage operation over the measured power interval.

Figure 9b shows efficiency at discrete load settings and inverter input voltages of 30, 40, and 50 V. The measurements collectively span 25–250 Ω and 85.51–94.81% efficiency; the 50 V series starts at 30 Ω. The 30 V curve reaches 94.81% at 120 Ω. The reduction at the lowest resistance settings is consistent with increased current-related loss, although the overall curves alone do not identify the contribution of each loss mechanism. The connecting lines in Figure 9 are visual guides between measured settings.

3.3. Total Loss Reconstructed from the Efficiency Measurements

The measured inverter input-to-output difference provides an aggregate check on the loss mechanisms in Section 2.4. Using the efficiency as a fraction,

$$P_{loss,meas} = P_{in,inv} - P_{out} = P_{out}\left(\frac{1}{\eta_{inv}} - 1\right). \quad (14)$$

Figure 10 applies Equation (14) to the same 22 efficiency observations in Figure 9a. The reconstructed total loss increases from approximately 0.32 W at 4.92 W output to 13.04 W at 183.69 W output. At the highest-power observation, the inferred input power is 196.73 W, and the loss is 6.63% of that input. Representative values are tabulated in Table A2. This conversion introduces no additional experiment and inherits the measurement boundary, averaging interval, rounding, and uncertainty of the efficiency data.

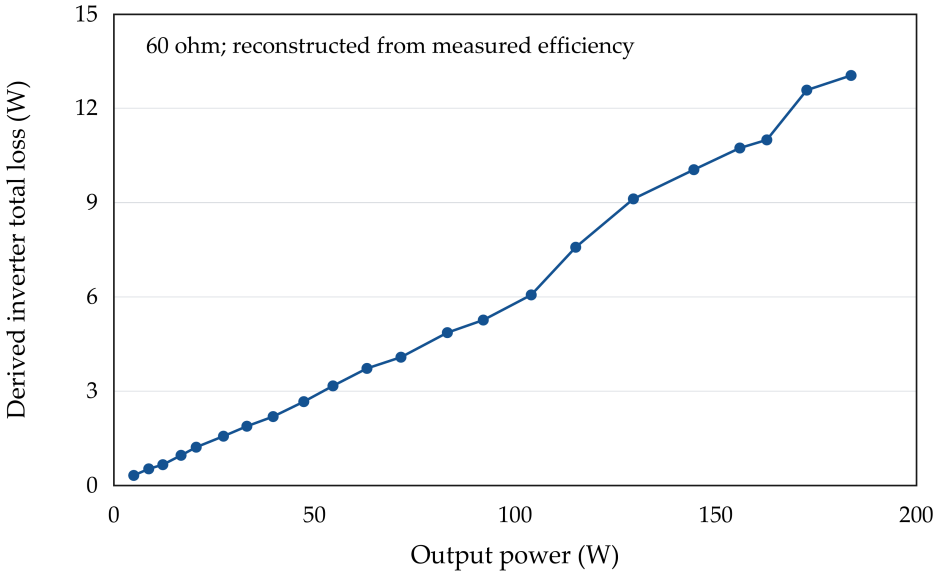


Figure 10. Total inverter loss reconstructed from the existing 60 Ω efficiency–power data using Equation (14). Points are algebraic transformations of the measured efficiency values; the connecting line is a visual guide.

The higher losses at higher output power are compatible with the current-dependent conduction and winding terms in Equations (5) and (9), together with operating-point-dependent switching loss. The curve alone cannot determine which component dominates. At the low-resistance settings in Figure 9b, the lower efficiency is likewise consistent with increased current stress. At light load, extending dead time can reduce residual turn-on loss, while the accompanying diode-conduction interval introduces the competing term in Equation (8). The present loss model therefore explains the design tradeoff underlying the switching observations without assigning unsupported numerical shares to individual components.

3.4. Ex Vivo Porcine Small-Intestine Welding

Figure 11 presents a representative tissue-welding output waveform and photographs of welded porcine small-intestine specimens. The example demonstrates bipolar voltage and current delivery to tissue. Together with the burst-pressure results, it links the electrical implementation to the intended welding application: a transformer-coupled two-switch source can deliver the pulse sequence needed to form pressure-bearing ex vivo welds.

Figure 12 shows individual burst-pressure observations and the mean ± sample standard deviation for each group. The results are 31.76 ± 2.63 mmHg at 30 V, 30.30 ± 2.11 mmHg at 40 V, and 34.84 ± 5.59 mmHg at 50 V ($n = 5$ per group). These correspond to approximately 4.24 ± 0.35, 4.04 ± 0.28, and 4.65 ± 0.75 kPa, respectively. The individual values are provided in Table A1. The 50 V group has the highest sample mean and the largest dispersion; the group distributions overlap. The observations demonstrate the formation of pressure-bearing ex vivo welds under the tested conditions. The group size and dispersion support a descriptive comparison rather than selection of an optimal input voltage.

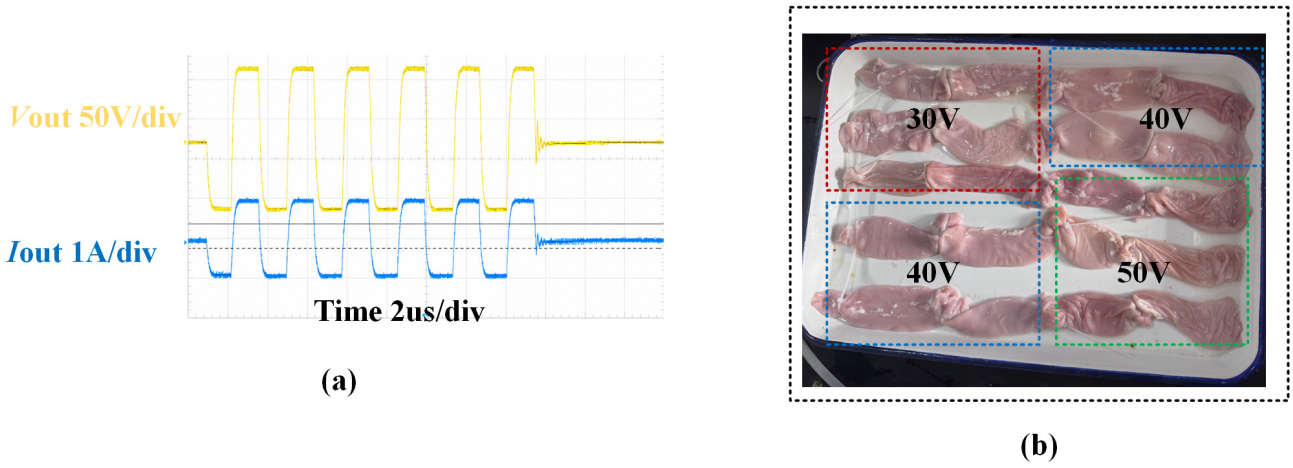


Figure 11. (**a**) Representative output voltage and current during tissue welding and (**b**) photographs of ex vivo porcine small-intestine welds. Voltage labels identify inverter input settings.

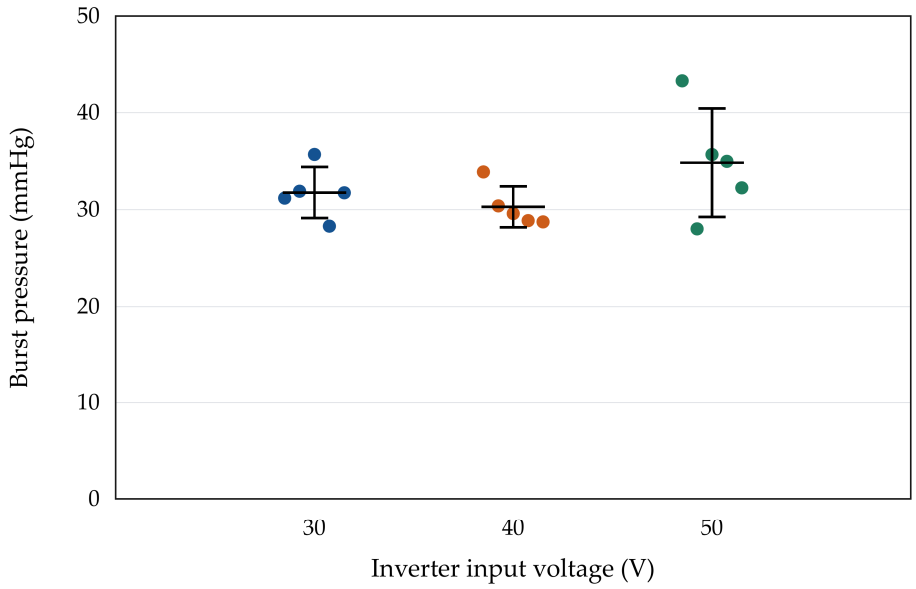


Figure 12. Individual burst-pressure observations and mean ± sample standard deviation at a clamping force of 82.4 N (n = 5 per voltage group). Dots show observations; horizontal bars show means; whiskers show one sample standard deviation.

4. Discussion

4.1. Engineering Interpretation

The practical outcome is a 400 kHz transformer-coupled pulse source that produces bipolar excitation with two controlled inverter switches and supports preliminary porcine tissue welding. The architecture separates input-voltage adjustment from the alternating-polarity switching sequence. This is useful when a welding protocol requires a defined voltage setting and burst pattern, while the inverter remains the focus of high-frequency commutation design. The reported efficiency and burst-pressure results address different aspects of this implementation: electrical conversion and ex vivo mechanical integrity.

Wide resistive-load sweeps provide a repeatable way to characterize high-frequency inverter operation. For example, Jiang et al. use a manually adjusted 50–1500 Ω resistor and six representative waveform cases to evaluate a dual-frequency electrosurgical inverter [12]. In the present implementation, the six 30–1000 Ω cases span a resistance ratio of 33.3:1 at

100 ns dead time. The additional 1200 and 1500 Ω cases demonstrate timing-based extension of the light-load capability at the same 400 kHz switching frequency. These are substantial load-span measurements; they characterize operation at the tested resistive conditions.

The dead-time dependence is explained by the charge needed for the switching-node transition. A 100 ns setting supports the selected 30–1000 Ω cases, while the tested 1200 and 1500 Ω cases benefit from a 200 ns setting. Equation (3) identifies the accompanying upper timing constraint: the diode clamp must persist until gate turn-on. Dead time is therefore an effective design variable for extending the demonstrated load capability, with the useful interval determined jointly by charge transfer and clamp persistence.

The reference generators clarify why a switching waveform alone is insufficient to predict efficiency. Yoon et al. include instrument impedance transformation in the design of a 4 MHz SiC full bridge [13]; Hwang et al. use a resonant matching network for a GaN full bridge and report that high-current turn-off reduces efficiency at lighter loads despite ZVS [14]. Xing et al. use fast frequency tracking and demonstrate 50-to-300 Ω and 300-to-50 Ω load steps [11], whereas Jiang et al. combine frequency selection with a current-controlled front end [12]. The present implementation instead uses fixed carrier frequency and two selected dead times. Its design rationale is the balance between commutation current, diode-clamp duration, and current-dependent losses, as expressed in Section 2.4.

Table 3 places the generator in the context of other electrosurgical inverter implementations. Different surgical functions require different frequencies, waveform spectra, and output regulation. The two-switch structure is a practical implementation choice for the present bipolar welding waveform. Its benefits must be weighed against switch-voltage stress, transformer symmetry, and floating gate-drive requirements. The table compares design context rather than assigning a universal efficiency or reliability ranking.

Table 3. Design context and reported resistive test conditions of the four reference generators and the present implementation.

Study	Main Inverter	Frequency	Resistive Test Conditions	ZVS Turn-on	Design and Application Focus
Yoon et al. [13]	SiC full bridge	3.5–4 MHz	20–600 Ω waveform cases	No	Instrument matching; electrosurgery
Hwang et al. [14]	GaN full bridge	4 MHz	5–200 Ω	Yes	Resonant matching; ZVS electrosurgery
Xing et al. [11]	Single-ended resonant	365–403 kHz	50–2000 Ω	Yes	Fast tracking; plasma-scalpel drive
Jiang et al. [12]	Class EF	3–4 MHz	50–1500 Ω	No	Dual-frequency selection; electrosurgery
This work	Clamped push–pull	400 kHz	30–1000 Ω at 100 ns; 1200 and 1500 Ω at 200 ns	Yes	Two-switch bipolar welding source; dead-time selection

Test conditions summarize the stated experiments and are not interchangeable definitions of a universal ZVS range. Different waveforms, powers, surgical functions, and measurement boundaries prevent a controlled numerical ranking of conversion efficiency.

4.2. Relevance to a Changing Tissue Load

Static resistive-load tests provide repeatable characterization of commutation over the selected operating points. The porcine small-intestine voltage–current waveform and burst-pressure observations provide complementary evidence of application feasibility

under the stated welding conditions. Together, these measurements link the converter characterization to the intended welding application.

Voltage adjustment alone also does not fix the energy delivered to tissue. Burst energy is the integral of instantaneous output power over the burst, and changes when current changes. Consequently, the present implementation is described in terms of voltage and timing settings rather than closed-loop energy regulation. A clinical welding endpoint and a feedback law are separate system functions beyond the evidence presented here.

4.3. Scope and Measurement Limitations

The demonstrated ZVS load span is specified by the tested resistive conditions and the two programmed dead times. Extension to other input voltages, temperatures, or burst-startup conditions depends on the corresponding commutation trajectory. The charge calculation in Appendix A explains parameter sensitivity; quantitative prediction accuracy has not been established against measured transition times. Device-capacitance variation, branch asymmetry, and gate propagation delay can alter the useful timing interval.

Efficiency is reported for the inverter boundary identified in Section 2.5. The front-end buck loss is excluded, and the documentation does not separately quantify the contribution of independently supplied drive and auxiliary circuits. Despite probe calibration, residual gain and offset errors, relative channel delay, the DC-source readout accuracy, and the respective averaging intervals contribute to efficiency uncertainty. The frequency-dependent impedance of the resistor assemblies is also not independently characterized in the available record. Consequently, the total losses reconstructed in Section 3.3 provide an aggregate measurement-based result, while the individual terms in Section 2.4 remain a theoretical framework rather than a calibrated component-by-component prediction.

The tissue evaluation contains five burst-pressure observations per voltage and provides no clinical comparator or long-term healing outcome. Accordingly, the tissue data are interpreted as preliminary ex vivo feasibility observations. The circuit operation and timing dependence, rather than a biological efficacy claim, define the principal contribution of this study.

5. Conclusions

A 400 kHz clamped push–pull pulse generator was designed and evaluated for bipolar tissue welding. The buck-fed, transformer-coupled implementation combines adjustable inverter input voltage with a two-switch high-frequency stage. Selected 30–1000 Ω resistive-load traces demonstrate ZVS with 100 ns programmed dead time, while the tested 1200 and 1500 Ω cases recover the illustrated ZVS behavior at 200 ns. The fixed-load power sweep yields 93.21–94.83% inverter efficiency over the sampled 4.92–183.69 W interval, corresponding to reconstructed total losses of approximately 0.32–13.04 W. The loss model explains the competing effects of commutation margin, circulating current, and diode conduction. Ex vivo porcine small-intestine welds exhibit mean burst pressures of 30.30–34.84 mmHg across the three voltage groups. These results support the feasibility of the implementation and show how commutation timing affects its demonstrated load capability. The findings apply to the measured operating points and preliminary tissue tests.

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Data Availability Statement: Upon reasonable request, the original data of this article can be obtained from the corresponding author, including but not limited to efficiency testing and biological testing.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

FPGA	Field-programmable gate array
GaN	Gallium nitride
MOSFET	Metal–oxide–semiconductor field-effect transistor
RMS	Root mean square
SD	Standard deviation
SiC	Silicon carbide
ZVS	Zero-voltage switching

Appendix A. Reduced-Order Commutation Interpretation

The analysis in Section 2.2 can be interpreted using a local single-mode model. Let v be the incoming-switch drain voltage, i_c positive when discharging that node, L_c the effective commutation-mode inductance, and V_b the opposing network voltage. Under nearly fixed clamp voltage and load state,

$$L_c \frac{di_c}{d\tau} = v - V_b - R_c i_c,\ C_\Sigma(v) \frac{dv}{d\tau} = -i_c. \tag{A1}$$

Here $C_\Sigma(v)$ includes both participating output capacitances and node-referred parasitics. L_c is a network-referred mode quantity and should not be equated automatically with one primary-branch leakage inductance. For $R_c = 0$, constant $C_\Sigma = C_{eq}$, $v(0) = V_{sw}$, and $i_c(0) = I_0$, the local solutions are

$$i_c(\tau) = I_0 cos(\omega_0 \tau) + \frac{V_{sw} - V_b}{Z_0} sin(\omega_0 \tau), \tag{A2}$$

$$v(\tau) = V_b + (V_{sw} - V_b) cos(\omega_0 \tau) - I_0 Z_0 sin(\omega_0 \tau), \tag{A3}$$

$$\omega_0 = 1/\sqrt{(L_c C_{eq})},\ Z_0 = \sqrt{(L_c / C_{eq})}. \tag{A4}$$

These equations explain the joint dependence of the voltage trajectory on current and capacitance. If the current at the diode clamp is I_3 and an approximately constant opposing voltage gives $a = V_{opp}/L_c$, the clamp-current interval is $t_z \approx I_3/a$. For $0 \le T_{fw} < t_z$, diode conduction dissipates $E_D \approx V_F(I_3\, T_{fw} - a{T_{fw}}^2/2)$, where $T_{fw} = T_{dead} - T_{res}$. This term belongs to the actual diode-conduction interval; it is not an additional capacitance-energy barrier. A consistent energy balance must also include source work and changes in every participating stored-energy state.

Figure A1 shows representative LTspice transitions from the existing simulation set. The selected cases illustrate incomplete discharge and successful low-voltage turn-on. They support the physical interpretation of the timing window and are not a measured boundary map.

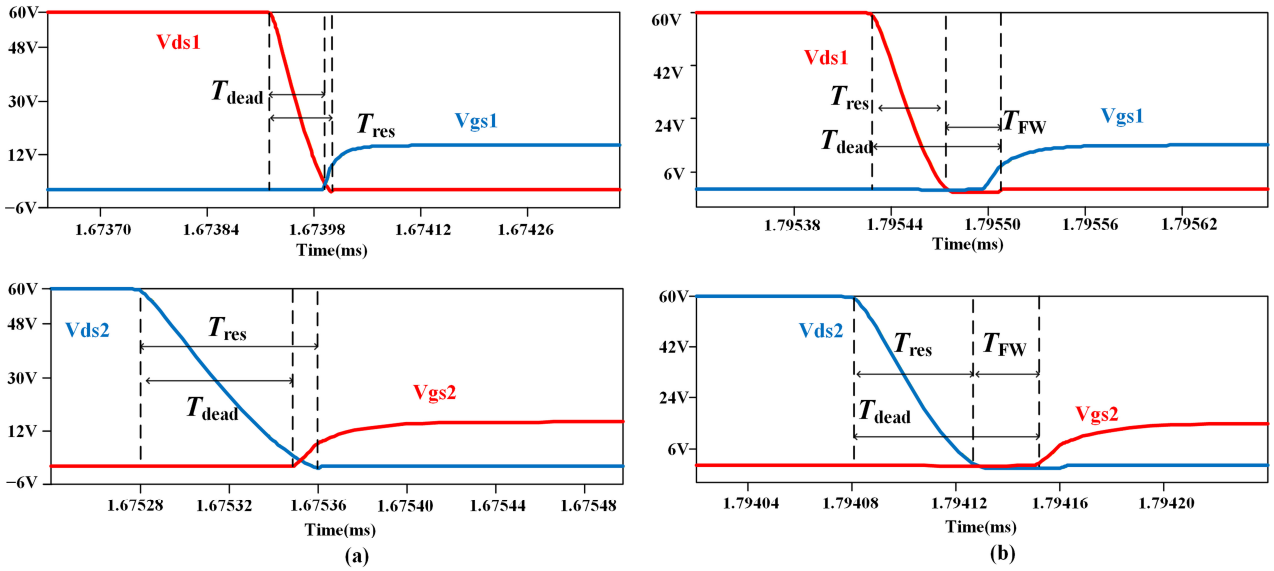


Figure A1. LTspice gate and drain voltage waveforms: (**a**) incomplete commutation at turn-on and (**b**) completed commutation with a finite low-voltage interval.

Figure A2 evaluates the constant-current estimate in Equation (2) with $I_0 \approx n^2 V_{in}/R_T + V_{in}/(4 f_s L_m)$, using $n = 3$, $f_s = 400$ kHz, $L_m = 26$ µH, $C_{par} = 100$ pF, and $V_{in} = 30$ V. At $R_T = 1000\ \Omega$ and an assumed per-device Q_{oss} of 28 nC, the estimate is 62.6 ns. The illustrated 10–80 nC range gives 26.2–167.5 ns at the same resistance. The result demonstrates sensitivity to the assumed charge; 62.6 ns is a selected calculation rather than a universal maximum. Burst startup, branch asymmetry, and nonlinear current variation are omitted from this estimate. The assumption in Figure 8 is based on the calculation results of actual board-level parasitic parameters and device parameters, while the assumption in Figure A2 is based on the display of physical effects during the conversion time using fixed charges and self-set parallel capacitance sizes.

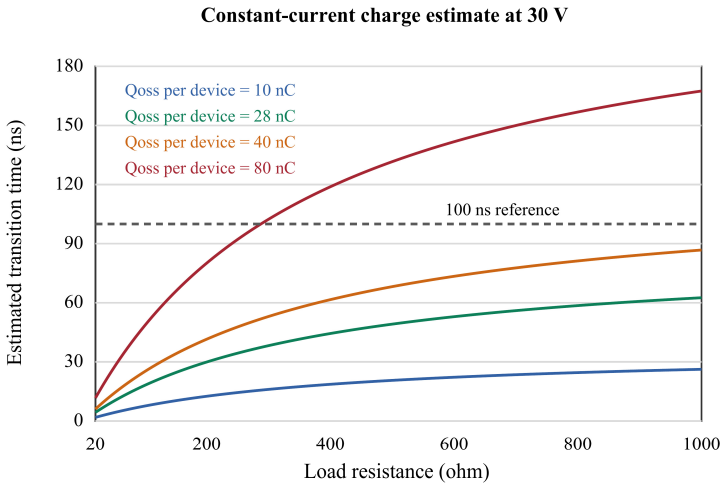


Figure A2. Constant-current transition-time estimates for the stated assumed device charges. Curves are sensitivity calculations, not measured ZVS boundaries.

Appendix B. Supporting Experimental Data

Table A1 reports the individual burst-pressure values used in Section 3.4. The tabulated sample standard deviation uses $n - 1$ in its denominator. No observations were removed.

Table A1. Stored individual burst-pressure observations at 82.4 N clamping force.

Observation	30 V (mmHg)	40 V (mmHg)	50 V (mmHg)
1	31.19	33.89	43.28
2	31.90	30.39	28.02
3	35.69	29.60	35.68
4	28.30	28.87	34.98
5	31.74	28.74	32.25
Mean	31.76	30.30	34.84
Sample SD	2.63	2.11	5.59

Table A2 gives representative total-loss calculations from the fixed 60 Ω efficiency sweep. The input power is reconstructed as P_{out}/η_{inv}, and the loss follows Equation (14). Values are rounded for reporting and do not represent independently measured component losses.

Table A2. Representative total inverter losses derived from the existing efficiency measurements.

Output (W)	Efficiency (%)	Inferred Input (W)	Total Loss (W)
4.92	93.86	5.24	0.32
12.17	94.83	12.83	0.66
47.30	94.66	49.97	2.67
103.98	94.49	110.04	6.06
155.97	93.56	166.71	10.74
183.69	93.37	196.73	13.04

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