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An Integrated 48 mV Cold–Start Circuit for the Boost Converter of a DC Energy Harvester Using a Schmitt Trigger Clock Booster and an Ultra–Low–Voltage Ring Oscillator

Mahmoud Ahmed [1,†], Sebastien Genevey [2], Yves Audet [1] and Yvon Savaria [1,*]

[1] Department of Electrical Engineering, Polytechnique Montréal, Montreal, QC H3T 1J4, Canada; mahmoud.ahmed@polymtl.ca (M.A.); yves.audet@polymtl.ca (Y.A.)
[2] Dolphin Design, 1bis A et 2A Chemin du Pre Carre, 38240 Meylan, France; sebastien.genevey@dolphinsemi.com
* Correspondence: yvon.savaria@polymtl.ca
† Current Address: Synopsys Inc., Mississauga, ON L5B 1M2, Canada.

Abstract

This paper proposes an on–chip, ultra–low–power cold–start circuit for a low–voltage, fast start–up of a boost converter for autonomous thermal energy harvesting from slight temperature differences. An improved charge transfer obtained from a Schmitt trigger (ST) clock booster enables voltage multiplication of the low input voltage during a cold start, providing low power consumption and a high boosting ratio. The start–up charge pump operates with an on–chip clock generated by an ultra–low–voltage ring oscillator that comprises modified Schmitt trigger (ST) delay cells, as previously reported by the authors. The proposed start–up architecture combines a previously reported advantageous one–shot control mechanism to start the boost converter efficiently. Theoretical analysis supports the proposed start–up scheme, and it is implemented in 22 nm FD–SOI CMOS technology. Simulation results show that, when combined with an inductive boost converter, the proposed harvesting system starts operating in 1.2 s when harvesting energy from a 48 mV DC source. To the best of the authors' knowledge, 48 mV is the lowest reported minimum start–up voltage for a simulated fully integrated start–up circuit operating without additional sources of energy. The complete primary boost converter that was simulated requires a standard 82 µH off–chip inductor.

Keywords: clock booster; DC–DC converter; integrated cold start; ring oscillator; thermoelectric energy harvesting; TEG; start–up techniques; Schmitt Trigger; cold start–up; dynamic body biasing; low–voltage cold start; ultra–low power; energy harvesting; sub–threshold

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1. Introduction

Achieving battery–free operation is urgently needed to avoid battery replacement costs and reliability issues, particularly in implantable biomedical devices or remote sensors in marine or space environments [1,2]. Therefore, harvesting ambient energy has become an exciting way to supply power to devices or to charge small batteries [3]. Unlike solar power, human body heat can be harnessed regardless of illumination conditions. Additionally, it does not require vibrating media as opposed to mechanical motion harvesting, which is not always available in many applications. On the other hand, RF energy

is generally available in the environment. However, ambient RF energy density and incident power in free space are relatively limited [4–6]. Body heat is thus an ideal energy source for self−powered wearable or biomedical devices, such as pacemakers [7–9].

Nevertheless, TEGs for body−wearable or implantable applications typically limit the output voltage to around 40 to 60 mV for temperature differences of 1 to 2 K between the body and the ambient temperature. Thus, effective harvesters starting from around 50 mV are needed [10–12]. This very low output voltage cannot power conventional CMOS electronic circuits. This calls for highly efficient voltage multiplier circuits (boost DC–DC converters) to boost the input voltage to the desired output value [12]. A conventional DC–DC boost converter requires a DC voltage of at least 500 mV to start the main boost converter controller and trigger the remaining electronics. This can be achieved through a start−up circuit powered by the primary DC energy source [12].

A comprehensive discussion of recent ultra−low−voltage cold−start techniques for thermoelectric and self−powered microsystems has been recently published by the authors in [13]. One promising technique is a DC–AC–DC conversion using ring oscillators (ROs) and a charge pump. However, an ultra−low−voltage RO is needed since the simple inverter RO requires a relatively large supply voltage (VDD > 100 mV) to allow for correct logic operation. Furthermore, a charge pump is less effective in the sub−threshold region unless the clock amplitude is significantly boosted. Therefore, this work presents a fully integrated, ultra−low−power start−up circuit comprising an RO built using a modified Schmitt trigger (ST) delay cell suitable for low−voltage start−up DC energy−harvesting systems, as previously presented by the authors in [14].

This paper introduces a novel Schmitt trigger clock booster architecture to double the amplitude of complementary clock signals generated by the RO. Unlike conventional boosters that fail in the sub−threshold region due to severe leakage, the proposed architecture inherently suppresses this leakage through an active feedback mechanism. This structural innovation provides high boosting ratios and ultra−low power consumption independently of the underlying technology node. Consequently, a higher clock amplitude will lead to more effective charge pump operation. Furthermore, our rigorous theoretical analysis (presented in Section 5.2) was explicitly motivated by the observation that migrating to finer line−width technology nodes does not inherently resolve the fundamental minimum start−up voltage limits. Therefore, architectural innovations like the proposed active leakage suppression are strictly necessary. While the ring oscillator delay cell [14], SGU [15], and voltage reference [16] are adapted from prior works, the primary novel contributions of this paper are the ST clock booster topology featuring sub−threshold active leakage suppression and the integrated converter start−up theoretical analysis. The proposed start−up architecture is then combined with the one−shot control mechanism of [15] to enable effective boost converter start−up. A theoretical approximation of the proposed start−up minimum voltage is derived. Then, the proposed structure is implemented in a complete boost converter and simulated using 22 nm FD−SOI technology. While the advanced 22 nm FD−SOI process undeniably offers excellent device characteristics, its selection is primarily driven by the requirements of modern ultra−low−power Internet of Things (IoT) nodes.

Today, energy harvesters are increasingly integrated on the same System−on−Chip (SoC) as advanced digital microprocessors and RF transceivers. Implementing the proposed architecture with an advanced node demonstrates its compatibility and practical relevance for these highly integrated, state−of−the−art commercial applications.

Results show that the proposed system can start from a supply voltage as low as 48 mV, the lowest reported start−up voltage for a simulated fully integrated start−up circuit. The rest of this paper is organized as follows. Section 2 describes the start−up architecture. Sections 3 and 4 elaborate on the design of the exploited ultra−low−voltage ring oscillator

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and proposed clock booster. Section 5 analyzes the charge pump sub−threshold operation and derives a theoretical voltage limit for start−up circuits. Section 6 summarizes the strobe generation and one−shot start−up mechanisms. Section 7 presents the simulation results for the design implemented using 22 nm FD−SOI. Finally, the paper concludes in Section 8.

2. Operation of the Proposed Start−Up Circuit Combined with a One−Shot Control Mechanism

The proposed hybrid start−up architecture integrates our novel Schmitt trigger (ST) clock booster with an adapted ultra−low−voltage ring oscillator [14] and strobe generation unit [17]. Collectively, these modules enable a robust 48 mV cold−start limit.

An on−chip start−up charge pump suffers from reduced charge transfer (Q = CV) because of the low input voltage and limited on−chip capacitance resulting from its limited silicon area. This is exacerbated by the low start−up clock frequency at a low supply voltage, which results in a low output current. Therefore, charging a large storage capacitor with a charge pump's low output power is ineffective for low−voltage start−ups. However, although a TEG provides a low output voltage, its low source impedance (typically a few ohms) enables a moderate amount of current to charge an inductor, thus generating higher energy per cycle.

Hence, an ultra−low−power, low−voltage start−up circuit is proposed, combined with the one−shot control mechanism adapted from [17]. This mechanism quickly hands over the power transfer process to a more efficient current−mode inductive boost converter, thereby speeding up the low−voltage start−up process instead of relying solely on a start−up charge pump.

The proposed start−up architecture, depicted in Figure 1, initially boosts the input voltage to power a strobe generation unit (SGU). The voltage−boosting ability of the start−up charge pump is enhanced by using a proposed Schmitt trigger (ST) clock booster to double the amplitude of the clock generated by a low−voltage, on−chip ring oscillator (RO). The SGU generates a pulse V_{PULSE} to switch on an auxiliary low−side switch M_{N0} and load the inductor with current from the TEG. A sharp falling edge of the one−shot pulse V_{PULSE} forces an overshoot of voltage V_S and forward−biases a diode−connected PMOS, M_{P1}. The inductor current immediately charges a small on−chip storage capacitor C_{INT} (150 pF) to a voltage V_{INT} > 380 mV within the strobe cycle itself.

A thyristor−based ring oscillator (TRO) designed to start oscillation at low supply (380 mV) is powered immediately by V_{INT}. It takes control by charging the inductor with a higher current per cycle through a wider switch M_{N1}. V_{INT} can then be connected either to the load or to a subsequent Maximum Power Tracker controller. M_{N0} is disabled during primary operation as V_{PULSE} goes low. The proposed start−up scheme reduces the power burden on the voltage multiplier and achieves low−voltage start−up.

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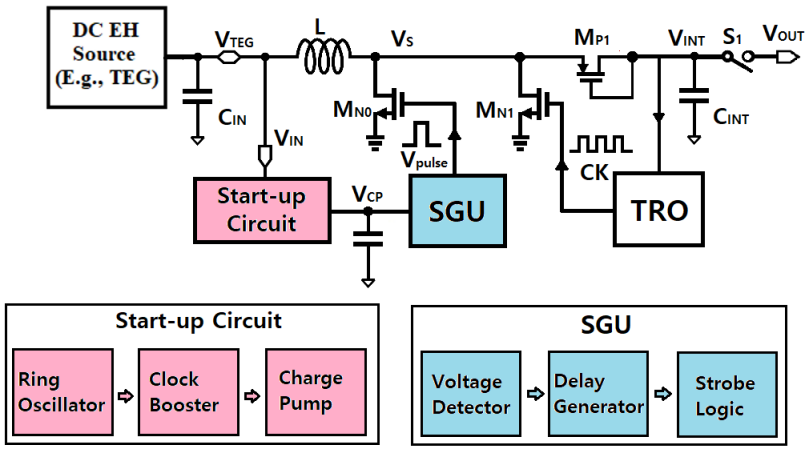


Figure 1. Proposed integrated start–up architecture depicting the main blocks for the proposed start–up circuit and the blocks of the strobe generation unit (SGU). The SGU architecture is adapted from [16] for the quick triggering of the thyristor–based ring oscillator (TRO) to control the primary inductive boost converter.

3. Ultra–Low–Voltage Ring Oscillator

A key block in the proposed start–up circuit is the ultra–low–voltage ring oscillator. The RO generates the clock signal that drives the subsequent charge pump from a very low supply voltage. A classic RO comprises an odd number (three or more) of delay stages, which are simple inverters. However, due to the significant deterioration of the transistors' transconductance with supply voltage reduction, the inverter's DC voltage gains, *A* decreases severely, and oscillation may not build up. Thus, a CMOS inverter with a higher voltage gain is required.

This work adopts the low–voltage ring oscillator architecture and modified Schmitt trigger delay cell presented in [14]. The fundamental principles of operation and circuit implementation have been thoroughly described in that work.

4. Proposed Clock Booster

The second key block in the proposed start–up circuit is the clock booster. We propose an ST clock booster that efficiently generates an amplitude higher than the available supply voltage. The conventional clock booster [15,18,19] functions well in the triode region, but operating in the sub–threshold region requires introducing leakage–suppression techniques to the traditional design. Integrating an ST into the clock booster design makes it more efficient in the sub–threshold region.

We first review conventional clock–boosting techniques and architectures and then introduce the proposed clock booster. The functionality and performance are validated by simulation and comparison against other state–of–the–art architectures. The results show that the proposed clock booster performs better regarding the trade–off between power consumption and the boosting ratio, as explained in [14].

4.1. Clock–Boosting Techniques

As mentioned, the RO can be implemented in a start–up circuit for DC energy harvesters, such as TEGs, solar cells, etc. In this type of circuit, an RO usually generates complementary clock signals to drive a charge pump circuit and produce a higher voltage to start up the subsequent system. However, the signals generated by the RO are limited to a maximum swing of (0–V_{IN}) when no transistor leakage is considered, where V_{IN} is the voltage generated from the DC energy harvester and is used as a supply for the RO circuit. Consequently, the charge pump's efficiency would be limited, and the start–up time

would be extended. Nevertheless, we suppose that some of the energy harvester's power is sacrificed to realize an efficient sub−threshold clock booster. In that case, the generated signals would have a theoretical maximum swing of (0–2 VIN) since the clock booster circuit's key role is to provide a clock amplitude of 2 V_{DD} at each node (where V_{DD} is the supply voltage) [18].

Boosting the clock is advantageous because switches are hard to turn on at ultra−low supply. However, while increasing the transistors' sizes can reduce their on−resistance and help them switch more quickly, it adds more node parasitic capacitance and suffers from charge injection. Therefore, low−voltage clock booster circuits are extensively adopted to sufficiently turn on switches while small transistor sizes can be maintained [20]. Additionally, clock boosting is advantageous for the subsequent system it drives. For instance, if the following block is a Dickson charge pump (DCP), clock boosting helps to improve its performance since using higher clock amplitudes will decrease each diode threshold drop stage, as explained in [21]. Also, clock boosting enables a higher output voltage with fewer stages, leading to a smaller output equivalent resistance and efficiency improvement (an increase in the output voltage per stage results in fewer stages). Therefore, the proposed start−up circuit will produce a DC voltage of around 500 mV from the DC energy harvester start−up equation's output voltage ≈ 50 mV to power the controller of the main DC–DC boost converter.

Moreover, Ref. [19] explains how reducing the number of stages can improve the speed performance of a DCP by a square factor. However, reducing the number of stages would reduce the steady−state output voltage of the DCP. Consequently, doubling the clock amplitude can be exploited to solve this dilemma at the expense of added circuit complexity due to the clock booster [18–20].

Cascading multiple clock boosters in series can also increase clock signal swing; however, the trade−off between their power consumption and efficiency gain must be considered first. All the above reasons make the clock−boosting technique attractive, mainly for applications in which its area of occupation must be reduced while maintaining the same rise time or limited supply voltage, like in energy−harvesting systems.

Furthermore, a clock booster was employed to enhance the charge pump's performance long before targeting the sub−threshold region of operation, as reported in [22]. For instance, Ref. [15] proposes a circuit with a boosted voltage generator. One of its major components needs a charge pump circuit to generate $3V_{DD}$ voltage for its supply. Their booster has formed the basis for conventional clock boosters, known as "Nakagome's cell".

Table 1 summarizes the different architectures of clock boosters implemented in the literature. The conventional clock booster implemented in [15,18,19] is used to reduce the required number of stages and improve power efficiency.

Table 1. Review of different clock booster architectures in the literature.

Ref.	Clock Booster Type	Technology	Frequency (MHz)	Total Pumping Capacitance (pF)	Minimum Supply Voltage	Boosting Ratio	Results Type
[15]	Conventional	0.3 µm triple−well	5.6	0.08	1	1.8×	Measurements
[18]	Conventional	0.25 µm	1	25	0.3	2×	Simulations
[19]	Conventional	65 nm	1	240–480	1.2	2×	Simulations
[20]	All−Nmos	28 nm FD−SOI	1	30	0.05	1.8×	Simulations
[21]	Dual inverter	180 nm	0.512	8	0.35	1.9×	Simulations
[22]	Dual inverter	0.18 µm 5M2P	0.195	N/A	0.2–0.4	N/A	Measurements

[17]	Gate−boosted switches by cross−coupled complementary CPs	0.18 µm CMOS	0.025	16 + 1040 for CP capacitance	0.057	6.8×	Measurements

Additionally, Ref. [19] conducted theoretical analysis and provided a solution that allows either a reduction in the rise time while occupying the same area or an area reduction for the same rise time.

Furthermore, Ref. [23] adopted an All−NMOS clock booster topology, a variation in Nakagome's cell introduced in [15]. The output nodes are connected to two pseudo−inverters to recover the full voltage swing of $2V_{IN}$ for its operation. This topology presents a more compact solution, as NMOS transistors have smaller dimensions than the corresponding PMOS transistors.

A third variation in clock boosters is presented in [24]. Hereafter, we call this topology a "dual−inverter clock booster", as two inverters are used in each branch. Its high boosting ratio can be traded with the power, area, and speed to optimize its performance.

Finally, Ref. [17] proposed a different scheme to realize the clock booster by integrating it with the subsequent charge pump. It shows that, for ultra−low−voltage operation, each stage needs high VGS, which can be generated by borrowing voltages from later stages of the charge pump. Consequently, they proposed gate booster (GB) circuit blocks that implement dynamically biased inverters to generate the gate clocks. The proposed scheme is suitable for sub−threshold operation and can boost the clock up to six times or more, albeit at the expense of a large area due to the large number of charge pump stages and pumping capacitors (16 pF + 1040 pF for charge pump capacitance in [17]).

4.2. Proposed ST Clock Booster

We propose a sub−threshold Schmitt trigger (ST) clock booster to double the amplitude of complementary clock signals (generated from the RO or any other oscillator) while offering better performance than conventional architectures (better power consumption and boosting−ratio trade−off).

The conventional clock booster [15,18,19] functions well only in the triode region and not the sub−threshold region due to significant reverse leakage currents that degrade the pumped voltage. Our architectural innovation is to incorporate ST cells into the clock booster structure to achieve active leakage suppression. Regardless of the technology node, the ST cells use internal feedback mechanisms to actively cut off leakage paths when the complementary clock phases transition. Figure 2a illustrates the proposed clock booster structure. It comprises two input capacitors, two NMOS devices, and two ST cells. Its operation, as explained in detail in Figure 2b,c, is as follows. When CLK is low, CLK_B is high, C_1 charges up to V_{DD} through N_6, P_1 and P_0 are turned off, and the output signal CLK_2 through N_1 and N_0 is electrically connected to the ground. Node G is connected to the ground through P_2 and turned on through feedback from CLK_2. Hence, leakage through P_1 is suppressed significantly. When CLK is high, CLK_B is low, C_1 charges up to $2V_{DD}$, P_1 and P_0 are turned on, and the output signal CLK_2 through P_1 and P_0 is boosted to $2V_{DD}$. Node F is connected to V_{DD} through N_2, which turns on due to feedback from CLK_2. Hence, leakage through N_1 is suppressed significantly. A similar operation happens at the right branch to generate complementary clock signals (CLK_2, CLK_{B2}).

To verify the effectiveness of the proposed clock booster and validate the actual advantage in terms of less power consumption and a high boosting ratio, the proposed clock booster and the most significant state−of−the−art clock boosters have been designed and simulated using a 22 nm FD−SOI technology for the sake of comparison, and results are shown in Figure 3a,b). All clock boosters were tested under similar input and output conditions at a supply voltage of 50 mV, as the primary target of the proposed clock booster

is to operate in the sub−threshold region for energy−harvesting systems at the lowest possible VDD (i.e., VIN). As illustrated in Figure 3a,b, the proposed clock booster achieves a higher boosting ratio and lower power consumption than both conventional inverter and All−NMOS clock boosters over a large input frequency range (5–40 KHz). Only the dual−inverter clock booster has a lower power consumption than the proposed clock booster; however, it suffers from degraded boosting ratio over the indicated frequency range. Therefore, the proposed clock booster achieves the best balance between low power consumption and a high boosting ratio (best performance) over an extended input frequency range. Furthermore, Figure 4 shows the waveforms of the clock boosters when the input clock signal is generated from the proposed RO at 50 mV input voltage. The proposed clock booster achieves a higher boosting ratio than other architectures due to advanced leakage suppression.

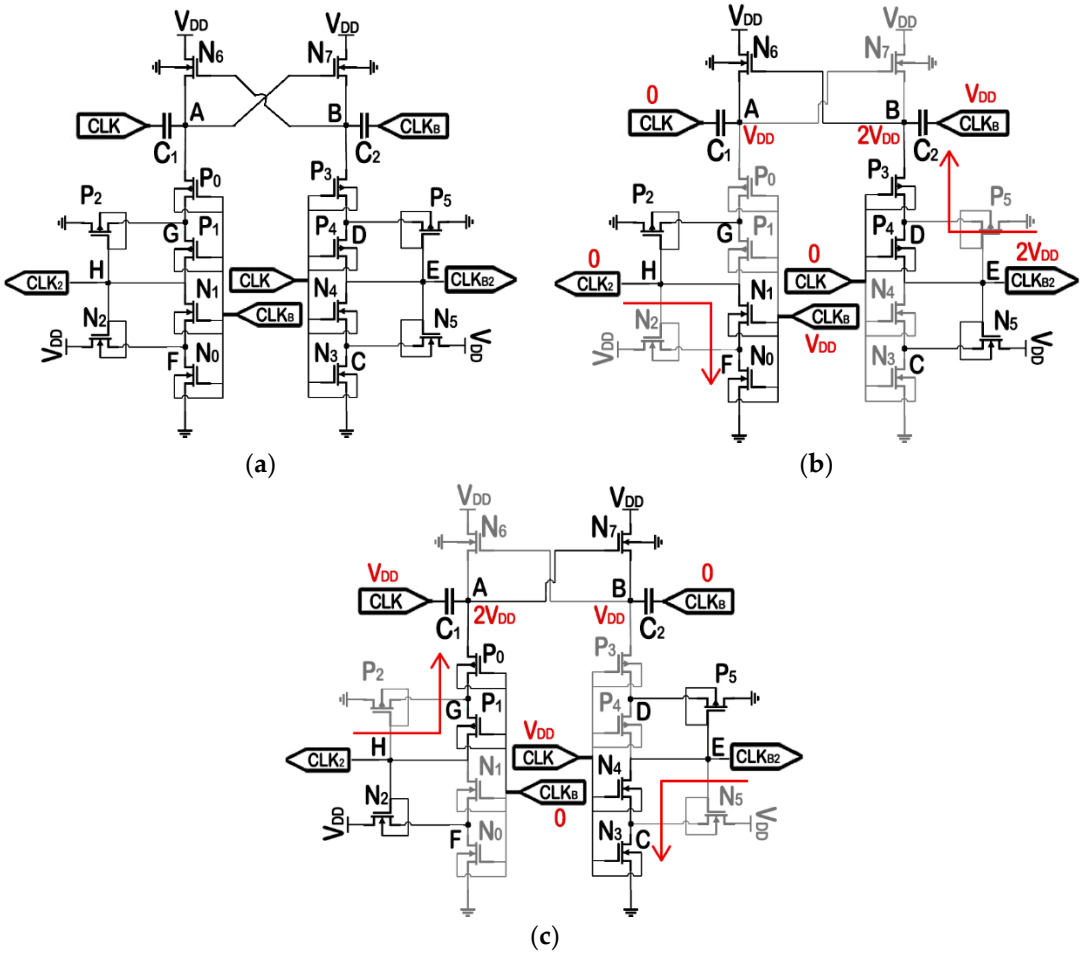


Figure 2. (**a**) Proposed sub−threshold ST clock booster structure; (**b**) first−stage operation (discharging on left side); (**c**) second−stage operation (charging on left side). In (**b**,**c**), red text denotes specific node voltages, red arrows indicate the direction of active current paths, and greyed−out components represent inactive or turned−off transistors during that stage.

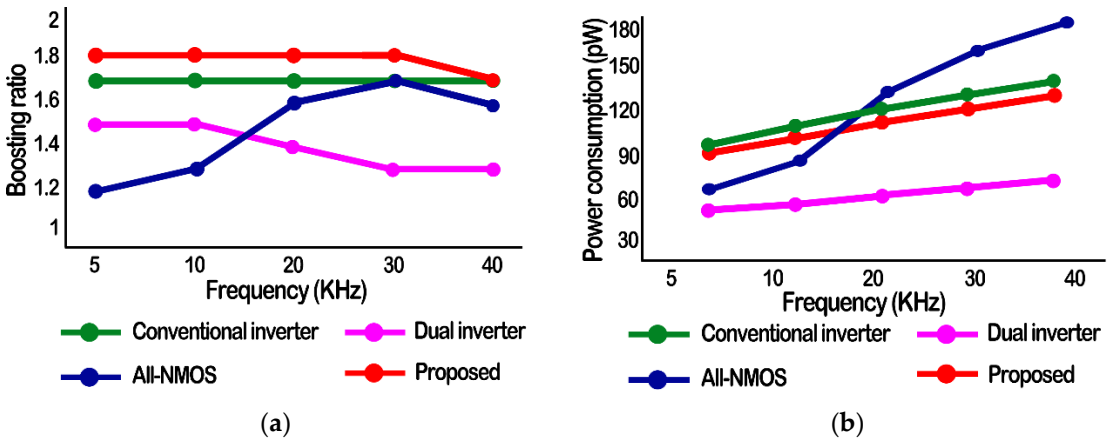


Figure 3. Simulated performances of the proposed clock booster in a 22 nm FD–SOI technology vs. published works @ 50 mV input supply producing different frequencies. (**a**) Boosting ratio vs. input clock frequency. (**b**) Power consumption vs. input clock frequency.

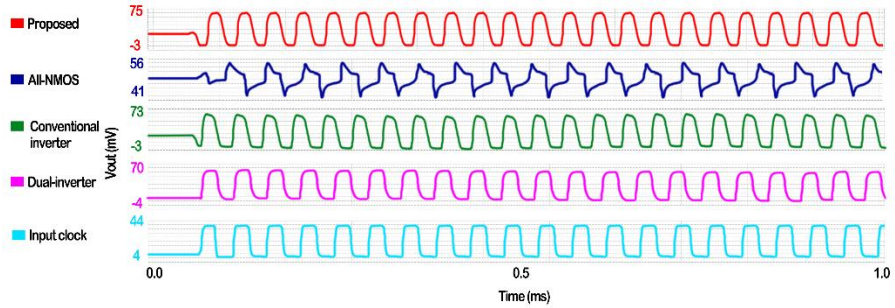


Figure 4. Simulation results of clock boosters at 50 mV input clock generated from the proposed RO using 22 nm FD–SOI CMOS technology.

5. Charge Pump Design

Charge pumps (CPs) are clocked circuits implemented by switched capacitors. Therefore, they can be fully integrated. In our context, the CP boosts the voltage the TEG generates to an intermediate value, high enough to power the subsequent controller to start the main boost converter. A general block scheme of an N−stage CP is shown in Figure 5, where each i−th stage comprises a charge transfer switch (CTS) and a pumping capacitor, denoted as C. The CTS transfers charge from the input to output irreversibly.

The authors of [25] proposed the first integrated CP, where the CTS was a diode−connected n−type MOSFET, which works in saturation or the cut−off region. Although it is simple and allows adequate current drivability, its efficiency and voltage gain are strongly affected by the V_{TH} of the transistors [25–28]. Moreover, additional analysis is needed, as the transistors operate in the sub−threshold region given that the start−up CP is supplied (40–100) mV generated by the TEG.

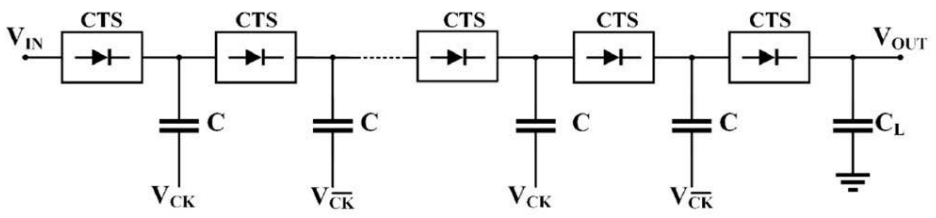


Figure 5. Simplified scheme of a linear Dickson charge pump from [26].

5.1. Charge Pump in the Sub–Threshold Region

When the CP works under ultra–low voltage conditions, the transistors of the CTS work in the sub–threshold region (i.e., with V_{GS} voltage lower than the transistor threshold voltage V_{TH}). The transistor current–voltage relationship in this region is given by [29] as

$$I_{SUB} = I_0 . \frac{W}{L} . e^{\left(\frac{|V_{GS}|-|V_{TH}|}{nV_T}\right)} . \left(1 - e^{-\frac{|V_{DS}|}{V_T}}\right) \quad (1)$$

where n is the sub–threshold slope; $I_0 = \mu_0 . C_{ox} . (n-1)$; V_T^2 is a constant; $V_T = kT/q$ is the thermal voltage; W/L is the transistor aspect ratio; V_{DS} is the drain–to–source voltage; and V_{TH} is the threshold voltage, whose value is given as

$$V_{TH} = V_{TH0} - \lambda_{DS} V_{DS} - \lambda_{BS} V_{BS} \quad (2)$$

where V_{BS} is the bulk–to–source voltage, V_{TH} is the zero–bias threshold voltage (i.e., the value of V_{TH} for V_{DS} and V_{BS} equal to zero), and λ_{DS} and λ_{BS} are positive technology parameters used to model the drain–induced barrier–lowering (DIBL) effect and the body effect, respectively.

In this work, the conventional dual–branch structure, as depicted in Figure 6a, is selected for implementing the start–up CP. Its latch configuration reduces ripple and enhances charge transfer, thus improving power efficiency.

Since cross–coupled CPs are similar to dual–branch CPs, the pumping capacitances of a single stage are halved compared to the classical Dickson CP. Therefore, transistors should be made smaller. Moreover, gate and body biasing techniques can also be applied to improve their operations [26].

Ref. [20] derived an approximation for the dual–branch CP's minimum input voltage in the sub–threshold region. The result is further analyzed in the following subsection to derive an approximation for the start–up voltage limit of the proposed start–up circuit comprising the RO, clock booster, and dual–branch CP.

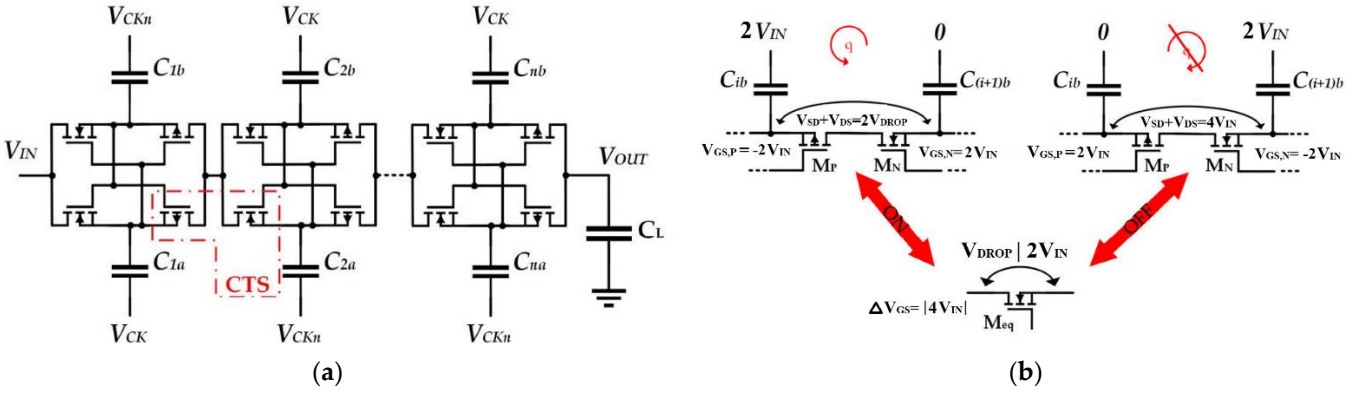


Figure 6. Dual–branch charge pump from [26]: (**a**) simplified scheme, where the red dash–dotted box outlines a single charge transfer switch (CTS); (**b**) voltage distribution in the on and off states, where red solid arrows indicate state transitions and red curved arrows indicate charge flow direction.

5.2. Minimum Voltage Limit of the Proposed Start–Up Circuit

The theoretical derivation of the minimum start–up voltage limit relies on the following key assumptions:

- Sub–Threshold Operation: The charge transfer switch (CTS) transistors operate strictly in the deep sub–threshold region ($V_{IN} < 100$ mV).
- Equivalent Switch Model: The dual–branch CP CTS is modeled as a single equivalent transistor combining the parallel n–type and p–type coefficients ($\lambda_{DS,eq}$, $\lambda_{BS,eq}$).

- Ideal Clock Boosting: The input voltage amplitude is perfectly doubled without resistive losses ($V_{CK} = 2V_{IN}$).
- Ideal DBB: Dynamic body biasing provides the maximum threshold voltage modulation ($\Delta V_{GS} = \Delta V_{BS} \approx 4V_{IN,min}$).

According to Figure 6b, the CTS in the dual−branch CP is modeled with only one transistor whose equivalent coefficients $\lambda_{DS,eq}$ and $\lambda_{BS,eq}$ are the parallel of the corresponding n−type and p−type MOS transistor coefficients (i.e., $\lambda_{DS,eq} = \lambda_{DS,n}//\lambda_{DS,p}$ and $\lambda_{BS,eq} = \lambda_{BS,n}//\lambda_{BS,p}$, respectively).

Furthermore, to evaluate the effectiveness of a transistor working as a switch, a commonly used metric is the ratio between the current flowing during the forward conduction, I_{FWD}, and the backward current when the switch is off, I_{BWD}, which is desirable for this to be far greater than unity.

Assuming I_{FWD} and I_{BWD} as described by (1), in which the expression in (2) replaces the threshold voltage V_{TH}, we can calculate their ratio as

$$\frac{I_{FWD}}{I_{BWD}} \approx \left(\frac{e^{\frac{V_{GS.FWD,eq}+\lambda_{DS,eq}V_{DS.FWD,eq}+\lambda_{BS,eq}V_{BS.FWD,eq}}{nV_T}}}{e^{\frac{V_{GS.BWD,eq}+\lambda_{DS,eq}V_{DS.BWD,eq}+\lambda_{BS,eq}V_{BS.BWD,eq}}{nV_T}}} \right) . \left(\frac{1 - e^{-\frac{V_{DS.FWD,eq}}{V_T}}}{1 - e^{-\frac{V_{DS.BWD,eq}}{V_T}}} \right) \quad (3)$$

By assuming the voltage differences between values in forward and backward conditions during on and off phases, (3) can be rewritten as:

$$\frac{I_{FWD}}{I_{BWD}} \approx \frac{1 - e^{-\frac{V_{DS.FWD,eq}}{V_T}}}{1 - e^{-\frac{V_{DS.BWD,eq}}{V_T}}} . e^{\frac{\Delta V_{GS}+\lambda_{DS,eq}\Delta V_{DS}+\lambda_{BS,eq}\Delta V_{BS}}{nV_T}} \quad (4)$$

Considering $V_{DS.FWD,eq}$ and $V_{DS.BWD,eq}$ are lower and far greater than V_T, respectively, we can approximate (4) as

$$\frac{I_{FWD}}{I_{BWD}} \approx \frac{V_{DS.FWD,eq}}{V_T} . e^{\frac{\Delta V_{GS}+\lambda_{DS,eq}\Delta V_{DS}+\lambda_{BS,eq}\Delta V_{BS}}{nV_T}} \quad (5)$$

Considering a CTS with only one equivalent transistor along the input−output path, as shown in Figure 6b, the voltage across its drain−source nodes is equal to a voltage drop, V_{DROP} or 2 V_{IN} when the switch is on or off, respectively (i.e., $V_{DS.FWD,eq} = V_{DROP}$, and $V_{DS.BWD,eq} = 2\ V_{IN}$).

Furthermore, we define the unacceptable lower bound as $(\frac{I_{FWD}}{I_{BWD}})min = 1$, and since $V_{DS.FWD,eq} = V_{DROP} << V_{DS.BWD,eq} = 2V_{IN,min}$, we can obtain the $V_{IN,min}$—the minimum input voltage value at which I_{FWD} equals to I_{BWD}—of the dual−branch CP as

$$nV_T ln\left(\frac{V_T}{V_{DROP}}\right) \approx \Delta V_{GS} + \lambda_{BS,eq}\Delta V_{BS} - 2\lambda_{DS,eq}V_{IN,min} \quad (6)$$

Alternatively, when rearranged:

$$V_{IN,min} \frac{\Delta V_{GS} + \lambda_{BS,eq}\Delta V_{BS} - nV_T ln\left(\frac{V_T}{V_{DROP}}\right)}{2\lambda_{DS,eq}} \quad (7)$$

V_{IN} for the charge pump, combined with the ring oscillator's minimum supply voltage, constitutes the proposed system's minimum start−up limit. Thus, we can approximate the ideal start−up limit from (7) by assuming the proposed ring oscillator is supplied by the same source as the charge pump (i.e., TEG energy harvester). Its output clock is ideal (i.e., $V_{CLK} = V_{IN}$), and it is then doubled by the proposed clock booster (i.e., V_{CLK} =

$2V_{IN}$). As illustrated by Figure 6b, $\Delta V_{GS,P} = \Delta V_{GS,N} \approx \Delta 4V_{IN,min}$. Also, applying dynamic body biasing (DBB) renders $\Delta V_{GS} = \Delta V_{BS} \approx 4V_{IN,min}$.

Thus, (7) becomes

$$V_{IN,min}\frac{4V_{IN,min}(1+\lambda_{BS,eq}) - nV_T ln\left(\frac{V_T}{V_{DROP}}\right)}{2\lambda_{DS,eq}} \quad (8)$$

Finally, $V_{IN,min}$ is the limit for the start−up circuit, which can be approximated as:

$$V_{IN,min}\frac{nV_T ln\left(\frac{V_T}{V_{DROP}}\right)}{4+4\lambda_{BS,eq}-2\lambda_{DS,eq}} \quad (9)$$

By inspecting (9), the result is independent of the zero−bias threshold current, I_0, and the transistor aspect ratio, W/L. Moreover, the gate and body biasing techniques, which increase the corresponding voltage difference ΔV_{GS} and ΔV_{BS}, lower the limit by increasing the denominator of (9).

The building blocks were designed and simulated using 22 nm FD−SOI technology, and the parameters of the implemented transistors (flip−well, low−threshold transistors) are summarized in Table 2. The derived theoretical limit is validated using simulation results of the proposed RO and clock booster with a 45 mV supply. For a clock frequency f_{CK} = 25 KHz, the simulated value of $V_{DROP} \approx 1.5$ mV. The non−ideal performance of the proposed RO and clock booster is accounted for by replacing the value of ΔV_{GS} in (9) to be 2.1 V_{IN} instead of 4 V_{IN}. The value of V_{IN} is theoretical (i.e., in the case of an ideal RO and clock booster). On the other hand, the value of 2.1 V_{IN} is obtained from simulation as illustrated by Figure 6b. Thus, the theoretical limit of the proposed start−up architecture can be approximated as $V_{IN,min} \approx 42$ mV.

The simulated start−up voltage limit is 45 mV, which is very close to the derived theoretical value expressed through (9).

Table 2. MOS transistor parameters in 22 nm FD−SOI CMOS technology.

	W/L (μm/μm)	**n**	**V_{TH0} (mV)**	**λ_{DS}**	**λ_{BS}**
SLVT−NMOS	10.24/0.1	1.2	333.6	0.011	0.083
EXLVT−PMOS	1/0.2	1.2	197.5	0.012	0.075

6. Strobe Generation and One−Shot Start−Up

The one−shot start−up mechanism using an SGU is adapted from [17]. The working principle is explained as follows: as shown in Figure 7, the SGU is powered by the output of the start−up charge pump V_{CP} to generate the control pulse V_{PULSE} required to kick−start the inductive boost converter.

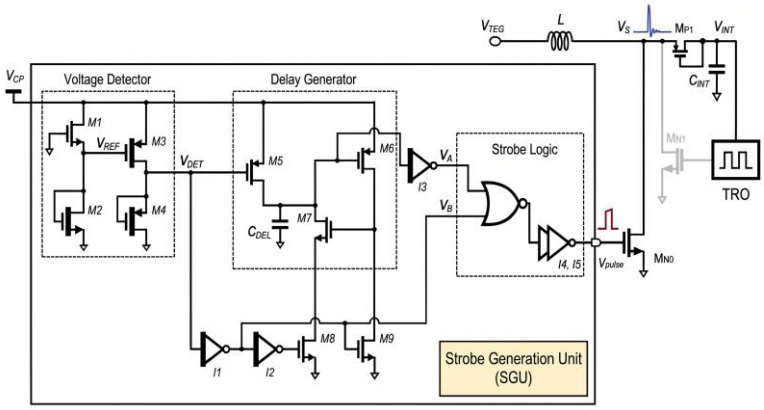


Figure 7. Circuit schematics of the Modified Strobe Generation Unit (M-SGU), design adaptation based on concepts from [17].

The SGU consists of a voltage detector, a delay generator, and a strobe logic circuit. Because the charge pump's output power is low, the SGU must operate with a very small quiescent current. The voltage detector output V_{DET} asserts V_{PULSE} once V_{CP} crosses a threshold that is sufficiently higher than the V_{TH} value of M_{N0} to energize the inductor with the required start−up current.

A low−power reference generator is implemented using low−V_{TH} and high−V_{TH} transistors, namely M_1 and M_2, respectively, as adapted from [30]. Static current is minimized by using long−channel devices for M_1 and M_2; however, the settling of the reference voltage is still fast compared to the slow rise in V_{CP}. It is worth noting that a temperature−compensated voltage reference in [30] requires digital trimming, which is not implemented in our design due to some complexity. Additionally, the design in [30] is tested using relatively larger technologies (65, 130, and 180 nm).

The detector comprises high−V_{TH} PMOS transistors M_3 and M_4. The current through M_3 is compared against the leakage current through M_4 (gate−source shorted); with the rise in V_{CP}, the V_{GS} of M_3 increases, and as the current through M_3 goes above the leakage current of M_4, the output V_{DET} starts rising and follows V_{CP}.

M_{N1} is sized to energize the inductor with the required start−up current without substantially slowing the falling−edge transition of V_{PULSE} due to a larger gate capacitance. V_{DET} is delayed to generate V_A using a thyristor−based latch formed by the transistors M_6 and M_7. The capacitor C_{DEL} is precharged to V_{CP} by M_5 before V_{DET} rises. Once M_5 is turned off, the latch is enabled by turning M_8 and M_9 off using V_{DET}. As C_{DEL} is discharged by the leakage current while V_{CP} rises, the V_{SG} of M_6 increases, which charges the gate of M_7; the M_6 and M_7 regenerative feedback quickly discharges C_{DEL}. The thyristor latch avoids a crowbar current during voltage transitions and minimizes power consumption.

V_{PULSE} is finally generated through V_A and V_B using NOR logic (M_{10}–M_{13}) and buffered to the gate of M_{N0}. All internal buffers (I_1–I_3) are designed with high−V_{TH} transistors to reduce the leakage current.

A diode−connected PMOS with a low static current consumption is used to reduce the voltage drop in the current path from the inductor to the capacitor C_{INT}. An energy−efficient TRO [16] is designed to oscillate at a supply voltage as low as 380 mV. This enables the clock CK to start immediately after the strobe cycle and take over control of the inductive boost converter.

As the TRO takes control, the inductor is energized using a wider switch M_{N1} and operated in a discontinuous conduction mode (DCM), which is suitable for this low−power level. Moreover, unless the energy stored in the inductor during the strobe cycle is sufficient to power the TRO, the inductive boost converter cannot successfully

start up with the one−shot strobe pulse. This fundamental requirement is expressed as follows:

$$\frac{1}{2}L\left(\frac{V_{TEG}}{R_{N0}}^2\right) > \frac{1}{2}C_{INT}V_{INT}^2 + \frac{V_{INT}I_{TRO}}{f_s} \quad (10)$$

where R_{N0} is the on−resistance of M_{N0} during the strobe cycle, f_s is the frequency of CK, and I_{TRO} is the current drawn by the TRO. Conduction loss and the leakage current through the diode−connected PMOS are negligible and are not included for simplicity. R_{N0} is dependent on the voltage drive V_{PULSE} and the size of M_{N0} during the strobe period, whose upper limits are bounded by the available output power of the start−up circuit at the cold−start voltage.

7. Simulation Results

The proposed cold−start architecture is implemented using 22 nm FD−SOI CMOS technology. Figure 8 shows the proposed 23−stage start−up circuit layout occupying an area of 0.9 × 1.2 mm². The 45 mV pre−layout and 48 mV post−layout start−up results correspond to the 46−stage version, whereas the 23−stage version achieves a 50 mV post−layout start−up. The main building blocks of each stage are the RO, clock booster, and dual−branch CP. Leakage suppression has become easier in FD−SOI technologies [31], as fully depleted devices do not suffer from high leakage like regular bulk technologies while enabling effective back−gate biasing schemes.

A voltage source with an added 5 Ω series resistance is used to imitate a typical TEG source. This nominal 5 Ω series resistance model follows the experimentally validated methodology adopted in the comparable state−of−the−art sub−100 mV cold−start literature [17].

The primary boost converter uses an 82 µH off−chip inductor. The inductor is exploited in the start−up phase, as the one−shot pulse generated by the SGU generates an overshoot on the inductor side to force it into starting up the primary boost converter.

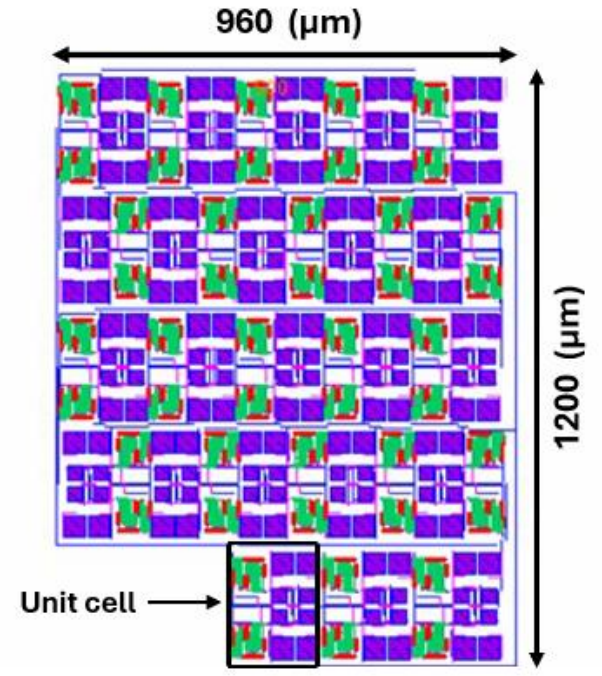


Figure 8. Layout of the proposed 23−stage start−up circuit implemented with 22 nm FD−SOI CMOS technology.

The simulation was performed for an input voltage range relevant to the target application, namely body−heat energy harvesting, where the cold−start block is mainly exposed to sub−100 mV TEG voltages due to the small ΔT between the skin and ambient environment.

As shown in Figure 10b, the primary converter starts with a minimum source voltage of 48 mV. Although the stand−alone start−up circuit operates at a lower input voltage, the leakage current of the SGU loads the start−up CP output and prevents start−up at a lower voltage. The minimum operational voltages of the key blocks are summarized in Table 3. Due to effective leakage suppression of both the proposed RO and clock booster, the boosted clock at 45 mV reaches 1.7× of the RO output, as shown in Figure 9. The start−up block can also operate at 45 mV and charge the intermediate capacitor C_{INT}.

The simulated input and output transient waveforms of the cold−start process in Figure 10 demonstrate that the primary boost converter starts at a minimum input voltage of 45 mV pre−layout and 48 mV post−layout, which corresponds to a temperature gradient of ΔT ≈ 1.6°C. These differences are likely due to layout effects and related parasitics in the target technology. Under the 48 mV input condition, it takes 1.2 s for the SGU to generate the pulse. After self−starting, the inductor boosts the output to 1 V.

The no−load condition refers to the absence of an external application load during the initial cold−start phase. In this phase, the start−up block draws <6 μA, extracting ~345 nJ over 1.2 s, safely covering the minimal picojoule−level energy required to trigger the TRO. However, the system is designed to subsequently power a Maximum Power Point Tracking (MPPT) controller, which consumes 1 to 50 μW [32,33]. To validate this transition, the circuit was simulated with a load mimicking this specific MPPT power requirement. The boost converter, once successfully started up, draws ~ 6.4 mA from the TEG 50 mV input voltage, yielding a total input power (P_{in}) = 50 mV X 6.4 mA = 320 μW. An MPPT equivalent load of 25 KΩand 1 V output voltage yields an output power = $\frac{V^2}{R_{Load}} = \frac{1^2}{25K} =$ 40 μW. Therefore, the power conversion efficiency = $\frac{P_{out}}{P_{in}} = \frac{40}{320} = 12.5\%$.

This efficiency level ensures a robust, self−sustaining cold start capable of energizing the MPPT controller as its first logical load stage.

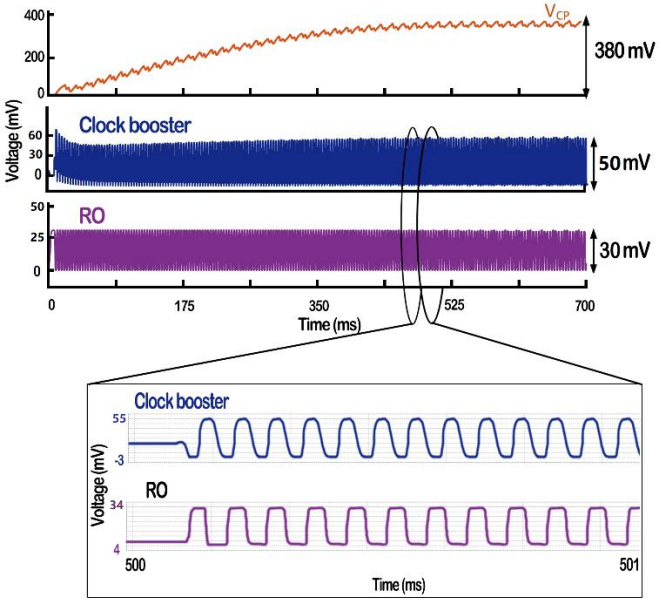
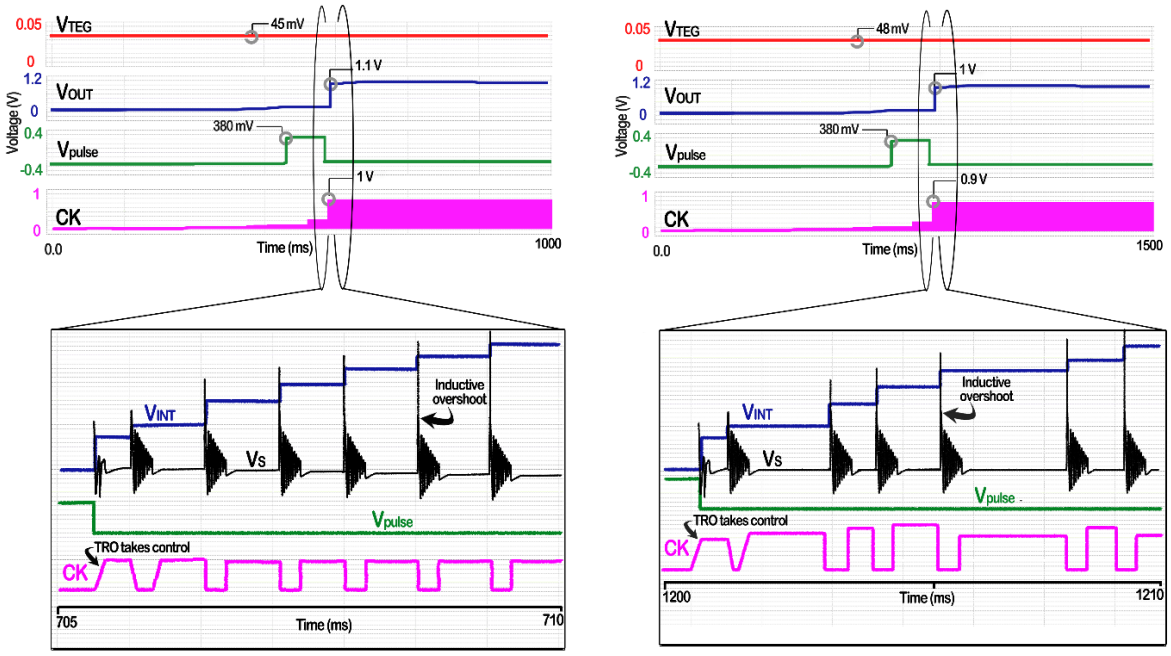


Figure 9. Simulated waveforms of the start−−up clock generated by the ultra−−low−voltage ring oscillator, as boosted by the ST clock booster, and the output of the start−−up charge pump VCP at 45 mV supply.

Table 3. Summary of simulated post−layout minimum operating voltage using 22 nm FD−SOI CMOS technology.

Block	Minimum Operational Voltage
Start−up ring oscillator	32 mV
Start−up clock booster	45 mV
Start−up charge pump	45 mV
Complete cold−start circuit	48 mV

The pumping efficiency of the start−up charge pump is maximized at low input voltages to reduce the minimum start−up voltage. At higher input voltages, a large swing of the boosted clocks causes the CTS to draw more current and increase internal loading. In addition, a low pumping−clock frequency due to the large number of delay stages in the RO reduces the pumping efficiency at higher input voltages. Nevertheless, the boosted output of the start−up charge pump at higher input voltages can easily power the SGU to generate the start−up strobe.



(**a**) (**b**)

Figure 10. Simulated star−t−up transient of the proposed cold−start architecture, with a zoomed−−in view of the waveform showing the triggering of the primary converter with the fast−−falling edge of the strobe pulse for (**a**) pre−−layout simulation at 45 mV and (**b**) post−layout simulation at 48 mV under a no−−load condition.

Before the operation of the inductive converter, the cold−start block is the only active block and draws less than 6 µA of current from the source. However, while the cold−start block draws current from the source during the regular operation of the boost converter, this small input current (see Figure 11) is drawn from the LS input voltage. The power consumed by the cold−start block is negligible compared with the input power of the boost converter and does not affect overall efficiency. As such, the cold−start block is not functionally deactivated during regular operation. Nevertheless, disabling the cold−start block with the start of the inductive converter will increase the maximum input voltage range of the boost converter.

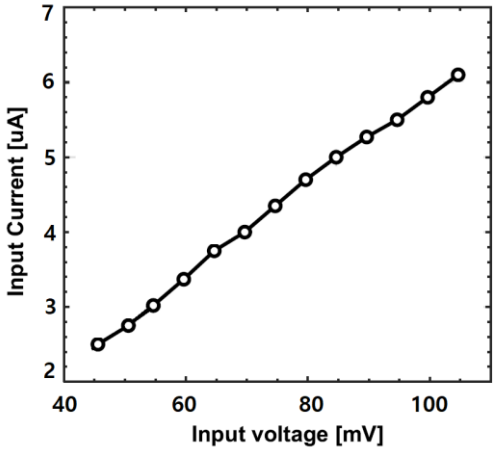


Figure 11. The current drawn from source by the cold−start block at various input voltages.

The minimum input voltage for converter start−up is validated by performing a process−corner analysis over a supply range from 48 to 65 mV. Table 4 summarizes the minimum start−up voltage across process corners and temperatures ranging from −25 °C to 75 °C. While these bounds represent standard industrial IC qualification limits rather than direct body−contact conditions (where the practical ambient envelope spans approximately from 0 °C to 40 °C with the skin at 32–35 °C), they illustrate the sub−threshold trade−offs of the architecture.

At elevated temperatures (75 °C), sub−threshold leakage accelerates the SGU triggering, generating the one−shot pulse prematurely before the charge pump adequately charges C_{INT}. Conversely, at low temperatures (−25 °C), the ring oscillator frequency drops, lowering charge pump current drivability. In the realistic human−wearable range (15 °C to 35 °C), the start−up voltage remains well within 48–55 mV.

Future implementations targeting wider temperature ranges could mitigate premature SGU triggering by employing a leakage−matched voltage detector or incorporating PTAT compensation within the delay generator.

Table 4. Minimum start−up voltage at different process corners and temperatures.

Corner	−25 °C	25 °C	75 °C
TT	100 mV	48 mV	78 mV
FF	120 mV	48 mV	75 mV
SS	100 mV	65 mV	130 mV

Table 5 compares our simulations with silicon−measured performances from other works. Because physical circuits naturally experience performance variations, the 48 mV cold−start voltage should be interpreted as a simulated nominal result rather than measured data. The general start−up mechanism is similar across all references, as they consist of a ring oscillator and a charge pump with variations. The only exception is [34], where they implement an integrated LC oscillator of very small inductance instead of an RO. However, the boost converter inductor is still necessary and adds to the area. Although Ref. [35] measures a similar input voltage in less time, the off−chip inductor of the proposed architecture is smaller and saves more area. Moreover, the approximated theoretical limit, as presented in Section 5.2, indicates that the minimum start−up voltage achieved from a start−up circuit, generally comprising an RO and a charge pump, is limited to values in the order of 2(KT/q) (i.e., 50 mV), and using finer line−width technologies will not significantly push this limit any lower. Furthermore, the minimum required input voltage is expected to increase under extreme temperature or process−corner conditions in

sub−threshold circuits due to the temperature sensitivity of ultra−low−voltage transistor characteristics. Therefore, we recommend an optimized implementation of the voltage detection mechanism to trigger the main boost converter, rather than the conventional design reused from [30]. Finally, the proposed design provides two versions that reflect a trade−off between the minimum start−up voltage and start−up time. Increasing the number of start−up stages makes a lower minimum start−up voltage possible at the expense of a longer start−up time. Thus, the proposed start−up is most suitable for EH systems, where a very low input voltage limit is crucial.

Table 5. Comparison with state−of−the−art integrated cold−start voltages.

Ref.	Year	Process	Start−Up Mechanism	Cold−Start Voltage	Boost Inductor	Start−Up Time	Output Voltage	Output Load	Results Type
[17]	2019	180 nm	Ring oscillator + boosted gate charge pump	57 mV	220 µH	135 ms	1.8 V	No load	Measurements
[36]	2018	65 nm	Ring oscillator + charge pump	210 mV	22 µH	2.3 s (1)	1 V	229 µA	Measurements
[37]	2018	180 nm	Ring oscillator + charge pump	60 mV	220 µH	−	1 V	4.5 µA	Measurements
[7]	2016	180 nm	Ring oscillator + charge pump	60 mV	500 µH (2)	8 ms (1)	2.5 V	52 µA	Post−layout simulations
[38]	2016	130 nm	Ring oscillator + charge pump	70 mV	>200 µH	1.5 s	1.25 V	13.6 µA	Measurements
[35]	2021	180 nm	Ring oscillator + boosted gate charge pump	50 mV	100 µH	252 ms	1.2 V	No load	Measurements
[39]	2019	180 nm	Ring oscillator + charge pump	129 mV	82 µH (3)	150 s (1)	0.8 V	84.5 µA	Measurements
[40]	2022	180 nm	Ring oscillator + charge pump	128 mV	100 µH	80.5 ms	1.2 V	3.15 mA	Pre−layout simulations
[34]	2022	130 nm	LC oscillator + charge pump	70 mV	5.6 µH (4)	40 ms (1)	1 V	96.4 nA	Post−layout simulations
[41]	2023	28 nm	Tri−state buffer + ring oscillator	90 mV	100 µH	>5 s	1.4 V	764 µA	Measurements
[42]	2019	180 nm	Ring oscillator + charge pump	60 mV	N/A	150 ms	1.2 V	20 µA	Measurements
This work (5)	2024	22 nm FD−SOI	Ring oscillator + clock booster + charge pump	48 mV	82 µH	225 ms	1.5 V	No load	Pre−layout simulations 1
This work (5)	2024	22 nm FD−SOI	Ring oscillator + clock booster + charge pump	50 mV	82 µH	335 ms	1.5 V	No load	Post−layout simulations 1

This work [5]	2024	22 nm FD–SOI	Ring oscillator + clock booster + charge pump	45 mV	82 µH	700 ms	1 V	No load	Pre–layout simulations 2
This work [5]	2024	22 nm FD–SOI	Ring oscillator + clock booster + charge pump	48 mV	82 µH	1.2 s	1 V	No load	Post–layout simulations 2

[1] Estimated from transient plots. [2] Totals of 100 µH and 400 µH for the start–up and steady–state boost converters, respectively. [3] Inductance value of transformer. [4] Inductance value of start–up LC oscillator only. The main boost inductance value is not mentioned. [5] Designs 1 and 2 include 23–stage and 46–stage start–up circuits, respectively.

8. Conclusions

This paper proposes a fully integrated ultra–low–power start–up circuit that achieves low–voltage start–up of a boost converter for autonomous thermal energy harvesting from human body heat. The good performance we obtained was partly derived from exploiting an RO built using a modified Schmitt trigger (ST) delay cell suitable for low–voltage start–up DC energy–harvesting systems, as previously reported by the authors. Another key ingredient leading to the reported performance is a novel clock booster that performs better than previously reported circuits. This clock booster offers a unique combination of low power consumption and a high boosting ratio. An on–chip clock generated from an ultra–low–voltage RO drives the start–up charge pump, which is boosted by a Schmitt trigger clock booster. The proposed start–up architecture also leverages a previously reported but very effective one–shot control mechanism to realize an effective start–up of the boost converter. The derived theoretical limit of the proposed start–up architecture supports simulation results and indicates a trade–off between full integration and an ultra–low start–up voltage limit. Post–layout simulation results of the proposed start–up circuit, implemented using 22 nm FD–SOI CMOS technology, validate its capability to assist an inductive boost converter in starting operation within 1.2 s when supplied with an input voltage of 48 mV from the harvesting source under nominal conditions (25 °C). To the best of the authors' knowledge, this is the lowest minimum voltage reported among simulated fully integrated start–up circuits operating without multiple energy sources.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
CMOS	Complementary Metal–Oxide Semiconductor
CP	Charge Pump
CTS	Charge Transfer Switch
DBB	Dynamic Body Biasing
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCP	Dickson Charge Pump
DIBL	Drain–Induced Barrier Lowering
EH	Energy Harvester
FD–SOI	Fully Depleted Silicon–On–Insulator
GB	Gate Booster
GND	Ground
MPPT	Maximum Power Point Tracking
RF	Radio Frequency
RO	Ring Oscillator
SGU	Strobe Generation Unit
ST	Schmitt Trigger
TEG	Thermoelectric Generator
TRO	Thyristor–Based Ring Oscillator
C_{ox}	Oxide Capacitance Per Unit Area
V_{DS}	Drain–to–Source Voltage
V_{GS}	Gate–to–Source Voltage
V_{TH}	Threshold Voltage
W/L	Transistor Width (W)–to–Length (L) Ratio

References

1. Fluur, C.; Bolse, K.; Strömberg, A.; Thylén, I. Patients' experiences of the implantable cardioverter defibrillator (ICD); with a focus on battery replacement and end–of–life issues. *Heart Lung* **2013**, *42*, 202–207. https://doi.org/10.1016/j.hrtlng.2012.11.006.
2. Polonelli, T.; Muller, H.; Kong, W.; Fischer, R.; Benini, L.; Magno, M. Aerosense: A Self–Sustainable and Long–Range Bluetooth Wireless Sensor Node for Aerodynamic and Aeroacoustic Monitoring on Wind Turbines. *IEEE Sens. J.* **2023**, *23*, 715–723. https://doi.org/10.1109/JSEN.2022.3224307.
3. Elvin, N.; Erturk, A. (Eds.) *Advances in Energy Harvesting Methods*; Springer: New York, NY, USA, 2013. https://doi.org/10.1007/978–1–4614–5705–3.
4. Moloudian, G.; Hosseinifard, M.; Kumar, S.; Simorangkir, R.B.V.B.; Buckley, J.L.; Song, C.; Fantoni, G.; O'flynn, B. RF Energy Harvesting Techniques for Battery–Less Wireless Sensing, Industry 4.0, and Internet of Things: A Review. *IEEE Sens. J.* **2024**, *24*, 5732–5745. https://doi.org/10.1109/JSEN.2024.3352402.
5. Shaikh, F.K.; Zeadally, S. Energy harvesting in wireless sensor networks: A comprehensive review. *Renew. Sustain. Energy Rev.* **2016**, *55*, 1041–1054. https://doi.org/10.1016/j.rser.2015.11.010.
6. Li, B.; Shao, X.; Shahshahan, N.; Goldsman, N.; Salter, T.; Metze, G.M. An Antenna Co–Design Dual Band RF Energy Harvester. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 3256–3266. https://doi.org/10.1109/TCSI.2013.2264712.
7. Ashraf, M.; Masoumi, N. A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit for Pacemakers. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2016**, *24*, 26–37. https://doi.org/10.1109/TVLSI.2015.2391442.
8. Chong, Y.–W.; Ismail, W.; Ko, K.; Lee, C.–Y. Energy Harvesting For Wearable Devices: A Review. *IEEE Sens. J.* **2019**, *19*, 9047–9062. https://doi.org/10.1109/JSEN.2019.2925638.
9. Jauregi, I.; Solar, H.; Beriain, A.; Zalbide, I.; Jimenez, A.; Galarraga, I.; Berenguer, R. UHF RFID Temperature Sensor Assisted With Body–Heat Dissipation Energy Harvesting. *IEEE Sens. J.* **2017**, *17*, 1471–1478. https://doi.org/10.1109/JSEN.2016.2638473.

10. Chen, P.−H.; Ishida, K.; Ikeuchi, K.; Zhang, X.; Honda, K.; Okuma, Y.; Ryu, Y.; Takamiya, M.; Sakurai, T. Startup Techniques for 95 mV Step−Up Converter by Capacitor Pass−On Scheme and V_{TH}−Tuned Oscillator With Fixed Charge Programming. *IEEE J. Solid−State Circuits* **2012**, *47*, 1252–1260. https://doi.org/10.1109/JSSC.2012.2185589.
11. Im, J.−P.; Wang, S.−W.; Ryu, S.−T.; Cho, G.−H. A 40 mV Transformer−Reuse Self−Startup Boost Converter With MPPT Control for Thermoelectric Energy Harvesting. *IEEE J. Solid−State Circuits* **2012**, *47*, 3055–3067. https://doi.org/10.1109/JSSC.2012.2225734.
12. Ferreira, J.V.T.; Galup−Montoro, C. Ultra−low−voltage CMOS ring oscillators. *Electron. Lett.* **2019**, *55*, 523–525. https://doi.org/10.1049/el.2019.0281.
13. Ahmed, M.; Genevey, S.; Ali, M.; Savaria, Y.; Audet, Y. Recent Start−Up Techniques Intended for TEG Energy Harvesting: A Review. *IEEE Access* **2024**, *12*, 34116–34130. https://doi.org/10.1109/ACCESS.2024.3372849.
14. Ahmed, M.; Trigui, A.; Genevey, S.; Audet, Y.; Savaria, Y. A 32−mV Supply Ring Oscillator Composed of Modified Schmitt Trigger Delay Cells for Integrated Start−Up Circuits in DC Energy Harvesting Systems. *IEEE Access* **2024**, *12*, 129660–129672. https://doi.org/10.1109/ACCESS.2024.3457839.
15. Nakagome, Y.; Tanaka, H.; Takeuchi, K.; Kume, E.; Watanabe, Y.; Kaga, T.; Kawamoto, Y.; Murai, F.; Izawa, R.; Hisamoto, D.; et al. An experimental 1.5−V 64−Mb DRAM. *IEEE J. Solid−State Circuits* **1991**, *26*, 465–472. https://doi.org/10.1109/4.75040.
16. Liu, X.; Sanchez−Sinencio, E. 21.1 A single−cycle MPPT charge−pump energy harvester using a thyristor−based VCO without storage capacitor. In *2016 IEEE International Solid−State Circuits Conference (ISSCC)*; IEEE: New York, NY, USA, 2016; pp. 364–365. https://doi.org/10.1109/ISSCC.2016.7418058.
17. Bose, S.; Anand, T.; Johnston, M.L. Integrated Cold Start of a Boost Converter at 57 mV Using Cross−Coupled Complementary Charge Pumps and Ultra−Low−Voltage Ring Oscillator. *IEEE J. Solid−State Circuits* **2019**, *54*, 2867–2878. https://doi.org/10.1109/JSSC.2019.2930911.
18. Abdelaziz, S.; Emira, A.; Radwan, A.G.; Mohieldin, A.N.; Soliman, A.M. A low start up voltage charge pump for thermoelectric energy scavenging. In *2011 IEEE International Symposium on Industrial Electronics*; IEEE: New York, NY, USA, 2011; pp. 71–75. https://doi.org/10.1109/ISIE.2011.5984135.
19. Ballo, A.; Grasso, A.D.; Giustolisi, G.; Palumbo, G. Optimized Charge Pump With Clock Booster for Reduced Rise Time or Silicon Area. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1977–1981. https://doi.org/10.1109/TCSII.2019.2898716.
20. Daly, D.C.; Chandrakasan, A.P. A 6−bit, 0.2 V to 0.9 V Highly Digital Flash ADC With Comparator Redundancy. *IEEE J. Solid−State Circuits* **2009**, *44*, 3030–3038. https://doi.org/10.1109/JSSC.2009.2032699.
21. Pan, F.; Samaddar, T. *Charge Pump Circuit Design*; McGraw−Hill: New York, NY, USA, 2006.
22. Wu, C.−Y.; Wey, W.−S.; Yu, T.−C. A 1.5 V CMOS balanced differential switched−capacitor filter with internal clock boosters. In *Proceedings of ISCAS'95—International Symposium on Circuits and Systems*; IEEE: New York, NY, USA, 1995; pp. 1025–1028. https://doi.org/10.1109/ISCAS.1995.519941.
23. Ballo, A.; Grasso, A.D.; Palumbo, G. A Subthreshold Cross−Coupled Hybrid Charge Pump for 50−mV Cold−Start. *IEEE Access* **2020**, *8*, 188959–188969. https://doi.org/10.1109/ACCESS.2020.3032452.
24. Hu, H.; Gupta, S. A 0.22−μW Single−Bit VCO−Based Time−Domain Sensor−to−Digital Front−End With Reduced Supply Sensitivity. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 148–159. https://doi.org/10.1109/TCSI.2021.3096838.
25. Dickson, J.F. On−chip high−voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. *IEEE J. Solid−State Circuits* **1976**, *11*, 374–378. https://doi.org/10.1109/JSSC.1976.1050739.
26. Ballo, A.; Grasso, A.D.; Palumbo, G. A Review of Charge Pump Topologies for the Power Management of IoT Nodes. *Electronics* **2019**, *8*, 480. https://doi.org/10.3390/electronics8050480.
27. Palumbo, G.; Pappalardo, D. Charge Pump Circuits: An Overview on Design Strategies and Topologies. *IEEE Circuits Syst. Mag.* **2010**, *10*, 31–45. https://doi.org/10.1109/MCAS.2009.935695.
28. Tanzawa, T. *On−chip High−Voltage Generator Design: Design Methodology for Charge Pumps*; Springer: New York, NY, USA, 2013. https://doi.org/10.1007/978−1−4614−3849−6.
29. Gariboldi, R.; Pulvirenti, F. A monolithic quad line driver for industrial applications. *IEEE J. Solid−State Circuits* **1994**, *29*, 957–962. https://doi.org/10.1109/4.297702.
30. Seok, M.; Kim, G.; Blaauw, D.; Sylvester, D. A Portable 2−Transistor Picowatt Temperature−Compensated Voltage Reference Operating at 0.5 V. *IEEE J. Solid−State Circuits* **2012**, *47*, 2534–2545. https://doi.org/10.1109/JSSC.2012.2206683.
31. Dghais, W.; Rodriguez, J. *UTTB FDSOI Back−Gate Biasing for Low Power and High−Speed Chip Design*; Springer: Cham, Switzerland, 2015; pp. 113–121. https://doi.org/10.1007/978−3−319−18802−7_16.

32. Galea, F.; Casha, O.; Grech, I.; Gatt, E.; Micallef, J. Ultra Low Frequency Low Power CMOS Oscillators for MPPT and Switch Mode Power Supplies. In *2018 14th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*; IEEE: New York, NY, USA, 2018; pp. 121–124. https://doi.org/10.1109/PRIME.2018.8430355.
33. Ibrahim, M.A.A.; Aboudina, M.M.; Mohieldin, A.N. An ultra−low−power MPPT architecture for photovoltaic energy harvesting systems. In *IEEE EUROCON 2017 −17th International Conference on Smart Technologies*; IEEE: New York, NY, USA, 2017; pp. 201–205. https://doi.org/10.1109/EUROCON.2017.8011105.
34. Xue, C.; Shao, L.; Zhao, L.; Yang, X.; Zhou, H.; Lin, Y.; Ding, Y.; Li, W.; Qu, W. A Dickson Hybrid Boost Converter With On−Chip Cold−Start for Thermoelectric Energy Harvesting. In *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*; IEEE: New York, NY, USA, 2022; pp. 2754–2757. https://doi.org/10.1109/ISCAS48785.2022.9937525.
35. Bose, S.; Anand, T.; Johnston, M.L. A 3.5−mV Input Single−Inductor Self−Starting Boost Converter With Loss−Aware MPPT for Efficient Autonomous Body−Heat Energy Harvesting. *IEEE J. Solid−State Circuits* **2021**, *56*, 1837–1848. https://doi.org/10.1109/JSSC.2020.3042962.
36. Luo, Z.; Zeng, L.; Lau, B.; Lian, Y.; Heng, C.−H. A Sub−10 mV Power Converter With Fully Integrated Self−Start, MPPT, and ZCS Control for Thermoelectric Energy Harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *65*, 1744–1757. https://doi.org/10.1109/TCSI.2017.2757505.
37. Dezyani, M.; Ghafoorifard, H.; Sheikhaei, S.; Serdijn, W.A. A 60 mV Input Voltage, Process Tolerant Start−Up System for Thermoelectric Energy Harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *65*, 3568–3577. https://doi.org/10.1109/TCSI.2018.2834312.
38. Goeppert, J.; Manoli, Y. Fully Integrated Startup at 70 mV of Boost Converters for Thermoelectric Energy Harvesting. *IEEE J. Solid−State Circuits* **2016**, *51*, 1716–1726. https://doi.org/10.1109/JSSC.2016.2563782.
39. Cao, P.; Qian, Y.; Xue, P.; Lu, D.; He, J.; Hong, Z. A Bipolar−Input Thermoelectric Energy−Harvesting Interface With Boost/Flyback Hybrid Converter and On−Chip Cold Starter. *IEEE J. Solid−State Circuits* **2019**, *54*, 3362–3374. https://doi.org/10.1109/JSSC.2019.2924095.
40. Wu, C.; Zhang, J.; Zhang, Y.; Zeng, Y. A 7.5−mV Input and 88%−Efficiency Single−Inductor Boost Converter with Self−Startup and MPPT for Thermoelectric Energy Harvesting. *Micromachines* **2022**, *14*, 60. https://doi.org/10.3390/mi14010060.
41. Ali, M.; Chandrarathna, S.C.; Moon, S.−Y.; Jana, M.S.; Shafique, A.; Qraiqea, H.; Lee, J.−W. A Compact and Efficient Boost Converter in a 28 nm CMOS with 90 mV Self−Startup and Maximum Output Voltage Tracking ZCS for Thermoelectric Energy Harvesting. *Sensors* **2023**, *23*, 6243. https://doi.org/10.3390/s23136243.
42. Coustans, M.; Krummenacher, F.; Kayal, M. A Fully Integrated 60 mV Cold−Start Circuit for Single Coil DC–DC Boost Converter for Thermoelectric Energy Harvesting. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1668–1672. https://doi.org/10.1109/TCSII.2019.2922683.

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