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Research on Zero-Crossing Distortion Suppression Method for Three-Phase Line-Voltage Cascaded Boost High Power Factor Rectifier

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Abstract

The three-phase line-voltage cascaded Boost high power factor rectifier topology has been extensively studied for front-end rectification in high-power charging equipment. However, obvious current distortion occurs near the input voltage zero-crossing point under high-power conditions, which introduces severe harmonics and degrades system stability. Conventional studies often attribute zero-crossing distortion to spike distortion and discontinuous inductor conduction, yet these explanations cannot fully account for the waveform distortion observed in practical engineering scenarios. Based on the one-cycle controlled three-phase Boost PFC converter, this paper establishes a dynamic model to analyze the evolution of distortion under power-frequency grid and various load conditions. The study reveals the key source of current zero-crossing distortion: the fundamental phase shift of input current induced by inductor inertia and digital control delay. Furthermore, a reference current phase-lead scheme is adopted to suppress current zero-crossing distortion. Simulation and experimental results demonstrate that the proposed model can accurately capture current distortion characteristics. This phase compensation strategy can effectively improve the input current waveform, reduce harmonic content and enhance system stability near the rated operating condition, providing theoretical basis and technical support for the optimal design of PFC systems in high-power DC charging piles.

Keywords: power factor correction; boost PFC; current zero crossing; current distortion; phase compensation

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1. Introduction

Unidirectional electric vehicle (EV) charging piles dominate practical applications owing to their lower implementation cost compared with bidirectional chargers [1,2]. Bidirectional chargers support both charging and discharging, which complicates topology, control and protection schemes. Additional functions including anti-reverse power feed, anti-islanding and overcurrent protection are mandatory, raising both hardware expense and software complexity.

By contrast, unidirectional chargers only transfer power from the grid to batteries. The front-end diode rectifier blocks reverse power flow inherently at the topological level. It prevents battery backfeeding under faults such as charging-port short circuits and improves operational reliability [3]. Since no active power is fed back to the grid, islanding

risk is eliminated. The strict anti-islanding compliance for distributed energy resources is unnecessary, which simplifies safety logic and reduces overall system complexity and engineering cost.

However, conventional unidirectional charging piles employ a diode rectifier front-end with a large DC-side filter capacitor. Diodes conduct only when the instantaneous grid voltage exceeds the capacitor voltage, which narrows the conduction angle in each fundamental cycle. This yields discontinuous pulse-shaped grid current, deviating from the sinusoidal waveform synchronized with grid voltage. The resulting severe current distortion and harmonic pollution deteriorate grid power quality and violate grid-code requirements for high-power power-electronic equipment, forming a major bottleneck for power rating upgrading of charging piles [4].

With advances in power factor correction (PFC), AC/DC converters can operate at near-unity power factor to reshape grid-side current and suppress input distortion, matching the trend of power-electronic systems toward high efficiency, low harmonics and low electromagnetic interference. The front-end PFC rectifier dominates the overall efficiency, grid-tied power factor and grid compatibility of high-power charging piles, rendering it a critical component for charger design and optimization [5].

To fulfill the demand for high-power charging, the topology construction of current charging pile power systems mainly relies on modular rectifier units. Three-phase two-level or three-phase Vienna rectifiers are widely adopted as the core topological units, combined with modular architectures such as line-voltage cascading or interleaved parallel connection to achieve power expansion [6,7]. However, in conventional two-level and interleaved parallel architectures, the intensive deployment of a large number of active switching devices inevitably increases system hardware redundancy, significantly raising the complexity and optimization difficulty of control strategy design. In contrast, the line-voltage cascaded topology proposed in Ref. [8] can effectively reduce the number of power switching devices and fast recovery diodes under the same power transmission level. It not only lowers the voltage stress of each power device but also achieves dual optimization of control complexity and hardware cost, providing a new technical approach and solution for the design of high-performance PFC conversion units in high-power charging piles.

Although the three-phase line-voltage cascaded Boost high power factor rectifier topology offers many advantages, its inherent residual current distortion during operation is particularly prominent under high-power and wide-load conditions. Such distortions are mainly concentrated near the current zero-crossing points, forming typical zero-crossing distortion phenomena. This phenomenon can lead to excessive harmonic content and reduced system stability. In severe cases, it may even cause false protection actions, directly threatening the safe and stable operation of charging equipment and the power grid. It has become one of the key factors restricting the performance improvement of high-power charging piles.

Conventional research predominantly attributes zero-crossing distortion to spike distortion and the intermittent conduction of inductance discontinuous conduction [9], which makes it difficult to fully explain waveform distortion phenomena in practical engineering applications and also prevents the targeted proposal of effective suppression methods. Under conventional power frequency steady-state conditions, such distortions have small amplitudes and limited impact on overall system performance, so a systematic mechanism analysis and theoretical explanation framework has yet to be formed. However, in high-performance operation scenarios of large-power charging piles, the coupling effects of complex operating conditions such as strong interference, wide input voltage range and large-range dynamic load switching significantly exacerbate zero-crossing distortion.

Therefore, there is an urgent need to conduct research on the mechanism revelation and suppression technologies for this type of distortion [10].

Refs. [11–16] conducted in-depth research on the PFC rectifier topology for unidirectional energy flow at the mechanism level, pointing out that the distortion of the grid voltage zero-crossing point is induced by the coupling of multiple factors, which can mainly be summarized into three aspects. Firstly, the instantaneous amplitude at grid voltage zero-crossing points nears zero, leading to an inadequate effective driving voltage for the inductance and significantly constraining the dynamic current tracking capability, consequently resulting in a lag in reference current tracking and directly inducing current distortion [11]. Secondly, the load fluctuation range of charging piles is wide. The equivalent gain of current loops varies dynamically with the load, leading to a decrease in system phase margin and deterioration of damping characteristics. This further affects the dynamic response in the zero-crossing region and exacerbates current distortion [12]. Thirdly, the inherent phase lead characteristics of the system's input voltage and current, when combined with the aforementioned issues [13], cause the current to cut off prematurely before the voltage zero-crossing point. Additionally, influenced by the unidirectional clamping effect of the rectifier bridge [14], there is a significant current overshoot and oscillation after the zero-crossing point. The coupled effects of multiple mechanisms collectively exacerbate the current distortion problem in the zero-crossing region. However, the aforementioned studies predominantly concentrate on conventional PFC rectification topology and fail to provide an in-depth analysis and systematic exposition of the current distortion characteristics pertinent to the three-phase PFC converter discussed in this paper. Meanwhile, research on the multi-factor coupling mechanism of zero-crossing distortion in three-phase PFC converters under high-power and wide-load conditions remains insufficient. Existing theoretical models exhibit obvious limitations, failing to fully reveal the essence of distortion and thus unable to provide a solid theoretical basis for the design of distortion suppression schemes. Therefore, it is necessary to further deepen the modeling and analysis of the internal distortion mechanism. Notably, current zero-crossing distortion—especially the zero-crossing distortion dominated by odd harmonics with insignificant even harmonics—is a typical and widespread issue in high-power charging applications, and becomes particularly severe under wide-load and high-frequency ripple input conditions. As the power rating of charging piles increases and grid-side harmonic suppression requirements become stricter, the impacts of supply frequency fluctuations and ripple components on the converter are intensified. The rate of change of the input voltage at the zero crossing increases significantly, greatly increasing the difficulty of real-time current tracking [15]. The neural-network-based DC-bus voltage calibration method presented in [16] offers strong disturbance rejection capability, such adaptive neural schemes demand heavy online computation. Meanwhile, under high-frequency operation, magnetic saturation, high-frequency losses and stray leakage inductance effects of the power inductor further degrade the dynamic response performance of the current loop. Ultimately, the zero-crossing distortion problem is significantly amplified, becoming a core technical bottleneck that urgently needs to be addressed in high-power PFC converters. For modular cascaded and parallel AC-DC converters, parameter mismatch and unbalanced load distribution may induce inter-module circulating currents, which increase device current stress and power loss. Ref. [17] presents a scalable filter topology based on coupled inductors for multi-module parallel converters, which suppresses cross-module circulating current by introducing secondary series loops. Nevertheless, extra magnetic components and contactors are required, which increases volume and cost. Sun investigated the zero-crossing distortion problem of single-phase average-current-controlled Boost PFC converters in [18]. Different from the conventional understanding attributing distortion to cusp distortion or

DCM effect, his work pointed out two essential origins: the inherent current leading-phase effect and insufficient damping of the current loop. On this basis, a reference current phase-delay compensation scheme was proposed to mitigate zero-crossing distortion for single-phase applications. Nevertheless, the above analysis and compensation method are oriented to single-phase diode-bridge PFC topology, which cannot be directly applied to the line-voltage cascaded three-phase Boost PFC with one-cycle control studied in this paper.

Nevertheless, existing investigations mostly focus on conventional PFC topologies. The zero-crossing distortion mechanism unique to the line-voltage cascaded Boost rectifier remains insufficiently understood, and dedicated suppression methods are lacking.

This paper investigates the input current phase lag and resultant severe zero-crossing distortion across wide load ranges for the line-voltage cascaded Boost PFC rectifier presented in [8]. Taking the single-cycle controlled three-phase line-voltage cascaded PFC converter as the research subject, this work develops its dynamic model and reveals the distortion mechanism arising jointly from current phase lag and underdamped current loops. On this basis, an improved single-cycle control scheme with reference-current phase-lead compensation is proposed. The scheme compensates the phase lag and mitigates zero-crossing distortion over wide load conditions, offering a feasible approach for harmonic reduction and dynamic performance optimization of high-power grid-tied PFC converters.

The rest of this paper is organized as follows. Section 2 establishes the steady-state and small-signal models of the rectifier based on single-cycle control principles and introduces the topology and inherent characteristics of the line-voltage cascaded rectifier. Section 3 analyzes the inherent fundamental phase-shift and the generation mechanism of input-current zero-crossing distortion using the developed models. Section 4 proposes the reference-current phase-lead compensation control strategy to mitigate phase shift and current distortion. Section 5 verifies the performance of the proposed control scheme by simulation results. Finally, Section 6 concludes this paper.

2. Topology and Inherent Characteristics of Line-Voltage Cascaded Boost Rectifier

The topology and control strategy of the line-voltage-cascaded three-phase high power factor rectifier investigated in this paper are illustrated in Figure 1 [8]. Although numerous studies have expounded on the fundamental operational mechanism of the three-phase line-voltage-cascaded Boost converter utilizing a single-cycle approach, a concise overview of its topology and core operational principles remains essential to ensure the coherence and comprehensiveness of the theoretical analysis.

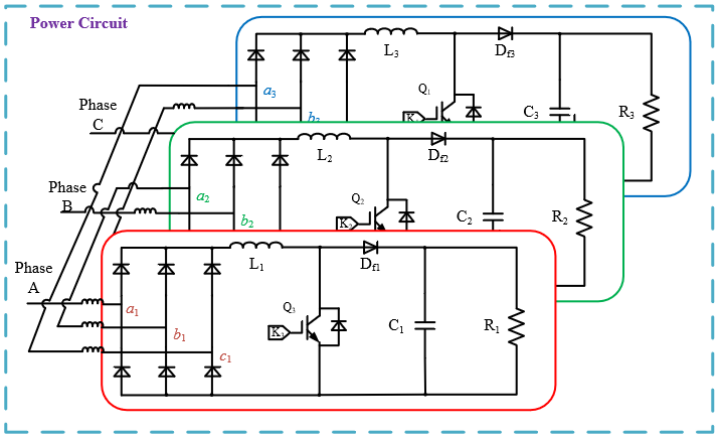


Figure 1. Three-phase line voltage cascaded rectifier topology.

2.1. Topology Description and Basic Operating Principle

The topology is comprised of three independently cascaded three-phase diode rectifier plus Boost converter modules, each aligned with the A, B and C phases of the three-phase power grid in Figure 1.

Identical power circuit and control configurations are employed in each module, endowing the overall system with modularity and scalability. Within the power circuit, the three-phase input voltage is subjected to full-wave rectification via a three-phase diode rectifier bridge, thereby supplying power to the Boost module of each respective phase. The main circuit of every module encompasses input filter inductors L_1, L_2, L_3, active power switches Q_1, Q_2, Q_3, fast recovery diodes D_{f1}, D_{f2}, D_{f3}, DC-side output capacitors C_1, C_2, C_3, along with equivalent loads R_1, R_2, R_3. Utilizing the natural commutation characteristics inherent in a three-phase diode bridge, each module is designed to operate solely during the intervals when the corresponding line voltage remains positive throughout the power frequency cycle.

According to the polarity of three-phase voltages, the line-voltage cascaded rectifier is divided into six 60° electrical-angle regions within one power-frequency cycle, each corresponding to a distinct circuit operating mode, as shown in the top-left subgraph of Figure 2. These regions fall into two categories.

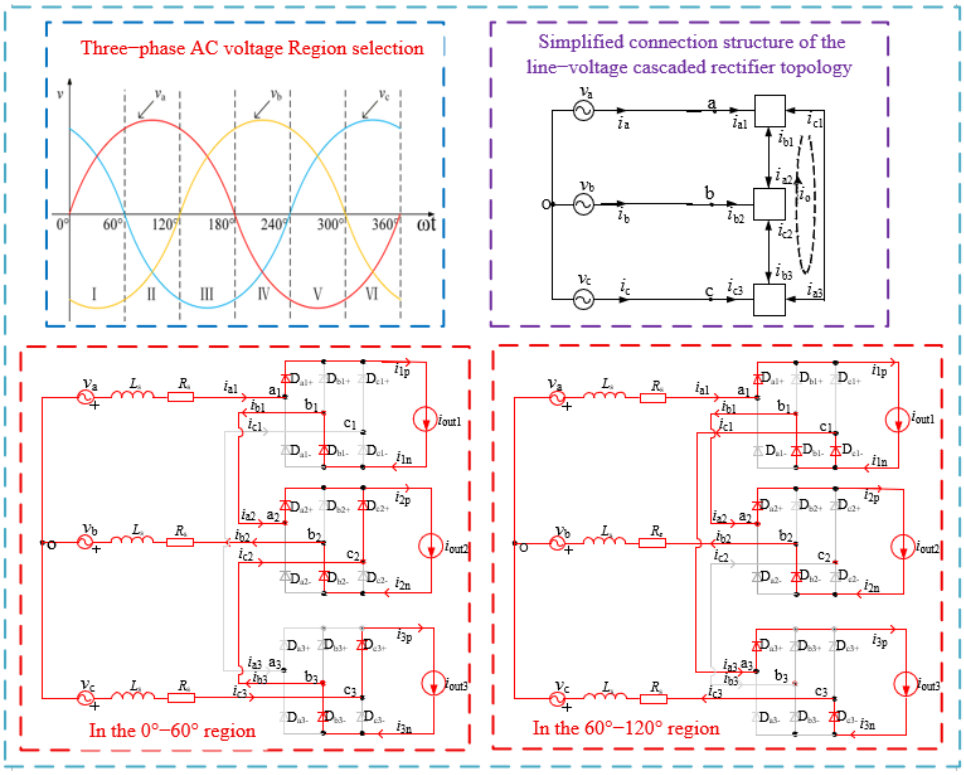


Figure 2. Region division, simplified connection structure and operating modes of line-voltage cascaded rectifier.

In the 0–60°, 120–180° and 240–300° regions, two phases possess higher instantaneous voltages than the third. Taking the 0–60° region as an example, currents in the modules of the two high-voltage phases flow from the AC source to the rectifier, whereas the current of the low-voltage phase module flows back to the source. Reverse-biased diodes block current between the two high-voltage phases. Take the 0–60° region to analyze the conduction path of the proposed topology, as shown in the down-left subgraph of Figure 2.

Here, v_a and v_c are positive and v_b is negative. Currents of Module 1 v_a and Module 3 v_c flow toward Module 2 v_b, with no current between Module 1 and Module 3.

In the 60–120°, 180–240° and 300–360° regions, two phases have lower instantaneous voltages than the third. For the 60–120° region, the module current of the single high-voltage phase flows from the AC source to the rectifier, and currents of the two low-voltage phase modules return to the source. No current conducts between these two low-voltage phases. In the 60–120° region, as illustrated in the down-right subgraph of Figure 2, v_b and v_c are negative while v_a is positive. The current of Module 1 v_a flows into both Module 2 and Module 3, and no current passes between Module 2 and Module 3.

2.2. Circulating-Current and Current-Sharing Characteristics

2.2.1. Derivation of Circulating Current Under Ideal Operating Conditions

Under ideal operating conditions, the three-phase input voltages are perfectly balanced sinusoids, all power modules feature identical circuit parameters and no parameter mismatch exists among the three parallel-connected phase modules. For the line-voltage cascaded rectifier, the phase currents of three modules are determined by the instantaneous line voltages and switching states. Since each phase module shares identical operating duty cycles and conduction sequences within every 60° electrical-angle sector, the currents of three modules can be evenly distributed.

For the simplified connection structure shown in Figure 2, balanced input voltages and loads are maintained among the three-phase modules, yielding identical phases referenced to the source neutral point O. The internal circulating-current loop equations are derived via Kirchhoff's Voltage Law (KVL). Equation (2), derived from Equation (1), demonstrates zero loop voltage and zero loop current, implying the absence of inter-phase circulating current under ideal operating conditions.

$$\begin{gathered} v_{b1} = v_{a2};\ v_{c1} = v_{b3};\ v_{c1} = v_{a3}; \\ u_{b1c1} = v_{b1} - v_{c1};\ u_{a3b3} = v_{a3} - v_{b3};\ u_{c2a2} = v_{c2} - v_{a2}; \end{gathered} \tag{1}$$

$$\begin{gathered} u_{b1c1} + u_{a3b3} + u_{c2a2} = 0; \\ i_{a3} + i_{b1} + i_{c2} = i_{a2} + i_{b3} + i_{c1}; \end{gathered} \tag{2}$$

2.2.2. Zero-Sequence Circulating Current Under Non-Ideal Operating Conditions

In practical engineering applications, grid voltage unbalance and load imbalance originating from mismatched module parameters degrade the performance of the power electronic converter. To facilitate analysis, the non-ideal condition of unbalanced input currents induced by three-phase grid unbalance is equivalent to that caused by unbalanced three-phase loads. Detailed analysis of the branch currents in each module is carried out. Taking the intra-phase current ib1 of one phase as an example, its Fourier decomposition is expressed in Equation (3).

$$i_{b1} = \frac{I_m}{\sqrt{3}} sin(x - 150^\circ) + \frac{I_m}{\sqrt{3}} \frac{\sqrt{3}}{4} sin(3x + 81^\circ) + \frac{I_m}{\sqrt{3}} \frac{1}{20} sin(9x + 81^\circ) + \frac{I_m}{\sqrt{3}} \frac{1}{56} sin(15x + 81^\circ) + \cdots\cdots \tag{3}$$

Apart from the fundamental component of ib1, a zero-sequence component exists within the delta loop. Nevertheless, the zero-sequence circulating current is confined to the delta loop and cannot flow into the grid.

2.3. Steady-State Analysis Under Ideal Operating Conditions

The foregoing analysis is carried out subject to the unity-power-factor constraint of input voltage and current.

The control circuit section utilizes one-cycle control (OCC) for power factor correction and input current waveform correction, establishing a classic single-loop control configuration: the voltage outer loop computes the mean value of the DC-side output voltage from the three-phase module, compares this value with the reference voltage Vdc*, and subsequently generates a control signal via a PI controller on the left side of the Figure 3 This signal is then transmitted to a carrier generator to produce a triangular carrier signal with a fixed frequency, which serves as the basis for duty cycle modulation. Regarding current control (integrated within the one-cycle control law), the system captures the absolute values of the three-phase current sampling signals i_x (where x = a, b, c), multiplies them by the sampling resistor Rs, and thereby derives control signals Rs*i_x (where x = a, b, c) that are directly proportional to the current amplitudes. Within the one-cycle control framework, these current signals are directly juxtaposed with the triangular carrier signal to generate the driving pulses K_1, K_2 and K_3 for the switching transistors in each module.

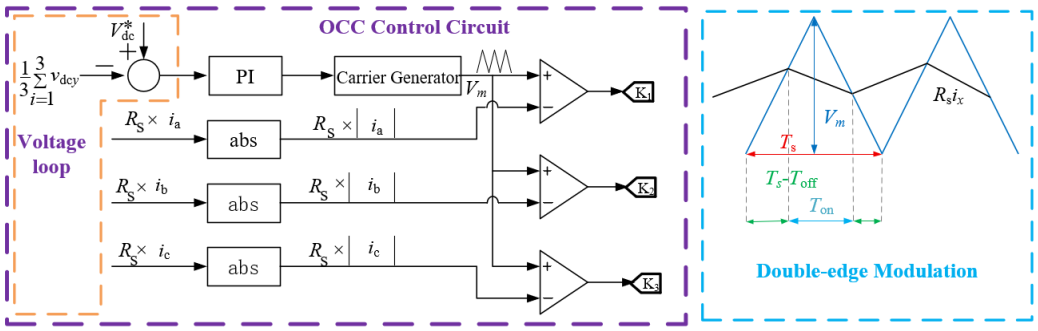


Figure 3. OCC PFC converter of the one-cycle control strategy.

In contrast to traditional dual closed-loop control, OCC obviates the necessity for an independent current inner-loop controller. Instead, it directly facilitates synchronous tracking of the input current with respect to the grid voltage by ensuring that the average inductor current remains proportional to the input voltage throughout each switching cycle, thereby enabling the system to operate with an approximate unity power factor. Additionally, as demonstrated by the waveform on the right side of the Figure 3, Ref. [1] employs a double-edge modulation strategy. By symmetrically allocating the conduction and cutoff times within the switching cycle, this strategy effectively mitigates current ripple and electromagnetic interference, thereby further optimizing the system's steady-state performance. This single-loop configuration is characterized by its simplicity in control, rapid dynamic response, and the absence of a requirement for additional voltage sensors, rendering it exceptionally well-suited for application scenarios involving line voltage cascaded three-phase Boost PFC topology.

This operational mode can be equated to a Boost converter subsequent to single-phase voltage rectification, facilitating the decomposition of the three-phase system into three distinct single-phase systems for analytical purposes, thereby markedly streamlining the processes of modeling and control design.

2.3.1. The Steady-State Modal of Novel Topology

The objective of OCC is that, under stable operating conditions of the system, the integral of the current sampling signal at the conclusion of each switching cycle is equivalent to the integral of the input voltage over the duration of the switch's turn-off period, as shown in Equation (4).

$$\int_0^{T_s} R_s |i_x(t)| dt = \int_{T_{on}}^{T_s} V_m(t) dt, (x = a, b, c) \quad (4)$$

where R_s represents the sampling resistor, T_s denotes the switching period and t_{on} indicates the on-time of the switch. Neglecting the switching ripple effects, we approximate i_x(t) as a constant value i_x (n) within one switching period, and the variation of V_m(t) within the switching period is minimal, approximating it as $V_m(n)$. Consequently, Equation (4) simplifies to Equation (5).

$$| i_x(t) | T_s = V_m(n)(T_s - T_{on}),(x = a,b,c) \tag{5}$$

$d_x(n) = T_{on}/T_s$ indicates the on-duty ratio of the switching device during the nth switching cycle; the fundamental principle of single-cycle modulation is to enforce the fulfillment of the proportional relationship outlined in Equation (6) within every switching cycle.

$$(1 - d_x(n)) = \frac{R_s(n)|i_x(n)|}{V_m(n)}, (x = a, b, c) \tag{6}$$

To investigate the influence of the OCC strategy on the port characteristics of the Boost converter, it is imperative to integrate the control law with the physical constraints inherent in the power circuit. Under the continuous conduction mode of inductor current, the Boost converter adheres to the volt-second balance principle in a steady state, expressed as $u_x(n) = (1 - d_x(n))u_{dcy}(n),(x = a,b,c;y = 1,2,3)$, $u_x(n)$, $u_{dcy}(n)$, $d_x(n)$, which denote the rectifier bridge output voltage, the DC output terminal voltage and the duty cycle of the switch during the nth switching cycle, respectively. This equation elucidates the intrinsic relationship between voltage and duty cycle within the power circuit, which remains unaffected by the control methodology employed. Conversely, the OCC strategy directly establishes the relationship between the duty cycle, input voltage, and output voltage through modulation techniques, referred to as the control law. To reveal the port characteristics of the converter under control action, the control law is substituted into the volt-second balance relation, eliminating the intermediate variable $d_x(n)$, and yielding the relationship under the control strategy as shown in Equation (7).

$$u_x(n) = |i_x(n)|R_e, \quad R_e = \frac{R_s u_{dcy}(n)}{V_m(n)}, (x = a, b, c; y = 1, 2, 3) \tag{7}$$

The equation reveals that, under the influence of OCC, the input port of the Boost converter demonstrates purely resistive characteristics, with its equivalent resistance, Re, being dictated by the control parameters and the output voltage. Equation (7) delineates the steady-state model of a three-phase bridge combined with a Boost PFC rectifier operating under OCC. Here, Re signifies the equivalent resistance that mirrors the magnitude of the load power. Under steady-state conditions, provided that the capacitance is adequately large and the bandwidth of the PI controller is relatively constrained, Re maintains a constant value throughout a single power frequency cycle. The input characteristics of the converter inherently adjust the input current in response to variations in the grid voltage. Nevertheless, in practical engineering, to precisely capture the system's characteristics, the voltage across the inductor must be taken into account when formulating the rectifier model. Consequently, the transfer function between the voltage and current at the input terminal is expressed as follows:

$$\frac{I_x(s)}{V_y(s)} = \frac{\frac{1}{R_e}}{1 + s\frac{L}{R_e}} = \frac{K}{1 + \tau s}, \ \tau = \frac{L}{R_e}, K = \frac{1}{R_e} \tag{8}$$

2.3.2. Small-Signal Model of Novel Topology

Drawing upon the derived large-signal state-space averaging model, a linearized small-signal model for the converter is constructed by introducing small-signal perturbations at the system's steady-state operating point and subsequently applying linearization approximation to the nonlinear terms within the model, as presented below:

$$\begin{cases} L\frac{d\hat{i}_a}{dt} = \hat{v}_a - \frac{R_s U_{dc1}}{V_m}\hat{i}_a + \frac{R_s \bar{I}_m U_{dc1}}{V_m^2}\hat{v}_m - \frac{\bar{I}_m R_s}{V_m}\hat{u}_{dc1} \\ L\frac{d\hat{i}_b}{dt} = \hat{v}_b - \frac{R_s U_{dc2}}{V_m}\hat{i}_b + \frac{R_s \bar{I}_m U_{dc2}}{V_m^2}\hat{v}_m - \frac{\bar{I}_m R_s}{V_m}\hat{u}_{dc2} \\ L\frac{d\hat{i}_c}{dt} = \hat{v}_c - \frac{R_s U_{dc3}}{V_m}\hat{i}_c + \frac{R_s \bar{I}_m U_{dc3}}{V_m^2}\hat{v}_m - \frac{\bar{I}_m R_s}{V_m}\hat{u}_{dc3} \\ C\frac{d\hat{u}_{dc1}}{dt} = \frac{R_s \bar{I}_m}{V_m}\hat{i}_a + \frac{R_s \bar{I}_m^2}{V_m^2}\hat{v}_m - \frac{1}{R_1}\hat{u}_{dc1} \\ C\frac{d\hat{u}_{dc2}}{dt} = \frac{R_s \bar{I}_m}{V_m}\hat{i}_b + \frac{R_s \bar{I}_m^2}{V_m^2}\hat{v}_m - \frac{1}{R_2}\hat{u}_{dc2} \\ C\frac{d\hat{u}_{dc3}}{dt} = \frac{R_s \bar{I}_m}{V_m}\hat{i}_c + \frac{R_s \bar{I}_m^2}{V_m^2}\hat{v}_m - \frac{1}{R_3}\hat{u}_{dc3} \end{cases} \quad (9)$$

From Equation (9), the small-signal block diagram of the dual-loop structure for the proposed topology rectifier, consisting of an outer DC voltage control loop and an inner OCC current loop, can be derived as shown in Figure 2.

In Figure 4, the region enclosed by the red dashed box represents the equivalent current-loop model. By introducing the concept of current tracking control into the analysis, it reflects the dynamic relationship between the converter's input voltage and inductor current under OCC, intuitively revealing its operating mechanism. This model maps the output of the voltage controller to the reference command of the input current, clearly demonstrating the current-following objective of OCC.

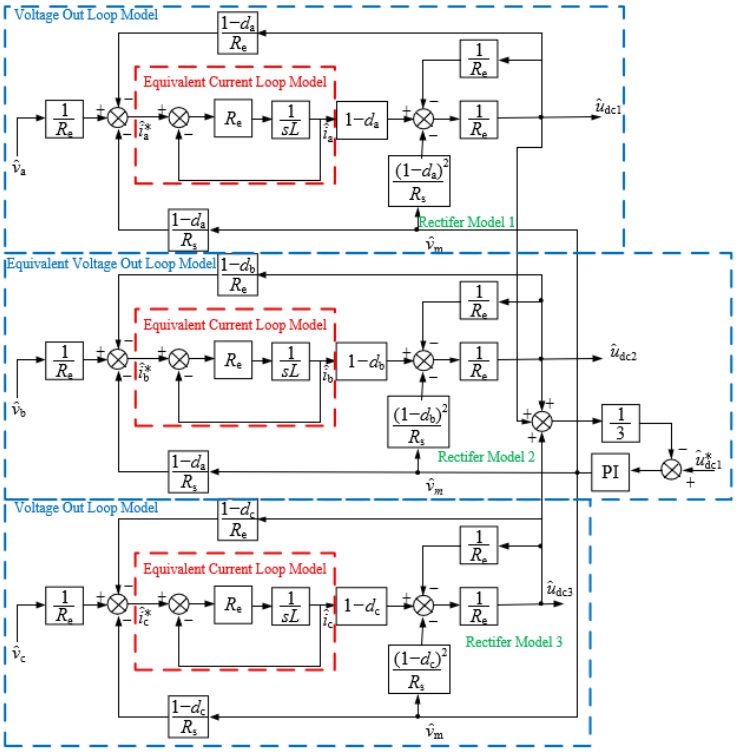


Figure 4. Block diagram of small signal system.

Meanwhile, the equivalent current-loop adopts a proportional control structure, whose gain is determined by the equivalent resistance Re. Consequently, the dynamic performance of the current loop is directly related to the system load condition. Additionally, due to the

existence of a load disturbance channel $(1-d_a)^2/\mathrm{R_s}$ in the model, load power fluctuations directly impact the output voltage.

Figure 5 presents the open-loop loop gain Bode diagrams of the current loop and voltage loop derived from the established small-signal model, instead of the transfer function of the plant only. The upper subplot corresponds to the open-loop Bode characteristic of the current loop, while the lower subplot is for the voltage loop.

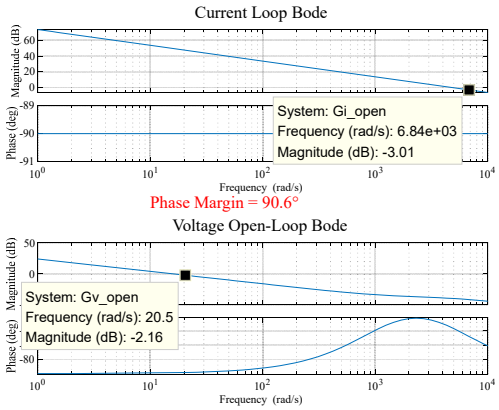


Figure 5. Open-loop loop gain Bode diagrams of the current loop and voltage loop based on the small-signal model.

In the time domain, the time constant $\tau = L/R_\mathrm{e}$ indicates that the response of the inductor current to the input voltage represents a first-order inertial process without overshoot. The response speed is determined by L/R_e. A heavier load (a smaller R_e) leads to a smaller time constant and a faster response. It is a standard first-order inertial element, with a static gain $K = 1/R_\mathrm{e}$. Therefore, the system exhibits stronger current tracking capability under heavy-load conditions. In the frequency domain, the first-order inertial element acts as a low-pass filter, with a transition frequency $\omega_\mathrm{c} = 1/T = R_\mathrm{e}/L$. Signals below this frequency can pass through with nearly no attenuation, while signals above this frequency experience an amplitude attenuation at a slope of -20 dB/dec, accompanied by a monotonic increase in phase lag from 0° to -90°. This characteristic limits the current tracking bandwidth of the system, which is the fundamental reason for the current phase lagging behind the voltage.

The open-loop Bode plots of the current loop and voltage loop based on the small-signal model are shown in Figure 5. The current loop demonstrates a first-order low-pass characteristic, but its crossover frequency is tracking high-frequency modulation signals. The current phase deviation at zero crossing mainly arises from the combined fundamental-frequency phase lag: the phase shift from the inductor inertial effect and the additional phase lag introduced by digital control delay, rather than insufficient bandwidth or insufficient dynamic response.

3. Current Phase Compensation Mechanism and Phasor Analysis Based on Single Cycle

In a three-phase line-voltage cascaded PFC converter, the existence of the boost inductor leads to the input current lagging behind the grid voltage, giving rise to an inherent phase-shift angle $\theta_{\mathrm{zero}} arctan(L/R_e)$. This lag angle is determined by the fundamental frequency, the boost inductance and the equivalent load resistance, and it increases as the load power increases. This is also the fundamental cause for the converter to externally present inductive reactive characteristics. To realize controllable adjustment of the current phase, this paper puts forward an improved OCC strategy.

By adjusting the phase of the control voltage across the switch, the leading effect of the inductor voltage drop is eliminated, enabling dynamic adjustment from under compensation to full compensation.

3.1. Phasor Relationship Between Inductive Voltage Drop and Switch-Tube Voltage

Based on the inductance volt-ampere characteristic, the grid voltage, inductance current and equivalent control voltage across the switching transistor adhere to the following phasor relationship $v_x + u_L + u_t$, where the inductance voltage drop leads the current by 90°. This phenomenon is the fundamental cause of the current lagging behind the grid. To counteract this leading component, the control voltage ut at the terminal of the switching transistor must lag behind the current by β. The inductance voltage drop can be partitioned into two parts: the part borne by the control side is $j\omega L\dot{I}_x\alpha$ and the part borne by the grid side is $j\omega L\dot{I}_x(1-\alpha)$. Only through the superposition of these two parts can a grid voltage with a controllable phase relative to the current be acquired.

Figure 6 illustrates the phasor diagrams of the power supply voltage and current under various compensation states.

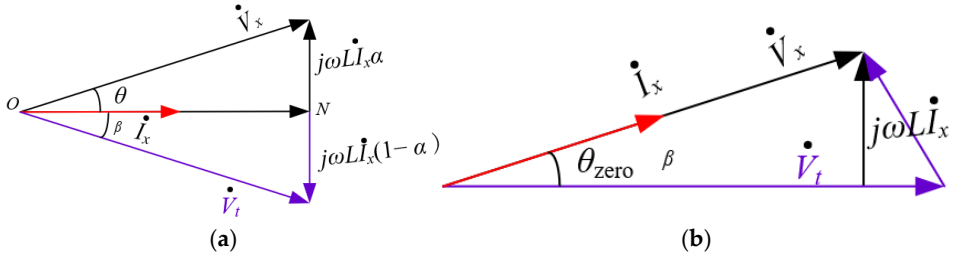


Figure 6. Phasor diagram of compensated power voltage and current: (**a**) under-compensation condition; (**b**) full-compensation condition.

Under the under-compensation condition (Figure 6a), the lag angle of the switch voltage ut is relatively minor. The inductor voltage drop is not completely offset, and the input current still lags behind the grid voltage by an angle θ.

Under the full-compensation condition (Figure 6b), through the adjustment of the phase of the switch modulation signal, the angle by which the switch voltage lags behind the current is fully counteracted by the inductor voltage drop. At this juncture, the input current is in phase with the grid voltage, attaining unity power factor operation.

3.2. Implementation Logic of Current Phase Compensation

From the phasor relationship, it can be observed that the phase of the input current is not solely determined by the grid voltage, but it instead influenced by the combined effect of the grid voltage and the switch voltage. Assuming a specific input power, let θzero denote the inherent angle by which the current lags behind the grid voltage prior to compensation, and β represent the angle by which the switch modulation signal lags behind the current. Then, the lag angle of the compensated current is $\theta = \theta_{\text{zero}} - \beta$. Through dynamic adjustment of the phase β of the switch modulation signal, the phase of ut can be altered ($u_t = (1 - d)U_{\text{dcy}}$), thereby compensating for the current's lag angle. When $\beta = \theta_{\text{zero}}$, θ = 0, resulting in a unity power factor; when $\beta < \theta_{\text{zero}}$, the current still lags behind the grid voltage, and the converter externally exhibits inductive characteristics, capable of absorbing reactive power.

To attain the control objective of unity power factor, the impedance equivalent to the voltage across the switching tube demonstrates capacitive characteristics, which counteract the characteristics of the boost inductor within the circuit. The simulated resistor in each phase is transformed from a pure resistor into a complex impedance composed of a resistor

and a reactor connected in series, mirroring the reactance necessary for achieving unity power factor operation of the input voltage and current.

Under the premise of a certain input power P_{in}, let θ_{zero} be the angle at which v_x lags before compensation i_x, and β be the angle at which the control voltage across the switch lags behind i_x. Then $\theta = \theta_{zero} - \beta$ represents the angle at which i_x lags behind v_x after compensation.

By adjusting the amplitude and phase of u_t (the control voltage across the switch), the angle at which i_x lags behind v_x is reduced, thereby improving the power factor. Figure 6 depicts the compensated power supply voltage and current phasor diagrams. After compensation, the angle at which i_x lags behind v_x is θ, and the angle at which u_t lags behind i_x is β. Combining this with Figure 6a, the amplitude and phase of u_t can be derived as follows:

$$\begin{cases} I_x = \frac{P_{in}}{V_x cos\theta} \\ \omega L I_x (1-\alpha) = V_x sin\theta \\ ON = V_x cos\theta \\ tan\beta = \omega L I_x \frac{\alpha}{ON} \end{cases} \tag{10}$$

Based on Equation (10), it can be inferred that

$$\beta = arctan\left(\frac{2\omega L P_{in} - V_x^2 sin2\theta}{2V_x^2 cos^2\theta}\right),\ V_t = V_x \frac{cos\theta}{cos\beta} \tag{11}$$

When $\theta = 0$, by substituting it into Equation (11), we derive $\beta = arctan(\omega L/R_e) = \theta_{zero}$. This value fully compensates for the angle by which the input current lags behind the power-supply voltage, thereby attaining a unity power factor between the input power supply and the current, as depicted in Figure 6b. Here, β denotes the compensation quantity, and with the increase in β, θ gradually diminishes. When $\theta < 0$, it is termed over-compensation, which may lead to significant distortion at the current zero-crossing point.

4. Improved Control Strategy

Disregarding the angle θ by which the input current lags behind the grid voltage, which is induced by the inductance voltage drop, the OCC system fails to attain unity power factor operation in a genuine sense. The core control equation of its improved OCC system is

$$(1-d)sign(i_x) = (\frac{R_s}{v_m} + \frac{j(\omega L + X_e)R_s}{v_m R_e})i_x \tag{12}$$

In Equation (12), the first term on the right hand side denotes the active component consumed by the load, whereas the second term represents the reactive component consumed by the load. The second term will be employed to compute the phase shift angle of the input current. If X_e (equivalent reactance introduced by the phase compensation control term) in the second term equals zero, the voltage and current at the input terminal of the control system will attain true unity power factor operation. Consequently, Equation (13) can be equivalently presented as

$$(1-d)sign(i_x) = (\frac{R_s}{v_m} - \frac{j\omega L R_s}{v_m R_e})i_x \tag{13}$$

Equation (12) is the general formula with configurable equivalent reactance X_e. Unity power factor can be achieved by setting $X_e = -\omega L$ to cancel the inductive term.

Equation (13) is the practical implementation case with $X_e = 0$. Instead of adding extra hardware reactance, a–j phase shift is introduced in control algorithm to compensate the current lag caused by filter inductor. Equation (12) serves for theoretical analysis, while

Equation (13) is adopted for practical control realization. The signal-flow block diagram of the general control equation described by Equation (13) is shown in Figure 7.

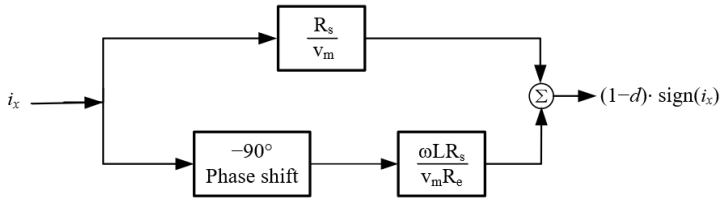


Figure 7. Signal flow block diagram of the control scheme in Equation (13).

Figure 8 illustrates the control block diagram for lagging phase shift. The sampled current undergoes a $-90°$ phase shift, is multiplied by the reactive power compensation coefficient k and is then superimposed with the current sampling signal to generate the modulation signal for the switch. This allows the voltage across the switch to automatically track the synthesized current signal, thereby establishing the control strategy for the voltage lagging behind the current of the switch.

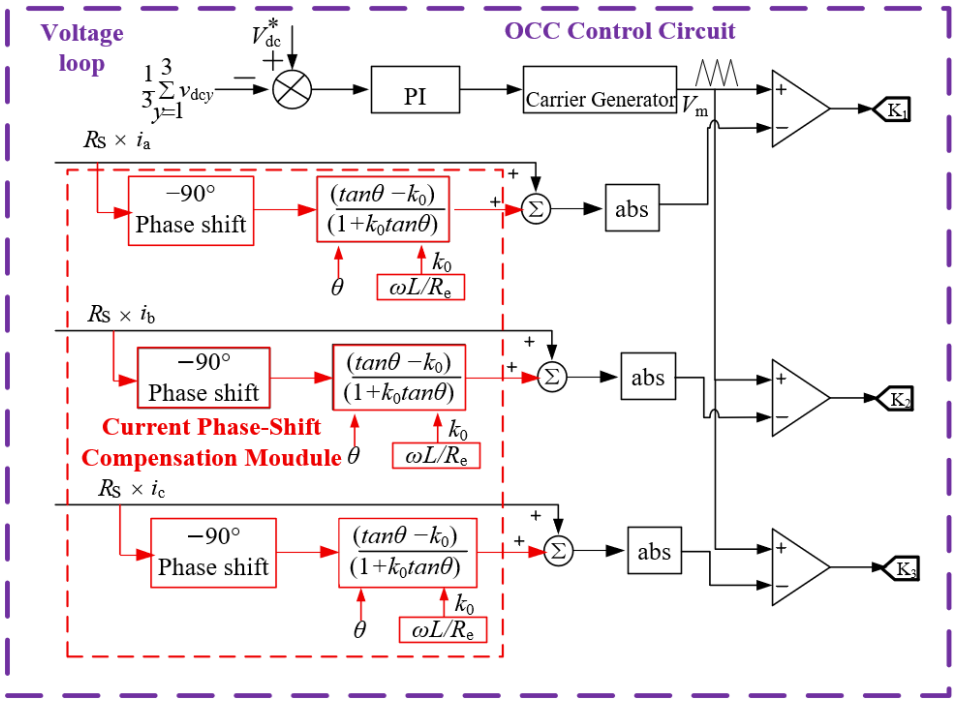


Figure 8. Phase−shift control strategy for full compensation and under−compensation hysteresis angles.

The foregoing analysis is predicated on full compensation. However, in the actual design of compensation schemes, the minimum adjustment unit for compensation depth through digital control is typically $0.5T_s$, which makes it arduous to guarantee full compensation. To mitigate the fundamental phase shift, it is generally operated in an under-compensation state, with the objective of approximating full compensation as closely as feasible. Consequently, the improved control strategy is devised based on the under compensation scheme. In conjunction with Figure 8, Equation (12) and Equation (13), the modulation signal of the switch transistor lags the sampled current by β, namely, $\beta = \theta_{zero} - \theta$. Subsequently, the reactive power compensation k is adjusted to

$$k = tan\beta = \frac{tan\theta_{zero} - tan\theta}{1 + tan\theta_{zero}\theta} \quad (14)$$

5. Simulation and Experiment

5.1. Simulation Waveform Under Under-Compensation State

Based on the simulation parameters from the previous section, with a rated load power P_{in} = 20 kW, U_{in} = 220 V, L = 2 mH, R_1 = 20 and U_{dc1} = 365 V, the equivalent input impedance Re and the angle β at which the switch terminal voltage u_t lags behind i_x at unity power factor are respectively

$$R_e = \frac{U_{in}^2}{P_{in}} = \frac{220^2}{6845} = 7.07 \tag{15}$$

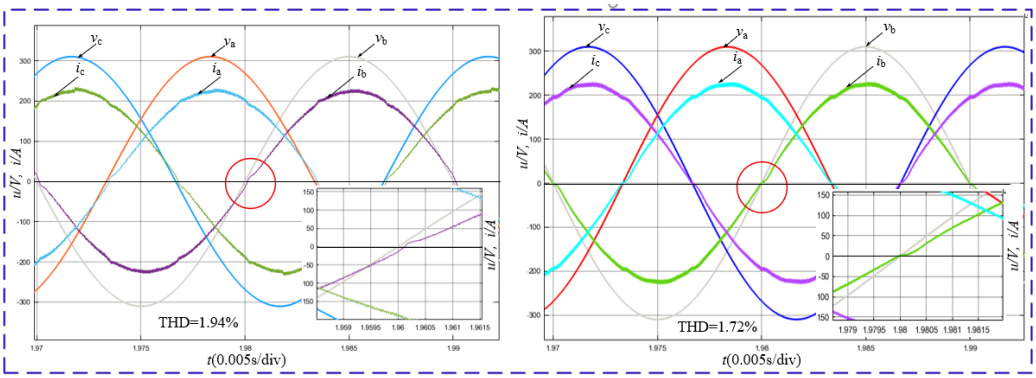
$$\beta = arctan\left(\frac{\omega L}{R_e}\right) = 5.1^\circ = 0.089 \tag{16}$$

By integrating Equation (15) with Equation (16), the delay time Δt corresponding to β can be computed, and the quantity of switching cycles n corresponding to the delay time is

$$n = \frac{\Delta t}{T_s} = \frac{\frac{\beta}{2\pi f_1}}{T_s} = 3.11 \tag{17}$$

Consequently, $\Delta t = 3.11T_s$, and complete compensation cannot be realized.

From the simulated experimental waveform of voltage and current in the under-compensation state presented in Figure 9, it can be discerned that the phase θ of the input current lagging behind the power supply voltage diminishes after compensation in comparison to that before compensation. This verifies the efficacy of the compensation method. The total harmonic distortion (THD) of the input current in Figure 9 is less than 5%, which satisfies the requirements of power grid quality.



(**a**) (**b**)

Figure 9. Simulation waveform of input voltage and current in lack compensation state (before and after compensation): (**a**) before compensation; (**b**) after compensation.

Following the rated-condition analysis above, Figures 10–14 present quantitative results under light-load, half-load and heavy-load conditions, comparing the total harmonic distortion (THD) and zero-crossing phase error of three schemes: uncompensated one-cycle control (OCC), the proposed fixed phase compensation method and the conventional SOGI-FPLL quadrature signal compensation scheme as the benchmark. The zero-crossing phase error is defined as the phase difference between the fundamental grid-side current and grid voltage; a positive value means the current leads the grid voltage, and a negative value means the current lags the grid voltage.

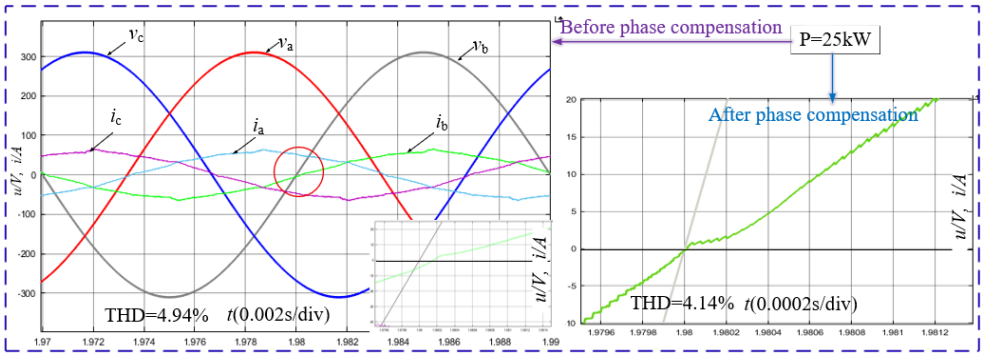


Figure 10. Waveforms before and after phase compensation for OCC under 25 kW condition.

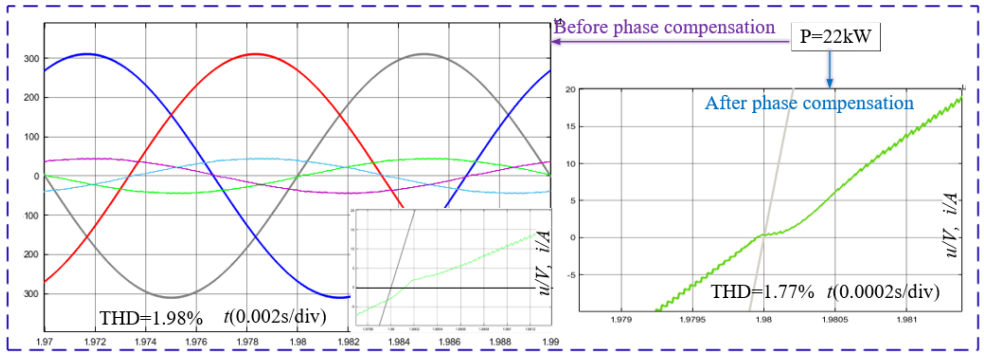


Figure 11. Waveforms before and after phase compensation for OCC under 22 kW condition.

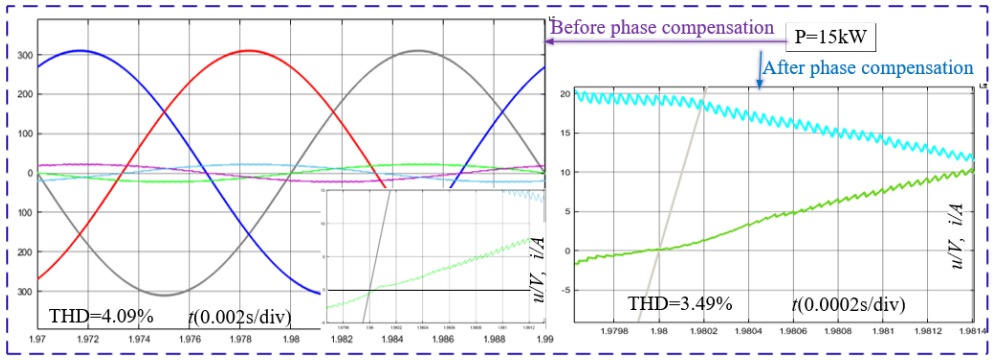


Figure 12. Waveforms before and after phase compensation for OCC under 15 kW condition.

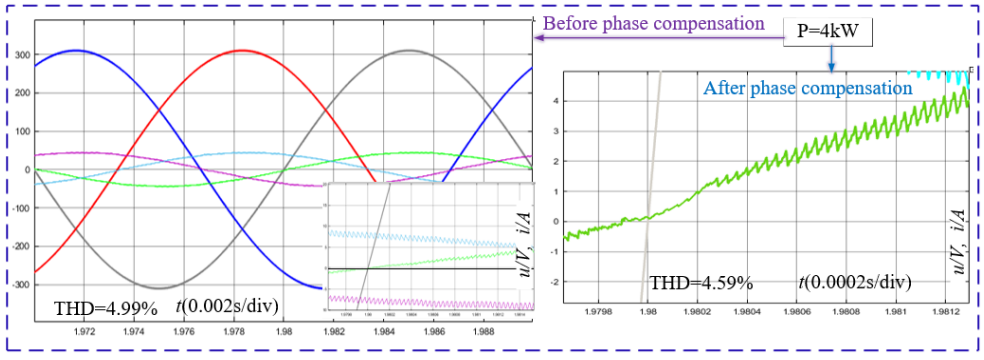


Figure 13. Waveforms before and after phase compensation for OCC under 4 kW condition.

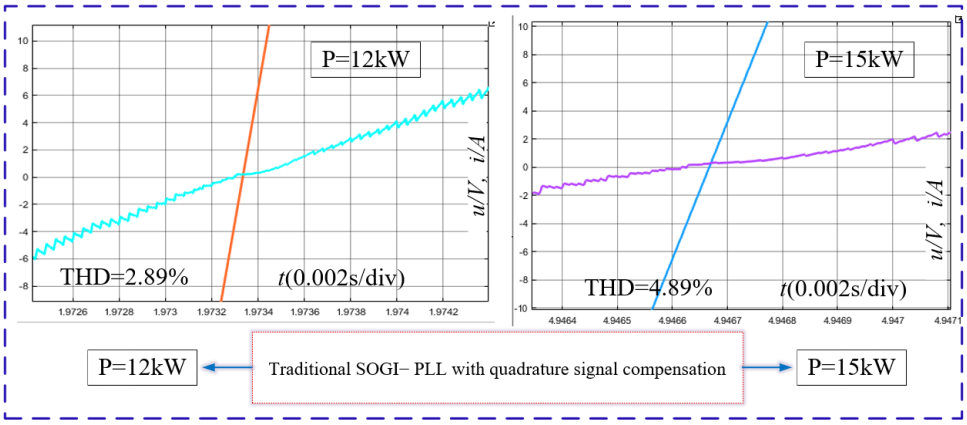


Figure 14. Waveforms of traditional SOGI-PLL with quadrature signal compensation under 12 kW (**right**) and 15 kW (**left**) operating conditions.

Following the rated-condition analysis above, the quantitative results under light-load, half-load and heavy-load conditions, including THD and zero-crossing phase error of the three schemes, are summarized in Table 1.

Table 1. Comparison of grid-side performance among uncompensated OCC, the proposed fixed phase compensation method and SOGI-PLL orthogonal signal compensation under different load conditions.

Shame	Power Range	ControI Complexity	THD	The Phase
Uncompensated OCC	4–25 kW	Low	<5%	>−18°
Proposed fixed phase compensation	4–25 kW Optimal near 20 kW	Low (no PLL)	<5%	−5°~+5°
SOGI–PLL orthogonal compensation	12–15 kW	High (with PLL)	<5%	−5°~+5°

The phase lead angle is defined as positive, and the phase lag angle is defined as negative.

5.2. Simulations and Experiments

To verify the feasibility of the proposed topology, a 1.7 kW prototype was built, as depicted in Figure 15.

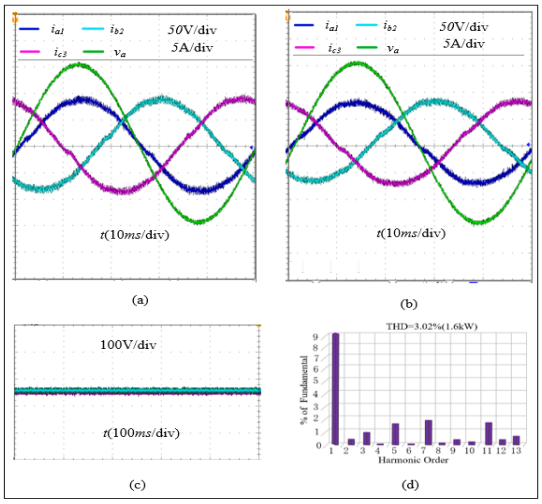


Figure 15. Waveforms of grid voltage, grid-side current, output voltage and THD before and after phase compensation: (**a**) before phase compensation; (**b**) after phase compensation; (**c**) output voltage; (**d**) THD (3.02%).

The experimental parameters of the prototype listed as U_{in} = 110 V, L = 2 mH, R_1 = 110 Ω, C = 2200 uF, f_s = 10 kHz and U_{dc} = 250 V, FQPF13N50C and Mur1660CD were

chosen for the power-switch and fast-recovery diode. A TMS320F28335 DSP was used as the controller.

Figure 15 shows the steady-state waveforms and harmonic spectrum at light load (1.7 kW). Figure 15a,b illustrate the three module currents and phase-A grid voltage before and after the fixed-phase compensation. It can be observed that the zero-crossing distortion of currents is effectively mitigated after compensation, and the phase alignment between grid-side current and grid voltage is improved. Figure 15c depicts the output DC voltage with small ripple and stable magnitude. The harmonic spectrum of grid-side current is given in Figure 15d, where THD is 3.02%, indicating that the harmonic distortion of the rectifier meets relevant power-quality standards under rated operating conditions.

6. Conclusions

This paper investigates the coupling mechanism of zero-crossing distortion originating from input current phase lag and limited current-loop bandwidth under power-frequency grid operation. The input current phase lag leads to desynchronization between current tracking and grid voltage, while insufficient bandwidth fails to cope with fast-voltage transients at zero crossings and exacerbates waveform distortion. A phase compensation strategy is proposed by imposing phase lag on the switch-terminal voltage. By adding a 90° phase-shifted current component to the sampled current, the fundamental phase of the switch voltage is adjusted to produce a modulation signal lagging the input current. This scheme regulates the input current phase and reduces the fundamental phase difference between grid voltage and current to mitigate waveform distortion. The adopted reference current phase-lead method compensates the inherent current phase lag, enhances the tracking performance for zero-crossing transients and suppresses zero-crossing distortion effectively. Moreover, the studied topology inherently restricts zero-sequence circulating current within the delta loop and avoids injecting such circulating current into the grid under non-ideal operating conditions, and the proposed phase compensation scheme does not compromise this feature. Simulations and experiments validate the feasibility of the improved strategy.

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