

Article

A Two-Phase High-Step-Down DC-DC Converter with Zero-Voltage Switching and Automatic Current Sharing

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Abstract

This paper proposes a two-phase high-step-down converter with zero-voltage switching (ZVS) and automatic current sharing, which is suitable for power conversion systems requiring a high step-down voltage conversion ratio. The proposed structure consists of three power switches, two energy-transferring capacitors, two freewheeling diodes, and one differential-mode transformer. This structure is compared with the conventional two-phase series-capacitor buck converter, which requires two independent inductors at the output side and thereby limits the power density. Therefore, in this paper, the dual-inductor structure with a differential-mode transformer is presented. The turns ratio of the differential-mode transformer is designed as one, enabling the two phases to achieve good symmetry. This design not only effectively improves the overall power density, but also realizes current sharing between the two-phase output currents by means of the differential-mode transformer. In addition, due to the leakage inductance continuity of the differential-mode transformer and the discharge path of the energy-transferring capacitors, the power switches can achieve zero-voltage switching during switching transitions, thereby significantly reducing switching losses. On the other hand, the voltage-dividing characteristic of the series capacitors can effectively reduce the voltage stress on the power switches. According to the above features, the proposed converter not only significantly improves the overall conversion efficiency, but also enhances the operational stability and reliability of the system. In this study, the operating principle of the proposed circuit is first analyzed, with some experimental results to verify effectiveness.

Keywords: high step-down; DC-DC converter; multiphase structure; zero-voltage switching; automatic current sharing; differential-mode transformer



Academic Editor: Pedro J. Villegas

Received: 15 September 2026

Revised: 4 October 2026

Accepted: 6 October 2026

Published: 12 October 2026

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1. Introduction

As is well known, the 48V structure is the main power supply option for data centers and telecommunications equipment [1,2]. For today's switching power supplies, the power switch method has an impact on conversion efficiency, electromagnetic interference (EMI), thermal management, and component stress. Among these, common switching control techniques can be divided into two main categories: hard switching and soft switching [3]. For hard switching, voltages and currents with stresses and spikes cause severe electromagnetic interference (EMI). Common soft switching methods are primarily divided into two major categories: zero-voltage switching (ZVS) [4] and zero-current switching (ZCS) [5].

For relatively low output requirements, the corresponding duty cycles should be relatively low for a single-stage buck, making it easy for the switching control to be interrupted. Therefore, the literature [6] proposes a multi-stage buck converter structure to increase the duty cycle. However, significant limitations occur in applications requiring high efficiency and high power density. To further improve the voltage gain, coupled inductor technology is presented and widely used in buck converters [7,8]. The literature [7] presents an ultra-high-step-down converter combining a coupling inductor and an energy-transferring capacitor to achieve high-step-down conversion without using an extremely short duty cycle, while also featuring ZVS. The literature [8] further improved switching behavior through resonant operation, reducing switching losses and improving efficiency. The literature [9] proposes a two-phase interleaved series-capacitor tap-down (SC-TaB) buck converter with low voltage stress at startup. By introducing a capacitor on the high-voltage side in parallel with the switching bridge arms, this design effectively distributes the switching voltage stress at startup. Furthermore, this structure uses the leakage inductance of the tap-coupled inductor in conjunction with the series capacitor to form a resonant path, enabling all power switches to achieve ZVS over a wide load range, thereby reducing switching losses and improving high-frequency efficiency. At the same time, interleaved operation helps suppress output current ripple. However, this structure incorporates a larger number of capacitors and switching components, leading to increased circuit complexity and control complexity. Therefore, studies [10,11] propose typical two-phase series-capacitor buck converters with automatic current sharing. These structures use the voltage-divider characteristics of energy-transferring capacitors to reduce the voltage stress on the synchronous rectifier. Studies [12,13] further build upon the structure of a traditional two-phase series-capacitor buck converter by introducing a set of parallel resonant tanks to assist the power switch in achieving zero-voltage switching (ZVS), thereby effectively reducing energy losses during the switching process and improving the overall conversion efficiency under high-frequency operation. However, to achieve soft switching characteristics, this structure requires the addition of passive components such as resonant inductors and resonant capacitors, significantly increasing the number of passive components in the circuit. The literature [14] proposes a two-phase series-capacitor buck converter structure. The phase shift in the operating signals of this converter effectively suppresses output current ripple and reduces the need for output filtering. The literature [15] proposes an interleaved high-step-down converter that, by incorporating a diode-capacitor energy-transferring module into this circuit, increases the equivalent duty cycle under high step-down voltage gain and reduces voltage stress on power devices. Via the interleave operation, the currents in each phase are shunted, and the output current ripple is effectively suppressed, making it suitable for high-output-current applications. In the literature [16], by combining GaN components with high-frequency operation, a high-power-density design capable of converting 48 V to 1 V at hundreds of amperes is successfully achieved, while, in [17], through the integration of magnetic components, the system power density is enhanced. The literature [18] builds upon the structure of a traditional two-phase series-capacitor-interleaved buck converter by adding additional power switches and energy-transferring capacitors. This design not only further increases the overall step-down voltage gain but also more effectively reduces the voltage stress on the power switches.

In summary, this paper focuses on investigating a high-performance two-phase series-capacitor buck converter. Building upon the structure proposed in the literature [18], this paper presents an improved two-phase high-step-down converter featuring ZVS and automatic current sharing. While retaining the existing advantages of a high step-down ratio and low switching voltage stress, the proposed topology further enables the soft

switching of all switches over all power ranges with current balancing between the two phases, without the need for additional sensing or complex control. Compared to the original structure [18], which only achieves current balancing under stringent operating conditions and suffers from high switching losses, the proposed circuit can effectively overcome these shortcomings.

2. System Structure

This paper presents a two-phase high-step-down converter with zero-voltage switching and automatic current sharing. The proposed circuit extends from [18], as shown in Figure 1.

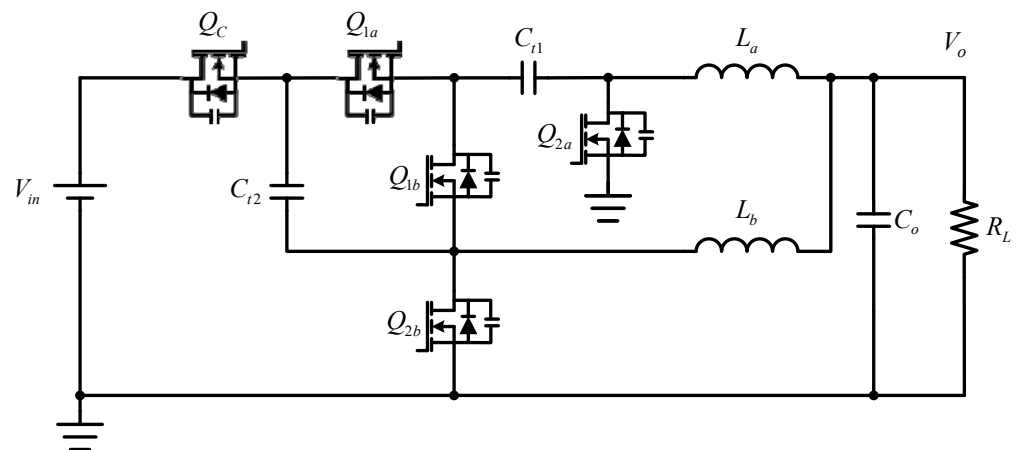


Figure 1. High-efficiency, non-isolated converter with a high step-down voltage gain [18].

The proposed two-phase high-step-down voltage gain circuit, as shown in Figure 2, consists of three power switches, S_1 , S_2 and S_3 ; two energy-transferring capacitors, C_1 and C_2 ; two freewheeling diodes, D_1 and D_2 ; and a differential-mode transformer, T_1 , with current sharing functionality. The differential-mode transformer consists of a magnetizing inductor L_m , a primary winding N_P , a secondary winding N_S , and two leakage inductances L_{k1} and L_{k2} . The output stage consists of an output capacitor and an output load.

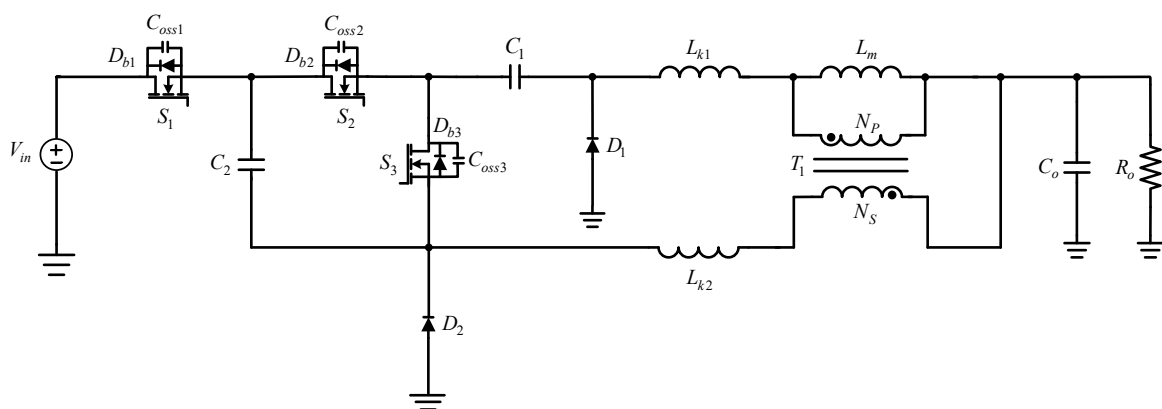


Figure 2. Proposed improved converter.

3. Basic Operating Principles

The following will analyze the operating principles of the proposed two-phase high-step-down voltage gain converter with zero-voltage switching and automatic current sharing, along with the relevant theoretical derivations.

3.1. Circuit Definitions and Assumptions

Prior to the circuit operation analysis, some definitions and assumptions regarding the circuit symbols are first described, as shown in Figure 3.

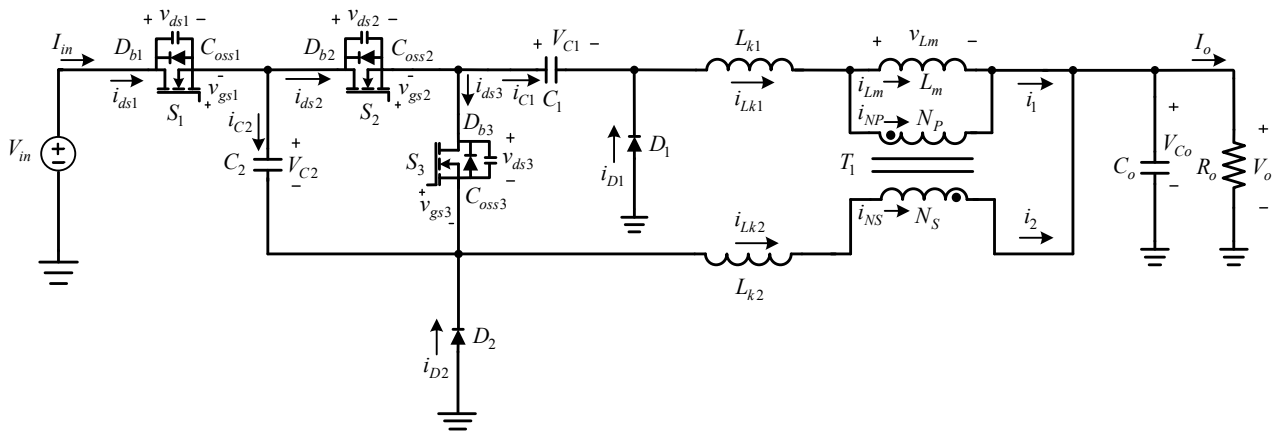


Figure 3. Proposed circuit with symbols added.

- (1) V_{in} is the DC input voltage of the circuit; I_{in} is the DC input current of the circuit; V_o is the DC output voltage; I_o is the DC output current; R_o is the output resistance.
- (2) S_1 , S_2 and S_3 are power switches with their on-resistance neglected; D_{b1} , D_{b2} and D_{b3} are the body diodes of S_1 , S_2 and S_3 , respectively; C_{oss1} , C_{oss2} and C_{oss3} are the capacitances of S_1 , S_2 and S_3 , respectively.
- (3) C_1 and C_2 are the energy-transferring capacitors; their capacitances are sufficiently large such that the voltages across C_1 and C_2 can be considered constant, and it is assumed that $C_1 = C_2$.
- (4) The differential-mode transformer T_1 consists of a magnetizing inductor L_m , a primary winding N_p , a secondary winding N_s , and two leakage inductances L_{k1} and L_{k2} ; it is assumed that $N_p = N_s$ and $L_{k1} = L_{k2}$.
- (5) D_1 and D_2 are the freewheeling diodes of the circuit.
- (6) C_o is the output capacitor; its capacitance is sufficiently large to be treated as a constant, i.e., $V_{C0} = V_o$.
- (7) v_{gs1} is the gate drive signal for S_1 , v_{gs2} is the gate drive signal for S_2 , and v_{gs3} is the gate drive signal for S_3 .
- (8) v_{ds1} is the voltage across S_1 , v_{ds2} is the voltage across S_2 , and v_{ds3} is the voltage across power switch S_3 . i_{ds1} is the current flowing through S_1 , i_{ds2} is the current flowing through S_2 , and i_{ds3} is the current flowing through S_3 .
- (9) V_{C1} is the voltage across C_1 , V_{C2} is the voltage across C_2 , i_{C1} is the current flowing through C_1 , and i_{C2} the current flowing through C_2 .
- (10) i_{D1} is the current flowing through D_1 , and i_{D2} is the current flowing through D_2 .
- (11) v_{Lm} is the voltage across L_m , i_{Lm} is the current flowing through L_m , i_{Lk1} is the current flowing through L_{k1} , i_{Lk2} is the current flowing through L_{k2} , i_{NP} is the current flowing through N_p , and i_{NS} is the current flowing through N_s .
- (12) It is assumed that the duty cycle of the first phase is D_A , the duty cycle of the second phase is D_B , and the duty cycles of the two phases are equal, i.e., $D_A = D_B = D$.
- (13) i_1 is the output current of the first phase, and i_2 is the output current of the second phase.
- (14) T_s is the switching period, and f_s is the switching frequency, where $T_s \times f_s = 1$.
- (15) All diodes and capacitors are assumed to be ideal components.

3.2. Operating Principles

Figure 4 shows the operating timing sequence of the proposed converter in the steady state. Within each switching cycle, the operating state can be divided into six states. Among these, in operating modes 1 and 4, the magnetizing current of the differential-mode transformer undergoes commutation. However, this commutation behavior merely reflects a change in the polarity of the magnetic flux and does not affect the energy-transferring paths or the operational behavior of other components. Therefore, this section does not classify the commutation process of the magnetizing current as a separate operating state, but it merely indicates the corresponding current path. There are six operating states that are described in the following.

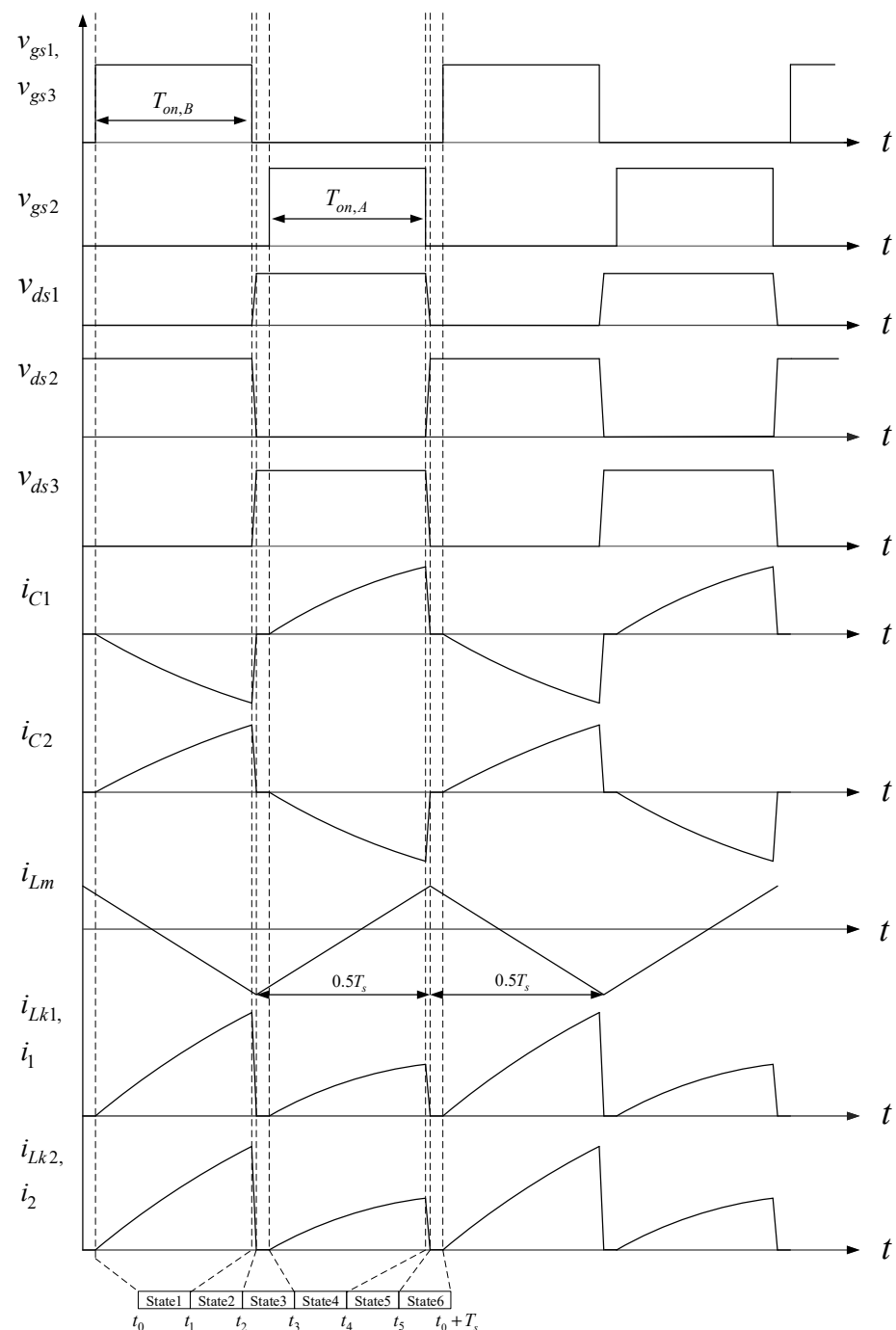


Figure 4. Operating timing sequence for the proposed circuit.

State 1: $[t_0 \leq t < t_1]$

As shown in Figure 5, when $t = t_0$, switches S_1 and S_3 are turned on, while S_2 is turned off. Since, in the previous state, the body diodes D_{b1} and D_{b3} have already been turned on, switches S_1 and S_3 can achieve ZVS turn-on. As $t > t_0$, the input current I_{in} flows through switch S_1 into the circuit and charges the energy-transferring capacitor C_2 . Simultaneously, the freewheeling diode D_1 conducts to the ground, causing the energy-transferring capacitor C_1 to begin discharging. According to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), energy is transferred to the load via the differential-mode transformer T_1 . When the currents in the two phases are unbalanced, the differential-mode transformer induces a compensating voltage in its two windings. The polarity of this compensating voltage automatically suppresses the phase with the higher current and boosts the phase with the lower current, thereby reducing the difference between the two-phase currents and gradually bringing them into alignment. Furthermore, under this operating condition, the magnetizing inductor T_1 transitions from forward demagnetization to backward magnetization. As shown in Figure 6, the magnetizing current decreases linearly, causing its voltage across to be clamped at v_{Lm} , which is $(V_{C2} - V_{in})/2$. When $t = t_1$, switches S_1 , S_2 and S_3 are turned off, and the circuit immediately enters State 2.

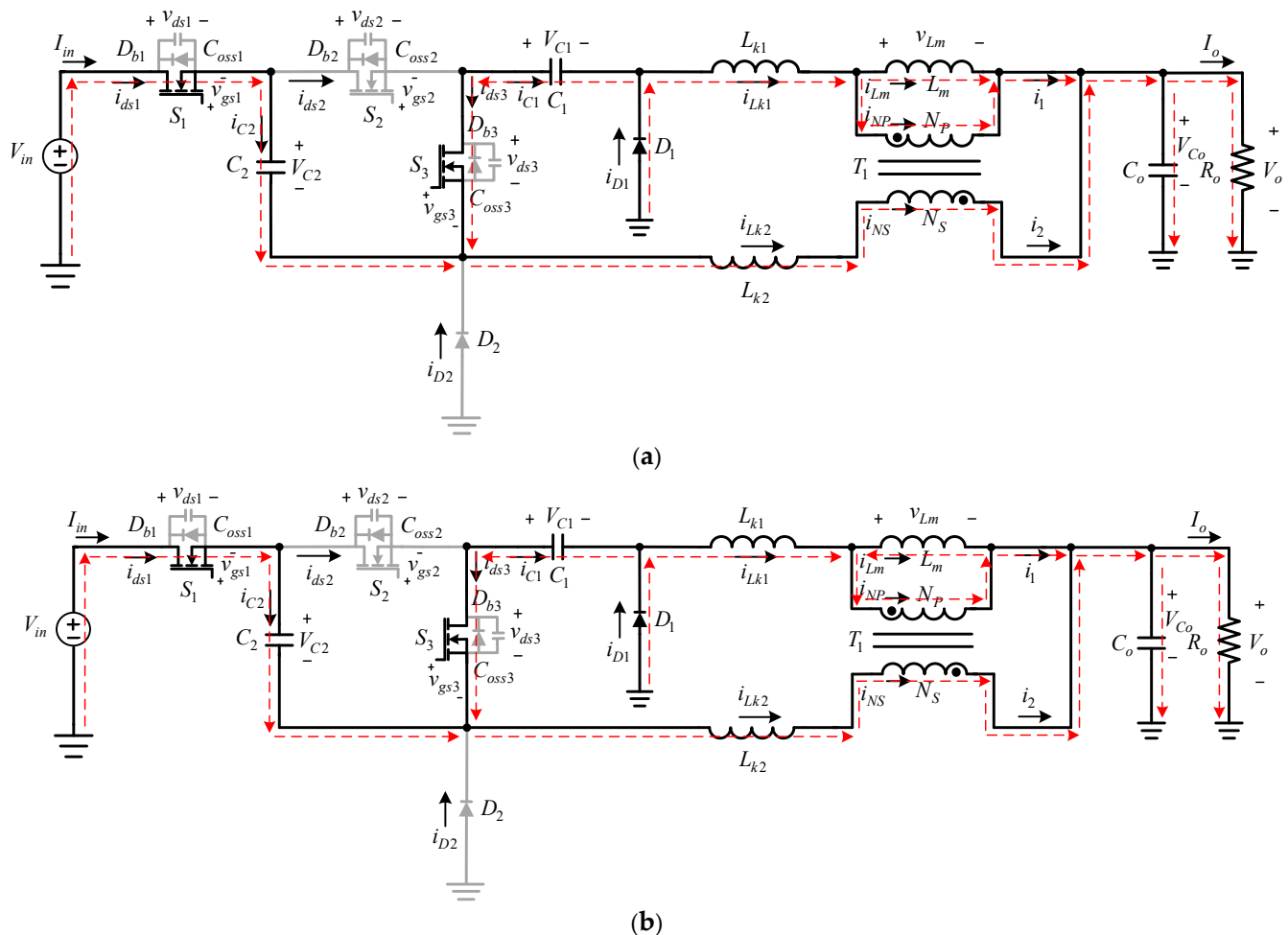


Figure 5. (a) Current flow for the current of the forward magnetizing inductor in State 1. (b) Current flow for the current of the backward magnetizing inductor in State 1.

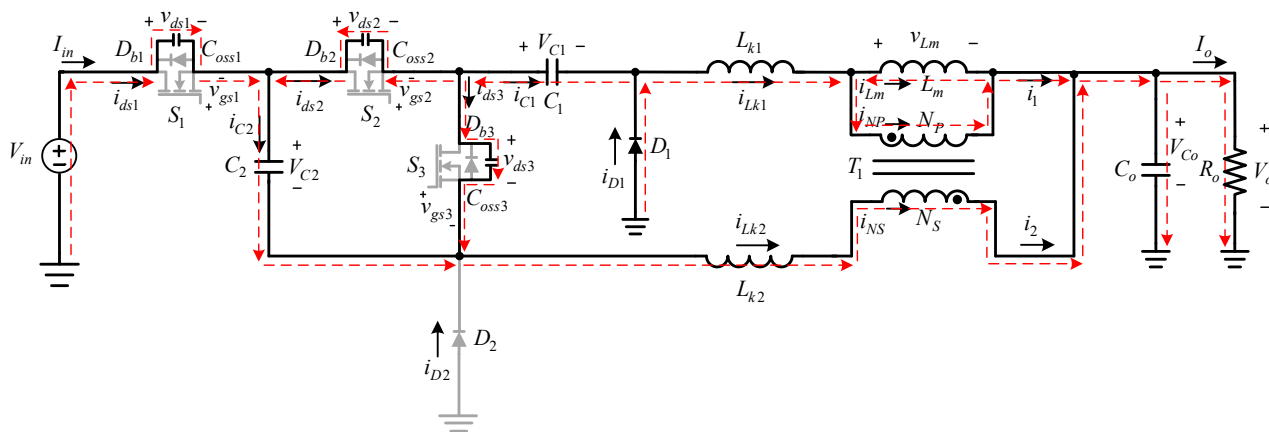


Figure 6. Current flow in State 2.

State 2: [$t_1 \leq t < t_2$]

As shown in Figure 6, when $t = t_1$, switches S_1 , S_2 and S_3 are all turned off; this state is the dead time. At this point, the current i_{C2} through the energy-transferring capacitor C_2 flows in the forward direction, as does the current through the freewheeling diode, while the current i_{C1} through the energy-transferring capacitor C_1 flows in the backward direction, supplying energy to the load via the differential-mode transformer T_1 . In this state, the magnetizing inductance L_m of the differential-mode transformer remains backward-magnetized, and the current i_{Lm} continues to decrease linearly. Since switches S_1 , S_2 and S_3 are all in the off state, the circuit must simultaneously satisfy Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). At this point, the input current I_{in} charges the output C_{oss1} of switch S_1 ; simultaneously, the current i_{C1} through the energy-transferring capacitor C_1 discharges the output C_{oss1} of the switch and charges the output capacitor C_{oss3} of switch S_3 .

When $t = t_2$, C_{oss1} is charged to $V_{in}/3$, C_{oss2} is discharged to zero, and C_{oss3} is charged to $2V_{in}/3$, the circuit immediately enters State 3.

State 3: [$t_2 \leq t < t_3$]

As shown in Figure 7, at this moment, $t = t_2$, and switches S_1 , S_2 and S_3 are still off. At this point, the output capacitors C_{oss1} and C_{oss2} of switches S_1 and S_3 have been charged to $V_{in}/3$ and $2V_{in}/3$, respectively, while the output capacitor C_{oss2} of switch S_2 has been completely discharged to zero. According to KCL and KVL, the current i_{C1} through the energy-transferring capacitor C_1 will cause the body diode D_{b2} of switch S_2 to turn on, preparing switch S_2 for ZVS in the next state. Moreover, the current i_{C2} through the energy-transferring capacitor C_2 and the current i_{D1} through the freewheeling diode D_1 continue to flow in the forward direction and decrease to zero; conversely, the current i_{C1} through the energy-transferring capacitor C_1 continues to flow in the backward direction and increases to zero, transferring energy to the load via the differential-mode transformer T_1 . In this state, the magnetizing inductance L_m of the differential-mode transformer T_1 enters the backward demagnetization, and the current begins to rise linearly.

At $t = t_3$, the switch S_2 turns on at ZVS, and the circuit immediately enters State 4.

State 4: [$t_3 \leq t < t_4$]

As shown in Figure 7, when $t = t_3$, switches S_1 and S_3 are in the off state, while switch S_2 begins to turn on. Since the body diode D_{b2} of switch S_2 had already turned on in the previous state, causing its voltage drop v_{ds2} to drop to zero, switch S_2 is able to turn on with ZVS. In this state, the freewheeling diode D_2 is grounded and conducting; the energy-transferring capacitor C_2 begins to discharge, while the energy-transferring capacitor C_1 is charged, and energy is transferred to the load through the differential-mode

transformer T_1 . In this state, the magnetizing inductor L_m also changes from backward demagnetization to forward magnetization. In Figure 9, the excitation current continues to rise linearly, causing its voltage drop v_{Lm} to be clamped at half the voltage difference between the two energy-transferring capacitors C_1 and C_2 , i.e., $(V_{C2} - V_{C1})/2$. Figure 8a,b show the current flows in State 4 during backward and forward magnetization, respectively, which are identical in both cases.

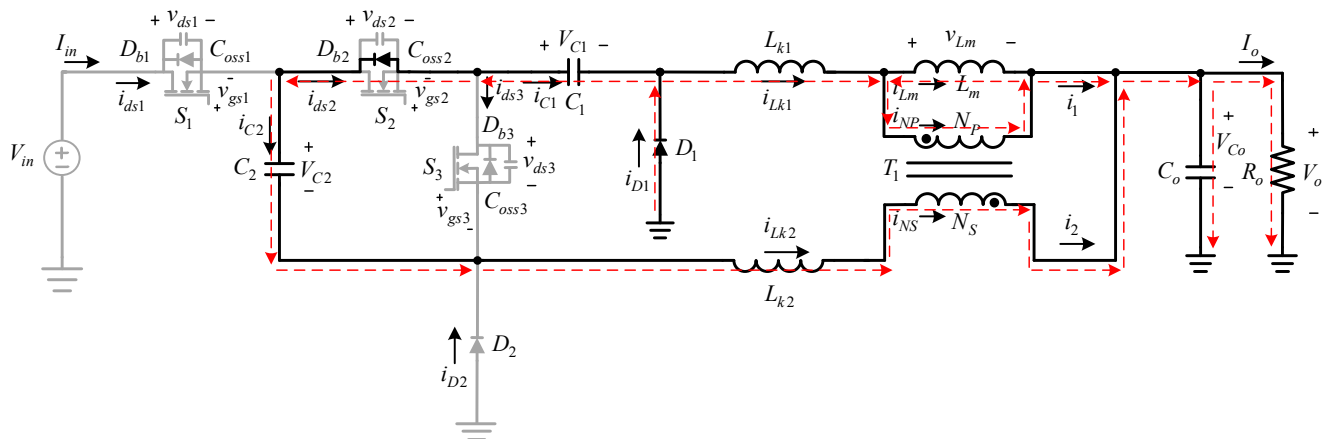
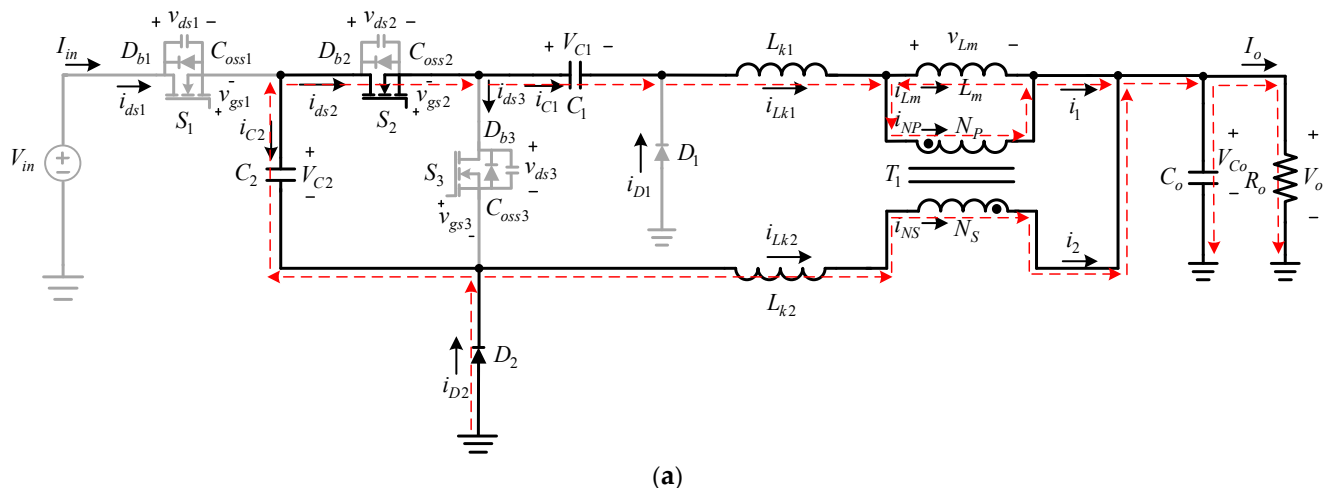
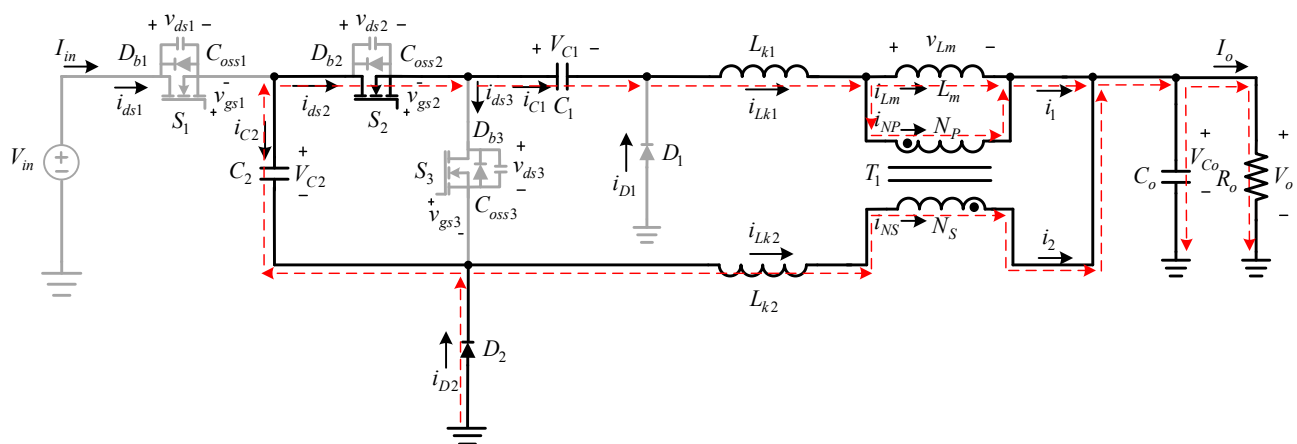


Figure 7. Current flow in State 3.



(a)



(b)

Figure 8. (a) Current flow in backward magnetization in State 4. (b) Current flow in forward magnetization in State 4.

When $t = t_4$, the switch S_2 turns off, and the circuit immediately enters State 5.

State 5: [$t_4 \leq t < t_5$]

As shown in Figure 9, when $t = t_4$, switches S_1 , S_2 and S_3 are turned off; this interval is the dead time of the switches. At this point, the current i_{C1} through the energy-transferring capacitor C_1 and the current i_{D2} through the freewheeling diode D_2 both flow in the forward direction, while the current i_{C2} through the energy-transferring capacitor C_2 flows in the backward direction, and energy is transferred to the load through the differential-mode transformer T_1 . In this state, the excitation inductance of the differential-mode transformer T_1 remains forward-excited, and its current i_{Lm} continues to rise. Since switches S_1 , S_2 , and S_3 are all in the off state, the circuit must simultaneously satisfy KCL and KVL. Therefore, the current i_{C2} through the energy-transferring capacitor C_2 discharges the output capacitor C_{oss1} of switch S_1 and charges the output capacitor C_{oss2} of switch S_2 . At the same time, the current i_{C1} through the energy-transferring capacitor C_1 discharges the output capacitor C_{oss3} of switch S_3 .

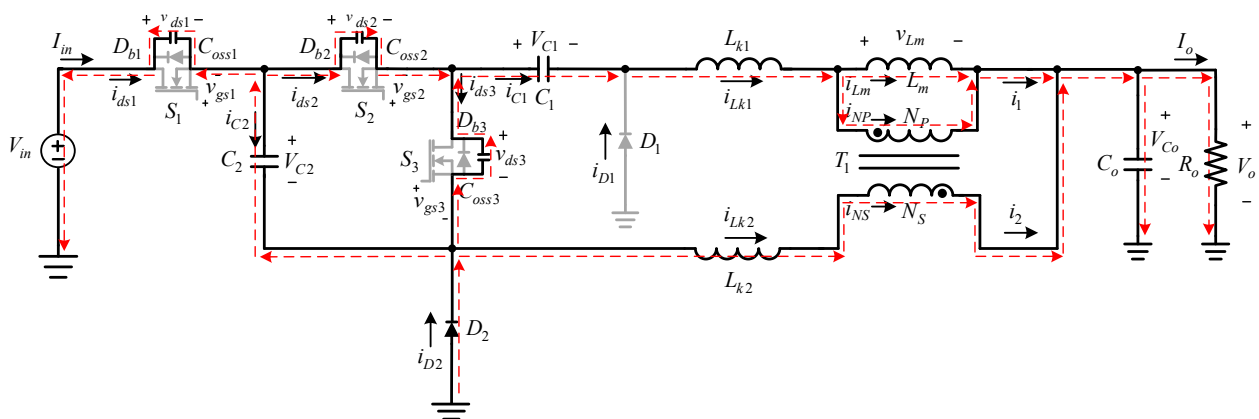


Figure 9. Current flow in State 5.

When $t = t_5$, both C_{oss1} and C_{oss3} are discharged to zero, and C_{oss2} is charged to $2V_{in}/3$, the circuit immediately enters State 6.

State 6: [$t_5 \leq t < t_0 + T_s$]

As shown in Figure 10, at $t = t_5$, switches S_1 , S_2 and S_3 are in the off state. At this point, the output capacitor C_{oss2} of switch S_2 has been charged to $2V_{in}/3$, while the output capacitors C_{oss1} and C_{oss3} of switches S_1 and S_3 have been discharged to zero. According to KCL and KVL, the current i_{C2} through the energy-transferring capacitor C_2 will turn on the body diode D_{b1} of switch S_1 ; simultaneously, the current i_{C1} through the energy-transferring capacitor C_1 turns on the output diode D_{b3} of switch S_3 , preparing switches S_1 and S_3 for ZVS in the next state. In addition, the current i_{C2} through the energy-transferring capacitor C_1 and the current i_{D2} through the freewheeling diode D_2 both continue to flow in the forward direction and decrease to zero, while the current i_{C2} through the energy-transferring capacitor C_2 continues to flow in the backward direction and increases to zero, with energy being transferred to the load through the differential-mode transformer T_1 . In this state, the magnetizing inductance L_m of the differential-mode transformer T_1 enters the forward demagnetization, and its current i_{Lm} begins to decrease linearly. At $t = t_0 + T_s$, both switches S_1 and S_3 achieve ZVS turn-on, and then the circuit enters the next cycle.

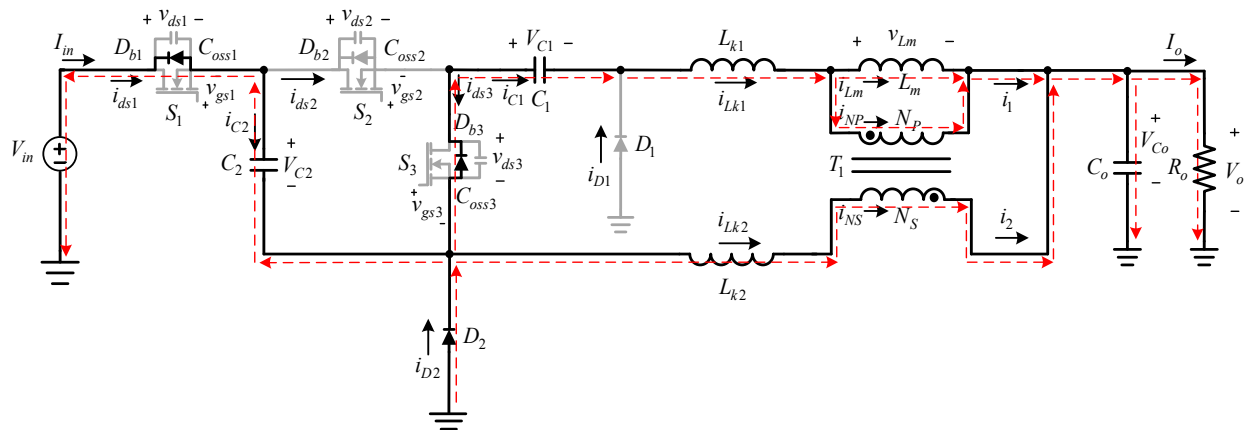


Figure 10. Current flow in State 6.

3.3. Voltage Gain

This subsection presents a derivation and analysis of the voltage gain as well as the voltages across the energy-transferring capacitors C_1 and C_2 for the proposed converter. Only the circuit operations in States 1 and 4 are taken into consideration.

As shown in State 1 in Figure 11, since the average voltage across the inductor is zero in the steady state, it can be deduced that the average voltage at switch Node 2 is equal to the output voltage V_o . Furthermore, based on the voltage relationships of each phase circuit during the on period, the following equations can be derived:

$$(V_{C2} - V_{C1})D_B = V_o \quad (1)$$

$$V_{in} = V_{C1} + V_{C2} \quad (2)$$

$$(V_{C2} - V_{C1})D_A = V_o \quad (3)$$

where D_A and D_B are the duty cycle of the first phase and the duty cycles of the second phase respectively.

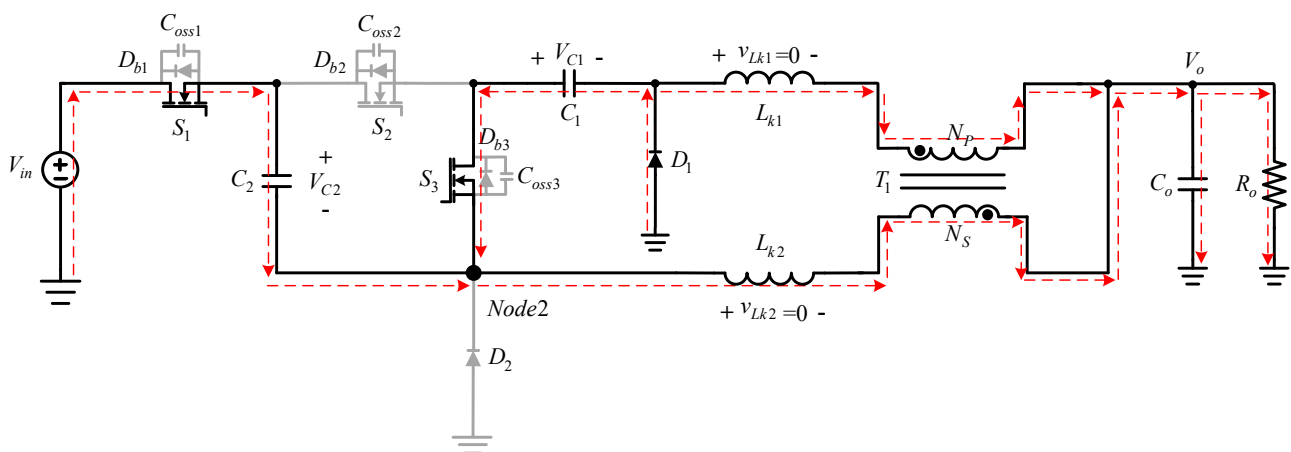


Figure 11. Analysis diagram for State 1.

As shown in Figure 12, during the operation of State 4, since the average voltage across the inductor is zero under periodic steady-state conditions, it can be deduced that the average voltage at switch Node 1 in this state is equal to the output voltage V_o . Furthermore, based on the voltage relationships of each phase circuit during the on period, the Equation (3) can be derived.

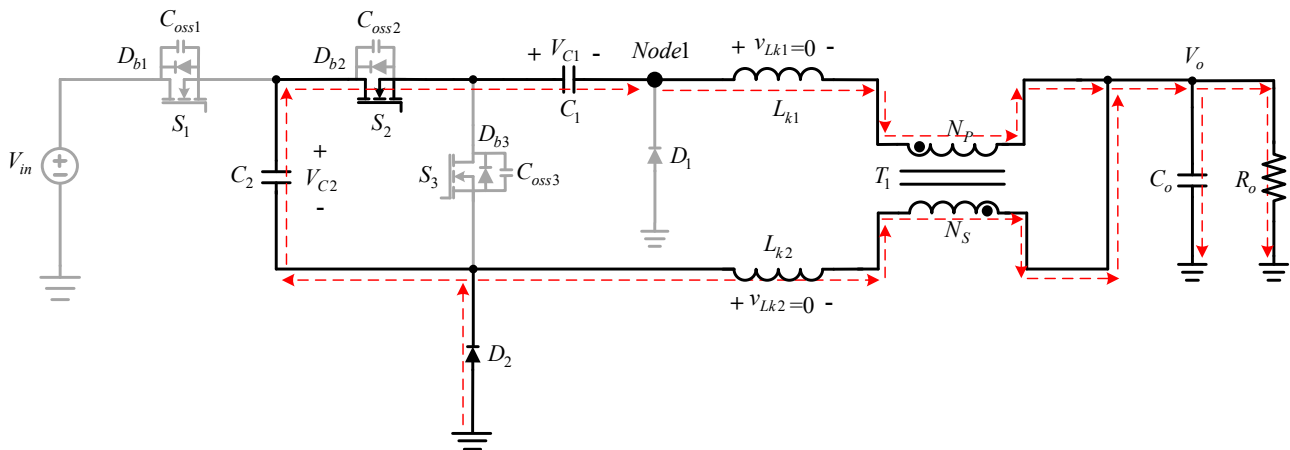


Figure 12. Analysis diagram for State 4.

First, by rearranging (1) and (3), the following equations can be obtained:

$$V_{C2} = \frac{V_{in}D_B - V_o}{D_B} = V_{in} - \frac{V_o}{D_B} \quad (4)$$

$$V_{C1} = \frac{V_{C2}D_A - V_o}{D_A} = V_{C2} - \frac{V_o}{D_A} \quad (5)$$

By substituting (5) into (2), the following equations can be obtained:

$$2V_{C2} = V_{in} + \frac{V_o}{D_A} \quad (6)$$

Next, substituting (1) into (6) the voltage V_{C2} of the energy-transferring capacitor C_2 can be obtained:

$$V_{C2} = \frac{D_A + D_B}{2D_A + D_B} V_{in} \quad (7)$$

Sequentially, substituting (7) into (2) yields the voltage V_{C1} of the energy-transferring capacitor C_1 :

$$V_{C1} = \frac{D_A}{2D_A + D_B} V_{in} \quad (8)$$

Finally, let the duty cycles of both phases be equal, i.e., $D_A = D_B = D$. Then, the voltages V_{C1} and V_{C2} can be obtained:

$$V_{C1} = \frac{1}{3} V_{in} \quad (9)$$

$$V_{C2} = \frac{2}{3} V_{in} \quad (10)$$

Substituting (7) into (1) yields the voltage gain:

$$\frac{V_o}{V_{in}} = \frac{D_A D_B}{2D_A + D_B} \quad (11)$$

The duty cycles of the two phases are equal: $D_A = D_B = D$. Consequently, the obtained voltage gain is

$$\frac{V_o}{V_{in}} = \frac{D}{3} \quad (12)$$

4. Design Considerations

In the following, the system configuration and specifications and the design of the differential-mode transformer are described.

4.1. System Configuration

Figure 13 shows the system configuration of the proposed two-phase high-step-down converter, which features ZVS and automatic current sharing. It consists of the main power circuit, the gate driving circuits (TLP250s) for the switches, and the output voltage feedback control circuit. Particularly, the analog signal is sampled by the analog-to-digital (ADC) and transmitted to the field-programmable gate arrays (FPGAs) to generate the PWM control signal. This signal is used to regulate the duty cycle of the switch to ensure stable operation of the converter and output voltage regulation.

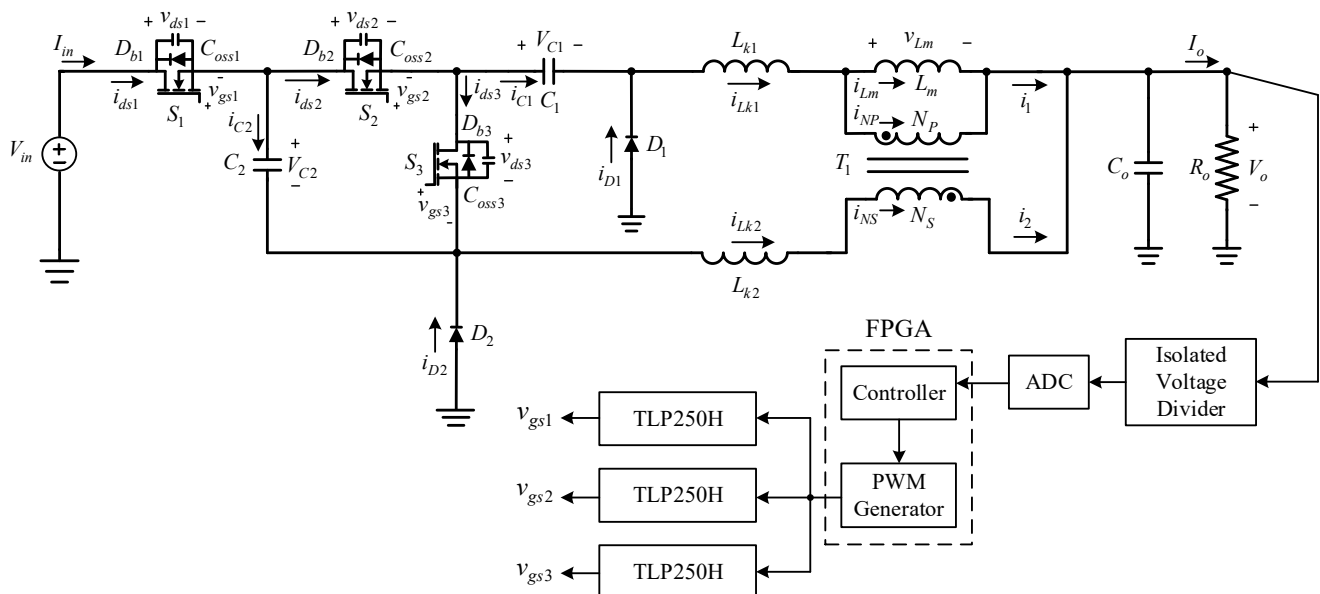


Figure 13. Proposed system configuration.

4.2. System Specifications

The specifications for the converter system proposed in this paper are shown in Table 1.

Table 1. System specifications.

Description	Symbol	Specification/Value
Input Voltage	V_{in}	300 V
Output Voltage	V_o	48 V
Rated Output Current	$I_{o, rated}$	4 A
Rated Output Power	$P_{o, rated}$	192 W
Switching Frequency	f_s	100 kHz
Current Error	$ \varepsilon $	<10%
ZVS Range	$\% P_{o, rated}$	25 ~ 100

4.3. Design of Magnetizing of Differential-Mode Transformer

Assume that the turns of T_1 $N_P = N_S$ are equal and the leakage inductances L_{s1} and L_{s2} of the differential-mode transformer T_1 are symmetrical. It is desired that the current error ($|\varepsilon|$) is within the range of 25% to 100% of the rated load.

As shown in Figure 14, where $I_{Lm, avg}$ indicates the average value of the excitation current, ΔI_{error} indicates the error between the two-phase currents, and the time during which the magnetizing inductor is subjected to a positive voltage is $0.5 T_s$, during the period from State 3 to State 5 ($t_2 \leq t < t_5$), the magnetizing inductance L_m of the differential

transformer T_1 transitions from backward demagnetization to forward magnetization, and its magnetizing current rises linearly, whereas during the period from State 6 to State 2 ($t_5 \leq t < t_2 + T_s$), the magnetizing inductance transitions from forward demagnetization to backward magnetization, and its magnetizing current decreases linearly.

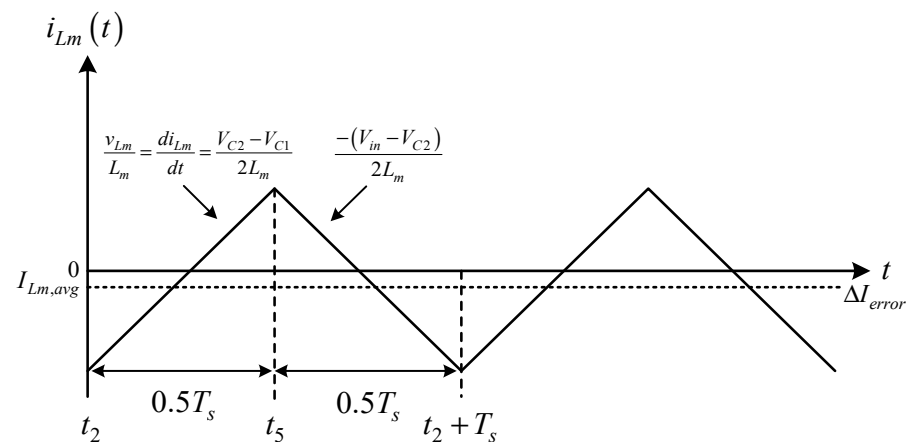


Figure 14. Operating behavior of the magnetizing inductor.

In State 4, the magnetizing current rises linearly, indicating that a positive voltage is applied across the magnetizing inductor. In a differential-mode transformer, the voltage across the magnetizing inductor is positive on the left and negative on the right (as shown by the defined direction), and a voltage of equal magnitude but opposite polarity is induced on the secondary side. Furthermore, by treating the output as an equivalent DC voltage source V_o , the circuit model for State 4 can be represented as shown in Figure 15.

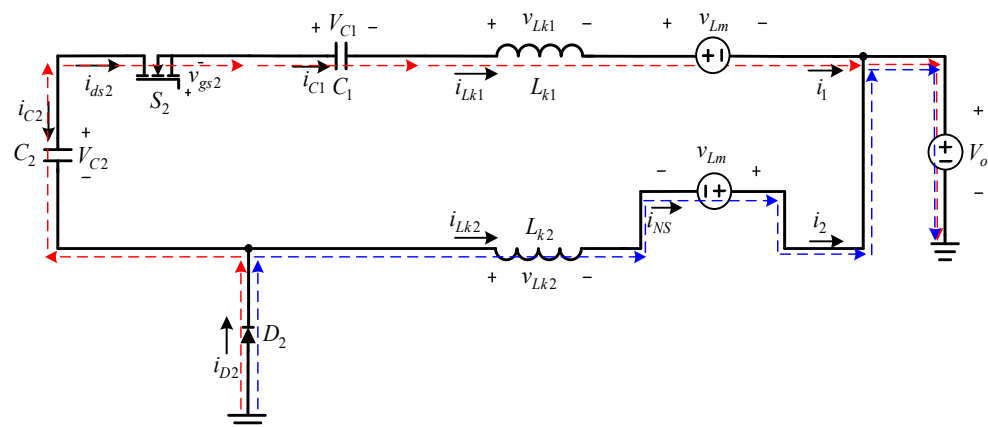


Figure 15. Operating behavior of the magnetizing inductor in State 4.

As shown in Figure 15, during State 4, the voltage across the magnetizing inductor L_m can be expressed as

$$v_{Lm} = V_{C2} - V_{C1} - v_{Lk1} - V_o \quad (13)$$

$$v_{Lm} = v_{Lk2} + V_o \quad (14)$$

In this research, based on the previous definitions and assumptions, the leakage inductance on the primary and secondary sides of the differential-mode transformer L_m are equal ($L_{k1} = L_{k2}$), and because the two-phase currents display automatic current sharing, the currents flowing through the leakage inductance on the primary and secondary sides of the differential-mode transformer L_m are approximately equal, with their average values both being approximately $I_o/2$. Therefore, the voltages v_{Lk1} and v_{Lk2} across the primary

and secondary leakage inductances i_{Lk1} and i_{Lk2} of the differential transformer L_m are also nearly equal. Therefore, in subsequent derivations, the two voltages can be treated as identical, that is,

$$v_{Lk1} = v_{Lk2} = v_{Lk} \quad (15)$$

From (12)–(15), it can be derived that, during State 4, the voltage v_{Lm} across the magnetizing inductor L_m can be calculated using the relationship between V_{C1} and V_{C2} :

$$v_{Lm} = \frac{V_{C2} - V_{C1}}{2} \quad (16)$$

Therefore, based on (16) and Figure 15, the average value $I_{Lm,avg}(=\Delta I_{error})$ of the magnetizing current can be expressed as

$$I_{Lm,avg} = \Delta I_{error} = \left[\frac{1}{2} \left(\frac{V_{C2} - V_{C1}}{2L_m} \times 0.5T_s \right) \times 0.5T_s \right] \times \frac{1}{T_s} \\ = \frac{V_{C2} - V_{C1}}{16 \times L_m \times f_s} \quad (17)$$

The output currents of the two phases, on average, are

$$I_{avg} = \frac{I_1 + I_2}{2} = \frac{\Delta I_{error} + I_{NP} + I_{NS}}{2} \\ = \frac{2I_1 - \Delta I_{error}}{2} \quad (18)$$

In addition, the current sharing percentage error (CSEP) ε can be expressed as

$$\varepsilon = \frac{|I_{avg} - I_1|}{I_{avg}} \times 100\% = \frac{|I_{avg} - I_2|}{I_{avg}} \times 100\% \quad (19)$$

where I_1 and I_2 are the first and second currents, respectively.

Substituting (18) and (19) into (17) yields the design criteria for the magnetizing inductance L_m as follows:

$$L_m = \frac{(1 - \varepsilon) \cdot (V_{C2} - V_{C1})}{32 \cdot \varepsilon \cdot I_1 \cdot f_s} \quad (20)$$

Therefore, to meet the design requirement of a two-phase current error rate less than 10% at light load shown in Table 1, the minimum value of the magnetizing inductance L_m required is

$$L_m \geq \frac{(1 - \varepsilon) \cdot (V_{C2} - V_{C1})}{32 \cdot \varepsilon \cdot I_1 \cdot f_s} \\ \geq \frac{(1 - 0.1) \cdot (200 - 100)}{32 \cdot 0.1 \cdot 0.5 \cdot 100 \times 10^3} \geq 562.5 \mu\text{H} \quad (21)$$

Furthermore, considering that the magnetizing inductance L_m of a differential-mode transformer T_1 is susceptible to non-ideal factors such as frequency variations, temperature effects, and manufacturing tolerances of magnetic components during actual operation, the actual inductance value may deviate from the theoretical value. Therefore, this paper adds a design margin of 1.25 times to the minimum required value of the magnetizing inductance L_m derived from theoretical calculations. Finally, the magnetizing inductance L_m is designed to be 708 μH .

5. Control Structure

Figure 16 shows the control structure for the proposed circuit. The overall circuit consists of an analog-to-digital converter (ADC), a proportional–integral (PI) controller, a pulse-width modulation (PWM) modulator, and a limiter. The control strategy involves measuring the feedback signal V_{sensor} from the output voltage and using the ADC to convert it from an analog signal to a digital signal. Sequentially, this signal is compared with the reference command V_{ref} to yield the error signal, which is sent to the PI controller to create

a control force. After this, control force is sent to the PWM modulator. Then, there are two paths for this control force. One is directly sent to Dead Time Generator 1 to generate v_{gs1} and v_{gs3} , and other is sent to Dead Time Generator 2 to generate v_{gs2} .

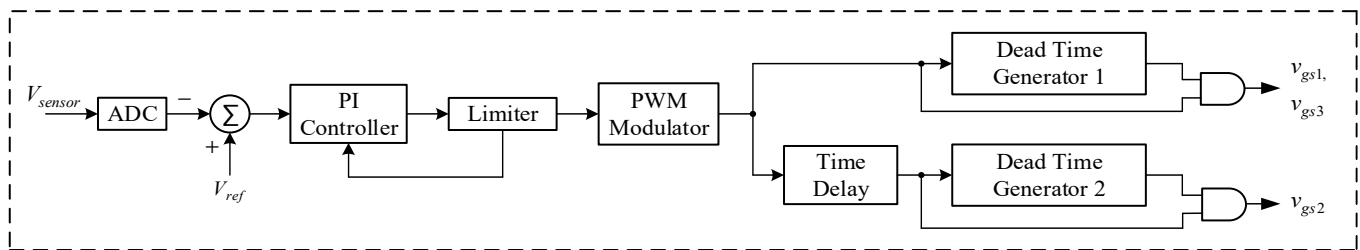


Figure 16. Control structure.

6. Experimental Results

6.1. Experimental Setup

Figures 17–19 depict the experimental setup, while the corresponding hardware component parameters are summarized in Table 2.

Table 2. Parameters of the hardware components.

Name	Symbol	Model/Specification
MOSFET	S_1	International Rectifier (El Segundo, CA, USA)/ IRFB4020PbF
MOSFET	S_2, S_3	STMicroelectronics (Plan-les-Ouates, Switzerland)/ STP14NM50N
SiC-Schottky Diode	D_1, D_2	Infineon (Neubiberg, Germany)/IDH12G65C6
Energy-Transferring Capacitor	C_1, C_2	Film Capacitor (Nichicon Corporation, Kyoto, Japan)/ $C_1 = C_2 = 15 \mu\text{F}/400 \text{ V}$
Differential-Mode Transformer	T_1	TDK (Tokyo, Japan) PC47PQ35/35Z-12 $L_m = 708 \mu\text{H}$ $L_{k1} = L_{k2} = 0.65 \mu\text{H}$ $N_p = N_s$: 13 turns $B_s = 0.42 \text{ T}$ at 100°C
Output Capacitor	C_o	Polymer Capacitor (Panasonic Corporation, Kadoma, Osaka, Japan) $220 \mu\text{F}/63 \text{ V} \times 3$

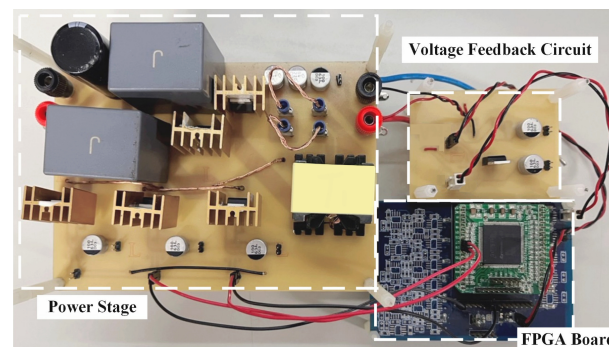


Figure 17. Photo of the experimental setup.

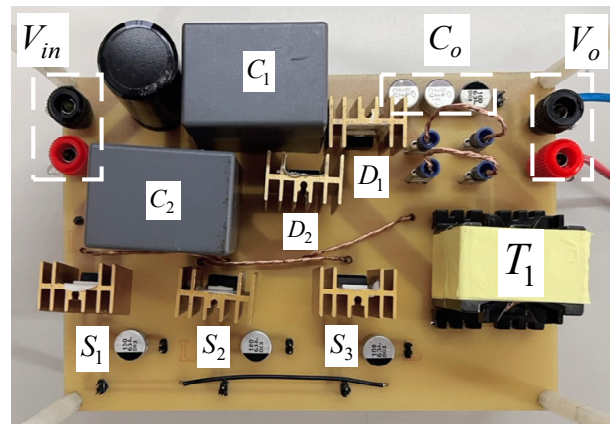


Figure 18. Top view.

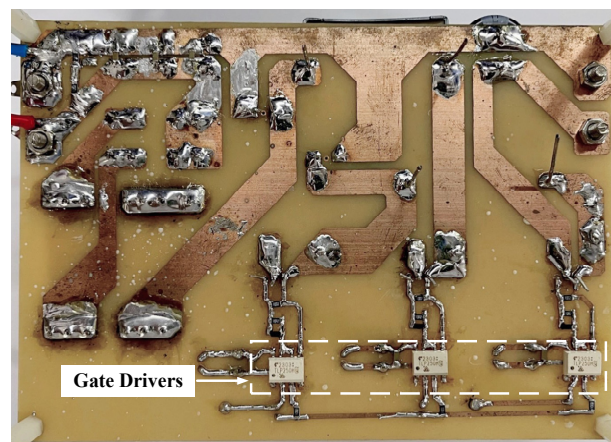


Figure 19. Bottom view.

6.2. Measured Waveforms at Light Load

Figure 20 shows the experimental waveforms of the gate driving signals for switches S_1 , S_2 and S_3 at light load. As shown in this figure, the gate driving signals for switches S_1 and S_3 are synchronized, while the gate driving signal for switch S_2 is delayed by 180 degrees relative to switches S_1 and S_3 . Furthermore, the duty cycles of all switches are approximately 48%.

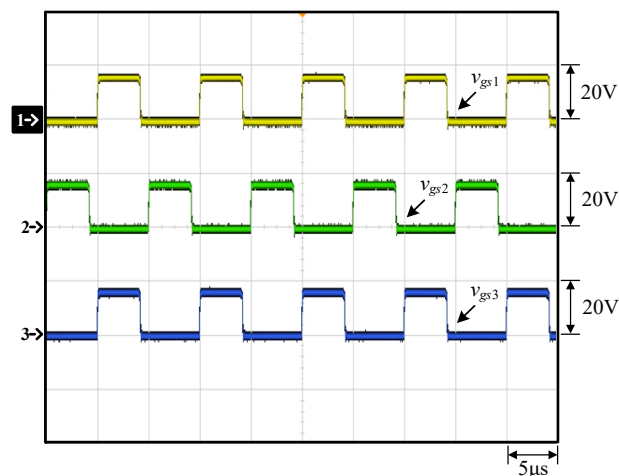


Figure 20. Experimental waveforms at light load: (1) v_{gs1} ; (2) v_{gs2} ; (3) v_{gs3} .

Figure 21 shows the experimental waveforms of the two-phase output currents i_1 and i_2 at light load. As can be seen from the figure, when switches S_1 and S_3 turn on simultaneously and switch S_2 turns off, the average values of the two-phase output currents i_1 and i_2 are approximately $2I_o/3$. Conversely, when switches S_1 and S_3 turn off and switch S_2 turns on, the average values of the two-phase output currents i_1 and i_2 are approximately $I_o/3$.

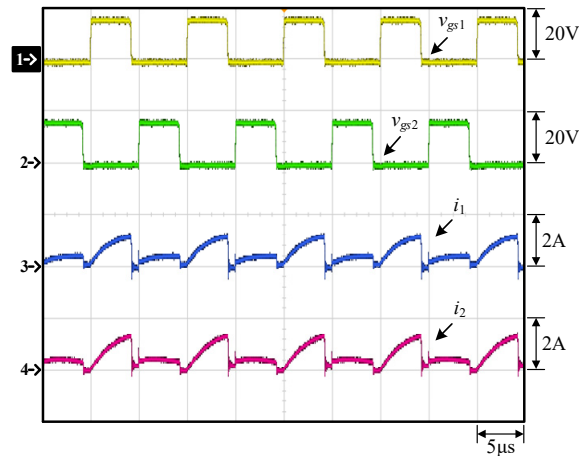


Figure 21. Experimental waveforms at light load: (1) v_{gs1} ; (2) v_{gs2} ; (3) i_1 ; (4) i_2 .

Figure 22 shows the experimental waveforms for the voltages across the energy-transferring capacitors at light load. As can be seen from the figure, the voltages across energy-transferring capacitors C_1 and C_2 stabilize at $V_{in}/3$, while the voltage across energy-transferring capacitor C_2 stabilizes at $2V_{in}/3$.

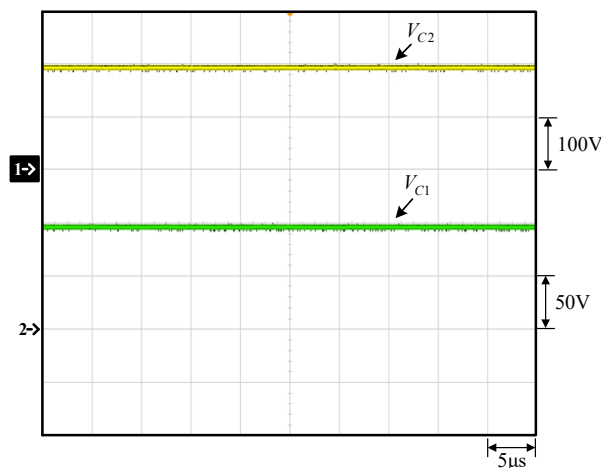


Figure 22. Experimental waveforms at light load: (1) V_{C2} ; (2) V_{C1} .

Figure 23 shows the experimental waveforms of the output voltage V_o and output current I_o at light load. As can be seen from this figure, the proposed circuit is able to maintain a stable output voltage V_o of 48 V through closed-loop control.

Figures 24–26 show the experimental waveforms of the gate driving signals and their corresponding drain–source voltages for all switches at light load. Figure 24 displays the gate driving signal v_{gs1} of switch S_1 and its corresponding drain–source voltage v_{ds1} . Figure 25 shows the gate driving signal v_{gs2} of switch S_2 and its corresponding drain–source voltage v_{ds2} . Figure 26 displays the gate driving signal of switch S_3 and its corresponding drain–source voltage v_{ds3} . All switches have ZVS turn-on.

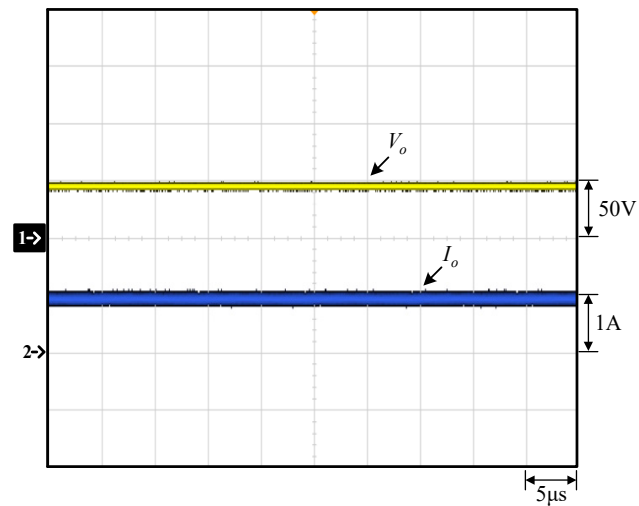


Figure 23. Experimental waveforms at light load: (1) V_o ; (2) I_o .

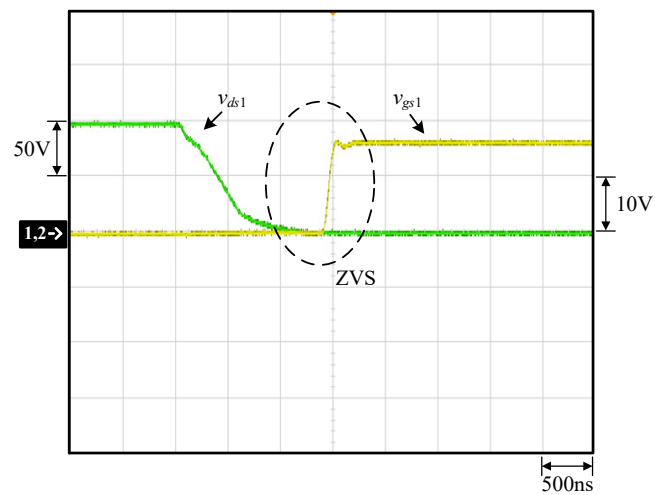


Figure 24. Experimental waveforms at light load: (1) v_{gs1} ; (2) v_{ds1} .

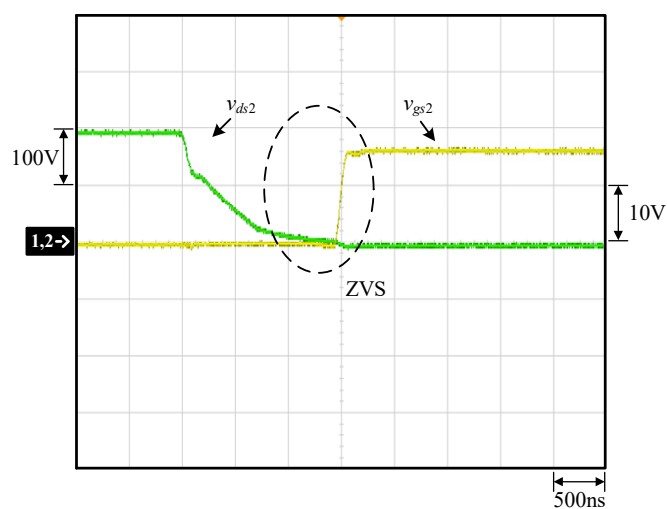


Figure 25. Experimental waveforms at light load: (1) v_{gs2} ; (2) v_{ds2} .

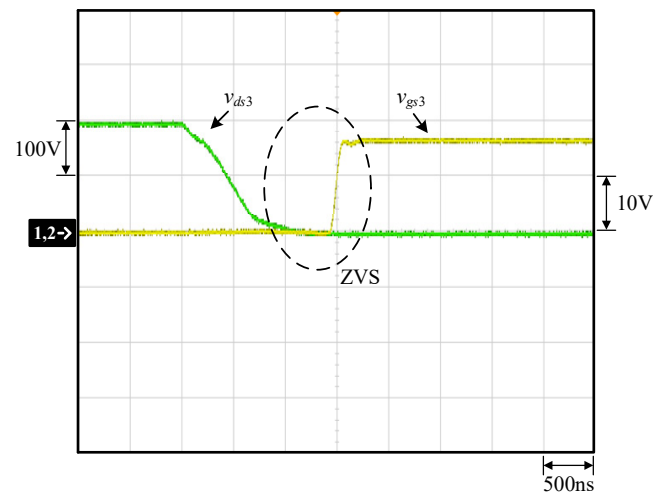


Figure 26. Experimental waveforms at light load: (1) v_{gs3} ; (2) v_{ds3} .

6.3. Measured Waveforms at Rated Load

From Figures 27–33, the items of the experimental measurements at rated load are the same as those at light load from Figures 20–26, respectively. The difference in waveform between them is the magnitude of each figure and its corresponding figure, but their waveforms are alike to some extent. All switches at rated load also have ZVS. Furthermore, as shown in Figure 28, the differential-mode transformer does not saturate under 100% load. This is because no near-short-circuit current occurs during its magnetization.

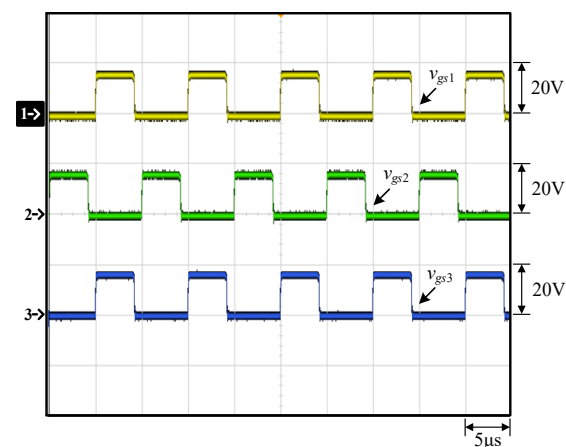


Figure 27. Experimental waveforms at rated load: (1) v_{gs1} ; (2) v_{gs2} ; (3) v_{gs3} .

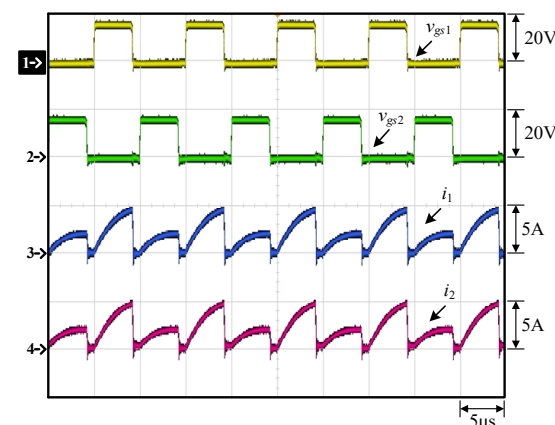


Figure 28. Experimental waveforms at rated load: (1) v_{gs1} ; (2) v_{gs2} ; (3) i_1 ; (4) i_2 .

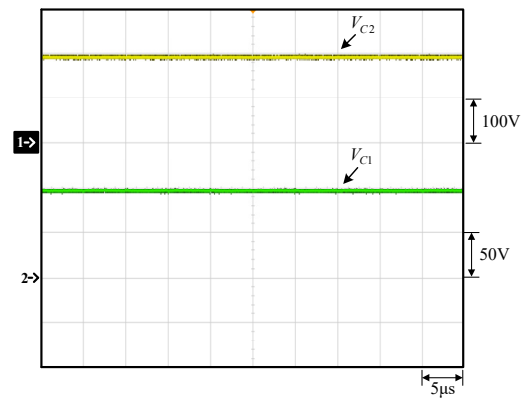


Figure 29. Experimental waveforms at rated load: (1) V_{C2} ; (2) V_{C1} .

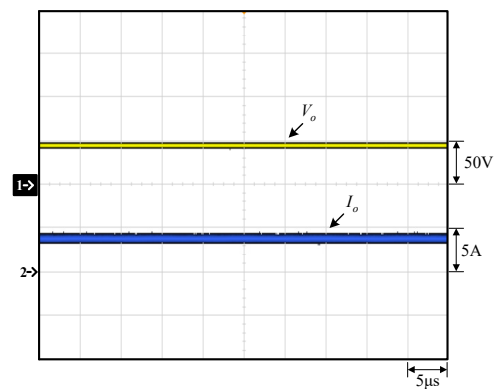


Figure 30. Experimental waveforms at rated load: (1) V_o ; (2) I_o .

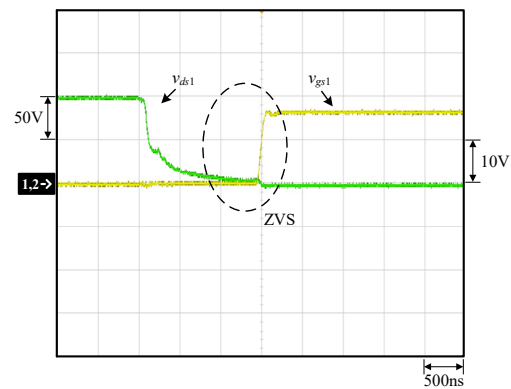


Figure 31. Experimental waveforms at rated load: (1) v_{gs1} ; (2) v_{ds1} .

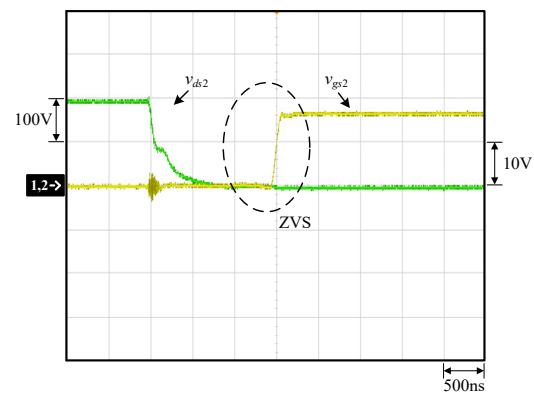


Figure 32. Experimental waveforms at rated load: (1) v_{gs2} ; (2) v_{ds2} .

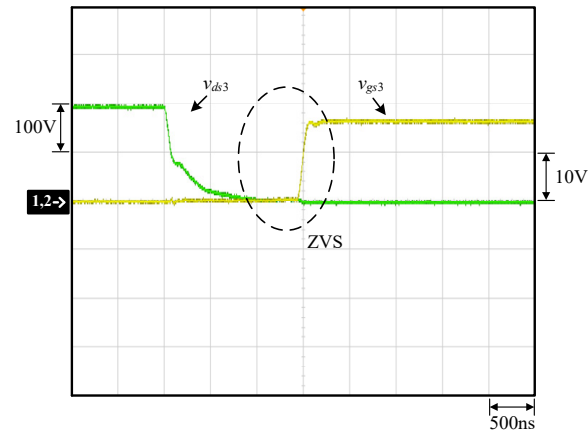


Figure 33. Experimental waveforms at rated load: (1) v_{gs3} ; (2) v_{ds3} .

6.4. Current Error Sharing Percentage

Figures 34 and 35 show the upload transient and the download transient, respectively. Both have a setting time of 0.27 ms.

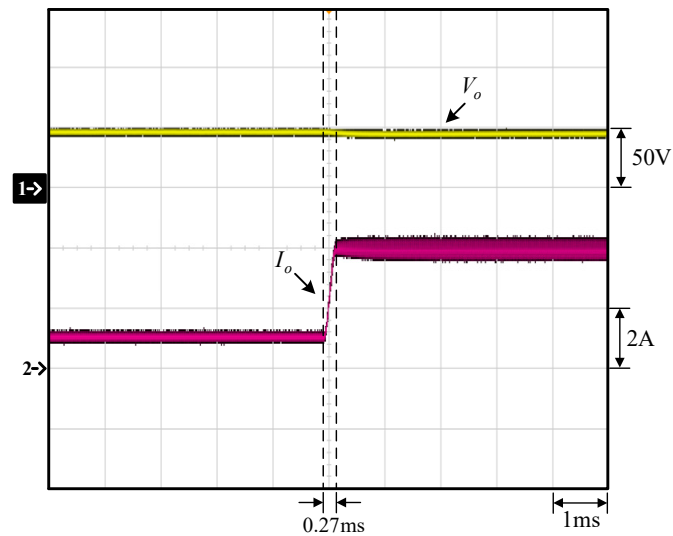


Figure 34. Upload transient from light load to rated load. (1) V_o ; (2) I_o .

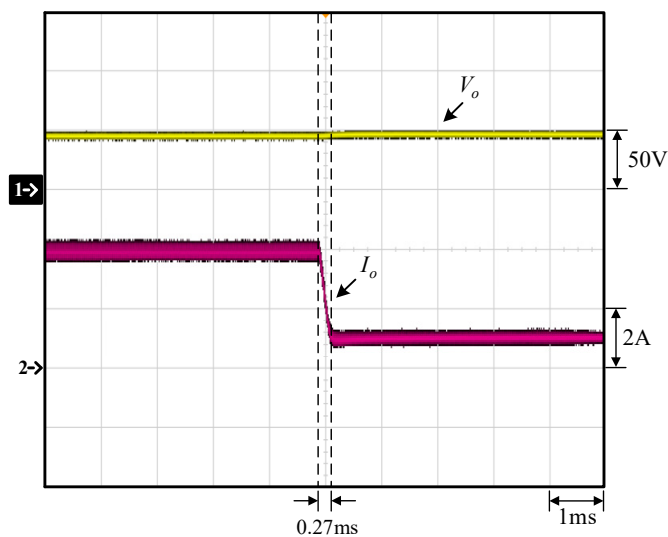


Figure 35. Download transient from rated load to light load. (1) V_o ; (2) I_o .

6.5. Current Error Sharing Percentage

Based on the experimental data collected for the proposed circuit under various load conditions, the current error sharing percentage (CSEP) of the two-phase output currents will be determined. Equation (19) is rewritten as

$$\varepsilon = \frac{\left| \frac{(I_1 + I_2)}{2} - I_1 \right|}{\frac{(I_1 + I_2)}{2}} \times 100\% = \frac{\left| \frac{(I_1 + I_2)}{2} - I_2 \right|}{\frac{(I_1 + I_2)}{2}} \times 100\% \quad (22)$$

Table 3 shows the results for the 25%, 50%, and 100% rated load conditions. Figure 36 shows the curve of the CSEP. The measurements show a minimum duty cycle of about 0.55. It should be noted that a differential-mode transformer with a turns ratio equal to 1 represents a passive current sharing device, which will force the two currents to be in-phase and equal. The main current sharing error comes from the magnetizing current. The smaller the magnetizing inductance, the larger the magnetizing current, and the larger the current sharing error.

Table 3. CSEP for the two-phase output currents under three different loads.

	25% Rated Load	50% Rated Load	100% Rated Load
I_1 (A)	0.55	1.05	2.02
I_2 (A)	0.49	1.03	2.09

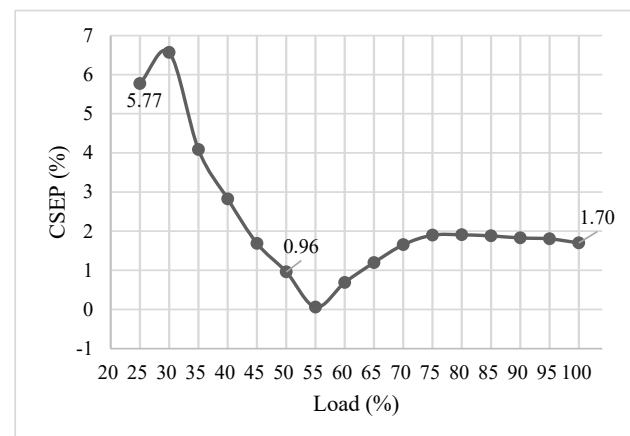


Figure 36. CSEP vs. rated load.

Figure 37 shows the efficiency versus load curve, where the efficiency remains above 92.87% across the entire load range and reaches a peak of 95.83% at rated load.

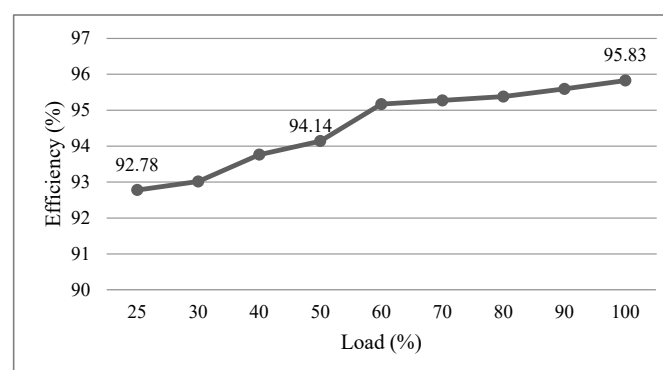


Figure 37. Efficiency vs. rated load.

7. Circuit Comparison

Table 4 presents a comparison of the proposed circuit with other related circuits. Reference [14] incorporates a series capacitor into a traditional two-phase buck converter, allowing the input voltage to be evenly distributed and thereby reducing the equivalent input voltage of both the upper and lower phases to $V_{in}/2$. Compared to a conventional buck converter, its effective duty cycle can be extended from D to twice that value, i.e., $D/2$. Furthermore, this series capacitor achieves a certain degree of current sharing. However, the switching method of this structure is hard switching; therefore, significant switching losses occur at the moment of switching, resulting in a peak efficiency of approximately 93.2%. Compared to the circuit in Reference [14], the circuit proposed in this paper, using a similar number of components, not only features automatic current sharing but also extends the effective duty cycle to three times the original value, i.e., $D/3$, and enables ZVS for all switches. Reference [15] integrates a diode-capacitor module into a two-phase buck converter, which effectively increases the voltage step-down ratio. However, this structure also significantly increases the number of components; the excessive number of diodes causes a sharp rise in conduction losses, and under hard switching operation, substantial switching losses occur during the switching transition, resulting in a peak efficiency of only approximately 85.1%.

Table 4. Comparison of the other existing circuits with the proposed circuit.

Reference Number	[14]	[15]	[18]	Proposed
Input Voltage (V)	12	60	48	300
Output Voltage (V)	1.5	1.8	1	48
Rated Output Power (W)	60	36	30	192
Number of Phases	Two	Two	Two	Two
Number of Components	8	14	10	9
Voltage Gain	$D/2$	$D/4$	$D/3$	$D/3$
Current Sharing Method	Capacitor	None	Capacitor	Differential Transformer
Current Sharing	Automatic	None	Under Certain Constraints	Automatic
Soft Switching	No	No	No	ZVS Turn On
Switching Frequency (kHz)	250	100	500	100
Peak Efficiency (%)	93.2	85.1	91.5	95.83

Key Features/Advantages

- Doubled duty cycle
- Halved switch voltage stress
- Inherent/automatic current balancing

- Significant duty cycle extension
- Reduced voltage stress on switches
- Interleaved ripple cancelation and auto-balancing

- High step-down conversion ratio with wide duty cycle
- Drastically reduced voltage stress and high efficiency
- Soft charging/low-current spike mechanism

- High step-down gain with reduced switch voltage stress
- ZVS turn-on across 25% to 100% of the rated load
- Sensorless automatic current sharing via differential-mode transformer

Table 4. Cont.

Reference Number	[14]	[15]	[18]	Proposed
Key Limitations/Disadvantages	• Floating gate driver complexity • Series-capacitor losses and stress • Startup and inrush transients	• Increased component count & complexity • Floating gate driver & EMI challenges • Capacitor losses & inrush current	• High component count & circuit complexity • Multiple floating switch nodes and gate drive overhead • Complex startup sequencing & transient control	• Design sensitivity and complexity of the differential-mode transformer • Floating gate drive requirements for multiple switches • Conduction losses from passive freewheeling diodes

Reference [18] adds an additional capacitor to a traditional series-capacitor buck converter. By utilizing the voltage-dividing effect of the two series-connected capacitors, this approach not only significantly reduces the voltage stress on the switching devices but also extends the effective duty cycle to three times its original value. However, this structure does not inherently possess automatic current sharing capabilities and relies on strict duty cycle settings to achieve current sharing. Furthermore, its switching method remains hard switching, which leads to increased switching losses, resulting in a peak efficiency of approximately 91.5% and limiting further improvements in conversion efficiency. As for the proposed circuit, all switches can achieve ZVS, thereby effectively suppressing switching losses and reducing current stress between phases. The experimental results show that the conversion efficiency of this circuit is significantly improved, with a peak efficiency up to 95.83%. Furthermore, it possesses a high CSEP capability above half load.

8. Conclusions

This paper proposes a two-phase high-step-down converter featuring ZVS and automatic current sharing. The proposed circuit is primarily based on a traditional series-capacitor step-down converter, with the addition of an energy-transferring capacitor. By utilizing the voltage-divider characteristics of the series capacitors, it effectively reduces the voltage stress on all the switches. Furthermore, this paper incorporates a differential-mode transformer between the two phases, utilizing its operational characteristics to achieve automatic current balancing between the two-phase outputs. The experimental results show that the CSEP above half load has excellent current balancing capability. At the same time, the leakage inductance generated by the non-ideal coupling of the differential-mode transformer provides a follow-current path during the switching process and helps discharge the parasitic capacitance of the switches, enabling all switches to achieve ZVS, thereby reducing switching losses. Additionally, the circuit has a full-load efficiency of 95.83%.

Author Contributions: Conceptualization, K.-I.H. and J.-J.S.; methodology, K.-I.H. and P.-C.W.; software, J.-J.S. and P.-C.W.; validation, K.-I.H. and J.-J.S.; formal analysis, K.-I.H. and P.-C.W.; investigation, K.-I.H. and P.-C.W.; resources, J.-J.S.; data curation, J.-J.S.; writing—original draft preparation, K.-I.H.; writing—review and editing, K.-I.H. and J.-J.S.; visualization, K.-I.H. and J.-J.S.; supervision, K.-I.H.; project administration, K.-I.H.; funding acquisition, J.-J.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Science and Technology, Taiwan, under Grant Number NSTC 115-2221-E-027-127-.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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