

Article

Monolithic Intrinsic-Capacitance Bootstrapped Inverter in E-Mode GaN-on-SOI: Design, Analysis, and Electro-Thermal Characterization

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Abstract

This paper presents, analyzes, and experimentally validates a bootstrapped inverter implemented via low-voltage enhancement-mode HEMTs offered by a 200-V E-mode GaN-on-SOI monolithic platform. Unlike conventional resistor–transistor logic (RTL), the proposed topology exploits intrinsic device capacitances to achieve a transient current-source-like pull-up behavior without dedicated bootstrap capacitors. A detailed analytical model is developed to describe the dynamic operation and to identify the conditions under which the low-to-high transition overcomes the RC limitation of RTL inverters. Measurements demonstrate a more than 30% reduction in rise time, higher static gain, and an overall improvement in total noise margins under comparable static current conditions. The temperature dependence of bootstrap efficiency from $-40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$ is also investigated. By combining experimental measurements with model-based parameter extraction, we show that the high-temperature performance crossover is attributed primarily to leakage-induced overdrive reduction. In contrast, threshold-voltage drift acts in the opposite direction and mobility degradation affects both topologies similarly.

Keywords: bootstrapped inverter; GaN logic gates; GaN device; GaN technology; GaN IC

1. Introduction

Gallium Nitride (GaN) high electron mobility transistors (HEMTs) have enabled major advances in power electronics owing to their high breakdown field, low parasitic capacitances, and high electron mobility [1–3]. While discrete GaN power devices have reached a high level of maturity, the realization of fully monolithic GaN integrated circuits (ICs) remains a critical challenge for compact high-frequency power systems [4–6]. In particular, the integration of low-voltage control and logic circuitry together with high-voltage power devices is essential to fully exploit the switching-speed potential of GaN technologies while minimizing parasitic effects associated with multi-die System-in-Package (SiP) solutions [7–9].

The design of monolithic GaN logic gates is fundamentally constrained by the absence of complementary p-channel devices, which restricts the available logic families to n-type-only topologies. In the specific 200-V GaN-on-SOI platform employed in this work, the lack of depletion-mode (D-mode) HEMTs further prevents the implementation of conventional direct-coupled FET logic (DCFL), commonly adopted in GaN-on-Si technologies [5,6,9,10]. As a result, resistor–transistor logic (RTL) is often adopted because of its simplicity and



Academic Editor: Costas Psychalinos

Received: 11 September 2026

Revised: 3 October 2026

Accepted: 7 October 2026

Published: 9 October 2026

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compatibility with enhancement-mode-only processes [4]. However, RTL gates inherently suffer from a severe speed–power tradeoff: increasing the pull-up resistance reduces static current consumption but significantly degrades the low-to-high transition speed due to RC-limited charging of the load capacitance.

Alternative pull-up strategies based on diode-connected enhancement-mode HEMTs alleviate the RC limitation [11] but restrict the output high level to approximately $V_{DD} - V_{TH}$, where V_{TH} is the HEMT threshold voltage, thereby degrading noise margins and switching robustness.

Bootstrapping techniques provide an attractive mechanism to enhance the effective gate overdrive in GaN circuits. Gate-driver architectures employing large bootstrap capacitors, often implemented using metal-insulator-metal (MIM) structures or off-chip components, have been presented [12]. Although effective for driving large power transistors, these approaches are not suitable for compact monolithic logic stages because of area overhead and integration complexity. Previous IC-oriented works are mainly focused on a theoretical/simulation framework [13,14] without considering thermal effects.

More broadly, the sensitivity of inverter-based circuits to threshold and supply variations has been addressed at the circuit level in recent works, e.g., [15], although not in the context of GaN technologies.

This research describes and implements an intrinsic-capacitance bootstrapped inverter implemented using the low-voltage 6-V transistors available in the IMEC 200-V E-mode GaN-on-SOI technology [16–19]. Unlike conventional bootstrap circuits, the proposed topology exploits the intrinsic gate capacitance of a GaN HEMT as the bootstrap storage element, eliminating the need for external capacitors while remaining fully compatible with standard E-mode-only process design rules. The dielectric isolation provided by the SOI substrate plays a key role in preserving the bootstrap efficiency by suppressing substrate coupling and charge leakage paths.

The main contributions of this work are summarized as follows:

- Development of a unified analytical electro-thermal framework describing the static and dynamic behavior of intrinsic-capacitance bootstrapped GaN logic;
- Experimental demonstration of a monolithic bootstrapped inverter in a 200-V GaN-on-SOI platform;
- Identification of leakage-induced overdrive degradation as the primary mechanism behind high-temperature bootstrap performance loss, demonstrated through experimental measurements coupled with indirect model-based parameter extraction.

Experimental results demonstrate a more than 30% reduction in rise time at room temperature together with improved gain and noise margins under comparable static current conditions with respect to conventional RTL implementations.

The remainder of this paper is organized as follows. Section 2 describes the proposed topology and operating principle. Section 3 presents the analytical modeling of the RTL [20] and bootstrapped inverters. Section 4 discusses the electro-thermal behavior. Sections 5 and 6 report simulation and experimental results, respectively. Section 7 presents parameter extraction and discussion, while Section 8 concludes the paper.

2. Circuit Description and Operation

2.1. Reference RTL Inverter

Figure 1a illustrates a conventional resistor–transistor logic (RTL) inverter implemented in an E-mode GaN-on-SOI technology [4]. The circuit employs a single E-mode GaN HEMT, Q_1 , as the pull-down device and a passive resistor R_1 as the pull-up element. This topology serves as the primary benchmark throughout this work. The principal ad-

vantage of RTL is its simplicity and robustness. However, as is well known, it suffers from a fundamental speed–power tradeoff, as will be briefly summarized in Section 3.1.

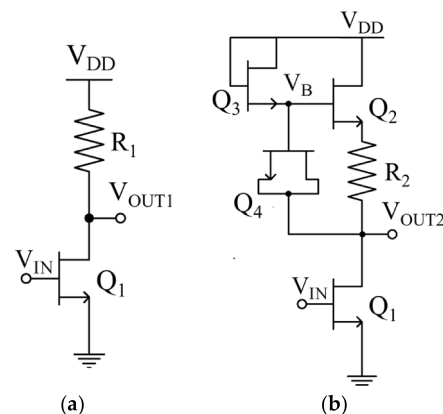


Figure 1. Circuit schematic diagrams of the implemented logic stages: (a) Conventional resistor–transistor logic (RTL) inverter employing a single E-mode GaN HEMT, Q_1 , and a passive pull-up resistor, R_1 ; (b) Proposed intrinsic-capacitance bootstrapped (BS) inverter. In the BS topology, Q_2 acts as the pull-up driver, Q_3 provides diode-connected precharge, Q_4 utilizes its intrinsic gate-to-channel capacitance for charge storage, and R_2 is employed to calibrate the output current and power-delay profile.

2.2. Intrinsic Bootstrapped Inverter Topology

Figure 1b shows the proposed bootstrapped (BS) inverter. As in RTL, the pull-down path is implemented by transistor Q_1 . The pull-up network instead consists of three transistors, Q_2 – Q_4 , and a balancing resistor R_2 . In this topology, Q_2 provides the pull-up current and Q_3 is diode-connected to establish the bootstrap precharge voltage onto Q_4 , which acts as a charge-storage element (capacitor). Unlike conventional driver-oriented bootstrapped circuits that rely on large MIM or even external capacitors, the proposed inverter achieves full monolithic integration by exploiting the intrinsic gate-to-channel capacitance of Q_4 . As a result, no off-chip passive components are required and the circuit remains fully compatible with standard E-mode-only GaN-on-SOI process design rules. The intrinsic bootstrap capacitance can be approximated as $C_{BS} \approx C_{GS4} + C_{GD4}$. The resistor R_2 introduces source degeneration to limit the pull-up current and is used to calibrate the power-delay profile.

To facilitate analytical insight, the operation of the proposed inverter is divided into two distinct phases: a pull-down (precharge) phase and a pull-up (bootstrap) phase.

(1) Pull-Down (Precharge) Phase

When $V_{IN} = V_{DD}$, transistor Q_1 is turned on and discharges the output node toward ground. During this phase, Q_3 becomes forward-biased and charges the intrinsic capacitance of Q_4 . As a result, the bootstrap node (the gate of Q_2) settles to the precharge voltage $V_{B,0}$, where subscript “0” indicates the precharge initial phase

$$V_{B,0} = V_{DD} - V_{TH3} \quad (1)$$

In other words, the bootstrap capacitor is initialized to a well-defined voltage, $V_{B,0}$, prior to each pull-up transition. Because the bootstrap node is refreshed during every low output phase, long-term charge retention is not required, provided sufficient switching activity is maintained.

(2) Pull-Up Phase

When V_{IN} transitions low, Q_1 turns off and the output node begins to rise. The charge stored in the intrinsic bootstrap capacitance forces the bootstrap node to follow the output voltage according to the first-order relationship

$$V_B(t) = V_{B,0} + \eta_{BS} V_{OUT}(t) \quad (2)$$

where $V_{OUT}(t)$ is measured from the initial output level at the onset of the pull-up phase, assumed to be approximately 0 V. The factor η_{BS} denotes the bootstrap coupling efficiency and accounts for the capacitive division between the intrinsic bootstrap capacitance C_{BS} and the total parasitic capacitance C_{PAR} connected to the bootstrap node

$$\eta_{BS} = \frac{C_{BS}}{C_{BS} + C_{PAR}} \quad (3)$$

C_{PAR} includes the gate–source capacitances of Q_3 , the gate–drain capacitance of Q_2 , and substrate-related parasitic capacitances.

The buried oxide (BOX) layer of the 200-V GaN-on-SOI platform plays a critical role in maximizing η_{BS} by suppressing substrate coupling and charge leakage paths that would otherwise degrade the bootstrap efficiency.

2.3. Modeling Assumptions and Validity

To maintain the mathematical tractability of the time transients, the proposed model introduces four fundamental physical assumptions, whose scientific validity is established as follows:

- (a) Saturation of Q_2 . The primary operational advantage of the BS topology relies on Q_2 acting as a quasi-constant-current pull-up source. The bootstrap mechanism ensures that the gate-to-source voltage $V_{GS2}(t)$ dynamically tracks the rising output voltage $V_{OUT}(t)$, thereby maintaining a nearly invariant gate overdrive voltage $V_{OV} = V_{GS2}(t) - V_{TH2} \approx \text{const.}$ Although Q_2 transitions from saturation to the triode region as $V_{DS2}(t) = V_{DD} - V_{OUT}(t) - I_{BS}R_2$ decreases, the source degeneration resistor R_2 stabilizes the pull-up current. As confirmed experimentally in Section 6, this yields a highly linear charging ramp over more than 90% of the output voltage swing.
- (b) Invariance of Load Capacitance (C_L). The output node is loaded by low-voltage (6 V) E-mode HEMTs. Unlike high-voltage GaN power-switching configurations that undergo massive drain-voltage sweeps of hundreds of volts, these digital sub-circuits operate strictly within a 0 to 6 V window. Within this narrow regime, the voltage dependence of the output capacitance C_{oss} is quantitatively negligible, validating the constant- C_L assumption.
- (c) Linearity of C_{gg} . Although intrinsic GaN capacitances are strongly voltage-dependent in general, the storage transistor Q_4 is biased with $V_{DS} = 0$ V and its gate-to-source voltage is precharged to $V_{DD} - V_{TH3}$, remaining well above the threshold throughout the bootstrap phase. Consequently, the 2DEG channel is never depleted [21] and the device stays within the voltage-independent plateau of its $C_{gg}(V_{GS})$ characteristic. This allows the gate capacitance to be modeled as a linear barrier capacitance, validating the linear divider formulation in (3).
- (d) Absence of Body Effects. The devices are implemented on a GaN-on-SOI platform. The underlying silicon-on-insulator substrate provides complete dielectric isolation, entirely eliminating the bulk substrate connection. Consequently, threshold voltage degradation via body-effect modulation is inherently absent.

Furthermore, under moderate capacitive loads, bootstrap efficiencies of approximately 0.86–0.87 are obtained due to minimized gate leakage and the weak thermal sensitivity

of the depletion capacitances. Finally, at elevated temperatures, non-ideal mechanisms, including threshold voltage degradation, enhanced gate leakage, and trap-assisted charge redistribution, progressively diminish the initial precharge voltage $V_{B,0}$ and discharge C_{BS} , limiting the bootstrap's effectiveness. These effects are analyzed in Section 4.

For ease of reference, Table 1 summarizes the most important symbols used mainly in this Section and in Sections 4 and 7.

Table 1. Main symbols used and their meaning.

Symbol	Meaning
V_{DD}, C_L	Supply voltage; load capacitance at the inverter output
Q_1 – Q_4, R_1, R_2	Pull-down HEMT; pull-up HEMT, precharge HEMT, storage HEMT of the BS stage; RTL pull-up resistor; degeneration resistor of the BS stage
$V_B, V_{B,0}$	Bootstrap node voltage (gate of Q_2); its precharge value at $V_{OUT} = 0$
$C_{BS}, C_{PAR}, \eta_{BS}$	Intrinsic bootstrap capacitance ($\approx C_{GS4} + C_{GD4}$); parasitic capacitance at the bootstrap node; coupling efficiency $C_{BS}/(C_{BS} + C_{PAR})$
$V_{TH}, \alpha_{VTH}, \Delta V_{TH}$	Threshold voltage; its temperature coefficient (negative); threshold shift $\Delta V_{TH}(T) = -\alpha_{VTH}(T - T_0) > 0$ for $T > T_0$
V_{OV}	Effective gate overdrive of Q_2 at the start of the pull-up, $V_{B,0} - V_{TH2}$
ΔV_{leak} (stat, dyn)	Voltage loss on the bootstrap node due to static (precharge) and dynamic (pull-up) leakage
$K(T), \beta$	Transconductance parameter (μC_g); $\beta = \frac{1}{2} K (W/L)_2$
γ, T_0	Mobility degradation exponent; reference temperature (293.15 K)
α, t_α	Output swing fraction V_{OUT}/V_{DD} ; corresponding rise time ($t_{0.5}$ = propagation delay, $t_{0.9} - t_{0.1} \approx t_{rise}$)
I_{SC}	Static short-circuit current of the gate (RTL or BS)
f_{SW}, D, t_{on}	Switching frequency, duty cycle, high-phase duration

2.4. Notes on the Adopted GaN-on-SOI Fabrication Process

Before delving into the analytical modeling and detailed performance analysis of the inverters, a brief overview of the adopted GaN-on-SOI technology is given, outlining the key fabrication processes and structural features relevant to device integration. The circuit topologies evaluated in this work are implemented on IMEC's 200-mm GaN-on-SOI technology platform, rated for 200 V. The fabrication process starts with the metal-organic chemical vapor deposition (MOCVD) of a GaN epitaxial stack on a silicon-on-insulator (SOI) substrate with a Si(111) top layer. Enhancement-mode (normally-off) operation is achieved by a p-GaN gate, implemented as a TiN/p-GaN stack. Vertical and lateral device isolation is obtained by combining the buried oxide, nitrogen implantation, and trenches etched through the GaN and Si layers down to the buried oxide. A local deep Si contact fixes the substrate potential, suppressing the back-gating effect [22].

3. Theoretical Analysis and Comparison

To establish an analytical framework for the monolithic GaN-on-SOI platform, this section defines the large-signal behavioral models governing both the conventional RTL inverter and the proposed intrinsic bootstrapped topology. For both configurations, the static short-circuit current (I_{SC}) and the dynamic low-to-high logical transition rise time (t_α) are derived to map the fundamental speed–power design space.

3.1. RTL Inverter Modeling

The standard RTL inverter relies on a passive pull-up network. Its static and dynamic performance metrics are therefore tightly constrained by the physical value of the pull-up resistor R_1 [20].

During the static pull-down phase, when the input is held high and the output settles to the logical low state ($V_{OUT} \approx 0$ V), a continuous short-circuit path exists from the supply voltage V_{DD} to ground through the active pull-down HEMT. Consequently, the maximum steady-state current drawn by the RTL gate is strictly limited by the passive pull-up resistor R_1

$$I_{SC,RTL} = \frac{V_{DD}}{R_1} \quad (4)$$

Next, the dynamic low-to-high transition (rise time) is analyzed. When the input abruptly transitions to a logical low state, the pull-down HEMT switches off and the load capacitance C_L (not depicted in Figure 1) charges toward V_{DD} through R_1 . Solving the classical first-order RC charging equation gives the time required for the output voltage to reach a specific logical transition fraction

$$\alpha = \frac{V_{OUT}}{V_{DD}} \quad (5)$$

The resulting α -rise time is [23]

$$t_{\alpha,RTL} = R_1 C_L \ln\left(\frac{1}{1-\alpha}\right) \quad (6)$$

It is worth noting that $t_{0.5}$ equals the standard *propagation delay*, τ_{PD} , while the standard 10% to 90% rise time is expressed by $t_{rise} = t_{0.9} - t_{0.1} \approx t_{0.9}$. Substituting R_1 from (4) into (6), we get

$$t_{\alpha,RTL} = \frac{V_{DD} C_L}{I_{SC,RTL}} \ln\left(\frac{1}{1-\alpha}\right) \quad (7)$$

which explicitly highlights the intrinsic speed–power tradeoff of RTL circuits: reducing the rise time for a given V_{DD} and C_L necessarily requires increasing $I_{SC,RTL}$, thereby increasing static power dissipation.

3.2. Bootstrapped Inverter Modeling

The proposed BS topology replaces the RTL passive pull-up network with an active one. At the end of the static precharge phase ($V_{OUT} = 0$ V), the bootstrap node is clamped to (1) and the nominal gate overdrive voltage available to the driver Q_2 is

$$V_{OV} = V_{B,0} - V_{TH2} \quad (8)$$

Assuming saturation-region operation of Q_2 , the short-circuit current is [24]

$$I_{SC,BS} = \frac{1}{2} K \left(\frac{W}{L}\right)_2 (V_{OV} - I_{SC,BS} R_2)^2 \quad (9)$$

where the transistor transconductance parameter K is defined by the product of the electron mobility μ and the gate capacitance per unit area C_g . Solving (9) for $I_{SC,BS}$ and R_2 yields

$$I_{SC,BS} = \frac{1 + 2\beta R_2 V_{OV} - \sqrt{1 + 4\beta R_2 V_{OV}}}{2\beta R_2^2} \quad (10)$$

$$R_2 = \frac{1}{I_{SC,BS}} \left(V_{OV} - \sqrt{\frac{I_{SC,BS}}{\beta}} \right) \quad (11)$$

where β is equal to $1/2 K (W/L)_2$. From (10), $I_{SC,BS}$ increases monotonically with V_{OV} .

During a low-to-high transition, the bootstrap capacitor C_{BS} dynamically elevates the bootstrap node in synchrony with the output voltage, thereby maintaining an approximately constant effective gate overdrive throughout the switching interval. Assuming hence a constant current behavior, the pull-up current is equal to $I_{SC,BS}$ and the generalized α -rise-time expression is

$$t_{\alpha,BS} = \frac{C_L \alpha V_{DD}}{I_{SC,BS}} = \frac{2\beta R_2^2 C_L \alpha V_{DD}}{1 + 2\beta R_2 V_{OV} - \sqrt{1 + 4\beta R_2 V_{OV}}} \quad (12)$$

3.3. Comparison

Taking the ratio of (7) and (12), we get

$$\frac{t_{\alpha,RTL}}{t_{\alpha,BS}} = \frac{I_{SC,BS}}{\alpha I_{SC,RTL}} \ln \left(\frac{1}{1 - \alpha} \right) \quad (13)$$

With both architectures fully modeled, their ideal performance can be compared through complementary design perspectives, i.e., under either constant I_{SC} or constant t_{α} . Assuming $I_{SC,RTL} = I_{SC,BS}$, (12) yields

$$\frac{t_{\alpha,RTL}}{t_{\alpha,BS}} = \frac{1}{\alpha} \ln \left(\frac{1}{1 - \alpha} \right) \quad (14)$$

The same expression at the second member is found by equating (13) to the unity, i.e., setting the same rise times $t_{\alpha,BS} = t_{\alpha,RTL}$, so that (14) expresses also the required short-circuit current ratio $I_{SC,RTL}/I_{SC,BS}$.

From (14), the performance advantage of the BS topology can be quantified for two practically relevant values of α . For $\alpha = 0.5$, giving τ_{PD} , the ratio $t_{0.5,RTL}/t_{0.5,BS} = 2 \ln 2 \approx 1.39$, indicating a 39% longer τ_{PD} for the RTL inverter. For $\alpha = 0.9$, corresponding to the standard 10–90% rise time, the ratio yields $t_{0.9,RTL}/t_{0.9,BS} = \ln 10 / 0.9 \approx 2.56$, meaning that the RTL t_{rise} is $2.56 \times$ larger (BS topology achieves a 61% reduction).

4. Temperature Effects

To fully capture the dynamic behavior with temperature and specifically across standard industrial and automotive temperature ranges (-40 °C to 150 °C), it is necessary to theoretically model the thermal degradation mechanisms impacting both the RTL and BS topologies.

4.1. RTL Inverter

For the RTL inverter, the pull-up transient is governed by a purely resistive 2DEG load, R_1 . Its slowdown at elevated temperatures is directly tied to the temperature-dependent electron mobility. Indeed, phonon scattering within the AlGaIn/GaN heterostructure induces a severe reduction in the 2DEG carrier mobility and the resistance scales according to

$$R(T) = R(T_0) \left(\frac{T}{T_0} \right)^{\gamma} \quad (15)$$

where T is the absolute temperature in Kelvin, T_0 is the reference ambient temperature, and γ is the mobility degradation exponent, with γ typically ranging between 1.5 and 2.5 [25–29]. By substituting (15) into the RTL α -rise time (6), it becomes evident that $t_{\alpha,RTL}$

shares the exact temperature dependence as R_1 , given that the load capacitance C_L remains virtually temperature-independent over the operating range

$$t_{\alpha,RTL}(T) = t_{\alpha,RTL}(T_0) \left(\frac{T}{T_0} \right)^\gamma \quad (16)$$

Therefore, $t_{\alpha,RTL}$ increases monotonically with temperature, following the same power-law scaling as $R_1(T)$.

4.2. Bootstrapped Inverter

Increasing temperature affects the GaN device parameters through threshold-voltage reduction (V_{TH}), mobility-driven degradation of the conduction parameter (K), and the exponential increase of parasitic leakage currents (I_{leak}).

The thermal behavior of the bootstrap node voltage $V_B(t, T)$ must be formulated in order to accurately capture this dynamic performance degradation. To evaluate $V_{B,0}(T)$, we consider first the steady-state pull-down phase ($V_{OUT} = 0$). Under this condition, a static equilibrium is established at the bootstrap node, where the current supplied by Q_3 , I_{D3} , must exactly balance the static leakage current $I_{leak,stat}$ draining from the node toward ground

$$I_{D3} = I_{leak,stat} \quad \text{for } V_{OUT} = 0 \quad (17)$$

In integrated GaN-on-Si smart power platforms, $I_{leak,stat}$ mainly originates from defect- and interface-assisted transport mechanisms within the GaN HEMT structure. Since these leakage paths are thermally activated, $I_{leak,stat}$ increases exponentially with temperature. Given the small current levels required to sustain equilibrium, Q_3 is forced to operate in its subthreshold conduction regime and the steady-state precharge voltage $V_{B,0}(T)$ is derived as a modification of (1)

$$\begin{aligned} V_{B,0}(T) &= V_{DD} - V_{TH3}(T) - \Delta V_{leak,stat}(T) \\ &= V_{B,0} + \Delta V_{TH3}(T) - \Delta V_{leak,stat}(T) \end{aligned} \quad (18)$$

where [30]

$$\Delta V_{leak,stat}(T) = n_{sub} V_T \ln \left(\frac{I_{leak,stat}(T)}{I_0(T)} \right) \quad (19)$$

in which $V_T = k_B T / q$ is the usual thermal voltage, n_{sub} is the subthreshold ideality factor, and $I_0(T)$ is the drain current of Q_3 at $V_{GS} = V_{TH3}$, which scales exponentially with temperature due to the thermal activation of traps. $\Delta V_{leak,stat} < 0$ when $I_{leak,stat} < I_0$ (low temperature) and > 0 otherwise.

The enhancement-mode p-GaN gate technology used in this work exhibits a threshold-voltage temperature variation that is well approximated by the linear model of (20), with $\alpha_{VTH} = -3 \text{ mV}/^\circ\text{C}$. This value, adopted for the analytical model, is the nominal coefficient extracted from the process design kit (PDK) at 27°C , typical corner.

$$V_{TH3}(T) = V_{TH3}(T_0) + \alpha_{VTH}(T - T_0) = V_{TH3}(T_0) - \Delta V_{TH3}(T) \quad (20)$$

where $\Delta V_{TH3}(T) = |\alpha_{VTH}|(T - T_0) > 0$ is positive for $T > T_0$. Consequently, the exponential growth of the static leakage current dominates the threshold voltage shift, leading to a progressive reduction of $V_{B,0}(T)$ with rising temperature.

During the pull-up transition, the charge stored on the bootstrap capacitance undergoes an additional transient depletion. This dynamic voltage loss, $\Delta V_{leak,dyn}(t, T)$,

is modeled by integrating the time-varying leakage current $I_{\text{leak,dyn}}(t, T)$ over the active switching interval $(0, t_{\text{on}})$

$$\Delta V_{\text{leak,dyn}}(t, T) = \frac{1}{C_{\text{BS}}} \int_0^{t_{\text{on}}} I_{\text{leak,dyn}}(t, T) d\tau \frac{\langle I_{\text{leak,dyn}} \rangle D}{C_{\text{BS}} f_{\text{SW}}} \quad (21)$$

where D is the switching duty cycle, f_{SW} is the operating switching frequency, and $\langle I_{\text{leak,dyn}} \rangle$ is the average value over the effective on-time interval $t_{\text{on}} = D/f_{\text{SW}}$.

Therefore, in the pull-up phase, (2) can be reformulated as

$$\begin{aligned} V_{\text{B}}(t, T) &= V_{\text{B},0}(T) - \Delta V_{\text{leak,dyn}}(t, T) + \eta_{\text{BS}} V_{\text{OUT}}(t) \\ &= V_{\text{B},0} + \Delta V_{\text{TH3}}(T) - \Delta V_{\text{leak}}(T) + \eta_{\text{BS}} V_{\text{OUT}}(t) \end{aligned} \quad (22)$$

where $\Delta V_{\text{leak}}(t, T) = \Delta V_{\text{leak,stat}}(T) + \Delta V_{\text{leak,dyn}}(t, T)$ is the compound static and dynamic leakage effect usually dominated by $\Delta V_{\text{leak,stat}}(T)$ for the ordinary values of f_{SW} . Moreover, referring to the structural parameters of the GaN platform, η_{BS} can be safely considered virtually constant across the entire operating temperature range, because the capacitive divider ratio is dictated by intrinsic gate capacitances and depletion-layer capacitances, which can be treated as constant and exhibit negligible temperature sensitivity.

Defining a tolerable dynamic overdrive loss ΔV_{max} as a fraction of the available overdrive margin at the worst-case operating temperature, f_{SW} becomes

$$f_{\text{SW,min}} = \frac{\langle I_{\text{leak,dyn}} \rangle D}{C_{\text{BS}} \Delta V_{\text{max}}} \quad (23)$$

This estimate indicates that switching frequencies above approximately 5 kHz are sufficient to limit the bootstrap overdrive degradation.

Operation at lower f_{SW} , or extended static phases, would require either increasing C_{BS} by scaling up Q_4 or reducing R_2 to widen the overdrive margin at the cost of higher static power. A quantitative estimate of f_{SW} is provided in Section 7.

Evaluating the reduction of the current drive capability of the pull-up HEMT Q_2 , while accounting for the voltage drop across R_2 , involves a complex implicit relationship. For the sake of analytical clarity, we adopt a simplified approach by neglecting this voltage drop. While this constitutes a simplified first-order model, simulation results confirm that Q_2 remains predominantly in saturation throughout the majority of the pull-up transient, validating this assumption within the operating range considered.

During the low-to-high output transition, the gate overdrive controlling Q_2 is

$$\begin{aligned} V_{\text{OV}}(t, T) &\approx V_{\text{B}}(t, T) - V_{\text{OUT}}(t) - V_{\text{TH2}}(T) \\ &= V_{\text{B},0}(T) - V_{\text{TH2}}(T_0) + (\eta_{\text{BS}} - 1)V_{\text{OUT}}(t) - \Delta V_{\text{leak}}(t, T) + \Delta V_{\text{TH2}}(T) + \Delta V_{\text{TH3}}(T) \\ &\approx V_{\text{OV}}(T_0) - \Delta V_{\text{leak}}(t, T) + 2\Delta V_{\text{TH}}(T) \end{aligned} \quad (24)$$

where $\Delta V_{\text{TH2}}(T) = \Delta V_{\text{TH3}}(T) = |\alpha_{V_{\text{TH}}}|(T - T_0)$ has been assumed.

Moreover, under the approximation $\eta_{\text{BS}} \approx 1$, (supported by the value $\eta_{\text{BS}} \approx 0.86 - 0.87$ reported in Section 5.3), the term $(\eta_{\text{BS}} - 1)V_{\text{OUT}}(t) \approx 0$. Consequently, the time dependence in V_{OV} disappears, provided that the leakage effect is dominated by $\Delta V_{\text{leak,stat}}(T)$.

Considering the degradation of the transistor transconductance parameter $K(T)$, which follows the inverse power law

$$K(T) = K(T_0) \left(\frac{T}{T_0} \right)^{-\gamma} \quad (25)$$

with γ defined already in (15), the rise time model from (12) is

$$\begin{aligned} t_{\alpha,BS}(T) &= \frac{2\beta(T_0)R_2^2(T_0)C_L\alpha V_{DD}\left(\frac{T}{T_0}\right)^\gamma}{1+2\beta(T_0)R_2(T_0)V_{OV}(T)-\sqrt{1+4\beta(T_0)R_2(T_0)V_{OV}(T)}} \\ &= t_{\alpha,BS}(T_0)\left(\frac{T}{T_0}\right)^\gamma \frac{f(V_{OV}(T_0))}{f(V_{OV}(T))} \end{aligned} \quad (26)$$

where

$$f(V_{OV}) = 1 + 2\beta(T_0)R_2(T_0)V_{OV} - \sqrt{1 + 4\beta(T_0)R_2(T_0)V_{OV}} \quad (27)$$

Comparing (16) and (26), the BS inverter exhibits an additional non-linear thermal penalty, other than factor $(T/T_0)^\gamma$, due to the overdrive compression factor $f(V_{OV}(T_0))/f(V_{OV}(T))$. As temperature increases, $V_{OV}(T)$ is progressively reduced by both the static and dynamic leakage contribution ΔV_{leak} , causing a stronger degradation than in the RTL topology. The V_{OV} reduction with temperature has several effects, most notably the reduction of $I_{SC,BS}$ from (9). Besides, a thermal crossover point T_{cross} may appear where $t_{\alpha,BS} = t_{\alpha,RTL}$, limiting the BS topology advantage. To increase T_{cross} , the degeneration resistance R_2 can be reduced to enlarge the room-temperature overdrive margin (also increasing $(W/L)_2$), trading higher static power for improved thermal robustness.

Finally, (26) can be analytically inverted, enabling direct extraction of the effective bootstrap overdrive voltage $V_{OV}(T)$ from the experimentally measured transient response. This will allow quantitative evaluation of the thermally induced bootstrap degradation mechanisms.

$$V_{OV}(T) = \frac{f(V_{OV}(T_0))\left(\frac{T}{T_0}\right)^\gamma \frac{t_{\alpha,BS}(T_0)}{t_{\alpha,BS}(T)} + \sqrt{2f(V_{OV}(T_0))\left(\frac{T}{T_0}\right)^\gamma \frac{t_{\alpha,BS}(T_0)}{t_{\alpha,BS}(T)}}}{2\beta(T_0)R_2(T_0)} \quad (28)$$

5. Simulation Results

To validate the analytical predictions and to quantify the performance improvement, circuit level simulations were carried out using the low-voltage device models provided by the 200-V GaN-on-SOI technology.

The process design kit (PDK) was supplied by IMEC and accessed through EURO-PRACTICE. The simulations included parasitic capacitances and temperature-dependent device parameters as defined in the PDK. The supply voltage was set to 6 V. Table 2 summarizes the main components' design parameters optimized for an inverter load C_L of 1 pF. Q_{1-3} are minimum-sized devices. Q_4 has an $8\times$ width. Resistance R_1 is set to limit the RTL current to 375 μ A. R_2 is calculated from (11) and (8) using $V_{TH} = 1.3$ V, $K = 48.5$ μ A/V² to provide similar short-circuit current.

Table 2. Component Parameters.

	W/L (μ m/ μ m)		Value (k Ω)
Q_{1-2-3}	6/1.3	R_1	16
Q_4	48/1.3	R_2	4.2

The inverter layouts, superimposed to the chip micrograph, are shown in Figure 2. The area of the BS and RTL inverters are about 1720 μ m² and 1580 μ m², respectively.

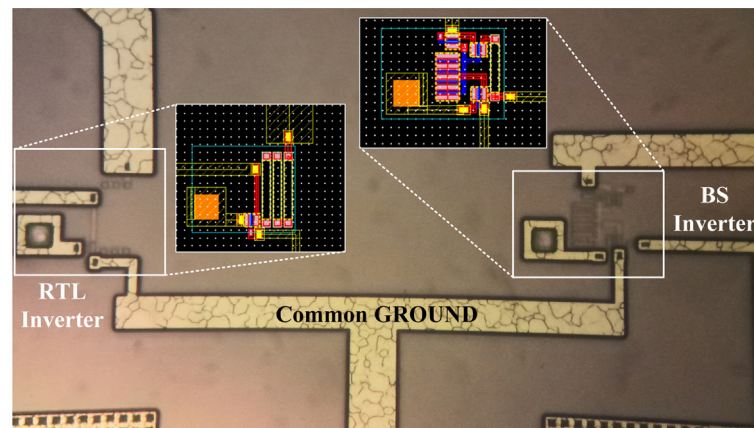


Figure 2. Layout details superimposed to the die photograph of the implemented GaN-on-SOI integrated circuits. The area of the BS and RTL inverters are about $1720 \mu\text{m}^2$ and $1580 \mu\text{m}^2$, respectively.

5.1. Quasi-Static Behavior

Figure 3 illustrates the simulated voltage transfer characteristics (VTCs) of both the conventional RTL inverter and the proposed BS inverter at 27°C . The BS inverter exhibits a significantly steeper transition compared to the RTL topology. This reflects the increased effective transconductance resulting from the bootstrap-enhanced gate overdrive of the pull-up device. As a consequence, the BS inverter achieves a higher small-signal gain, $|dV_{\text{OUT}}/dV_{\text{IN}}|_{\text{max}}$, and improved overall noise margin with a significantly enhanced low noise margin, NM_L .

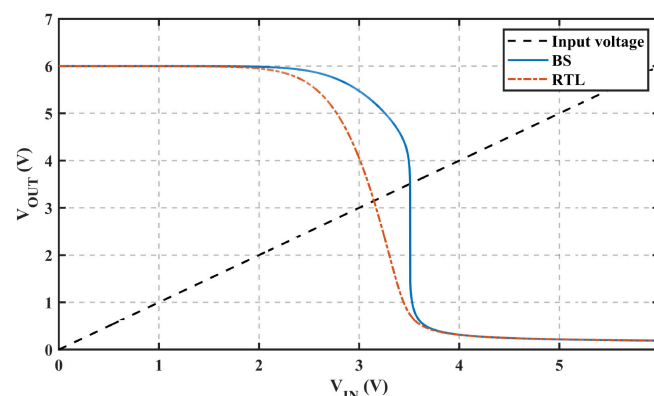


Figure 3. VTC of BS and RTL inverter. Simulated voltage transfer characteristics (VTC) of the proposed BS inverter compared to the reference RTL inverter at 27°C and $C_\text{L} = 1 \text{ pF}$. The BS configuration demonstrates a significantly steeper transition region and improved noise margins, resulting from the enhanced effective gate overdrive provided by the intrinsic bootstrap mechanism. The input voltage sweep is represented by the dashed line to identify the switching thresholds.

The estimated DC performance parameters at different temperatures are summarized in Table 3. The BS configuration offers superior static performance over the standard RTL inverter in terms of better overall noise margins, and slightly higher stability of threshold voltage against thermal drift. This confirms that the bootstrap mechanism effectively enhances DC switching sharpness without introducing additional static current consumption.

Table 3. Summary of simulated static performance with $C_L = 1$ pF.

Temperature (°C)		−40	0	27	80	120	150
Switching Threshold (V)	BS	3.54	3.52	3.5	3.48	3.47	3.46
	RTL	3.06	3.11	3.15	3.22	3.27	3.31
NM_H (V)	BS	2.27	2.28	2.30	2.32	2.34	2.35
	RTL	2.45	2.38	2.34	2.27	2.21	2.17
NM_L (V)	BS	2.47	2.58	2.65	2.76	2.84	2.9
	RTL	2.05	2.15	2.21	2.32	2.39	2.45
I_{SC} (μA)	BS	663	460	360	223	156	119
	RTL	562	433	364	264	211	180

5.2. Dynamic Behavior

The dynamic response of the two inverter architectures was evaluated by applying a 6-V 4-MHz step input and analyzing the output transitions. The response evaluated at 27 °C and with $C_L = 1$ pF is illustrated in Figure 4. For the BS (RTL) inverter, the extracted values of rise time, propagation delay (τ_{PD}), and power-delay product (PDP) are, respectively, 17.65 ns (34.39 ns), 9.96 ns (11.73 ns), and 10.51 pJ (13.22 pJ). The same figure confirms that Q_2 remains predominantly in saturation during the major part of the pull-up transient.

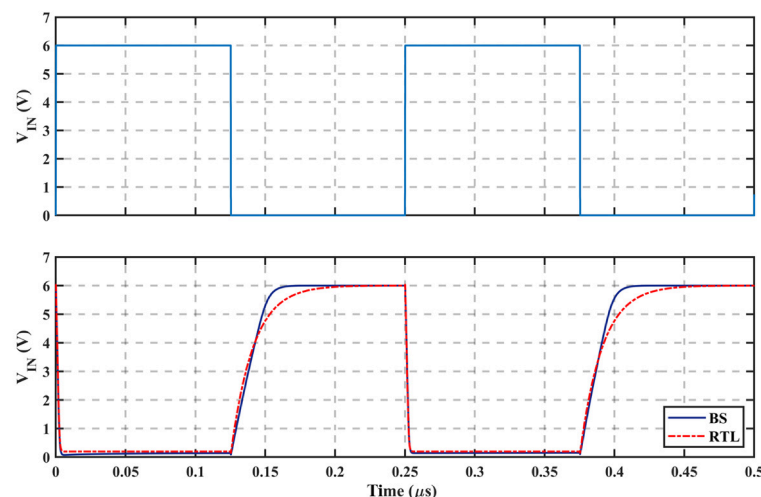
**Figure 4.** Simulated transient response of the BS and RTL inverters at 27 °C with $C_L = 1$ pF, showing quasi-constant-current and RC-limited charging, respectively.

Table 4 summarizes the dynamic performance parameters of the BS and RTL inverter topologies at 27 °C as a function of load capacitance. For both configurations, the timing and energy metrics exhibit a strong, direct proportionality to C_L across the multi-picofarad range. Specifically, scaling C_L tenfold from 1 pF to 10 pF yields a proportional increase in delay and energy metrics (as given by (6) and (12)). However, this strict proportionality deviates in the sub-picofarad regime, where a tenfold increase in C_L results in less than a fivefold increase in propagation delay. This non-linearity is attributed to the dominant impact of the inverters' intrinsic parasitic capacitances, which establish a baseline delay floor when the external load is negligible. For $C_L > 0.1$ pF, the BS architecture demonstrates a lower PDP metric. The significant reduction in t_{rise} observed for the BS inverter aligns with the analytical models presented in (6) and (12), confirming that the performance improvement stems directly from the modified pull-up mechanism. In contrast, t_{fall} remains comparable between the two designs, as the pull-down network is unchanged.

Table 4. Summary of simulated Dynamic Performance at 27 °C for different load capacitances ($C_L = 0.1, 1, 10$, and 30 pF).

C_L (pF)	t_{rise} (ns)		t_{fall} (ns)		τ_{PD} (ns)		PDP (pJ)	
	BS	RTL	BS	RTL	BS	RTL	BS	RTL
0.1	3.21	3.99	0.36	0.27	2.09	1.54	1.81	1.75
1	17.65	34.39	2.53	2.34	9.96	11.73	10.51	13.22
10	160.5	338.3	24.07	23.04	87.89	113.9	96.63	128.2
30	482	998	71.84	68.79	265.0	343.1	307.9	408.3

For $C_L = 0.1$ pF, the propagation delay of the BS inverter slightly exceeds that of RTL, as the intrinsic parasitic capacitances of the additional transistors Q_2 – Q_4 in the bootstrap network dominate over the external load. This regime is below the target operating point of the design ($C_L > 0.1$ pF)

5.3. Temperature-Dependent Dynamic Behavior

To analyze the temperature-dependent dynamic behavior of the proposed inverter, we simulated the step responses of the RTL and BS topologies across a temperature range from -40 °C to 150 °C (Figure 5).

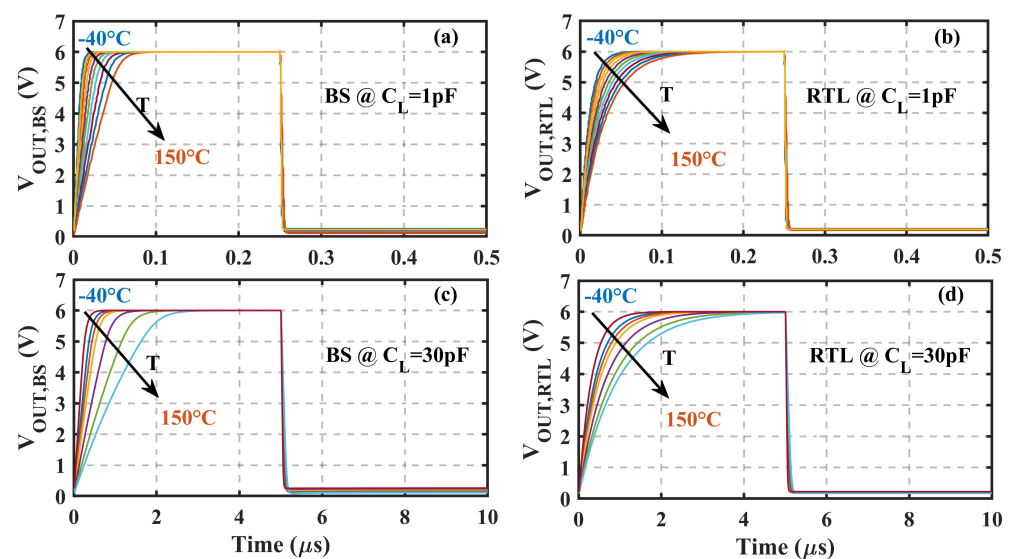


Figure 5. Simulated transient output voltage profiles for: the BS inverter for (a) $C_L = 1$ pF and (c) $C_L = 30$ pF and the RTL inverter for (b) $C_L = 1$ pF and (d) $C_L = 30$ pF, across the operating temperature range $[-40, -20, 0, 20, 40, 60, 80, 100, 120, 150]$ °C. The results demonstrate the better performance of the BS inverter and the degradation with temperature.

The responses of the BS and RTL inverters under a 1-pF load are shown in Figure 5a and Figure 5b, respectively, while the responses under a 30-pF load are shown in Figure 5c,d. The first case is representative of an inverter driving an on-chip load, whereas the second emulates an off-chip loading condition with an estimated capacitive load of 30 pF. The improved performance of the BS inverter is evident.

Figures 6 and 7 present the extracted rise time, fall time, propagation delay, and power-delay product of both the RTL and BS inverters as a function of temperature for load capacitances of 1 pF and 30 pF, respectively.

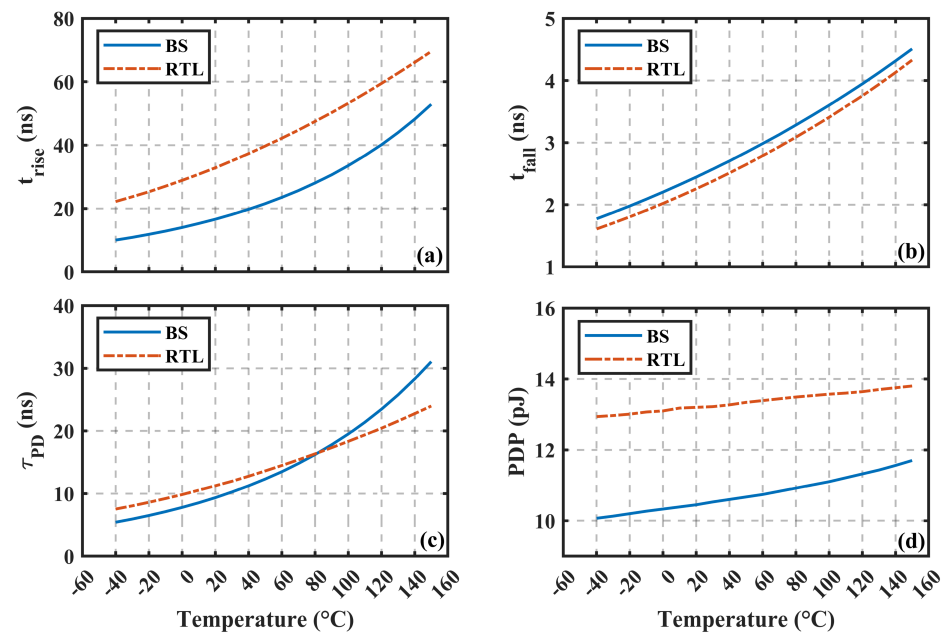


Figure 6. Simulated temperature-dependent dynamic performance metrics for the BS and RTL inverters with a load capacitance $C_L = 1$ pF: (a) rise time, (b) fall time, (c) propagation delay, and (d) power-delay product. The results highlight the crossover point where the leakage-induced overdrive collapse in the BS inverter balances its τ_{PD} advantage over the RTL reference.

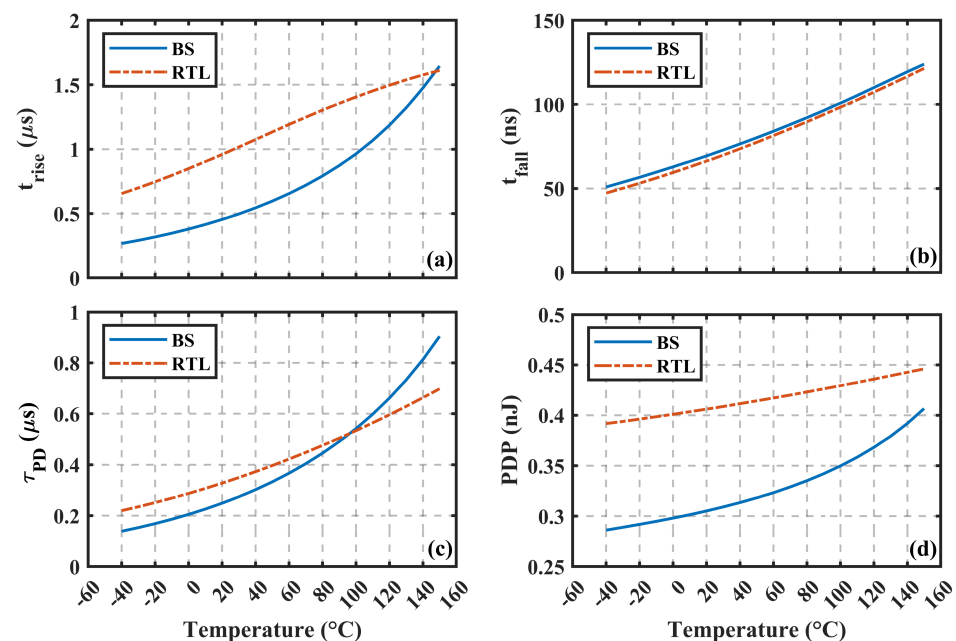


Figure 7. Simulated temperature-dependent dynamic performance metrics for the BS and RTL inverters with a load capacitance $C_L = 30$ pF: (a) rise time, (b) fall time, (c) propagation delay, and (d) power-delay product. With this capacitive load, the BS inverter performance (and specifically t_{rise}) converges to the RTL baseline at elevated temperatures.

As anticipated in Section 4, the dynamic parameters of both topologies deteriorate with increasing temperature, and this is further exacerbated by large capacitive loads. Eventually, a crossover point is reached, beyond which the t_{rise} (and τ_{PD}) of the BS inverter exceed those of the RTL implementation, as shown in Figure 6c for τ_{PD} and in Figure 7a and Figure 7c for t_{rise} and τ_{PD} , respectively.

The transient behavior of the bootstrapped node voltage, V_B , was also simulated for three temperatures: $-40\text{ }^{\circ}\text{C}$, $27\text{ }^{\circ}\text{C}$, and $120\text{ }^{\circ}\text{C}$, as shown in Figure 8. The dynamic response can be divided into three distinct operational phases: the initial precharge, the active bootstrap coupling, and the final decay settling.

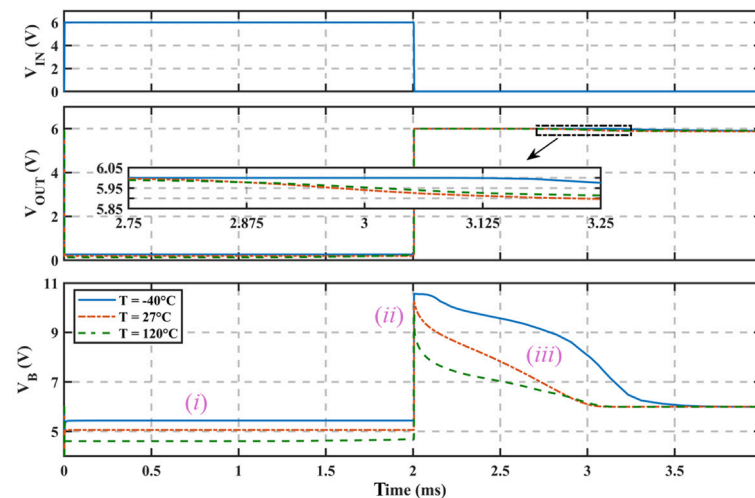


Figure 8. Simulated transient evolution of the bootstrap node voltage, V_B , and output voltage, V_{OUT} , during a low-to-high transition at temperatures of $-40\text{ }^{\circ}\text{C}$, $27\text{ }^{\circ}\text{C}$, and $120\text{ }^{\circ}\text{C}$. Distinct operational phases are highlighted: (i) stable precharge level, (ii) active bootstrap coupling with V_B increase, and (iii) transient decay and settling. The performance degradation at elevated temperatures is clearly visible in both the attenuated peak bootstrap voltage and the slower final settling profile caused by thermally activated leakage paths. The inset focuses on the final portion of the transient for V_{OUT} .

- (i) Initial Steady-State ($t < 2\text{ ms}$). Before the input transition, the output is low, and V_B settles to an initial precharge DC level, $V_{B,0}$, dictated by the pull-up diode-connected device (Q_3). Notably, this precharge voltage exhibits a significant temperature dependence, stabilizing at a lower value at $120\text{ }^{\circ}\text{C}$ (approximately 4.61 V) compared to $-40\text{ }^{\circ}\text{C}$ (approximately 5.44 V). This behavior is driven by the dynamic current balance at the node. At elevated temperatures, the exponentially higher subthreshold and junction leakage currents through the connected devices (Q_4 and Q_2) toward ground require Q_3 to source more current. Consequently, the gate-to-source voltage of Q_3 must increase, resulting in a larger voltage drop across the device and a lower $V_{B,0}$. The simulated values are collected in Table 5.

Table 5. Summary of simulated Precharge Voltage and Bootstrap Coupling Efficiency with $C_L = 1\text{ pF}$.

Temperature ($^{\circ}\text{C}$)		−40	0	27	80	120	150
Param.	$V_{B,0}\text{ (V)}$	5.44	5.2	5.06	4.79	4.61	4.48
	η_{BS}	0.856	0.863	0.866	0.870	0.871	0.871

- (ii) Bootstrap Peak ($t = 2\text{ ms}$). When the input switches low, the output node begins its rising transition. The capacitive coupling through Q_4 rapidly pushes V_B well above the supply voltage. The maximum peak voltage is highest at $-40\text{ }^{\circ}\text{C}$ (over 10.5 V). At $120\text{ }^{\circ}\text{C}$, the peak is visibly attenuated (around 9 V) due to the combination of the lower initial precharge level and instantaneous charge sharing exacerbated by high-temperature leakage. The extracted coupling efficiency, η_{BS} , is nearly constant to 0.86 , as summarized in the lower row of Table 5.

- (iii) Transient Decay and Settling ($t > 2$ ms). Following the peak, V_B begins to discharge toward its final steady-state high level (6.0 V) as the output completes its transition. The thermal impact on this decay profile is highly pronounced. At -40 °C, the superior driving capability of the circuit allows the node to maintain a higher potential longer, followed by a sharp and abrupt drop once the output fully completes its transition.

Conversely, at 120 °C, the peak drops quickly, but the subsequent transient tail is significantly slower and more gradual. This slower final settling at high temperatures occurs because the reduced carrier mobility and shifted threshold voltages degrade the overall driving current of the pull-up network, thereby slowing down the final voltage stabilization of the circuit.

Observe that at 120 °C, thermally accelerated leakage discharges the bootstrap node V_B from its peak boosted voltage over time. Taking into account the temperature dependence of the threshold voltage ($\alpha_{V_{TH}} = -3$ mV/°C), transistor Q_2 requires $V_B > V_{DD} + V_{TH2}$ (120 °C) ≈ 7.0 V to remain fully turned on and maintain its output state. As shown in Figure 8, V_B takes approximately $t_{collapse} \approx 0.5$ ms to decay to this 7.0 V threshold at 120 °C.

To guarantee that the circuit retains a substantial fraction of its bootstrap overdrive enhancement, we define a maximum allowable active-phase duration with a $5\times$ safety margin: $t_{on,max} = 0.2 \cdot t_{collapse} \approx 0.1$ ms at 120 °C. Assuming a 50% duty cycle ($D = 0.5$), this operational limit sets the minimum required switching frequency to: $f_{SW,min} = D/t_{on,max} \approx 0.5/0.1$ ms = 5 kHz.

Operating above 5 kHz ensures that V_B is refreshed long before thermal leakage can degrade the output rise time.

6. Measurement Results and Comparison

The proposed BS inverter and the reference RTL inverter were experimentally validated using a fabricated prototype die. The die was housed in a 28-lead side-brazed ceramic package and wire-bonded to a custom test board. Because a single prototype die was characterized in this work, statistical process variation analysis was not performed and remains a topic for future multi-sample studies.

An input signal was applied to the gates via a function generator, while the resulting output waveforms were captured using a high-impedance oscilloscope probe. In this off-chip experimental setup, the effective load capacitance at the output node is determined by the oscilloscope probe capacitance (11.0 pF, from the probe specifications), together with the parasitics of the ceramic package and of the printed circuit board (16.2 pF, measured). The resulting total capacitance, about 27.2 pF, is assumed to be identical for both inverter topologies and is consistent with the value of 27 pF extracted in Section 7 from the RTL rise time using the independently verified value $R_1 = 16$ k Ω . Note that the extraction of γ and $V_{OV}(T)$ in Section 7 relies only on the ratios of rise times at different temperatures, in which C_L cancels out. It therefore does not depend on the absolute value of C_L .

It should be noted that while this off-chip loading setup intentionally prioritizes comparative validation between topologies rather than intrinsic gate delays, in practical fully integrated monolithic applications C_L would be governed solely by local interconnects (typically $C_L \leq 1$ pF), enabling significantly faster intrinsic switching speeds as modeled in Section 5.

Figure 9 reports the measured VTCs of the RTL and BS inverters at room temperature. The VTCs were obtained by sweeping the input voltage with a 10-kHz ramp spanning 6 V, ensuring sufficient settling time at each bias point to capture steady-state behavior. As observed, the BS inverter exhibits a significantly steeper transition region compared to the RTL counterpart. When evaluated around the switching thresholds, that is measured at approximately 2.7 V and 2.9 V for the BS and RTL inverters, respectively, the small-signal

gain of the BS inverter is approximately three times higher than that of the RTL topology. This increased gain results in improved noise margins. Specifically, NM_H increases from 2.5 V (RTL) to 3.0 V (BS), and NM_L improves from 2.0 V to 2.4 V, an improvement of about 20% in both cases. These values are extracted via graphical evaluation from the experimental curves and are in reasonable agreement with the theoretical boundaries.

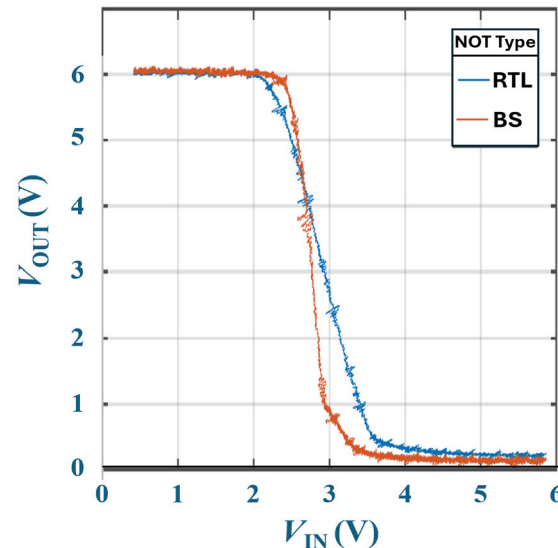


Figure 9. Measured voltage transfer characteristics (VTCs) of the BS and RTL inverters at room temperature. A 6-V 10-kHz ramp input is applied.

Note that the measured switching thresholds exhibit a downshift compared to the PDK simulations (≈ 3.5 V and ≈ 3.15 V, respectively). This shift is attributed to standard process-induced variations in the p-GaN gate work function and the V_{TH} of the fabricated E-mode HEMTs relative to nominal PDK models.

The measured I_{SC} at room temperature for both the RTL and BS inverters is approximately 370 μ A, in agreement with the design specifications and simulations. Since $I_{SC,RTL} = V_{DD}/R_1$ from (4), this provides an independent experimental confirmation of the nominal resistance value $R_1 \approx 16$ k Ω .

The measured transient responses of the RTL and BS inverters at 20 $^{\circ}$ C are shown in Figure 10. To facilitate a direct comparison and enhance graphical readability, the RTL characteristic has been shifted by 2 V for display purposes only, as the two curves would otherwise largely overlap. For both circuits, the falling transition is dominated by the pull-down transistor Q_1 and exhibits comparable behavior. During the low-to-high transition, the RTL inverter shows the characteristic saturating-exponential profile of RC-limited charging. In contrast, the BS inverter exhibits an approximately linear voltage ramp, indicating quasi-constant current charging enabled by the bootstrap mechanism. The linear ramp extends over more than 90% of the output excursion, consistent with Q_2 operating predominantly in saturation throughout the transition, as assumed in Section 2.3. Under the same loading conditions and comparable static current, the measured rise time is about 669 ns for the BS and 1.0 μ s for the RTL inverter. The BS inverter achieves a reduction in rise time of more than 30% relative to RTL.

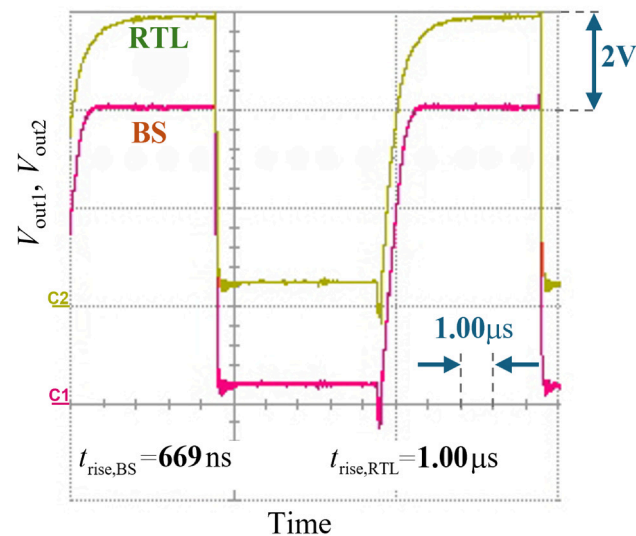


Figure 10. Measured transient response of the BS and RTL inverters at 20 °C for identical loading conditions ($C_L \approx 27$ pF). RTL trace has been vertically shifted by +2 V relative to BS for better readability.

The performance of both inverter topologies was also characterized across a temperature range from -40 °C to 150 °C. For the electro-thermal measurements, the test assembly was placed inside a temperature-controlled thermal chamber operating at atmospheric pressure, as illustrated in Figure 11. Prior to capturing the electrical waveforms at each thermal step, a 15-min soak time was observed to guarantee complete thermal equilibration of the package and substrate. Given the low static power dissipation of the circuits (≈ 2 mW at $V_{DD} = 6$ V), device self-heating effects are negligible.



Figure 11. Thermal chamber and instrumentation used for the measurements from -40 °C to 150 °C.

Finally, Table 6 provides a comparative analysis of GaN-based inverter solutions. The proposed solution is the only one exclusively using E-mode HEMTs, whereas [5,28,31] use E/D-mode structures. While the proposed work and [28] utilize higher supply voltages to achieve wider logic swings and robust noise margins, the designs in [5] demonstrate the scalability of the DCFL architecture at lower voltages, though at the expense of a reduced

output swing. It should be noted that the proposed inverter was characterized under off-chip conditions with a capacitive load of about 27 pF, and the one reported in [28] with a capacitive load of several pF, whereas the logic gate in [5] presents intrinsic stage delays. Therefore, the rise times are not directly comparable, because they refer to different loads. A final consideration concerns the aspect ratio of the driver and load HEMT, in which our solution compares favorably with a unitary $(W/L)_{\text{Driver}}$ to $(W/L)_{\text{Load}}$ ratio.

Table 6. Performance Comparison of GaN Inverters. The rise times are not directly comparable because they refer to different loads.

Ref./Year	This Work		[31]/2021	[28]/2020	[5]/2006
Technology	GaN-on-SOI		AlGaN/GaN	AlGaN/GaN	AlGaN/GaN
Logic Style	BS	RTL	DCFL (E/D)	DCFL (E/D)	DCFL (E/D)
V_{DD} (V)	6	6	10	3	2.5
Bootstrap Cap.	Intrinsic	None	None	None	None
Logic Swing (% of V_{DD})	95	96	98	97	69
$NM_{\text{H}}/NM_{\text{L}}$ (V/V)	2.30/2.65 ^(a) 3.0/2.4 ^(b)	2.34/2.21 ^(a) 2.5/2.0 ^(b)	7.20/1.70	1.67/0.78	1.13/0.53
t_{rise} (10–90%) (ns)	17.65 ^(a) 669 ^(b)	34.39 ^(a) 1.0×10^3 ^(b)	3.29×10^3 ^(c)	$>1.0 \times 10^3$	N.A.
$(W/L)_{\text{Driver}}/(W/L)_{\text{Load}}$	1	N.A.	40	15	10

^(a) Simulated with 1-pF load; ^(b) Measured off-chip at ambient temperature; ^(c) Measured off-chip.

The transient performance of both inverter topologies is shown in Figure 12. For the RTL inverter, a monotonic increase in the rise time from 722 ns at -40°C to 1.97 μs at 150°C is observed. The shape of the transient remains consistent throughout the entire thermal range. At low-to-medium temperatures (-40°C to 80°C), the BS inverter shows a significantly steeper slope than RTL, with $t_{\text{rise,BS}} < t_{\text{rise,RTL}}$. At -40°C , the BS rise time is 448 ns. However, the BS circuit exhibits a more pronounced sensitivity to thermal variations. As the temperature increases, the advantage in transition speed progressively diminishes, which is consistent with the simulated behavior for a 30-pF load, as shown in Figure 7a. At 120°C , the BS rise time (1.80 μs) already slightly exceeds that of the RTL (1.73 μs).

It is worth noting that at 150°C , the output of the BS inverter does not reach V_{DD} within the high phase of the applied pulse (i.e., in 4.5 μs), as seen in Figure 12b. This behavior is consistent with the strong reduction of the pull-up drive at this temperature. The bootstrap overdrive extracted in Section 7 decreases from 3.40 V at 20°C to 2.23 V at 150°C and the simulated static pull-up current drops from 375 μA to 119 μA , so that the charging of the load becomes considerably slower. However, a detailed explanation of the incomplete output swing cannot be given at present. The leakage currents of the bootstrap node were not measured directly; the overdrive reduction is obtained through a model-based extraction that accounts globally for all effects not included in the model. Further investigations, including direct measurements of the leakage currents of Q_2 – Q_4 versus temperature, probing of the bootstrap node, and measurements with longer high-phase durations, are planned to clarify this point.

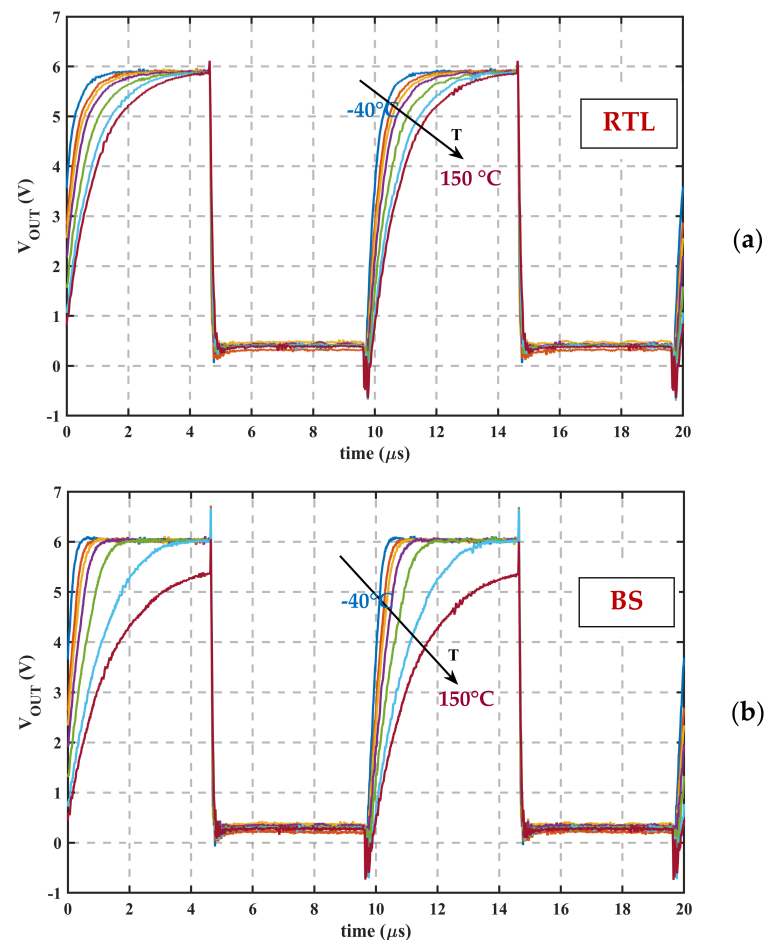


Figure 12. Measured transient response of the RTL (a) and BS (b) inverters over the temperature range $[-40, 0, 20, 40, 80, 120, 150]^\circ\text{C}$, with estimated $C_L = 27\text{ pF}$.

7. Parameter Extraction and Discussion

With the theoretical frameworks established in Sections 3 and 4 and the experimental characterization detailed in Section 6, the underlying physical and electro-thermal parameters driving the circuit performance degradation can be quantitatively decoupled and extracted. For this analysis, R_1 and R_2 are held at their nominal values and C_L is fixed at 27 pF. Indeed, the measured rise time of the RTL inverter can be exploited to extract the effective load capacitance. Given that $t_{\text{rise,RTL}} = R_1 C_L \ln(10)$, from (6), the extracted value of C_L is approximately 27 pF for $R_1 = 16\text{ k}\Omega$ (this latter confirmed by independent short-circuit current measurement). Observe that the simulated results were obtained with $C_L = 30\text{ pF}$, which provides the closest nominal simulation condition to the experimentally extracted $C_L = 27\text{ pF}$.

7.1. Mobility Degradation Extraction via RTL Inverter

The first row of Table 7 shows the measured rise time for RTL inverter. Here, the RTL inverter is used as a reference structure to extract the thermal behavior of the GaN-on-SOI platform, since its rise time is mainly affected by carrier mobility degradation and is not influenced by bootstrap charge retention effects. According to (16), the RTL rise time follows the temperature-dependent resistance variation through the power-law relation $t_{\alpha,\text{RTL}}(T) = t_{\alpha,\text{RTL}}(T_0)(T/T_0)^\gamma$, where $T_0 = 293.15\text{ K}$ (20°C) and $t_{\alpha,\text{RTL}} = 1.00\text{ }\mu\text{s}$ from measures. A non-linear fitting of the experimental data from -40°C to 150°C gives a mobility degradation exponent of $\gamma \approx 1.82$. This value is consistent with typical

GaN literature values ($1.5 < \gamma < 2.5$), where the degradation is mainly caused by phonon scattering [25–29].

Table 7. Measured, Simulated, and Extracted Temperature-Dependent Parameters for RTL and BS Inverters ($C_L = 27$ pF, $V_{TH} = 1.3$ V).

	T (°C) T (K)	−40 233.15	0 273.15	20 293.15	40 313.15	80 353.15	120 393.15	150 423.15	Equation
RTL	$t_{rise,RTL\ EXP}$ (μs)	0.72	0.85	1.00	1.16	1.46	1.73	1.97	/
	$t_{rise,RTL\ SIM}$ (μs) ($C_L = 30$ pF)	0.67	0.87	0.98	1.12	1.43	1.50	1.61	/
	$t_{rise,RTL\ CALC}$ (μs)	0.66	0.88	1.00	1.13	1.40	1.71	1.95	(16) $\gamma = 1.82$
	$R_1\ CALC$ (kΩ)	10.5	14.1	16.0	18.0	22.5	27.3	31.2	(15)
	$I_{SC,RTL\ SIM}$ (μA)	562	433	375	325	264	211	180	/
	$I_{SC,RTL\ CALC}$ (μA)	569	426	375	333	267	220	192	(4)
BS	$R_2\ CALC$ (kΩ)	2.8	3.7	4.2	4.7	5.9	7.2	8.2	(15)
	K_{CALC} (μA/V ²)	73.6	55.2	48.5	43.0	34.6	28.4	24.9	(25)
	$t_{rise,BS\ EXP}$ (μs)	0.45	0.56	0.67	0.78	1.16	1.80	2.36	/
	$t_{rise,BS\ SIM}$ (μs)	0.28	0.39	0.46	0.55	0.79	1.22	1.63	/
	$V_{OV\ EXTR}$ (V)	3.35	3.53	3.40	3.32	2.92	2.45	2.23	(27)
	$2\Delta V_{TH\ CALC}$ (V)	−0.36	−0.12	0.00	0.12	0.36	0.60	0.78	(20) $\alpha_{V_{TH}} = -3$ mV/°C
	$\Delta V_{leak\ EXTR}$ (V)	−0.31	−0.25	0.00	0.20	0.84	1.55	1.95	(23)
	$I_{SC,BS\ SIM}$ (μA)	663	460	375	305	223	156	119	/
	$I_{SC,BS\ CALC}$ (μA)	557	448	374	321	216	139	106	(10)

The subsequent rows of Table 7 report the simulated rise time values for $C_L = 30$ pF, which show good agreement with the measured data, together with the values calculated from (16) using the extracted γ . The calculated and measured/simulated values agree within a few percent over the entire investigated temperature range, confirming the accuracy of the $(T/T_0)^\gamma$ model in capturing the temperature dependence of the rise time.

Table 7 also reports the calculated values of the integrated resistors R_1 and R_2 across the temperature range, derived from (15) using the previously extracted γ . Both resistances increase by approximately 100% from 20 °C to 150 °C, reaching 32.4 kΩ and 8.5 kΩ, respectively, at the maximum operating temperature. R_1 is then used to calculate $I_{SC,RTL}$. Compared with the simulated value, the maximum percentage error is 5.7%.

7.2. Bootstrap Overdrive Compression

The same mobility degradation mechanism also affects the transconductance parameter K of the HEMT devices. Using the design parameters ($V_{OV}(T_0) = 3.40$ V, $I_{SC,BS} = 375$ μA, $R_2 = 4.2$ kΩ) and the aspect ratio $(W/L)_2 = 6/1.3$, the room-temperature transconductance parameter of Q_2 is calculated from (10) as 48.5 μA/V². At 150 °C, the mobility reduction halves this value to approximately 24.1 μA/V².

The measured and simulated rise times for the BS inverter are then shown in the same Table 7. Because the PDK transient models increasingly underestimate $t_{90,BS}$ at elevated temperatures, $V_{OV}(T)$ was extracted directly from the measured transient response rather than from simulation. This deviation is reasonably attributed to second-order effects in the bootstrap node dynamics. These subtle mechanisms are difficult to capture with standard PDK models calibrated mainly for static and large-signal power operation. Consequently, the overdrive $V_{OV}(T)$ cannot be reliably obtained from simulation and is instead extracted directly from the measured $t_{90,BS}$ via the analytical inversion (28).

As reported in Table 7, $V_{OV}(T)$ decreases from 3.40 V at 20 °C to 2.23 V at 150 °C. Since from (1) and (8) $V_{OV} = V_{DD} - V_{TH2} - V_{TH3}$ in the precharge condition, the reduction of the threshold voltage with temperature acts in the opposite direction: it increases the overdrive by $2\Delta V_{TH} = 2|\alpha V_{TH}|(T - T_0)$, i.e., by up to 0.78 V at 150 °C for $\alpha_{V_{TH}} = -3$ mV/°C, the nominal value provided by the PDK model at 27 °C (typical corner). The actual PDK-

modeled dependence varies slightly with both temperature and process corner; the constant value above is adopted as a representative coefficient for the analytical model. The net decrease of V_{OV} is therefore attributed to the leakage-related voltage loss ΔV_{leak} , which reaches about 1.95 V at 150 °C (about 1.55 V at 120 °C), i.e., about 2.5 times larger than the opposing threshold contribution over the whole temperature range. It should be noted that ΔV_{leak} is not measured directly but obtained as a residual of the extraction, and a direct measurement of the leakage currents is left for future work. The neglected term $(\eta_{BS} - 1)V_{OUT}$ in (24) varies by less than about 0.1 V over the temperature range, since η_{BS} varies only between 0.856 and 0.871 (Table 5). The leakage-dominated interpretation therefore remains model-based. However, the model-based extraction does not allow the incomplete output swing observed at 150 °C (Figure 12b) to be attributed to leakage alone, and its detailed origin is left for future investigation.

The resulting $I_{SC,BS\,CALC}(T)$ values, obtained by substituting the dynamically-extracted $V_{OV}(T)$ into the static model (10), agree with the simulated $I_{SC,BS\,SIM}(T)$ within about 10%, with the calculated values slightly above the simulated ones at 40–80 °C. This confirms that the measured speed loss is consistent with the simulated reduction of the static pull-up current.

8. Conclusions

An intrinsic-capacitance bootstrapped inverter using the 6-V HEMT devices of a 200-V E-mode-only GaN-on-SOI technology has been presented and experimentally validated. By exploiting the intrinsic gate capacitance of a GaN HEMT as the bootstrap storage element, the proposed topology achieves bootstrap-enhanced pull-up operation without external capacitors, depletion-mode devices, or additional process complexity.

An analytical electro-thermal framework was developed to model both the conventional RTL inverter and the proposed bootstrapped topology. The analysis showed that the transient speedup originates from the quasi-constant-current pull-up behavior enabled by the bootstrap mechanism, whereas high-temperature degradation is mainly attributed to leakage-induced overdrive loss, as indicated by a model-based parameter extraction.

Measurements performed from −40 °C to 150 °C confirmed the predicted trends. Under comparable static current conditions, the BS inverter achieved a more than 30% reduction in rise time at room temperature together with improved static gain and noise margins compared to RTL. The extracted mobility degradation exponent for the GaN-on-SOI platform was $\gamma \approx 1.82$, while the bootstrap overdrive voltage decreased from 3.40 V at 20 °C to 2.23 V at 150 °C, mainly owing to thermally activated leakage, partly compensated by the reduction of the threshold voltage.

Because PDK transient models were found to underestimate $t_{90,BS}$ by 30–40%, $V_{OV}(T)$ was extracted directly from the measured transient response rather than from simulation. The internal consistency of this extraction was verified by substituting the extracted $V_{OV}(T)$ into the static short-circuit current model (10), yielding agreement with simulated $I_{SC,BS}$ within approximately 10% across the temperature range. Since these two equations describe physically independent operating regimes, this agreement provides indirect validation of the overall electro-thermal framework.

The extracted parameters were further used to estimate the minimum switching frequency required to preserve bootstrap effectiveness, yielding $f_{SW,min} \approx 5$ kHz at the worst-case industrial temperature of 120 °C, well below the typical operating frequency range (>10 kHz).

The results demonstrate that intrinsic-capacitance bootstrapping is a viable approach for compact and fully monolithic GaN logic integration, enabling improved switching performance in E-mode-only GaN smart power platforms.

The analytical model assumes quasi-constant pull-up current and neglects higher-order effects such as channel-length modulation and velocity saturation, which may become relevant at reduced device dimensions. These aspects, together with process variation robustness and multi-stage cascading, together with the origin of the incomplete output swing of the BS inverter at 150 °C, which requires direct leakage measurements and bootstrap node probing, are left for future investigation.

Author Contributions: Conceptualization and validation, K.S., U.C., A.B., S.D. and S.P.; formal analysis, S.P. and A.B.; writing—original draft preparation, S.P. and K.S.; writing—review and editing, S.P., A.B., U.C. and S.D. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially supported by the Wide Bandgap (WBG) Pilot line, which is funded jointly by the Chips Joint Undertaking, through the European Union’s Digital Europe program and Horizon Europe program, as well as by the participating states Italy, Sweden, Poland, Finland, Austria, France, and Germany, under Grant Agreement n. 101183211.

Data Availability Statement: This research was also supported by the European Commission through Project ASCENT+: Access to European Infrastructure for Nanoelectronics funded under H2020 under Grant 871130, and by Italian Ministry of Research PON Ricerca e innovazione 2014–2020, Azione n. IV.6.

Acknowledgments: The authors acknowledge the support of individuals at STMicroelectronics: Calogero (Lillo) Ribellino and Daniele Sacco for chip packaging and Guglielmo Russo and Domenico Ragonese for measurement assistance. The authors also thank Olga Syshchyk at IMEC for her support in IC processing/fabrication.

Conflicts of Interest: The authors declare no conflicts of interest.

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