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RC-Less 4-Ray On-Chip ASK Demodulator for High-Density Implantable Devices

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Abstract

This paper presents a compact, low-power RC-less 4-ray Amplitude-Shift Keying (ASK) demodulator designed for high-density implantable devices. The proposed system addresses the challenges of wireless telemetry in high-density implantable systems, including high-speed data transfer and energy efficiency. In this paper, Schmitt trigger-based digital envelope detector (DED) enables flexible adaptation to various external influences through externally adjustable threshold levels. The system demodulates four types of data signals simultaneously, achieving high data rates while operating within a single frequency band using inductively coupled coils. Fabricated using the DB HiTeK 180 nm BCDMOS process, we tested the system in a benchtop wireless power transmission environment, demonstrating stable and accurate performance. The results indicate the system's potential for application in implantable medical devices, particularly in scenarios requiring high-density stimulation.

Keywords: data communication; ASK modulation; demodulation; wireless power transmission; implantable device; retina prosthesis

1. Introduction

Implantable devices are widely used in clinical practice to restore nerve or muscle function lost due to disease or injury [1–6]. These devices control electrical pulses through microelectrodes to induce specific biological responses, such as stimulating muscle movement in patients with spinal cord injuries [7–9] or providing visual stimulation for those with damaged retinas [10–13]. In these systems, the stimulator's performance directly influences the effectiveness of the treatment.

Recently, implantable systems aimed to improve treatment effectiveness by increasing the number of stimulation channels [2,14]. As deep-submicron CMOS technology has advanced, it is now possible to integrate hundreds or even thousands of stimulators onto a single chip [2,10,11,14]. This high-density integration enhances treatment accuracy and effectiveness, offering improved spatial resolution and more precise stimulation for applications such as visual prostheses and spinal cord injury therapies [2,14]. However, as the number of channels increases, it becomes difficult to supply the necessary power and data in a small, energy-efficient implantable telemetry system [15]. For instance, a 1000-channel retinal implant has been reported to require approximately 100 mW of

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continuous power and a data rate of around 1.23 Mbit/s to update all channels in real time [1,12].

To address these challenges, researchers in implantable devices have focused on developing small, energy-efficient telemetry solutions [16–19]. Earlier studies have used dual-band telemetry, which separates power and data transmission onto different frequency bands to avoid interference and simplify the communication link design [20,21]. However, this approach requires large on-chip filters, separate circuits for power and data frequencies, and additional digital processing components, all of which increase chip area and power consumption, making it less suitable for fully implantable systems with strict size and heat limitations [22].

In response to these limitations, single-band telemetry using inductively coupled coils has emerged as a promising alternative. This method delivers both power and data over a single frequency [23], helping reduce circuit size and power consumption, which are critical requirements for implants that must remain compact and avoid overheating surrounding tissue. Among different modulation techniques, amplitude-shift keying (ASK) is particularly effective, as it enables low-power, simple-circuit demodulation without requiring complex phase or frequency tracking, making it a practical choice for compact implantable devices [23–27]. This approach combines low-rate data directly with the power signal, enabling the use of a low-power receiver that helps maintain the implant's temperature within the safe human body range (36.5 °C to 37.5 °C) [17,19].

In single-band wireless links, a high-quality factor (Q factor) coil improves power-transfer efficiency but significantly narrows the channel bandwidth, thereby limiting the maximum achievable data rate [21,28]. To address this limitation, various approaches have been investigated to increase the data rate, including advanced modulation techniques and improved telemetry architectures [29,30]. Nevertheless, the fundamental trade-off remains because the transmitter and receiver share the same carrier frequency and LC resonant tanks [31]. To overcome this limitation without introducing additional frequency bands, the proposed ASK demodulator employs a four-parallel-ray architecture that encodes four data states within a single-band telemetry system, thereby increasing the effective data rate while maintaining high power-transfer efficiency and low-power operation.

In this paper, we propose a demodulator that uses Schmitt-trigger-based envelope detectors as its core building blocks, enabling fully on-chip ASK demodulation without the need for passive components such as resistors and capacitors. This integration minimizes circuit area and simplifies packaging, which are both important advantages for implantable applications. The circuit includes adaptive thresholding to compensate for signal degradation caused by coil misalignment, such as eye movements in retinal prostheses, and maintains ultra-low power operation to prevent tissue heating. The proposed system receives wireless power through an inductive link and is regulated by an on-chip rectifier and low-dropout (LDO) regulator to generate a $\pm$2.5 V supply for system operation. Implemented in a DB HiTek 180 nm BCDMOS process, the demodulator occupies 2200 μm^2, consumes 10 μW at a 2 Mbit/s data rate with a 13.56 MHz carrier, and demonstrates the proposed system in benchtop measurements, confirming its suitability for next-generation high-density implantable neuro-prosthetic systems.

2. Materials and Methods

Figure 1 illustrates the schematic diagram of the proposed 4-ray ASK demodulator system. ASK signals containing four types of data are modulated and transmitted by wireless power transmission signal generators and received through the coil of the receiver. These signals are used to operate the Clock Extractor (CE) and multiple channels of Digital Envelope Detectors (DEDs) (A). The DEDs can utilize dual-controllable threshold voltages,

V_H and V_L, generated by a hysteresis circuit, enabling the conversion of the modulated signal into raw binary bits. DED output signals from multiple channels are transmitted to a 3-to-2 decoder (B).

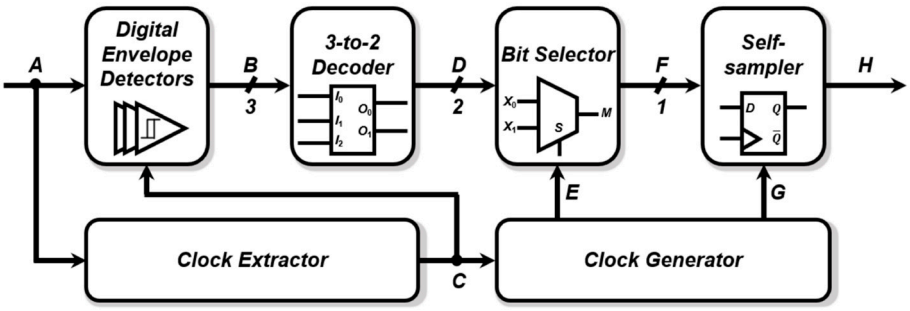


Figure 1. Proposed ASKD system architecture.

Meanwhile, CE performs restoration of the system clock from the received signals by referring to the chip ground voltage as a reference. The output of CE is utilized as the clock signal for synchronizing DED output signals and is employed as the input signal for the Clock Generator (CG) to generate a clock signal that operates at a consistent frequency throughout the system (C). The demodulated signals from multiple channels of DEDs are processed sequentially through a 3-to-2 decoder and bit Selector (D). Subsequently, these signals are directed to a self-sampler (SS) (F). The clocks utilized in these blocks are synchronized with the clock signal generated by CG (E, G). The SS precisely aligns the raw binary stream with the clock, delivering data in a non-return-to-zero (NRZ) form (H).

Schmitt triggers have been effectively used in ASK demodulator systems due to their superior noise immunity. In this paper, we propose an improved Schmitt trigger for the DED, which features externally adjustable thresholds. Proposed DED allows for the detection of the amplitude of ASK signals without the need for a voltage scaler, enabling the configuration of corresponding threshold voltages. In Figure 2, M_N, M_P are controlled through switches SW_N and SW_P, allowing the threshold values V_H and V_L of the DED to be adjusted externally. The expressions for V_H and V_L are derived under the assumption that M_N and M_P are in the 'off' state, to simplify the calculation, as shown below:

$$V_H = \frac{V_{DD} + (V_{TH1} + V_{SS})\sqrt{\frac{W_1 L_5}{W_5 L_1}}}{1 + \sqrt{\frac{W_1 L_5}{W_5 L_1}}} \quad and \quad V_L = \frac{V_{SS} + (V_{DD} - |V_{TH4}|)\sqrt{\frac{W_4 L_6}{W_6 L_4}}}{1 + \sqrt{\frac{W_4 L_6}{W_6 L_4}}}$$

W, L, and V_{TH} represent the width, length, and threshold voltage of each transistor. Through the above equation, it becomes evident that V_H and V_L are adjustable factors that can be adequately controlled by varying the size of the transistors. When the M_N and M_P transistors turn on, assuming equal transistor lengths, the original lengths designated as W_1 and W_4, respectively, expand to $W_1 + W_N$ and $W_4 + W_P$. By adjusting the transistor width, we can modify the threshold according to the amplitude variation in the input signal. This paper employs one Schmitt trigger per DED, with a total of three Schmitt triggers designed for multi-channel DEDs across three channels. The DED transistors in this paper are configured with W/L values of 1 µm/500 nm for NMOS and 2 µm/500 nm for PMOS.

To recover the system clock, a zero-crossing detector is employed as depicted in Figure 2. The CE is composed of a self-biased amplifier and an inverter. By employing the Chip ground voltage (V_{GND}) as the zero-crossing reference voltage for the proposed CE, a clock signal with a 50% duty cycle is generated. The clock signal output from the CE experiences transition speed limitations primarily due to two factors: the output resistance of the amplifier (R_{OUT}) and the loading capacitance (C_L). To mitigate these clock speed

limitations in our study, we have minimized the lengths of M_{15}, M_{17}, M_{18} and M_{19}. The specified time constant of the clock ($\tau = R_{OUT} \times C_L$) in this paper is set at 1.2 ns to ensure sufficient temporal resolution. The CE employed in this paper enhances efficiency in both power consumption and area usage by eliminating the need for bias circuitry through the utilization of a self-biased amplifier and chip ground reference.

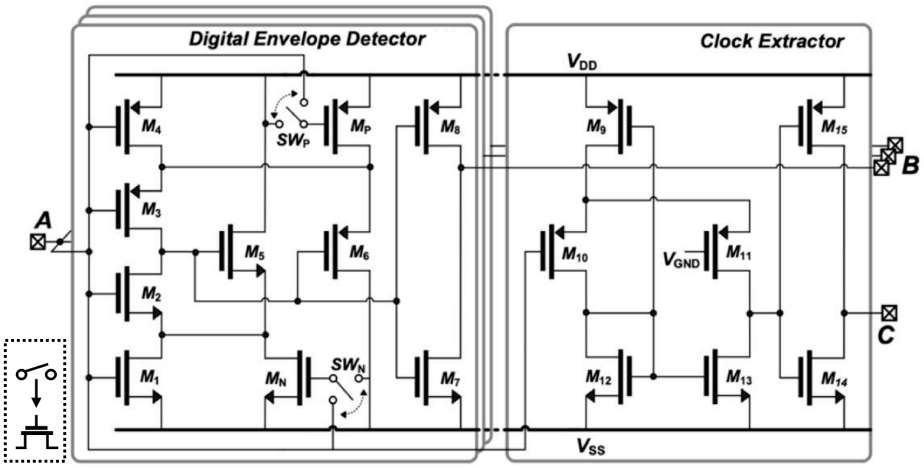


Figure 2. Circuits of DED and CE (The switches SW_N and SW_P are implemented as MOSFET switches for external threshold adjustment).

Figure 3 depicts the timing diagram of demodulating three data signals (B_1, B_2, B_3) from the received signal using the clock extracted from the CE output signal and the three DEDs output signals in proposed system. DED produces raw binary bits from each cycle without rectifying the carrier wave. When the signal exceeds V_H, the output becomes 'High' and remains so until it drops below V_L. The three output signals from the DEDs in Figure 2 are labeled as B_1', B_2' and B_3'. These three output signals from the DED enter D flip-flops that operate based on the clock signal extracted by the CE. Flip-flops are adjusted by a clock signal, which is extracted by the CE. Upon each ascending transition of this clock signal, the flip-flops responsively output signals that correspond to each data signal. Through this process, the signals B_1, B_2 and B_3 are generated.

Figure 4a illustrates the structure of a 3-to-2 decoder. Following the process outlined in Figure 1, the 3-to-2 decoder, which takes the three demodulated data signals as input, produces two output signals. One of the output signals, D_1, sends out the B_2 signal as is. Another output signal, D_2, is generated by an OR gate, which receives B_3 and the output signal of an XOR gate as its inputs. The output signal of the XOR gate is derived from the input signals of B_1 and B_2. In Figure 4b,c, the output signals of the 3-to-2 decoder are organized for each corresponding input signal case. Within this system, B_1 can be activated independently, whereas the activation of B_2 depends on B_1 being active, and B_3 requires both B_1 and B_2 to be active for its activation. This logical dependency characteristic of the multi-channel ASK signal allows for the representation of all possible input data states through the two signals D_1 and D_2. When only B_1 is active with a value of one (case I), D_2 becomes active. Should B_1 and B_2 both be active (case II), D_1 is then activated. When all DED outputs are active (case III), both D_1 and D_2 are activated. Finally, in the absence of any data signal (case IV), both D_1 and D_2 default to a value of zero.

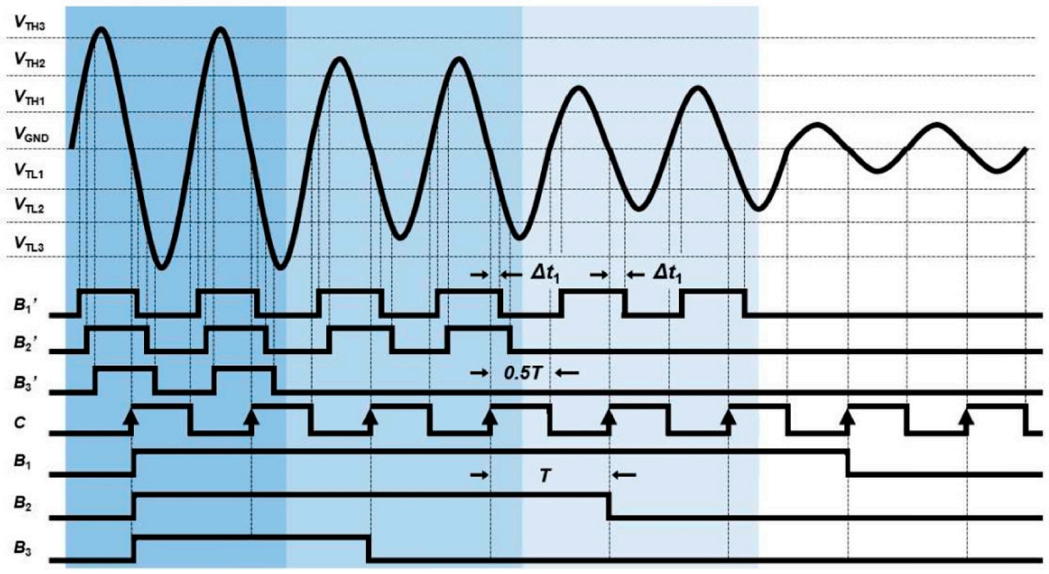
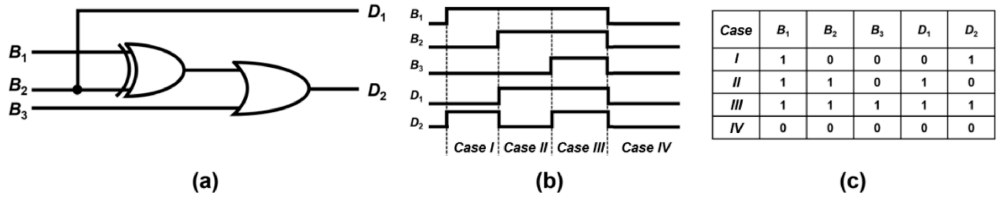


Figure 3. Timing diagram of multi-channel DEDs output signals, where the clock signal (C) is generated using the chip ground voltage (V_{GND}) as the zero-crossing reference, and the values of B_1', B_2' and B_3' at the rising edge of C are defined as B_1', B_2' and B_3'. Different colors indicate the four possible data states.



Case	B_1	B_2	B_3	D_1	D_2
I	1	0	0	0	1
II	1	1	0	1	0
III	1	1	1	1	1
IV	0	0	0	0	0

Figure 4. 3-to-2 decoder (**a**) architecture (**b**) timing diagram (**c**) truth table.

Figure 5 shows the structure and operational process of the Bit selector. The clock for the bit selector is derived from the clock signal generated by the CG (E). Constructed through two AND gates and one OR gate, the Bit selector emits the signal D_1 when the clock signal is High and, conversely, outputs the signal D_2 when it is Low. Figure 5b shows the bit selector's output results of the proposed system for the four types of data signals. The output of the bit selector is once again synchronized with the clock signal, which passes through SS consisting of a D flip-flop and finally becomes the complete output signal of proposed system. The configuration of proposed ASK demodulation system allows for the inclusion of diverse data signals within a single received signal, enabling highly efficient communication. The transistor count of each functional block is summarized in Table 1, including the number of PMOS and NMOS devices used in the implementation.

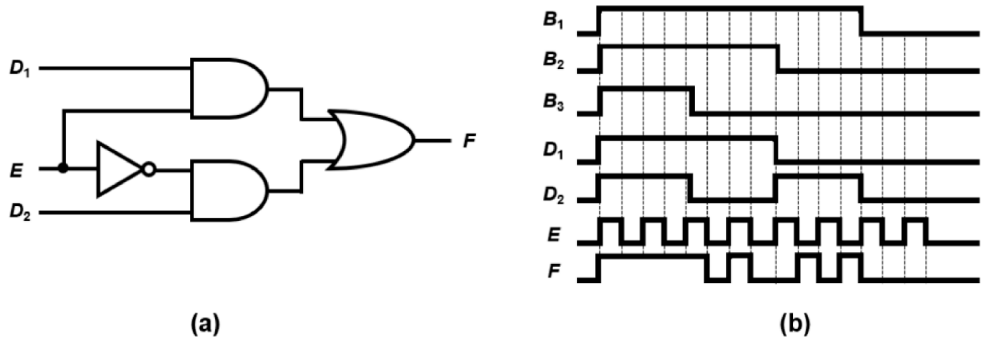


Figure 5. Bit selector (**a**) architecture (**b**) timing diagram.

Table 1. Transistor count of each functional block in the proposed system.

Digital Envelope Detectors	PMOS NMOS	42 42
Clock Extractor	PMOS NMOS	4 3
3-to-2 decoder	PMOS NMOS	10 10
Clock Generator	PMOS NMOS	64 84
Bit Selector	PMOS NMOS	16 26
Self-sampler	PMOS NMOS	5 7

3. Results

Figure 6a presents a photograph of the chip, fabricated using the DB HiTeK 180 nm BCDMOS process(South Korea). The active area of the chip is 720 µm × 306 µm, and the proposed system consumes 10 µW. Figure 6b shows a test bench for measuring the chip results to see whether the proposed system works properly. In the experiment, the proposed system was connected to a wireless power transmission system operating at a 13.56 MHz clock frequency, and signals with four types of data were generated from an FPGA module. Subsequently, the signals were delivered to the receiver via wireless power transmission and were applied as the input to the proposed system. Figure 7a–c shows an experiment output waveform generated from the fabricated chip.

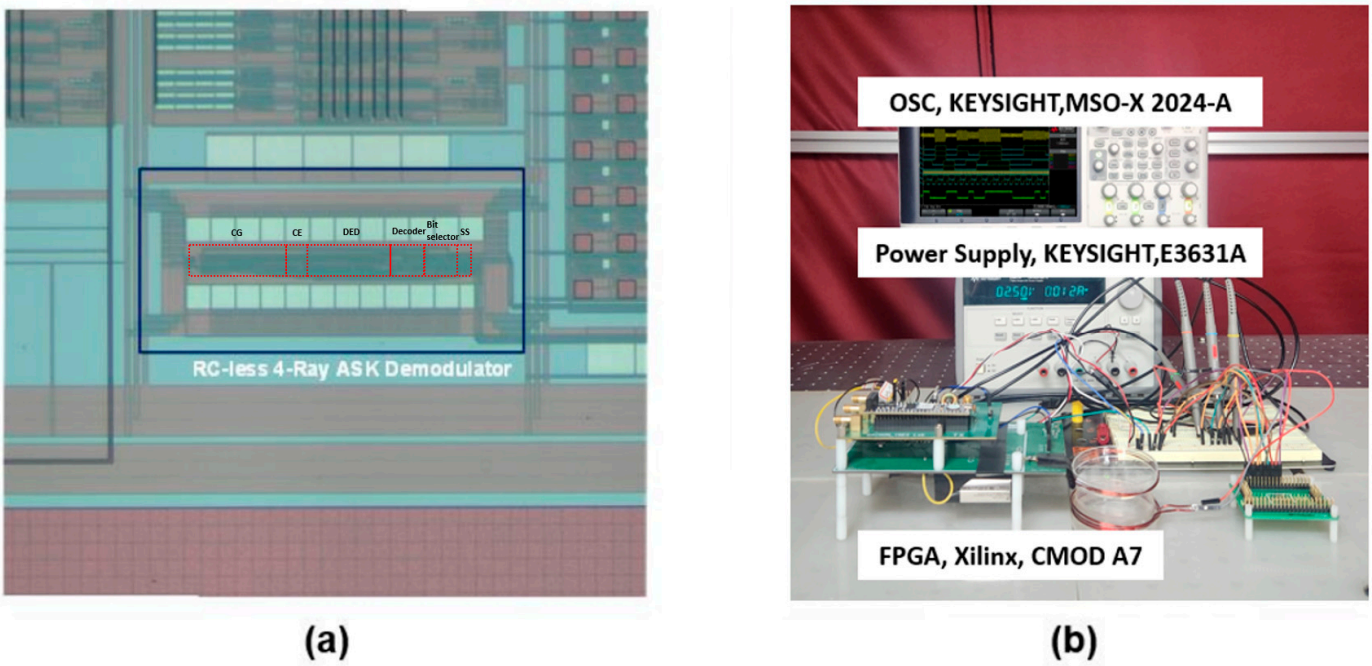
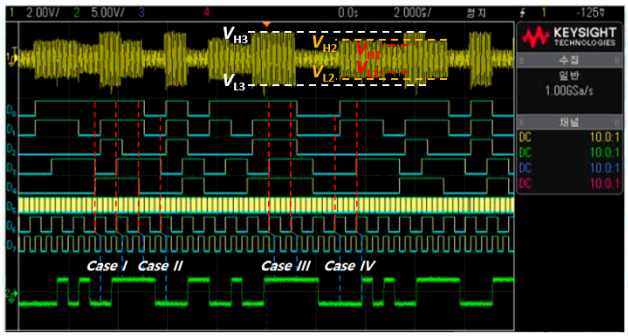
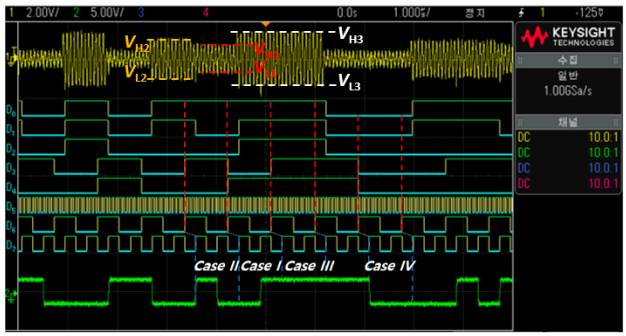


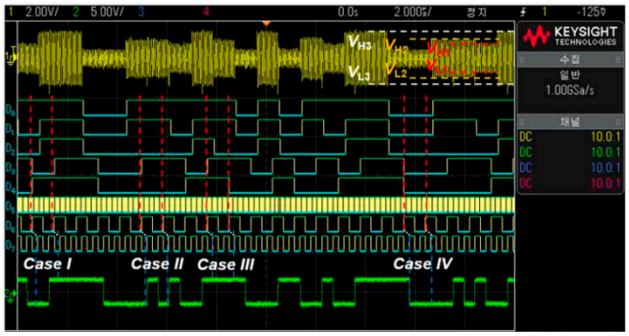
Figure 6. (**a**) Photograph of the fabricated RC-less 4-ray ASK demodulator chip; (**b**) test bench for measuring the results of proposed system.



(a)



(b)



(c)

Case	Digital Envelope Detectors Outputs			3-to-2 Decoder Outputs		Final Output
	$D_0(B_1)$	$D_1(B_2)$	$D_2(B_3)$	$D_3(D_1)$	$D_4(D_2)$	
I	1	0	0	0	1	0-1
II	1	1	0	1	0	1-0
III	1	1	1	1	1	1-1
IV	0	0	0	0	0	0-0

(d)

Figure 7. Experimental results of the ASK demodulation: (**a**–**c**) Measured waveforms; (**d**) Summary of measured data. The three colored lines indicate the boundaries separating the four different data states.

In the top section of Figure 7a–c, the depicted yellow signal illustrates the signal input to the receiving coil from the transmitting coil, denoted as '*A*' in Figure 2. This signal exhibits varying amplitudes corresponding to different data types. D_0, D_1 and D_2 depict the outcomes of data signal extraction from distinct channels within the multichannel DEDs, as indicated in Figure 3 'B_1, B_2 and B_3'. D_0 is activated when the received signal surpasses V_{H1}. Similarly, D_1 becomes active based on V_{H2}, while D_2 is enabled by V_{H3}, with each data signal following these activation criteria. The signals at D_3 and D_4 demonstrate the operation of the 3-to-2 decoder, which processes the outputs from the three DED channels, as delineated in Figure 4 'D_1 and D_2'.

The clock signal, designated as D_5 , is derived from the coil's received signal by the CE and serves as the timing reference within the DED, as indicated by '*C*' in Figure 2. The CG is responsible for producing both D_6 and D_7 signals, where D_6 serves as the clock for the Bit Selector, and D_7 acts as the clock for the SS. The final output of the proposed system is represented by the lowest green waveform in Figure 7a–c.

As previously described, three demodulated data signals (D_0, D_1, D_2) are consolidated into two via a 3-to-2 decoder. For clarity in exposition within this paper, D_3 and D_4 are referred to as the outputs of the 3-to-2 decoder, although they are synchronized with the clock signal of the subsequent Bit Selector. D_3 directly mirrors the signal from D_1, whereas D_4 is generated by subjecting the XOR outcome of D_0 and D_1 to an OR operation with D_2.

The output signals from the 3-to-2 decoder, after logic gate processing, are synchronized with the rising edge of the Bit Selector's clock signal, D_6, for use as inputs to the Bit Selector. The Bit Selector operates by outputting the signal from D_3 when the clock signal

D_6 is in a high state, and from D_4 when D_6 is in a low state. The output from the Bit Selector is synchronized with the rising edge of the self-sampler's clock signal, D_7, which operates at half the frequency of D_6. This synchronization ensures that the final output signal represents all data signals.

4. Discussion

In this work, we proposed a 4-ray on-chip ASK demodulation circuit without requiring any resistors or capacitors for low-power wireless data reception in implantable applications, and its performance was verified through bench-top experiments. To evaluate its demodulation performance, the fabricated chip was connected to a test PCB, and digital command signals generated by an FPGA(Cmod A7, Digilent, Inc., Pullman, WA, USA) were wirelessly transmitted through the resonant coil on the board. In inductively coupled wireless communication, our system accurately recovered the multi-level data command signals with clear amplitude separation and stable operation throughout the tests. These experiments confirmed that the proposed demodulation architecture operates well under inductively coupled wireless communication with transmission distances of implantable-device operation. Table 2 summarizes a comparison between the proposed system and previously reported wireless data communication circuits, highlighting lower power requirements and suitability for miniaturized implantable systems.

Table 2. Proposed system's specifications and comparison.

Reference	Modulation Index (%)	Data Rate (kbit/s)	Carrier Frequency (MHz)	Core Area (μm^2)	Energy Consumption (pJ/bit)	Power Consumption (μW)	Process (μm)
[31]	N.A.	678	13.56, 8.78	820,000	46	67.8	0.18
[32]	100	848	13.56	3500	11.6	9.9	0.13
[33]	4	4000	13.56	31,300	9.4	63.5	0.35
[34]	10	1000	13.56	514,800	280	280	0.18
[35]	10	2700	13.56	1440	45	45	0.18
This work	15	2000	13.56	2200	5	10	0.18

The next step of our research is to place the entire implantable device circuit on a single chip, including the wireless power transfer blocks and the stimulation circuits. In the current tests, the chip is connected to the wireless communication front ends through a test PCB, but future versions will integrate the rectifier, LDO, and wireless data path directly on the chip. This will reduce the external parts to only the inductive coil and the resonance capacitor. The recovered data and received power will be sent into the fully integrated on-chip system, allowing the data commands to control the on-chip digital controller and operate the full functions of the implantable device.

For in vivo testing of the fully integrated implantable device system, the system and the external coils will be packaged with biocompatible materials to ensure stable operation after implantation. This packaging is important because the device must keep its electrical and mechanical stability inside biological tissue during testing. After packaging, we will conduct in vivo experiments to collect system-level performance data under real physiological conditions. The results from the in vivo tests will help confirm the operation of the complete system, and we plan to write a follow-up paper that covers the fully integrated implantable device, including wireless power transfer, data communication, digital control, and stimulation functions.

5. Conclusions

RC-less 4-ray on-chip ASK Demodulator proposed in this paper was fabricated using the DB HiTeK 180 nm BCDMOS process. Experiments validated the system's ability to receive and process ASK signals comprising four types of data. The proposed system employs a Schmitt trigger with externally adjustable thresholds, enabling stable data reception for variations in signal conditions due to external influences. Furthermore, the CE and multi-channel DEDs developed in this study demonstrated high accuracy and efficiency, enabling stable data transmission. These results enhance the potential application of the proposed demodulator in implantable devices and are expected to contribute to the advancement of wireless power transmission systems.

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Data Availability Statement: The data presented in this study are included in this article.

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Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

ASK	Amplitude-Shift Keying
DED	Digital Envelope Detector
Q factor	Quality factor
CE	Clock Extractor
CG	Clock Generator
SS	Self-sampler
NRZ	Non-Return-to-Zero

References

1. Weiland, J.D.; Humayun, M.S. Retinal prosthesis. *IEEE Trans. Biomed. Eng.* **2014**, *61*, 1412–1424. [CrossRef]
2. Kang, H.; Kim, J.; Kim, J. Integrated High-Temporal-Resolution and High-Density Subretinal Prosthesis Using a Correlated Double-Sampling Technique. *Sensors* **2023**, *23*, 6501. [CrossRef] [PubMed]
3. Kim, J. Sensors, Circuits, and Systems for Biomedical Applications. *Sensors* **2023**, *23*, 3295. [CrossRef] [PubMed]
4. Oh, Y.; Hong, J.; Kim, J. Integrated Low-Voltage Compliance and Wide-Dynamic Stimulator Design for Neural Implantable Devices. *Sensors* **2023**, *23*, 492. [CrossRef] [PubMed]
5. Zawawi, R.B.A.; Kim, J. Two-Way Communication Digital Power Controllers for Wireless Retinal Prosthesis Systems. *Sensors* **2022**, *22*, 2970. [CrossRef] [PubMed]
6. Zawawi, R.B.A.; Choi, H.; Kim, J. High PSRR Wide Supply Range Dual-Voltage Reference Circuit for Bio-Implantable Applications. *Electronics* **2021**, *10*, 2024. [CrossRef]
7. Valente, V.; Eder, C.; Donaldson, N.; Demosthenous, A. A high-power CMOS class-D amplifier for inductive-link medical transmitters. *IEEE Trans. Power Electron.* **2015**, *30*, 4477–4488. [CrossRef]
8. Donaldson, N.; Perkins, T.; Pachnis, I.; Vanhoest, A.; Demosthenous, A. Design of an implant for preventing incontinence after spinal cord injury. *Artif. Organs* **2008**, *32*, 586–591. [CrossRef] [PubMed]

9. Liu, X.; Demosthenous, A.; Vanhoestenberghe, A.; Jiang, D.; Donaldson, N. Active books: The design of an implantable stimulator that minimizes cable count using integrated circuits very close to electrodes. *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 216–227. [CrossRef] [PubMed]
10. Tran, N.; Bai, S.; Yang, J.; Chun, H.; Kavehei, O.; Yang, Y.; Muktamath, V.; Ng, D.; Meffin, H.; Halpern, M.; et al. A complete 256-electrode retinal prosthesis chip. *IEEE J. Solid-State Circuits* **2014**, *49*, 751–765. [CrossRef]
11. Chen, K.; Yang, Z.; Hoang, L.; Weiland, J.; Humayun, M.; Liu, W. An integrated 256-channel epiretinal prosthesis. *IEEE J. Solid-State Circuits* **2010**, *45*, 1946–1956. [CrossRef]
12. Sivaprakasam, M.; Liu, W.; Wang, G.; Weiland, J.D.; Humayun, M.S. Architecture trade-offs in high density microstimulators for retinal prosthesis. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2005**, *52*, 2629–2641. [CrossRef]
13. Monge, M.; Raj, M.; Nazari, M.H.; Chang, H.-C.; Zhao, Y.; Weiland, J.D.; Humayun, M.S.; Tai, Y.-C.; Emami, A. A fully intraocular high-density self-calibrating epiretinal prosthesis. *IEEE Trans. Biomed. Circuits Syst.* **2013**, *7*, 747–760. [CrossRef] [PubMed]
14. Oh, Y.; Hong, J.; Kim, J. Retinal prosthesis edge detection (RPED) algorithm: Low-power and improved visual acuity strategy for artificial retinal implants. *PLoS ONE* **2024**, *19*, e0305132. [CrossRef] [PubMed]
15. Bashirullah, R. Wireless Implants. *IEEE Microw. Mag.* **2010**, *11*, S14–S23. [CrossRef]
16. Yoo, S.; Lee, J.; Joo, H.; Sunwoo, S.-H.; Kim, S.; Kim, D.-H. Wireless Power Transfer and Telemetry for Implantable Bioelectronics. *Adv. Healthc. Mater.* **2021**, *10*, 2100614. [CrossRef] [PubMed]
17. Xu, Z.; Khazaee, M.; Duy Truong, N.; Havenga, D.; Nikpour, A.; Ahnood, A.; Kavehei, O. A leadless power transfer and wireless telemetry solutions for an endovascular electrocorticography. *J. Neural Eng.* **2024**, *21*, 1741–2552. [CrossRef] [PubMed]
18. Oxley, T.J.; Opie, N.L.; E John, S.; Rind, G.S.; Ronayne, S.M.; Wheeler, T.L.; Judy, J.W.; McDonald, A.J.; Dornom, A.; Lovell, T.J.H.; et al. Minimally invasive endovascular stent-electrode array for high-fidelity, chronic recordings of cortical neural activity. *Nat. Biotechnol.* **2016**, *34*, 320–327. [CrossRef] [PubMed]
19. Nelson, B.D.; Karipott, S.S.; Wang, Y.; Ong, K.G. Wireless technologies for implantable devices. *Sensors* **2020**, *20*, 4604. [CrossRef] [PubMed]
20. Wang, G.; Liu, W.; Sivaprakasam, M.; Zhou, M.; Weiland, J.D.; Humayun, M.S. A Dual Band Wireless Power and Data Telemetry for Retinal Prosthesis. In Proceedings of the 2006 International Conference of the IEEE Engineering in Medicine and Biology Society, New York, NY, USA, 30 August–3 September 2006; pp. 4392–4395. [CrossRef] [PubMed]
21. Wang, G.; Wang, P.; Tang, Y.; Liu, W. Analysis of Dual Band Power and Data Telemetry for Biomedical Implants. *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 208–215. [CrossRef] [PubMed]
22. Zhou, A.; Yuce, M.; Liu, W. A non-coherent DPSK data receiver with interference cancellation for dual-band transcutaneous telemetries. *IEEE J. Solid-State Circuit* **2008**, *43*, 2003–2012. [CrossRef]
23. Kim, J. Optimum modulation scheme for single-band wireless biotelemetry system. *Electron. Lett.* **2014**, *50*, 1801–1803. [CrossRef]
24. Yuan, F. Design techniques for ASK demodulators of passive wireless microsystems: A state-of-the-art review. *Analog Integr. Circuits Signal Process.* **2010**, *63*, 33–45. [CrossRef]
25. Lotfi-Navaii, M.; Jalali, M.; Sadjedi, H. An ultra-low power RF interface for wireless-implantable microsystems. *Microelectron. J.* **2012**, *43*, 848–856. [CrossRef]
26. Lee, B.; Ghovanloo, M. An Overview of Data Telemetry in Inductively Powered Implantable Biomedical Devices. *IEEE Commun. Mag.* **2019**, *57*, 74–80. [CrossRef]
27. Ahmadi, M.M.; Pezeshkpour, S.; Kabirkhoo, Z. A High-Efficiency ASK-Modulated Class-E Power and Data Transmitter for Medical Implants. *IEEE Trans. Power Electron.* **2022**, *37*, 1090–1101. [CrossRef]
28. Karimi, M.J.; Schmid, A.; Dehollain, C. Wireless Power and Data Transmission for Implanted Devices via Inductive Links: A Systematic Review. *IEEE Sens. J.* **2021**, *21*, 7145–7161. [CrossRef]
29. Ghovanloo, M.; Najafi, K. A high-rate frequency shift keying demodulator chip for wireless biomedical implants. In Proceedings of the 2003 International Symposium on Circuits and Systems, Vancouver, BC, Canada, 23–26 May 2004; p. 5. [CrossRef]
30. Simard, G.; Sawan, M.; Massicotte, D. High-Speed OQPSK and Efficient Power Transfer Through Inductive Link for Biomedical Implants. *IEEE Trans. Biomed. Circuits Syst.* **2010**, *4*, 192–200. [CrossRef] [PubMed]
31. Karimi, M.J.; Jin, M.; Zhou, Y.; Dehollain, C.; Schmid, A. Wirelessly Powered and Bi-Directional Data Communication System With Adaptive Conversion Chain for Multisite Biomedical Implants Over Single Inductive Link. *IEEE Trans. Biomed. Circuits Syst.* **2024**, *18*, 636–647. [CrossRef] [PubMed]
32. Wang, D.; Li, D.; Wu, J.; Cai, J.-H.; Zhong, Q.-H.; Huang, X.; Hu, J.-G. A 0.35 mm^2 94.25μ W Fully Integrated NFC Tag IC Using 0.13μ m CMOS Process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2024**, *71*, 2612–2622. [CrossRef]
33. Zhou, J.; Chen, X.; Wu, T.; Wang, G. A Fully Differential High Efficient ASK Demodulator for Biomedical Implantable Application. In Proceedings of the 2017 IEEE 12th International Conference on ASIC (ASICON), Guiyang, China, 25–28 October 2017; pp. 508–511. [CrossRef]

34. Chen, Y.; Liu, Y.; Li, Y.; Wang, G.; Chen, M. An energy-efficient ASK demodulator robust to power-carrier-interference for inductive power and data telemetry. *IEEE Trans. Biomed. Circuits Syst.* **2022**, *16*, 108–118. [CrossRef] [PubMed]
35. Karimi, M.J.; Zhou, Y.; Dehollain, C.; Schmid, A. An Analysis of an ASK Demodulator With Dual Self-Biased Separated Voltages for Implantable Applications. *IEEE Trans. Circuits Syst. II Express Briefs* **2024**, *71*, 2986–2990. [CrossRef]

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