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A Substrate-Aware CMOS Micromagnetic Stimulation SoC with a Bent Micro-Coil and Programmable Triangular Current Driver

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Abstract

Microscopic magnetic stimulation (MSTI) induces electric fields without direct charge injection and can shape localized field gradients with asymmetric micro-coils. Most demonstrations still rely on external drivers, off-chip hardware, or separated coil validation, so the CMOS integration boundary remains poorly characterized. This work presents a fabricated 2×1 mm^2 0.18 µm CMOS magnetic-stimulation SoC that co-integrates ASK-compatible command decoding, FSM and register-based parameter control, a programmable current–voltage–current triangular driver, and a bent top-metal micro-coil, and it characterizes the on-chip driver-to-coil path together with a substrate-aware field model. Sensing-load reconstruction confirms command-to-waveform programmability, including duration-window decoding, burst-count control, and polarity reversal, with measured slew targets that give a peak current of $I_{pk} = 3.72$–21.6 mA. A quantitative comparison contrasts the current-mode triangular driver with conventional electrode stimulators, a coil-impedance measurement shows the coil stays resistive across 1 to 10 MHz, and the measured total SoC power is about 41 mW. Substrate-aware simulation at a 15 µm target plane shows that the grounded p-substrate retains 35.1–40.5% of the no-substrate peak x-directed field-gradient metric. The prototype establishes this electrical programmability and the substrate-aware gradient-transfer loss as a compact design-margin metric for CMOS-integrated magnetic stimulation. Direct biological activation is not claimed and is left to future in vitro validation.

Keywords: magnetic neural stimulation; micromagnetic stimulation; MSTI; micro-coil; neural-interface IC; CMOS SoC; command-pattern decoder; substrate-aware electromagnetic simulation

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1. Introduction

Electrical neuromodulation is clinically important, but electrode-based stimulation relies on charge transfer at the electrode–tissue interface and can be limited by unintended

activation, impedance variation, and chronic interface response [1–5]. Magnetic stimulation offers a complementary path because a time-varying coil current can induce an electric field without direct charge injection [6,7]. Macroscopic coils are not suitable for precise implant-scale interfaces. Microscopic magnetic stimulation (MSTI) has shown that small coils and asymmetric coil geometries can shape localized field distributions and neural responses [8–13].

The next integration step is to move magnetic stimulation from the external driver and separated coil demonstrations into a compact CMOS boundary. CMOS integration can combine command decoding, parameter storage, waveform generation, and the top-metal micro-coil on one silicon platform. This reduces the need for bulky external waveform hardware and shortens the electrical path between the driver and coil. It also creates a new field-transfer problem because the coil, passivation stack, and conductive silicon substrate become part of the stimulation boundary. Microfabricated magnetic-stimulation hardware has continued to develop toward miniaturized coil structures and high-resolution interfaces [14,15].

This boundary differs from prior micro-coil demonstrations that used external pulse generators or separated device probes [8,16]. It also differs from electrode-oriented wireless neural-interface ICs, where the stimulation target is usually an electrode or external transducer rather than an on-chip magnetic micro-coil [17,18]. Once the micro-coil is placed in the top metal above a conductive CMOS substrate, the oxide/passivation stack and substrate grounding condition can alter target-plane field transfer. RF CMOS inductor and substrate-loss studies provide qualitative support that conductive silicon and ground-shield structures affect on-chip inductive components [19–22]. These considerations motivate substrate-aware verification for CMOS magnetic stimulation.

A long-term architecture for minimally invasive MSTI is a dust-scale magnetic stimulation node. Here, dust-scale denotes a mm-class implantable node, with a target footprint on the order of 1 mm^2 and a sub-mm^3 volume. Such a node would use a single received protocol for power transfer and command data, followed by addressable digital control, compact waveform generation, an integrated micro-coil, and package-level biocompatibility. The present silicon prototype focuses on the CMOS command-to-waveform and field-transfer path within this architecture. The command decoder, FSM/register control, triangular driver, and bent top-metal micro-coil are implemented on-chip, whereas the wireless power-and-data receiver shown in Figure 1 is not implemented in this silicon and is drawn only as a system-level block. Current reconstruction additionally uses an external sensing resistor (Section 2.4). Figure 1 summarizes the system context and highlights the implemented command-to-waveform path and substrate-dependent field-gradient transfer.

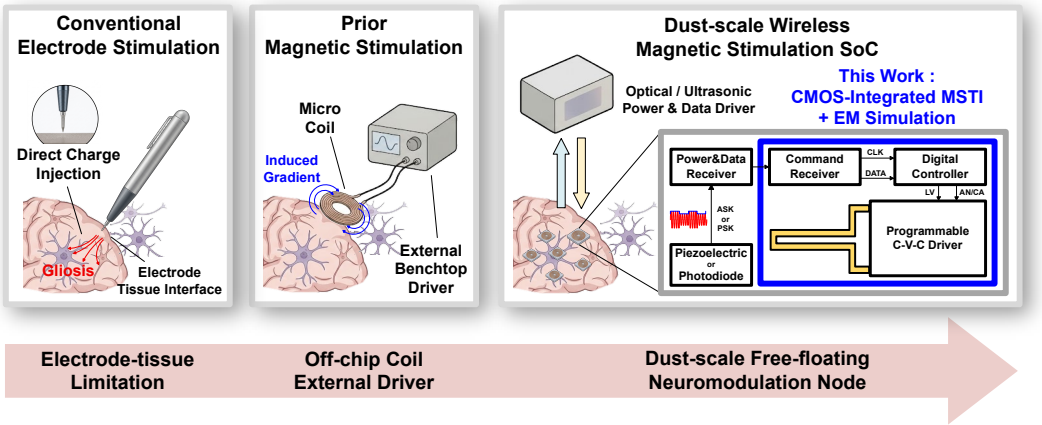

Figure 1. Conceptual positioning of the proposed CMOS-integrated MSTI core within a dust-scale wireless magnetic stimulation node.

The main contributions are threefold. First, a 2×1 mm^2 CMOS command-to-waveform driver with an integrated bent top-metal micro-coil is fabricated, combining on-chip command decoding, register/FSM control, and triangular current generation. Second, command-dependent driver-output programmability is verified using sensing-load waveform reconstruction. Third, no-p-substrate and grounded-p-substrate electromagnetic models are compared under measured slew-target excitation normalization to evaluate substrate-induced gradient-transfer loss. Direct biological activation and wireless power/data reception are outside the scope of this prototype.

2. Materials and Methods

2.1. Integrated SoC and Command Path

Figure 2 shows the proposed CMOS magnetic-stimulation SoC. The implemented chip receives an externally applied ASK-compatible command-pattern input. The decoder and FSM controller map the command frame to stimulation parameters and drive a programmable current–voltage–current waveform generator connected to the integrated 90-degree bent top-metal micro-coil. The command path is compatible with a single power-data protocol because one received frame can both identify the target node and locally set the waveform parameters.

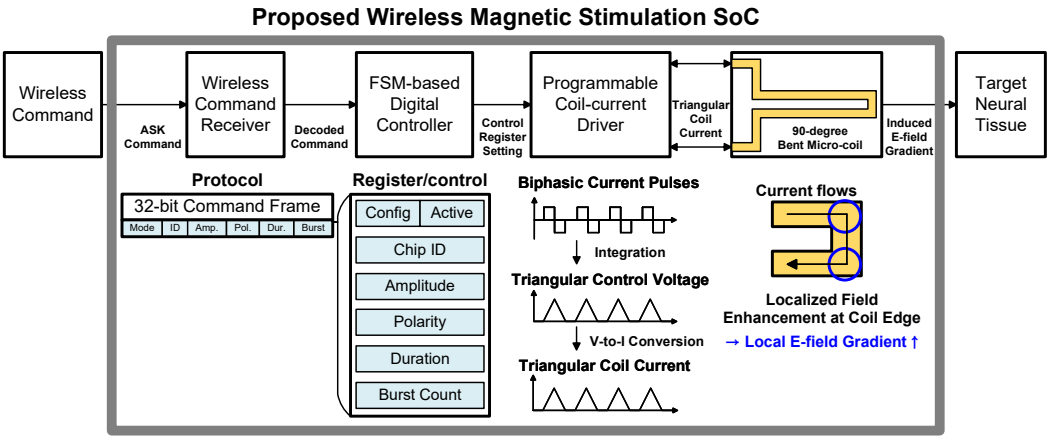

Figure 2. Overall system architecture of the proposed micro-sized magnetic neural stimulation SoC, including the ASK-compatible command receiver, FSM controller, programmable triangular driver-output generator, bent top-metal micro-coil, and field-gradient transfer concept. The arrows indicate the signal and field-transfer flow.

A 32-bit command frame carries the mode, node identifier, amplitude, output scale, polarity, duration, and burst-count fields. The controller updates the local registers only after mode and identifier matching, so one valid command transaction sets the waveform scale, timing, polarity, and repetition before the triangular driver phases begin.

2.2. Current–Voltage–Current Driver

Figure 3 shows the current–voltage–current driver. The driver uses a code-controlled current stage, an integration-voltage stage, and a voltage-to-current output stage. The first stage charges or discharges the integration capacitor. The integration node generates a triangular voltage, and the output stage converts that voltage into a driver-output current. The MLV-controlled scaling stage uses an active feedback loop to set the drain-side bias of the scaling transistors so that they operate in the triode region. With these devices biased in the triode, the stage acts as a code-dependent voltage-to-current converter. This avoids a large off-chip waveform source and maps digital fields to waveform scale, polarity, duration, and burst count.

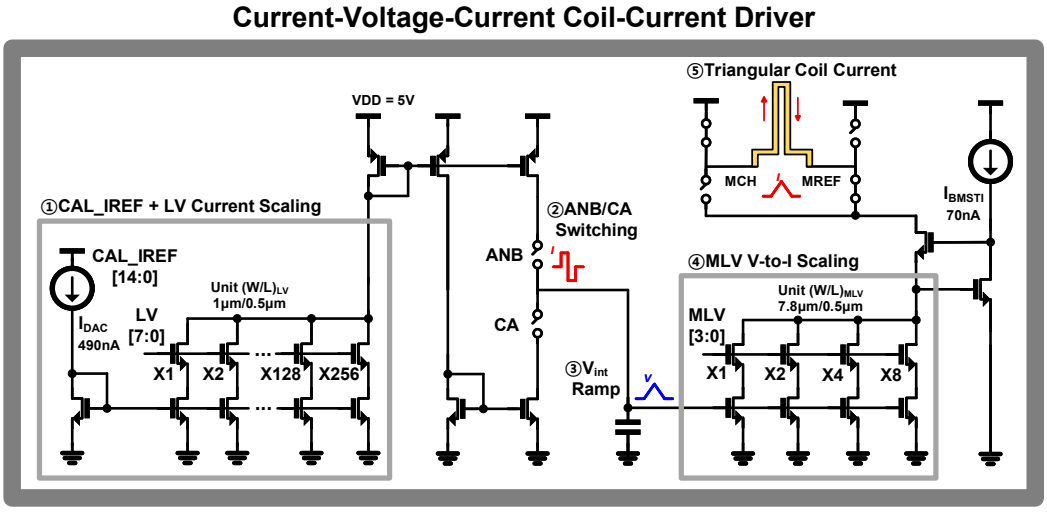

Figure 3. Current–voltage–current triangular driver schematic. The code-controlled current-scaling stage sets the integration-current level, the switching network selects the charge/discharge phase, and the active-feedback output stage biases the MLV-controlled scaling transistors in the triode for voltage-to-current conversion.

The waveform-generation principle can be expressed by the integration relation

$$\frac{dV_{\text{int}}}{dt} = \pm\frac{I_{\text{C1}}}{C_{\text{int}}}. \tag{1}$$

The current I_{C1} is set by CAL_IREF[14:0] and LV[7:0]. If the following stage has a code-dependent effective voltage-to-current coefficient $g_{\text{C2}}(\text{MLV})$, the approximate output-current slew rate is

$$\frac{dI_{\text{out}}}{dt} \approx \pm\frac{g_{\text{C2}}(\text{MLV})I_{\text{C1}}}{C_{\text{int}}}. \tag{2}$$

Because the active-feedback loop holds the scaling devices in the triode region at a fixed drain–source bias V_{DS}, the coefficient g_{C2} reduces to the triode-region transconductance of the MLV-selected device,

$$g_{\text{C2}}(\text{MLV}) \approx \mu_n C_{\text{ox}}\left(\frac{W}{L}\right)_{\text{MLV}} V_{\text{DS}}, \tag{3}$$

where $\mu_n C_{\text{ox}}$ is the process transconductance parameter and $(W/L)_{\text{MLV}}$ is the aspect ratio selected by the MLV code. Hence, g_{C2} scales approximately linearly with the MLV-selected device width, providing the code-dependent output-current slope. The MLV-controlled scaling devices are binary-weighted across the four MLV bits in a 1:2:4:8 ratio, so the MLV code sets $(W/L)_{\text{MLV}}$ in unit-width steps and produces the linear slope of Equation (3). The unit-transistor dimensions of the scaling and output stages (1 μm/0.5 μm and 7.8 μm/0.5 μm) and the I_{DAC} and I_{BMSTI} bias currents are annotated in Figure 3.

Thus, LV and MLV are the primary electrical scale knobs, PRMDR sets the integration interval, PRMPOLAR selects the phase order, and PRMBRST sets the repetition count. The resulting triangular waveform is treated as a slope-defined magnetic excitation because induced electric field and stimulation pulse dynamics depend on the time variation in the magnetic field or vector potential [23–25]. The activating function for magnetic stimulation follows the spatial gradient of this induced electric field, which scales with dB/dt. A constant-slew triangular drive therefore holds the induced field gradient uniform over each phase, so the digitally programmed slew sets the stimulation strength directly, while the biphasic phase order balances the induced field across the two polarities. An STB loop-gain analysis of the active-feedback triode-bias loop gives a DC loop gain of about

30.5 dB, a unity-gain frequency near 1.1 MHz, and a phase margin of about 88° with a gain margin of about 24 dB (Figure 4). The large phase margin shows that the triode-bias loop stays well-damped under worst-case load.

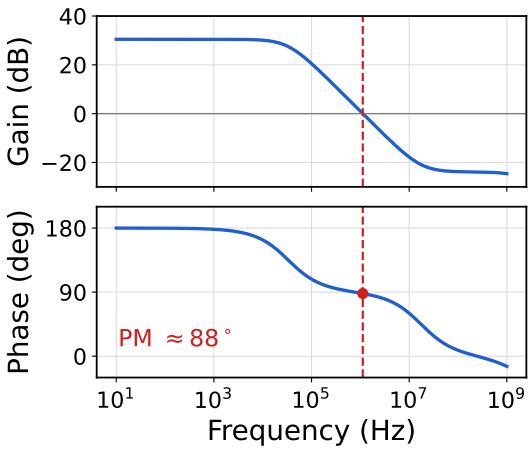

Figure 4. Simulated loop-gain magnitude and phase of the active-feedback triode-bias loop (STB analysis), shown as the two colored curves (magnitude and phase traces), with a unity-gain frequency near 1.1 MHz and a phase margin of about 88°.

Table 1 compares the C-V-C driver with representative H-bridge and switched-capacitor current stimulators [26–29]. Those electrode-driven topologies deliver sub-mA to few-mA currents into kΩ-scale loads, which requires a multi-volt on-chip compliance supply and a charge-balancing path. The proposed stage instead drives a low-impedance integrated micro-coil, producing a 3.72–21.6 mA triangular current at a coil terminal swing of only 3.85–22.3 mV (Section 2.5). It therefore needs no high-voltage compliance generator or charge-balancing network, and it sets slew, duration, polarity, and burst count directly from digital fields within a compact 627 × 76 μm^2 (0.048 mm^2) area. At the high-slew setting it consumes about 3.89 mW, so the driver efficiency referenced to the coil dissipation is near 6.2%, which is inherent to the current-mode drive into a sub-ohm coil rather than a kΩ electrode load.

Table 1. Quantitative comparison of integrated stimulation-driver topologies.

Topology (Reference)	Output Current	Compliance/Supply	Process/Area	Power/Efficiency
H-bridge current stimulator [26]	0.07–2.08 mA, 5-bit	12.5 V/13.2 V	180 nm, 0.15 mm^2	48% @2 mA
H-bridge, stacked HV switches [27]	up to 3.2 mA, 5-bit	10.2 V/11.2 V	180 nm, 0.18 mm^2 core	90 μW @3.2 mA
Switched-capacitor [28]	peak 4 mA	±2 V cap bank	0.35 μm, 12 mm^2 die	80.4% eff.
Adiabatic energy recycling [29]	0–450 μA	3.3 V	0.35 μm, –	82–84% (DC-DC)
This work (C-V-C triangular)	3.72–21.6 mA	3.85–22.3 mV/5 V	180 nm, 0.048 mm^2	3.89 mW @21.6 mA, $\eta \approx 6.2\%$

2.3. The 90-Degree Bent Top-Metal Micro-Coil

The micro-coil is implemented in the top metal layer of the 0.18 μm CMOS process. The 90-degree bend provides a layout-compatible asymmetric top-metal edge within the available silicon area, following prior asymmetric micro-coil studies [9–11,13]. The fabricated chip and COMSOL Multiphysics 6.3 stack are shown in Figure 5. The field analysis uses a local edge coordinate system, with $x = 0$ defined at the selected straight coil edge.

The electric-field-gradient component used in the activating-function interpretation is

$$A_{F,u}(\mathbf{r}) = \frac{\partial E_u(\mathbf{r})}{\partial u}. \tag{4}$$

The variable u denotes the evaluated target-neuron axis, and E_u is the electric-field component along that axis. This gradient-based metric follows the activating-function

interpretation of extracellular stimulation and the field-gradient analysis used in micro-coil stimulation studies [10,11,30]. In this framework, neural polarization is linked to spatial variation in the extracellular or induced electric field along the target fiber direction rather than to the local field magnitude alone. The field analysis in this work uses the x-directed component

$$A_{F,x}(x,y) = \frac{\partial E_x(x,y,z_0)}{\partial x}, \quad z_0 = 15\ \mu\text{m}. \tag{5}$$

z_0 is referenced to the top-metal coil surface. The edge-normal and edge-parallel cuts focus on the region where the simulated induced field changes most rapidly.

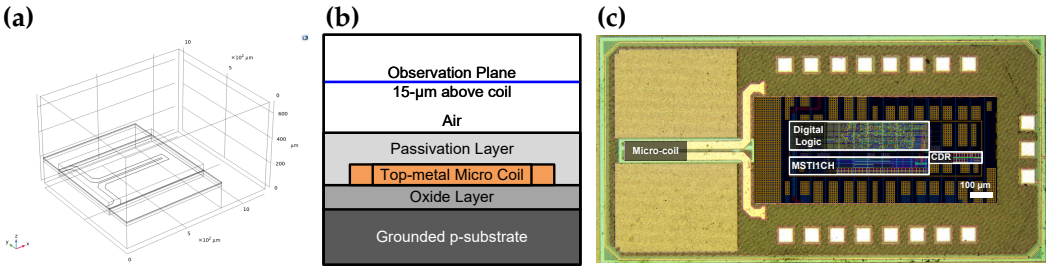

Figure 5. Implementation and substrate-aware verification model. Panel (**a**) shows the COMSOL coil and model geometry, panel (**b**) shows the substrate stack and observation plane, and panel (**c**) shows the fabricated 2×1 mm^2 chip micrograph.

2.4. Electrical Measurement and Current Reconstruction

The fabricated chip was characterized by pad-level driver-output reconstruction to verify programmable waveform generation. For the electrical sweep, the exposed driver-output node was connected to an external sensing resistor of $R_{\text{sense}} = 1\ \text{k}\Omega$. After removing the static differential offset, the equivalent sensing-load current is

$$I_{\text{EQ}}(t) = \frac{V_{\text{DIFF}}(t)}{R_{\text{sense}}}, \quad V_{\text{DIFF}}(t) = V_{\text{DIFF,raw}}(t) - V_{\text{off}}. \tag{6}$$

R_{sense} denotes the external sensing resistance. Because the integrated coil presents only $R_{\text{AC}} \approx 1.03\ \Omega$ and $L \approx 0.444$ nH (Section 2.5), its terminal voltage at the measured slew targets is in the mV range. The sensing-load reconstruction therefore captures the driver-output current that would flow into the integrated coil, and the small coil voltage is negligible against the driver compliance. The reconstructed I_{EQ} verifies command-dependent driver-output modulation under the sensing-load condition. As shown in Figure 6, the sensing-load terminal voltage is captured on a Keysight DSOX2004A oscilloscope, and the driver rail is supplied by a Keysight E3647A DC source. The 1 Ω and 1 kΩ sensing resistors are metal-film types rated to ±1% tolerance. Together with the oscilloscope amplitude accuracy, this bounds the reconstructed-current uncertainty to within about ±5%.

2.5. Substrate-Aware Electromagnetic Simulation

The electromagnetic model compares the idealized no-p-substrate air case with the grounded-p-substrate CMOS stack case. The field metric is evaluated on an observation plane 15 μm above the top-metal coil surface, following prior asymmetric micro-coil simulations [11]. The geometry comprises the top-metal copper coil, the oxide/passivation stack, and the p-type silicon substrate with its epitaxial layer (Figure 5b). The grounded-p-substrate and no-p-substrate cases isolate the substrate contribution. The COMSOL setup is summarized in Table 2. The wafer-stack layer thicknesses follow the foundry process design kit and are not disclosed.

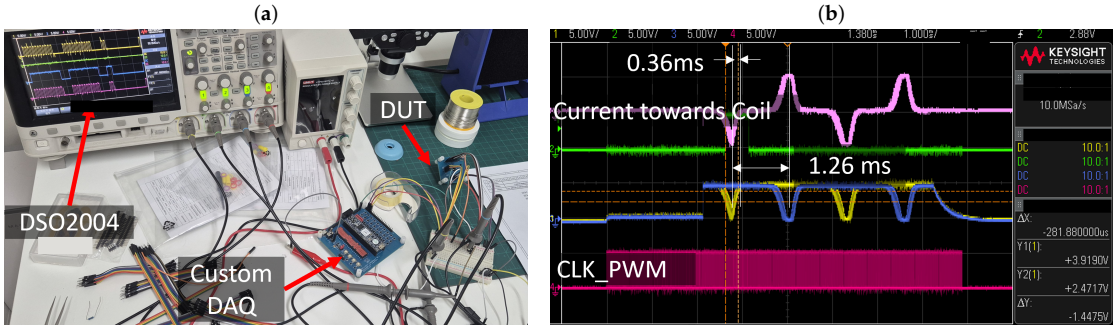

Figure 6. Measurement setup for sensing-load driver-output reconstruction. (**a**) Bench setup with the Keysight DSOX2004A oscilloscope, the Keysight E3647A DC source, the custom data-acquisition board, and the device under test. (**b**) Representative capture of the reconstructed current toward the coil together with the CLK_PWM control signal.

Table 2. Substrate-aware electromagnetic simulation setup.

Setting	Value
Formulation	Magnetic and Electric Fields (mef) A–V (magnetic vector potential **A**, electric scalar potential V)
Coil model	Numeric, single-turn
Study	Coil geometry analysis, then frequency domain at f_{ref} Time-dependent triangular run for waveform validation
Boundary conditions	Outer air: magnetic insulation ($\mathbf{n} \times \mathbf{A} = 0$) Grounded case: substrate bottom ground ($V = 0$) No-substrate case: substrate replaced by air
Coil (Cu)	$\sigma = 5.998 \times 10^7$ S/m
p^+ substrate	$\sigma = 1 \times 10^4$ S/m, $\varepsilon_r = 11.7$
Epitaxial layer	$\sigma = 0.2$ S/m, $\varepsilon_r = 11.7$
Oxide (SiO_2)	$\varepsilon_r = 3.9$
Passivation (Si_3N_4)	$\varepsilon_r = 9.7$
Mesh	Free tetrahedral, predefined coarse, refined around the coil 59,043 elements (+13,401 boundary triangles)
Solver	Direct, relative tolerance 1×10^{-3}
Time-dependent run	Triangular drive, period 1.32 ms (medium slew, $I_{\mathrm{tri}} = 6.4$ mA) Time step period/200 = 6.6 µs over two periods, strict steps

Low/medium/high sinusoidal excitation cases are normalized from measured slew targets $S_{\mathrm{meas}} = 0.00910/0.0194/0.0529$ mA/µs at $f_{\mathrm{ref}} = 390.625$ Hz, corresponding to $I_{\mathrm{pk}} = 3.72/7.91/21.6$ mA. The corresponding coil terminal-voltage magnitudes are 3.85/8.18/22.3 mV and the coil powers are 7.15/32.3/240 µW, which define the excitation cases for the substrate-transfer comparison. The reference frequency is used as the slew-equivalent sinusoidal fundamental of the linear electromagnetic model, and each I_{pk} is the sinusoidal peak that reproduces the measured slew at this frequency ($I_{\mathrm{pk}} = S_{\mathrm{meas}}/2\pi f_{\mathrm{ref}}$). Following the frequency-domain field-simulation approach of prior micro-coil studies [11], this representative sinusoid is preferred over a full time-domain triangular drive because resolving the triangular waveform would demand a much finer transient solution, while a single fundamental keeps the low/medium/high-field study within a practical simulation budget. In addition, matching the peak to the measured slew preserves the dominant dB/dt that sets the induced field, so the triangular drive is represented by its slew-equivalent sinusoid at f_{ref}. To check this, we ran a time-dependent simulation driven by the triangular pulse for the grounded medium case and compared it with the sinusoidal result. The two edge-normal $\partial E_x/\partial x$ distributions keep almost the same spatial shape, and their peaks differ

by only about 13%. Since the gradient distribution is preserved between the two drives, the substrate-transfer ratio that defines the substrate-aware metric is governed mainly by geometry and is largely insensitive to the drive waveform, so the sinusoidal approximation does not bias the retained-fraction comparison. The extracted coil parameters at this frequency, $R_{AC} = 1.03\ \Omega$ and $L = 0.444$ nH, are obtained from the electromagnetic model of the laid-out coil geometry (Figure 5a), where the frequency-domain and time-dependent studies agree. An impedance measurement over 1–10 MHz, presented in Section 3.3, confirms that the coil stays resistive and non-resonant across the excitation band.

3. Results

3.1. Fabricated Chip and Driver-Output Programmability

The proposed SoC was fabricated in a 0.18 µm CMOS process. The chip in Figure 5c occupies 2×1 mm^2, and the core circuit occupies 500×500 µm^2. Figure 7 shows representative reconstructed waveforms under the 1 kΩ sensing load.

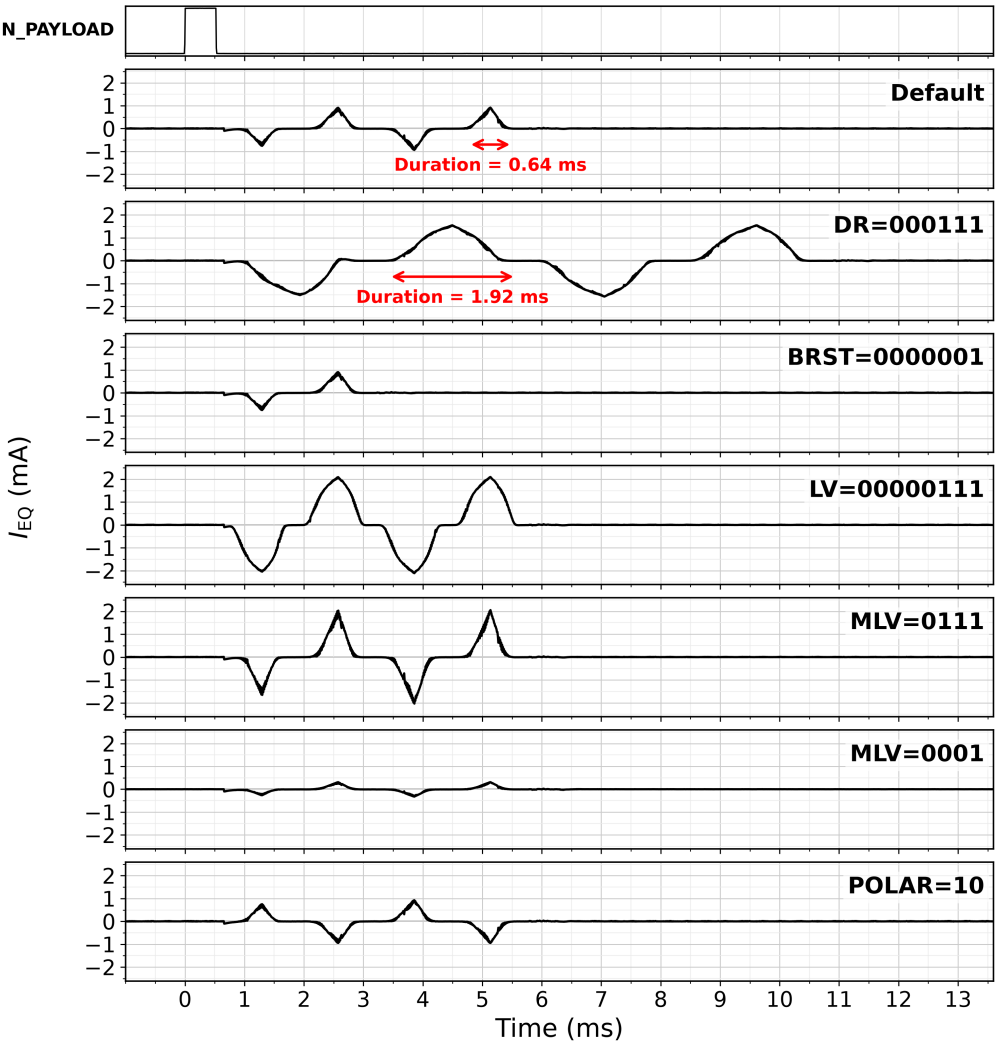

Figure 7. Representative timing reference and reconstructed I_{EQ} under the 1 kΩ sensing load for selected stimulation-parameter settings. The horizontal axis is time (ms), and the displayed window differs per row with the decoded duration and burst count.

The sensing-load sweep verifies that the fabricated driver-output path responds systematically to the programmed fields. The LV and MLV sweeps modulate the reconstructed waveform amplitude, the duration field changes the nominal steering interval from 320 µs to 2.56 ms, the burst field changes the decoded burst count from 1 to 8, and the po-

larity field reverses the waveform direction. These results verify command-to-output programmability at the fabricated-chip output pads. The measured slew-target extraction gives $I_{pk} = 3.72/7.91/21.6$ mA for the low/medium/high-field-simulation cases. A complementary reconstruction at a 1 Ω sensing load matched to the coil resistance confirms that the driver still delivers its programmed output into the coil-equivalent load. The medium- and high-slew settings reproduce the expected slew-dependent bipolar current at 1 Ω (Figure 8), and the reconstructed output stays within the same current range when other sensing resistances are used. Circuit-level simulation of the driver reproduces the same load-dependent behavior in detail.

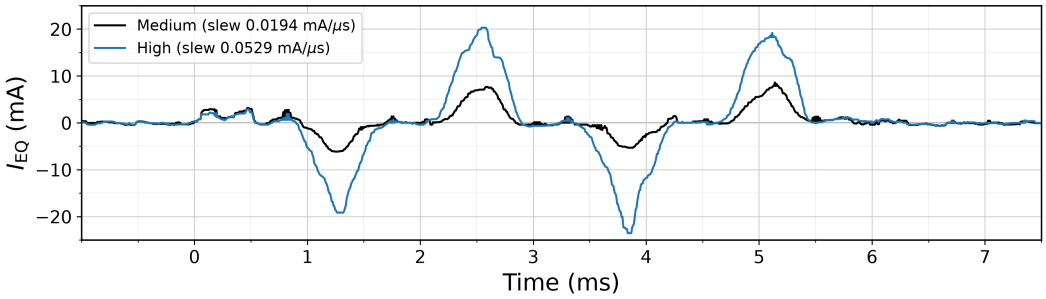

Figure 8. Reconstructed 1 Ω sensing-load current for the medium- and high-slew settings. The coil-equivalent 1 Ω load reproduces the slew-dependent bipolar drive current.

3.2. Substrate-Aware Field Simulation

The substrate-aware field analysis evaluates how identical coil-excitation normalization transfers to the electric-field-gradient metric in the integrated substrate environment. Figure 9 summarizes the analysis. Column (a) compares the edge-normal $\partial E_x/\partial x$ and $\partial E_z/\partial z$ components and overlays the triangular and sinusoidal drives for the grounded medium case, column (b) shows the substrate-transfer line cuts with the peak $|\partial E_x/\partial x|$ and the grounded-to-no-substrate retained ratio marked for each cut, and column (c) shows the low/medium/high-slew scaling. For a selected line cut, the peak gradient magnitude is

$$A_{pk}(c) = \max_{s \in \ell} |A_{F,x,c}(s)|. \tag{7}$$

The index c denotes either the no-p-substrate or grounded-p-substrate case. The retained peak-gradient fraction and the corresponding loss are

$$\eta_A = \frac{A_{pk}(\text{grounded})}{A_{pk}(\text{no-psub})}, \quad L_A = (1 - \eta_A) \times 100\%. \tag{8}$$

Using this definition, the edge-normal column cut at $x = 0$ retains 35.1% of the no-p-substrate peak $A_{F,x}$, corresponding to $L_A = 64.9\%$. The local coordinate system sets $x = 0$ at the selected coil edge and $y = 0$ at the lower edge reference. The lower and upper edge-parallel row cuts at $y = 0$ and $y = 85$ μm retain 37.5% and 40.5%, corresponding to losses of 62.5% and 59.5%, respectively. The peak $|\partial E_x/\partial x|$ values in Table 3 are the line-cut maxima plotted in Figure 9. The grounded-p-substrate low/medium/high-excitation sweep gives monotonic peak-map $A_{F,x}$ values of 0.00817, 0.0174, and 0.0474 V/m^2, corresponding to normalized scaling of 0.470/1.00/2.72. The high-slew grounded case reaches 95.5–110% of the medium no-p-substrate line-cut peaks.

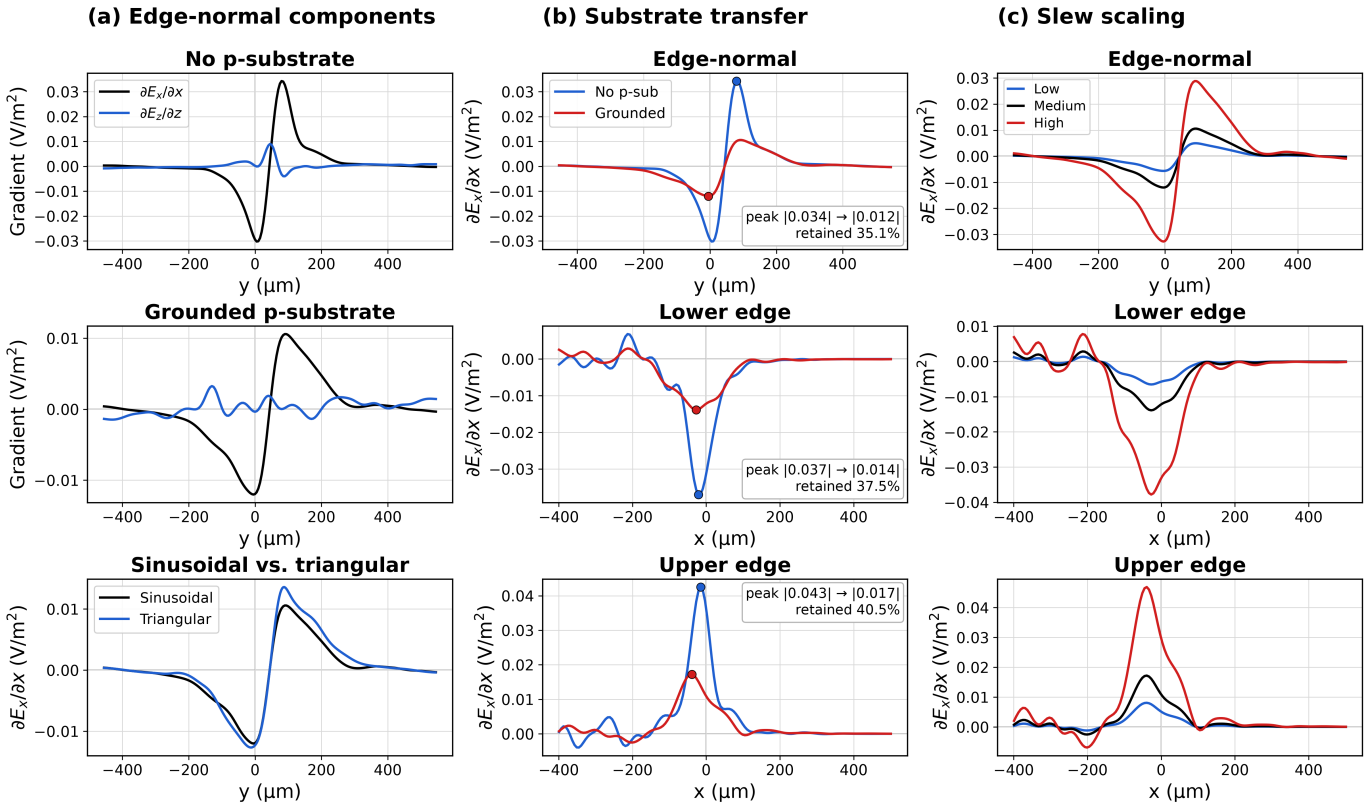

Figure 9. Electric-field-gradient line cuts for (**a**) edge-normal components, (**b**) substrate transfer, and (**c**) slew-dependent scaling.

Table 3. Substrate-induced peak-gradient loss extracted from $\partial E_x/\partial x$ line cuts. Peak $|\partial E_x/\partial x|$ values are in $\mathrm{V/m^2}$.

Line Cut	No p-Sub Peak	Grounded Peak	Retained η_A	Loss L_A
Edge-normal $x = 0$	3.43×10^{-2}	1.20×10^{-2}	35.1%	64.9%
Lower edge $y = 0$	3.70×10^{-2}	1.39×10^{-2}	37.5%	62.5%
Upper edge $y = 85$ μm	4.25×10^{-2}	1.72×10^{-2}	40.5%	59.5%

3.3. Coil Impedance Measurement

The coil impedance was measured over 1–10 MHz with a short-open-load correction (Figure 10). The corrected terminal impedance magnitude is about 32 Ω, resistive and almost frequency-independent, with a reactance below 0.4 Ω across the band. This flat resistive value reflects the packaged access path through the shared supply rails and pad structures rather than the coil itself, so the coil's own low-ohm impedance cannot be resolved from the external pins. The intrinsic coil resistance is taken from the COMSOL model (Section 2.5), and a sheet-resistance estimate of the coil geometry gives a consistent DC resistance of 1.80–2.71 Ω. Because ωL is only about 0.03 Ω at 10 MHz, far below R_{AC}, the coil quality factor stays well below one and the coil is resistance-dominated across DC–10 MHz. No resonance appears up to 10 MHz, so the self-resonance lies well above the operating band, and substrate-induced quality-factor degradation and self-resonance fall outside the excitation band.

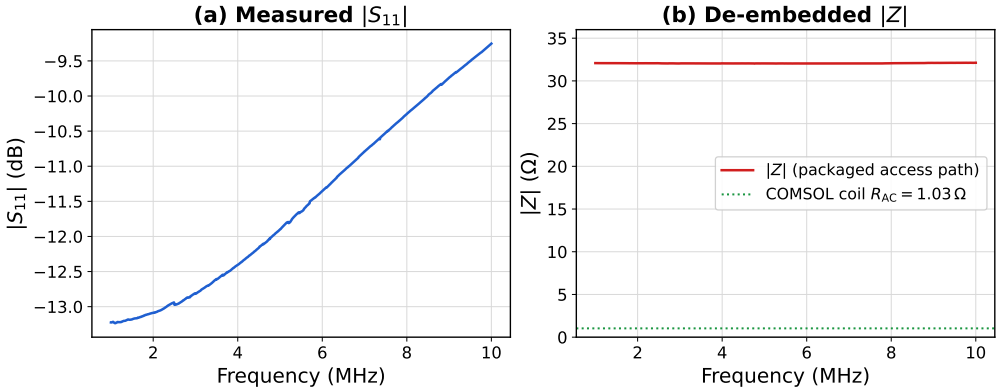

Figure 10. Coil impedance validation. (**a**) Measured $|S_{11}|$ of the packaged coil over 1–10 MHz (blue trace), monotonic with no resonance in the band. (**b**) De-embedded terminal impedance magnitude.

4. Discussion

The measured and simulated results define the CMOS integration boundary at the circuit-and-field level. The sensing-load sweep shows that decoded command fields map to driver-output amplitude, duration, burst count, and polarity. This supports the dust-scale protocol direction because a single received frame can be converted into local stimulation parameters without streaming an externally generated waveform.

CMOS integration changes the field-transfer boundary because the top-metal coil is separated from the target plane by oxide/passivation layers and grounded silicon. Under matched excitation normalization, the grounded substrate retains 35.1–40.5% of the no-p-substrate peak $A_{F,x}$ in the evaluated line cuts. This 35.1–40.5% spread is the spatial variation across the three evaluated line cuts of a single deterministic simulation model ($N = 1$), not device-to-device variability, so no multi-chip statistics are implied. The slew sweep shows that this substrate penalty appears as a driver-margin requirement because the high-slew grounded case approximately recovers the medium no-p-substrate peak-gradient level. Increasing the excitation raises the extracted coil dissipation from 32.3 to 240 µW, while the high-case terminal-voltage magnitude remains 22.3 mV. The mV-scale coil terminal swing indicates that supply headroom is dominated by driver bias and switching margins rather than by the coil voltage itself, leaving room for lower-voltage digital-control and receiver operation where those margins permit. The reported substrate-transfer metric is therefore used as an interface-level design margin rather than as a direct biological activation threshold.

Table 4 positions this work against prior magnetic-stimulation systems and micro-coil drivers. The distinguishing feature is the integration level. Command decoding, triangular current generation, and the micro-coil are co-integrated in CMOS with substrate-aware field verification, whereas prior micro-coil demonstrations drive the coil from external or bench-top instruments. Compared with the portable arbitrary pulse generator of [16], which generates the coil current externally, the present driver produces $I_{\mathrm{pk}} = 3.72$–21.6 mA on-chip from digital command fields. The reconstructed coil-current range and slew targets are comparable to those used in prior intracortical micro-coil studies [9,11,13]. However, because no biological activation was measured, the sufficiency of the induced field for neural activation is not claimed and is deferred to future in vitro validation. For implantable use, the low coil dissipation (7.15–240 µW) produces negligible local tissue heating at the coil, and the burst duty cycle further limits the deposited energy. The measured total SoC power is about 41 mW at $V_{\mathrm{DD}} = 4.55$ V, and the digital control logic accounts for most of it, with the triangular driver drawing about 3.89 mW and the clock-data recovery and I/O ring taking a smaller share. Referenced to the coil dissipation, the driver efficiency is about 6.2%, which is low because the stage forces current into a low-impedance micro-coil. In contrast to

the μW-scale coil heat, this 41 mW total is set by the digital logic, so continuous full-power operation would raise the on-chip power density and local heating. Burst duty-cycling and digital power-gating are therefore needed to keep the average dissipation and temperature rise low before implant deployment.

Table 4. Comparison with prior magnetic-stimulation systems and micro-coil drivers.

Work	Process/Platform	On-Chip Driver	Peak Coil Current	Induced $\partial E_x/\partial x$ (V/m^2)	Power	Substrate-Aware EM
Basham 2009 [7]	Discrete (PCB)	No	N/A (di/dt only)	N/A	N/A	No
Bonmassar 2012 [8]	Bench instrument	No	∼±10 A (limit)	N/A	N/A	No
Lee 2016 [9]	External driver	No	∼1 mA (sim), 7–74 mA	$\sim 5 \times 10^4$	0.4–10 mW	No
Lee 2021 [13]	External driver	No	∼1 mA (sim), 72–430 mA	$1.8–5.7 \times 10^3$	1.9–3.9 mW	No
Bloom 2024 [16]	Portable (PCB)	No	25 mA–5 A	N/A	N/A (sys. 40 W)	No
This work	**CMOS SoC,** 0.18 μm	**Yes (C-V-C)**	3.72–21.6 mA	0.00817–0.0474	**coil** 7.15–240 μW, **SoC 41 mW**	**Yes (**35.1–40.5%**)**

N/A, not applicable or not available. Bold entries denote this work.

For further miniaturization, CMOS integration provides the path from external waveform hardware toward addressable on-chip magnetic stimulation. The interface quantities established here are decoded waveform programmability, slew-normalized excitation, and substrate-aware gradient transfer. These quantities form the circuit and field-design basis for later integration of the receiver, package, and biological validation steps.

5. Conclusions

A fabricated substrate-aware CMOS magnetic-stimulation SoC was demonstrated with ASK-compatible command decoding, FSM/register control, a current–voltage–current triangular driver, and a bent top-metal micro-coil. Sensing-load reconstruction verifies captured command-to-output waveform programmability. Measured low/medium/high-slew targets of 0.00910/0.0194/0.0529 mA/μs and $I_{\mathrm{pk}} = 3.72/7.91/21.6$ mA define the normalized field-simulation cases. The grounded p-substrate retains 35.1–40.5% of the no-p-substrate peak $A_{F,x}$, establishing substrate-induced gradient-transfer loss as a compact design-margin metric for CMOS-integrated magnetic stimulation. A quantitative driver comparison, the measured total SoC power of about 41 mW, and a coil-impedance measurement confirming resistive in-band operation frame the system-level cost of this integration. These results support a CMOS MSTI path in which protocol decoding, waveform generation, and substrate-aware coil design are treated as one integrated interface.

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