

Article

Integrated Satellite Avionics with High Reliability and Low Cost Based on a Monolithic System-on-Programmable-Chip

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Abstract

Satellites become critical to space exploration, global communication, Earth observation, and navigation. There is a growing need for satellite avionics that are highly integrated, reliable, and low-cost, which is essential for mass production and reliable on-orbit operation. This work demonstrates integrated satellite avionics with high reliability and low cost based on a monolithic programmable system-on-chip (SoPC) through highly synergistic hardware–software co-design, with successful on-orbit validation. The system highly integrates satellite management, attitude and orbit control, power management, telecontrol and telecommand (TC&TM), and data storage into a monolithic PolarFire® SoC (System-on-Chip), and leverages an asymmetric multiprocessing (AMP) architecture. It achieves significant reductions in size, weight, power, and cost (SWaP-C) while ensuring comprehensive functionality and operational reliability. The Jilin-1 Gaofen-05A mission verified the proposed SoPC-based satellite avionics for low Earth orbit (LEO) commercial satellites. Long-term telemetry data confirms its stable operation, with a bus voltage ranging from 11.4 to 12.3 V, an average power consumption of 33.4 W, and a solar array output current of 6.2–6.5 A, all of which meet the design expectations. This work offers a feasible technical approach and engineering reference for commercial integrated satellite avionics featuring high reliability and cost efficiency.

Keywords: satellite avionics; high reliability; low cost; integrated architecture; hardware–software co-design; on-orbit validation



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1. Introduction

Satellite technology plays a vital role in key fields such as communications, navigation and Earth observation, serving as a core platform for human space exploration as well as the acquisition of space-based information and services [1,2]. Low-cost LEO satellites have been rapidly developed due to their significant advantages in affordability and rapid deployment in recent years [3,4]. Emerging commercial aerospace enterprises, such as SpaceX, Planet, and Capella, have achieved high-frequency, low-cost communication coverage and Earth observation capabilities by establishing large-scale, mass-produced commercial LEO satellite constellations. The total number of LEO satellites launched globally has now exceeded 10,000, and the launch rate continues to rise, marking the transition of this field from early-stage technological validation into a new era of scaled deployment [5]. The satellite avionics, defined as the core brain of satellites, are facing growing demands driven

by the industry's ongoing transformation [6–8]. To meet these demands, most current satellite avionics adopt a combination of Commercial Off-The-Shelf (COTS) components and traditional discrete architectures. COTS components offer advantages in cost and availability, while discrete architectures separate different functions into standalone modules connected via external buses. However, satellite avionics faces two critical engineering challenges under this situation. First, it is essential to address the reliability and space environmental adaptability issues of COTS components. Second, it is essential to resolve the performance and integration constraints in traditional discrete architectures.

Since 2010, some research institutions and commercial entities have consolidated satellite avionics and adopted COTS components [9], aiming to address the aforementioned challenges. For instance, the avionics of the Lunar Atmosphere and Dust Environment Explorer (LADEE) adopted a modular, universal spacecraft platform [10]. By adopting a modular approach for electronic components and systems, it achieved greater functional integration and substantially reduced the number of traditional standalone units, thereby alleviating the performance and integration constraints of discrete architectures. In 2017, Liu Kaijun et al. developed a commercial onboard computer based on the automotive-grade microcontroller (MCU) TMS570LS3137 [11]. The system's reliability was significantly enhanced through the implementation of triple modular redundancy (TMR) and related fault-tolerant techniques, directly addressing the reliability and space environmental adaptability of COTS components. In 2021, the CompuLab COMEX-IE38 module, an Intel Atom CPU-based system onboard the Mars rover Perseverance, successfully completed its scientific mission after the rover's landing [12]. In 2025, the radiation-hardened space computer onboard the Blue Ghost 1 satellite, developed by Resilient Computing based on the Xilinx 7A-200T FPGA chip, has been operating nominally in orbit [13]. These satellite avionics represent significant improvements over traditional designs and provide crucial technical references for overcoming the reliability concerns of COTS components and the integration limitations of discrete architectures. Such practices offer significant advantages, including cost reduction, optimized satellite avionics topology, minimized interface constraints, and accelerated development and debugging processes [14–16].

Although these institutions and researchers have achieved on-orbit success in developing avionics using COTS components, further improvements can still be made in two key areas. A primary challenge is improving the system reliability of integrated satellite avionics built upon COTS components. The lack of radiation characterization data regarding the degradation of non-space-grade components in the space environment obscures the accurate prediction of on-orbit operational lifetime. This uncertainty introduces reliability risks for critical hardware, such as the main processor and program memory. While hardware redundancy is a common mitigation strategy, adding shielding and redundant modules significantly increases system volume, weight, and power consumption [17–19]. Another limitation is the system's reliance on a traditional discrete architecture, in which each functional module is developed as a standalone unit [20–22]. As a result, the communication bandwidth between these units is constrained by the space-grade connectors and high-speed harnesses required for the space environment, components that add considerable mass and thereby increase overall system weight [23,24]. Furthermore, the reliability of the necessary transceivers adds complexity. These factors impede the system from fully leveraging the capabilities of highly integrated circuits. In this paper, we propose integrated satellite avionics based on a monolithic SoPC through highly synergistic hardware–software co-design. The satellite avionics employs a Flash-based FPGA, where the FPGA fabric of the SoPC is architecturally partitioned as a safety zone to monitor the on-orbit operation of its embedded CPU cores, thereby achieving a significant improvement in system reliability at a low cost [25]. This approach circumvents the challenges of achieving an

optimal trade-off among cost, performance, and space environment adaptability, which is caused by the lack of sufficient on-orbit flight heritage and radiation characterization data for COTS components [26,27]. Furthermore, distinct from conventional approaches that only achieve basic functional aggregation [28–31], all satellite avionics functions are integrated into a monolithic SoPC, through meticulously designed system architecture and software development. The system architecture is optimized in four dimensions: functional integration, power allocation, data interaction, and software development. This enables all satellite avionics functions to be integrated and fully exploit the capabilities of the high-performance SoPC.

Compared with conventional satellite avionics, this system adopts a monolithic SoPC with AMP architecture that decouples hardware and software and multiple functions, supporting dynamic reconfiguration and diverse mission adaptation. This design reduces system coupling and significantly enhances software flexibility. Moreover, the design avoids the “barrel effect” of tolerance to the space environment caused by the use of COTS components. In addition, software modules with different functions communicate via the on-chip bus, resulting in the advantage of extremely high bandwidth and high reliability. Finally, the proposed monolithic SoPC-based integrated satellite avionics has been successfully deployed on the Jilin-1 Gaofen-05A satellite. Its efficient and reliable on-orbit operation validates the rationality and feasibility of the design. The system effectively overcomes the drawbacks of traditional space avionics: (1) Architectural innovation for reliability: Instead of relying on costly radiation-hardened components or heavy redundant modules, we leverage the inherent SEU immunity of Flash-based FPGA to construct a hardware safety zone, achieving high reliability at low cost. (2) Holistic integration: We break the traditional discrete architecture by integrating all major avionics functions (OBC, AOCS, TC&TM, Power, Thermal, Storage) into a single SoPC through hardware–software co-design, aiming to fundamentally reduce SWaP-C. (3) Systematic COTS assurance: We implement a hierarchical screening strategy to enable the safe adoption of COTS components. To validate this design, a comprehensive ground test campaign and a long-term on-orbit experiment were conducted.

2. The Design of the Integrated Satellite Avionics

2.1. Safety Zone Design with Flash-Based FPGA

To enhance the space environmental reliability of satellite avionics, we conduct a systematic analysis of the space environment's effects on electronic components. This analysis aims to identify the key factors influencing the tolerance of different processor chips to the space environment, such as the fabrication process, technology node, manufacturing reliability, and operating environment. However, chips manufactured with specialized radiation-hardened aerospace processes are expensive, while processors relying on outdated process nodes lack the necessary performance. Flash-based or anti-fuse FPGAs offer a distinct advantage. Their unique physical structure provides enhanced tolerance to high-energy particles in space, making them virtually immune to single-event upsets in the logic configuration cells [32–36]. Due to their high reliability and cost advantages, Flash-based FPGAs stand out as COTS components that offer the optimal reliability-cost ratio for modern satellite avionics. Furthermore, employing advanced commercial processes, Flash-based FPGAs offer higher maximum clock frequency, smaller cell area, lower static and dynamic power consumption, and lower cost than traditional radiation-hardened FPGAs. They are nearly immune to configuration single event upset (SEU), feature high single event latchup (SEL) thresholds, and start immediately upon power-up. Although their total ionizing dose (TID) tolerance is slightly inferior, it remains sufficient for LEO orbits. Therefore, the satellite avionics adopts a Flash-based FPGA as its safety zone. A

system architecture is designed leveraging this component's superior radiation tolerance, which enhances robustness and performance in the space environment. The safety zone architecture is shown in Figure 1.

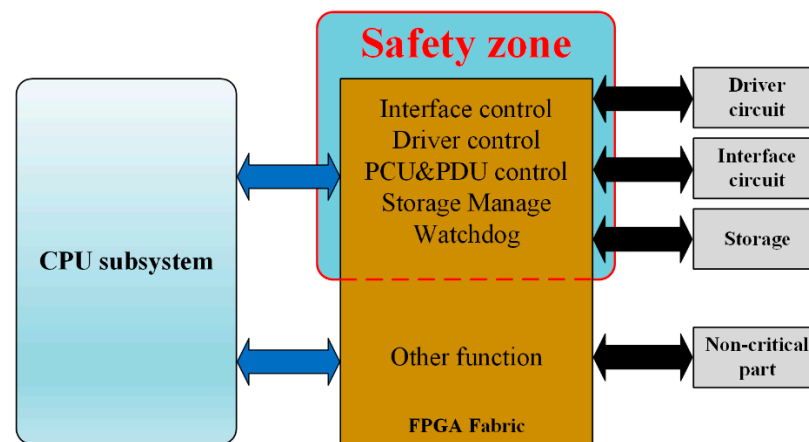


Figure 1. Safety zone architecture.

We adopt a fault-tolerant mechanism that safeguards complex systems with a trusted minimal zone. This reliable, isolated, minimized safety zone provides a safe base for system fault detection, isolation, and recovery, thereby ensuring the overall system survivability in various abnormal situations. Specifically, the FPGA fabric resources within the SoPC are configured to buffer all reconfigurable external output interfaces. This physically isolates the internal CPU core and other computing resources of the chip from the external interfaces. Consequently, any errors occurring in the CPU core can be detected and intercepted by the FPGA fabric, effectively containing the fault and preventing it from spreading.

A timed computing interface is implemented within the Flash-based FPGA; the CPU cores in the SoPC will access this interface within a specified timeout period and return the correct computed results to the FPGA as required. Through this mechanism, the FPGA fabric can monitor whether the CPU is running correctly. If the computation fails to complete on time or submits incorrect results, such a condition constitutes a defined CPU anomaly, and the FPGA will actively trigger a system reset for recovery. Compared to the traditional watchdog timer, this scheme not only fulfills the watchdog but also detects potential errors in the registers within the CPU and other computing resources through the computing process, which is a critical capability in the space environment. Meanwhile, critical operations are also entirely implemented within the FPGA fabric, such as power system initialization, health monitoring, fault diagnosis, watchdog management, and system reset. The safety zone also records the fault scene state. When the CPU core experiences an anomaly and resets, it maintains the system state prior to the fault, enabling the CPU to quickly resume operation from its previous state. Although the system has the capability of fault logging and fast recovery, some critical processes, including thermal control and power anomaly response, cannot tolerate system interruptions. Through design optimization, these functions are executed entirely by the FPGA, enabling uninterrupted operation from power-on.

2.2. The Integrated Satellite Avionics Architecture

Conventional discrete satellite avionics is constrained by limited inter-module transmission bandwidth, unsatisfactory SWaP-C performance and abundant failure nodes. To address these drawbacks, we propose a single-chip integrated satellite avionics architecture with a high-performance multi-core processor SoPC, the PolarFire SOC. This satellite avionics not only performs traditional onboard computer (OBC), but also integrates the

functionalities of the attitude and orbit control system, TC&TM system, thermal control system, power system, camera focusing system, and data storage system, by consolidating the hardware and software resources, as shown in Figure 2.

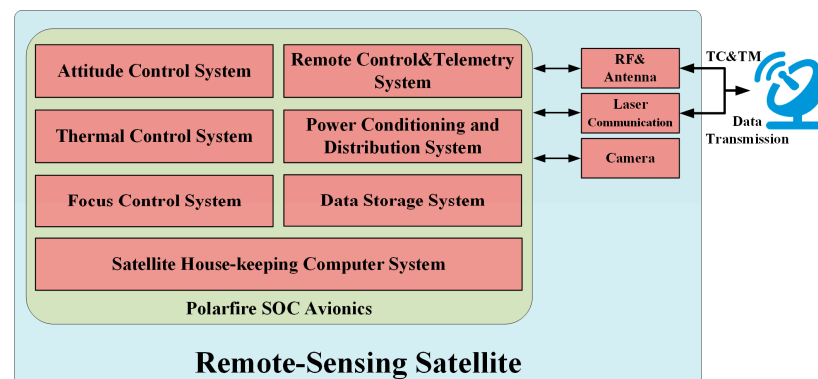


Figure 2. The satellite system architecture.

The integrated design is centered on the traditional OBC. Through hardware integration and software consolidation, an integrated architecture has ultimately been achieved. The minimum system of the PolarFire SoC is configured with 1 GB of LPDDR4 memory for software execution, 8 GB of eMMC storage for program and data storage, and an additional 1 Gb SPI Flash as backup memory. An external hardware watchdog (MAX706 TMJA, Analog Devices, Inc. (ADI), Wilmington, MA, USA) is employed to monitor system operation. For the attitude and orbit control system, the control and acquisition circuits for the flywheel are implemented by the FPGA fabric, with its control software running on an independent CPU core. The hardware control interfaces for the power and thermal control systems are entirely managed by the FPGA fabric, allowing the OBC software to modify configurations through the FPGA fabric as needed. For the TC&TM system, the baseband processing is implemented by the FPGA fabric with external ADC and DAC chips. After the external antenna down-converts the signal and sends it to the baseband, the OBC software interacts with the FPGA fabric to complete data uplink and downlink.

Two-star tracker sensors are connected to the PolarFire SoC's SerDes interfaces via GT links, and each star image processing algorithm is allocated to an independent dedicated CPU core for parallel execution. To facilitate data processing, the star sensor's original 10-bit pixel depth is extended to 16 bits with the lower 10 bits reserved as valid data. Accordingly, the single-frame star image size reaches $1280 \times 1024 \times 16$ bits, equivalent to 2.5 MB. Given the designed image acquisition frequency of 8 Hz, the raw data bandwidth of each star sensor is 20 MB/s. Data storage is handled by two SSDs connected to the PolarFire SoC via a PCIe interface, which is shared through a switch circuit. The SSD is mounted in PCIe Gen 2.0 $\times$ 4 mode, providing a theoretical bandwidth of 2 GB/s, which fully meets the bandwidth requirements of the camera. SSD read/write operations are directly executed by the FPGA fabric, with the OBC controlling data storage through interactions with the FPGA fabric. In terms of data transmission links, the single-channel rate of the downlink GT interface is configured at 5 Gbps. The laser communication link adopts two lanes to provide a 10 Gbps downlink bandwidth, while the X-band telemetry and command link occupies one lane at 5 Gbps to match the service data transmission demand. The overall satellite avionics architecture designed in this work is illustrated in Figure 3.

Figure 3. The satellite avionics architecture.

The overall system adopts a low-power design, which reduces heat dissipation requirements. Thus, the integrated satellite avionics utilizes a board-stacking architecture, which offers both simplicity and ease of assembly. It consists of three functionally independent printed circuit boards (PCBs), such as the central processor board, the interface board, and the power board. The central processor board integrates the core control circuit, TC&TM baseband, high-capacity storage module, and high-speed external interfaces. The interface board is primarily responsible for driving various peripherals, collecting status signals, and performing internal power conversion. The power board handles energy management, power distribution, and multi-stage voltage conversion tasks. All three PCBs are fabricated to identical dimensions of 200 mm $\times$ 85 mm and are interconnected via vertical pin board-to-board connectors for both signal and power transmission. This architecture greatly simplifies system debugging. The central processor and interface boards can be powered and tested independently using external supplies, while the power board's shunt regulation and conversion circuits can be validated on their own, without the other two boards. This loosely coupled structure not only enables parallel testing, accelerating the development process, but also establishes a foundation for scalable production and rapid system integration. The functional distribution and sketch of the satellite avionics are illustrated in Figure 4. The enclosure has an overall dimension of 233 mm $\times$ 103 mm $\times$ 61 mm and weighs less than 1.5 kg.

The integration of the satellite avionics enables it to accommodate various payload systems to execute different on-orbit missions. Therefore, a bus interface must be designed to connect the satellite avionics with these payload systems. Achieving sufficient system communication bandwidth requires a balance between the reliability of the communication bus and implementation costs under extreme environmental conditions and stringent resource constraints. Some aerospace-specialized buses, such as 1553B and SpaceWire, are developed to address such demands. However, these buses necessitate complex interface adaptation and protocol conversion, which increases system complexity. Additionally, these buses impose high demands on physical links, making them difficult to implement

at low cost. Thus, we adopt a monolithically integrated satellite avionics architecture, which addresses the issue by integrating the majority of systems into a single SoPC, thereby eliminating the need for external connections. For the small amount of information that still requires transmission, such as telecommand and telemetry data, the estimated maximum data throughput is only 10 KB/s. The PolarFire SoC chip integrates two CAN bus controllers, which, together with low-cost external interface chips, enable the construction of an enhanced dual-redundant CAN bus. This design avoids expensive space-grade dedicated buses and maximizes the use of components, significantly reducing system design cost while improving communication reliability through the dual-bus redundancy mechanism. The enhanced dual-redundant CAN bus requires only two low-cost transceiver chips in addition to the built-in controllers in the SoC, resulting in extremely high reliability, making it well-suited for LEO satellite applications.

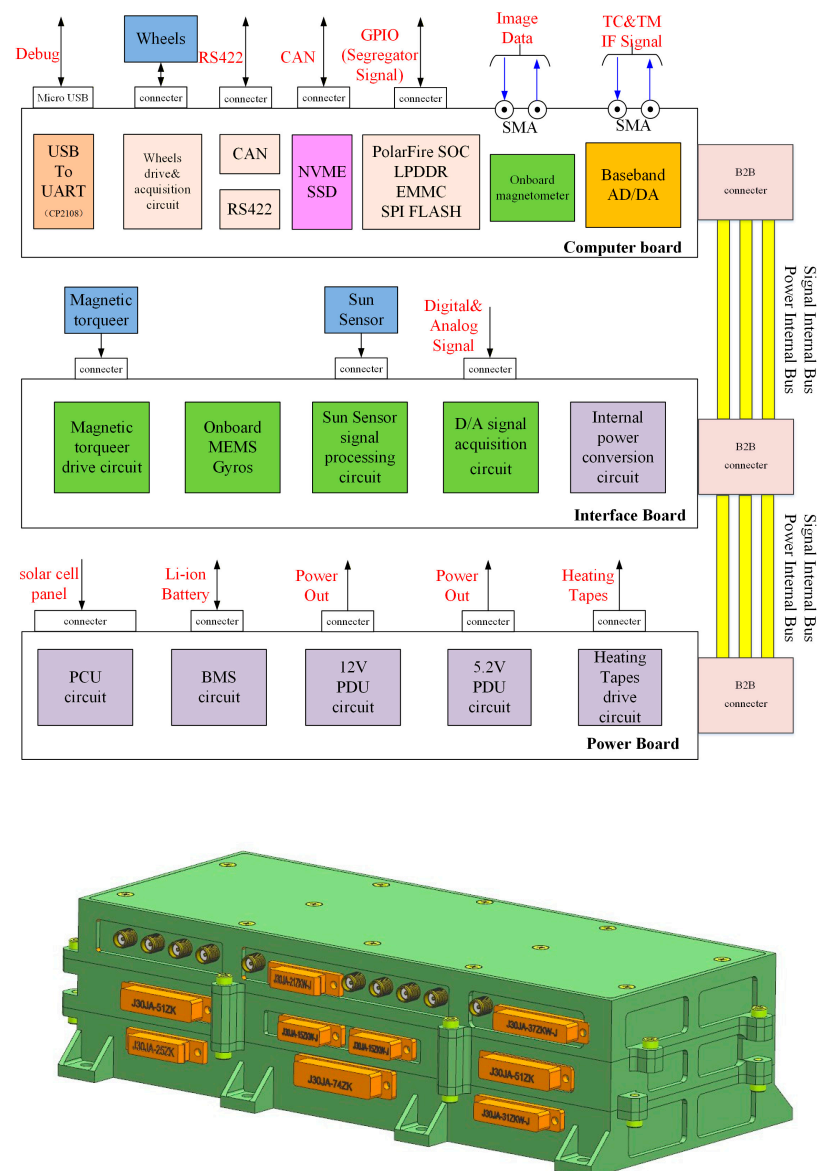


Figure 4. The structure of the satellite avionics.

The enhanced dual-redundant CAN bus based on a daisy-chain topology is used to establish a robust communication link between the payload system's equipment and the integrated satellite avionics; the connection method is shown in Figure 5. All nodes are connected in series via shielded twisted-pair cables, with resistors soldered at the

first and last nodes of the network. The bus employs a primary-backup hot redundancy scheme. The integrated satellite avionics acts as the master node, transmitting identical data simultaneously through two independent buses (Bus A and Bus B). It also receives signals from external devices via both buses and performs merge processing on the incoming data. When the master node finds that a designed number of errors have occurred on one of its buses cumulatively, it will perform a bus reset operation. Each external slave device node communicates over only one of the two buses at any time and can switch between the two buses autonomously. If no valid data is received on the currently active bus for six seconds sequentially, the node autonomously switches to another bus and repeats this process cyclically as needed. The unused bus interface is either reset or powered off to reduce system power consumption. By implementing redundancy at both the physical layer and the protocol layer, this design significantly improves the reliability and fault tolerance of the onboard bus communication network.

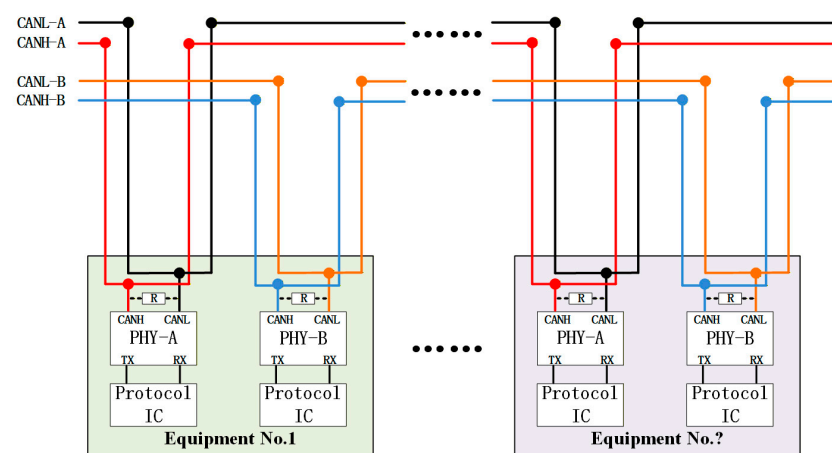


Figure 5. CAN bus interface diagram.

2.4. Power System and COTS Component Screening Strategy

The power system comprises solar panels, a lithium-ion battery pack, and the associated power control circuit. The schematic is shown in Figure 6. The solar panels choose triple-junction gallium arsenide (GaAs) solar cells with an average photoelectric conversion efficiency of no less than 30%. They can deliver an output current of 6.23 A at the end of life, under summer solstice conditions. The lithium-ion battery pack is assembled from commercial 18650 battery cells that have undergone rigorous consistency screening. These 18650 battery cells are configured in a parallel-series arrangement consisting of 6 cells in parallel and 3 groups in series, forming an onboard energy storage unit with a rated capacity of 15 Ah. This design not only ensures a reliable power supply but also achieves a comprehensive optimization of lightweight, low cost, and high energy density by incorporating high-efficiency solar cells and mature commercial 18650 battery cells.

The power system employs an unregulated bus voltage control strategy, where the bus voltage varies with the battery voltage during both sunlight and eclipse periods. This voltage is stably maintained within a range of 9 V to 12.3 V. Through precise charge and discharge management, the system regulates the battery cell's terminal voltage within a specific range between the minimum discharge voltage and the maximum charge voltage (3 V to 4.1 V). To efficiently manage the output of the solar array, the system employs Sequential Switching Shunt Regulator (S3R) technology. This regulator is capable of fully shunting the initial output current from the solar cell array. The shunt regulation unit utilizes a three-stage independent redundancy architecture. Each stage incorporates entirely independent control and power modules, delivering a per-stage shunt capability of 2.5 A.

These stages operate with hierarchical priority, achieved by setting different activation thresholds. Based on the on-orbit energy budget analysis, only two stages are necessary to guarantee power balance during normal operations. And the third stage acts as a hot redundancy. This configuration improves the reliability of the power supply system against fluctuating illumination conditions and certain fault modes.

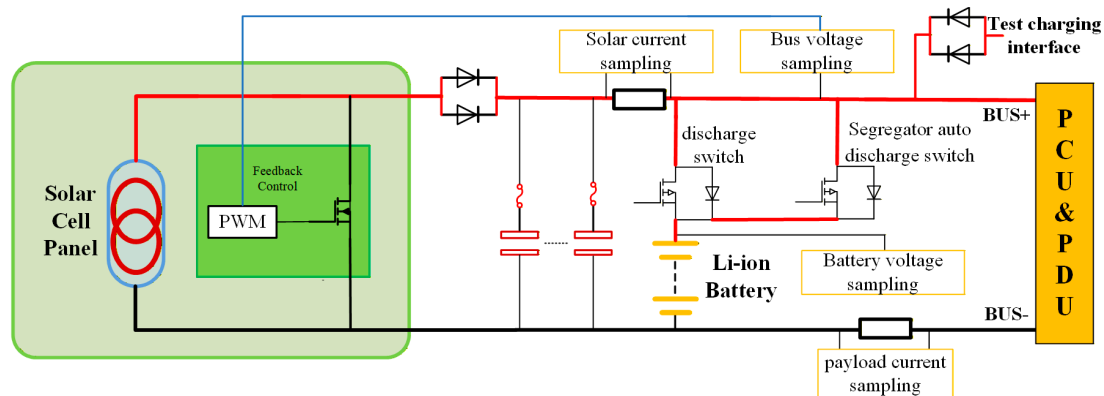


Figure 6. Power system diagram.

To address the concern regarding power management under extreme conditions, several safety designs have been integrated into the SoPC architecture. All controllable power distribution channels are initialized to the off state by the FPGA upon system reset. The distribution circuit is also off during cold start, ensuring external power can be disabled even if the control system fails. Software-based overvoltage and over-discharge protection trigger hardware handling first, followed by system reset if needed. Hardware-based over-discharge protection disconnects the battery when the voltage drops below a preset threshold. A self-diagnosis function monitors load current and automatically shuts down any channel that deviates from the normal range. To validate these designs, a 20 A short-circuit test was conducted. The results show a bus voltage fluctuation of only 652 mV, with power distribution automatically shut down 221 ms after the short circuit. The proposed non-regulated bus mechanism effectively handles drastic load variations, while the diagnosis mechanism enables rapid protection.

The power system utilizes commercial-grade 18650 lithium-ion cells as an alternative to traditional space-grade energy storage units. While space-grade batteries offer exceptional reliability, their customized production results in high costs and limited production capacity, which cannot meet the commercial satellite industry's demand for low cost and rapid supply. In contrast, the 18650 lithium-ion cells, as a highly standardized industrial commodity, offer the distinct advantages of massive annual production capacity, well-established supply chains, and low cost. And its reliability has been validated through years of large-scale commercial deployment. By performing rigorous consistency screening on commercial battery cells and assembling them into battery packs, the procurement cost can be reduced to approximately 1/40 that of traditional space-grade batteries. To validate the operational reliability of these 18650 lithium-ion cells for space missions, we develop a dedicated test scheme simulating the periodic charge–discharge cycling of battery packs in LEO satellites, and conduct systematic cycle life tests. This validation provides an empirical foundation for the low-cost, high-reliability application of commercial-grade 18650 lithium-ion cells in space missions. The discharge end voltage curve is shown in Figure 7.

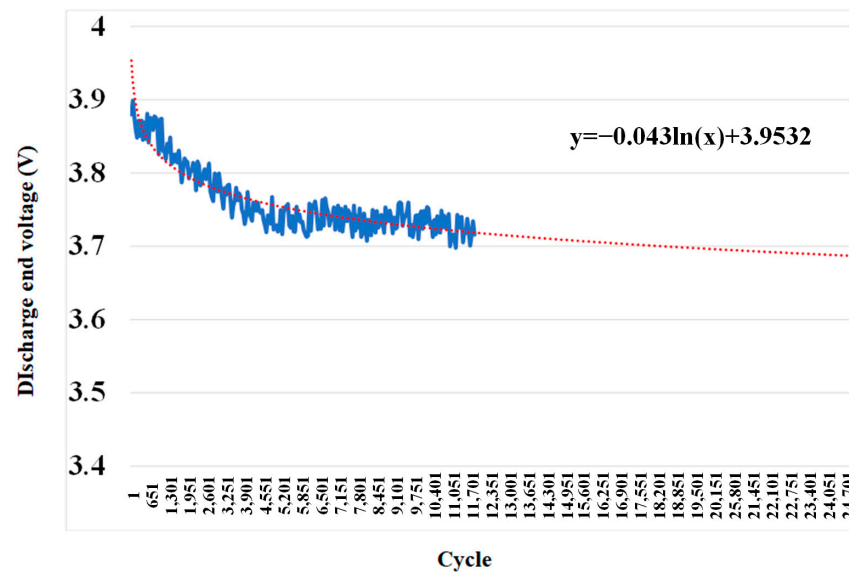


Figure 7. The discharge end voltage of each battery cell with different cycles, orbital period is 96 min, with sunlight time of 60 min.

Based on the above reliability test, the cell discharge voltage of the 18650 lithium-ion cells decreases significantly during the first 3000 discharge cycles, indicating severe performance degradation in the early stage. In the later cycling period, the fluctuation of discharge voltage is obviously reduced, and the performance degradation tends to be stable. Combined with the on-orbit condition of approximately 5000 charge–discharge cycles per year for LEO satellites, the lifetime prediction and curve fitting show that after five years of on-orbit operation, the discharge end voltage of each battery cell can still be maintained above 3.687 V, with the corresponding battery pack terminal voltage higher than 11 V. This can fully meet the voltage and energy supply requirements of the energy storage system throughout the satellite’s lifetime.

COTS components are adopted in the system, capitalizing on their short lifecycles and rapid functional iteration. To guarantee the reliable on-orbit performance of COTS components, a systematic protection against single-event effects (SEEs) is imperative. Hardware measures such as layout optimization, circuit redundancy, and watchdog timers enhance the system’s fault tolerance. In terms of software, self-diagnostic programs are combined with ground-based big data diagnostics to achieve coordinated space-ground fault tolerance. Additionally, rigorous derating practices are implemented during system design to mitigate component degradation and enhance operational reliability. To balance cost and reliability, we adopt a hierarchical screening strategy comprising board-level screening of assembled printed circuit boards and unit-level screening of non-standard equipment, aiming to identify early-life failures at a limited cost. A closed-loop failure analysis mechanism is established. When a batch-related quality issue is confirmed, the affected components are replaced and re-screened. For units where comprehensive screening is impractical, a sampling rate of 5–10% is implemented. Through these comprehensive measures, such as design, screening, and management, this system systematically constructs a reliability assurance framework tailored to the commercial satellite industry while adopting COTS components to achieve low-cost objectives.

2.5. Performance Comparison with Previous-Generation Avionics

To further evaluate the advantages of the proposed integrated design, a quantitative comparison is conducted between the avionics of the previously launched Jilin-1 Gaofen-03A satellite and the Jilin-1 Gaofen-05A avionics developed in this work. The data shows

that the proposed integrated design achieves improvements in many metrics. The design reduces cost by 80%, primarily by eliminating expensive controller and interface chips. The Integrated structure significantly reduces the number of independent modules and their interconnection harnesses, resulting in a 66% mass reduction and a 40% volume reduction. Meanwhile, the average power consumption decreases by approximately 30%, from 48 W to 34 W, owing to the elimination of multiple standalone controllers and transceivers. In terms of reliability, the Flash-based FPGA safety zone replaces the traditional hardware redundancy approach, providing a simpler approach and fewer potential failure points. This comparison quantitatively demonstrates the superiority of the monolithic SoPC design for cost-sensitive, mass-produced LEO commercial satellites. The key metrics are summarized in Table 1.

Table 1. Comparison table of two generations of avionics systems (excluding external passive components).

Feature	Jilin-1 Gaofen-03A Avionics	Jilin-1 Gaofen-05A Avionics (This Work)	Improvement
Architecture	OBC (Including AOCS) + TC&TM + Data Storage + Power modules	Single SoPC	Highly Integrated
Cost	75 k USD	15 k USD	80% cost down
Volume	150 × 120 × 140 mm	233 × 103 × 61 mm	40% reduction
Mass	4.5 kg	1.5 kg	66% reduction
Power consumption	Average 48 w	Average 34 w	~30% reduction
Reliability approach	Hardware redundancy design	Flash-based FPGA Safety Zone	Simpler, Fewer failure points

3. Design of the Software Architecture

3.1. AMP Software Architecture Design

The integrated satellite avionics trend towards a highly integrated architecture. However, relying solely on hardware integration is insufficient to achieve comprehensive system-level improvements. Therefore, the architecture for the satellite integrated avionics builds upon a highly synergistic hardware–software co-design, further enhanced by a highly integrated software solution. We adopt an AMP software architecture, where peripheral resources are statically partitioned and bound to designated cores, with loose coupling and inter-processor communication maintained via shared memory. The system comprises five processor cores. Upon power-on initialization, four U54 cores remain in a suspended state, while the E51 core runs the hardware service system (HSS) to bootstrap the remaining four U54 cores, which form an AMP computing cluster for task allocation and parallel processing per onboard software requirements. The basic architecture of this multi-core processor is illustrated in Figure 8.

In the AMP software architecture, the U54_1 core acts as the master core, forming a master-slave cooperative relationship with the other three U54 cores (U54_2/3/4). Inter-core communication is realized through shared L2 cache. The U54_1 core actively writes instructions and data requests to the shared area, while the other cores periodically query the area, execute corresponding tasks according to the instructions, and write back status and results to the shared cache. To prevent frequent interrupts caused by the abnormal operation of one core from interfering with other cores, the interrupt-based mailbox communication supported by the PolarFire SoC is not adopted in this design. Instead, a lightweight and reliable communication scheme based on shared memory is adopted. This scheme also serves as a method for the master core to monitor whether other cores operate normally.

Independent request-instruction zones and parameter reporting zones are allocated for each slave core in the L2 cache. Each zone is equipped with check bits and update flags. When any core performs a write operation, it will update the check information and refresh the flag bits to achieve reliable and confirmable communication, which ensures real-time performance while enhancing system fault tolerance. The main software data flow of the system is shown in Figure 9.

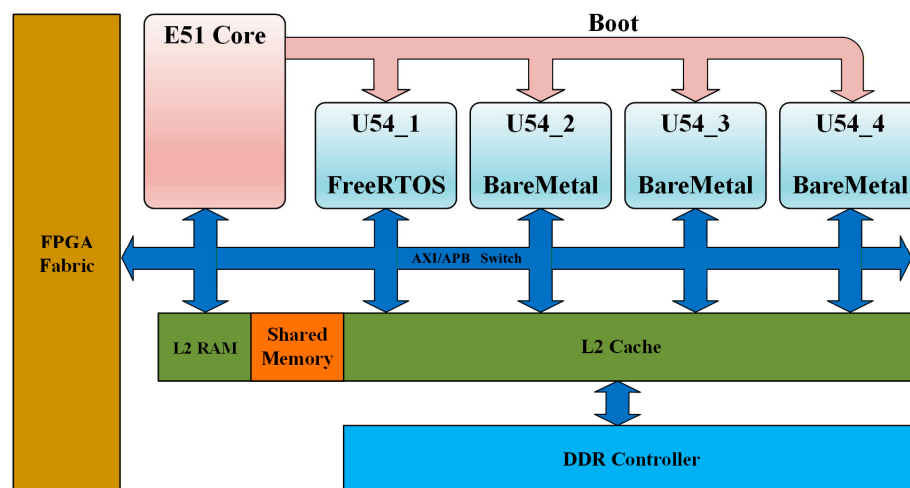


Figure 8. AMP software architecture.

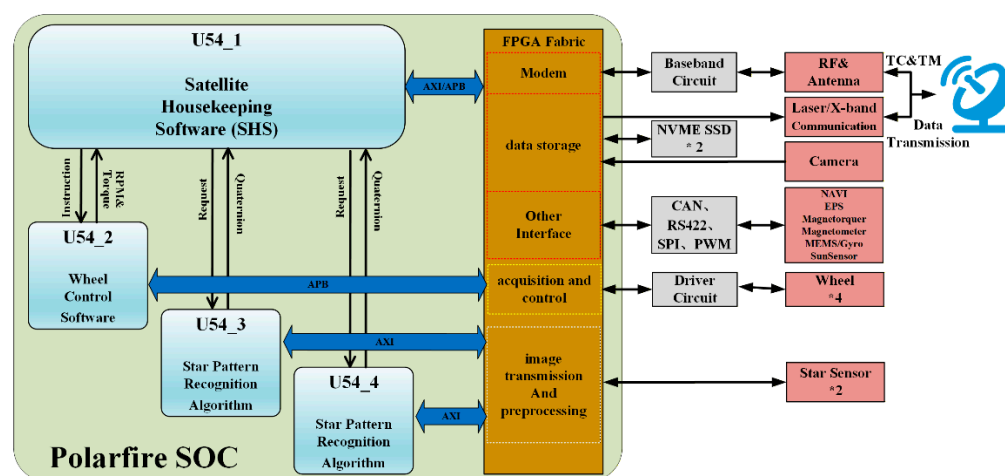


Figure 9. Software data flow.

The integrated satellite avionics implements a software-hardware collaborative integrated design based on the PolarFire SoC multi-core architecture. The E51 core runs in privileged mode, responsible for power-on initialization and booting the other application cores. After booting, it acts as a monitor to continuously check the status of the four U54 cores and the SoC hardware. To mitigate the impact of space single-event upsets on memory, the E51 core integrates a memory scrubbing function in its super-loop. By setting a reasonable scrubbing step, it periodically triggers the SECDED error correction mechanism to correct single-bit errors before they accumulate into multi-bit errors, significantly improving storage reliability. The U54_1 core, as the main application core, runs onboard management software based on FreeRTOS. It coordinates onboard data acquisition, task scheduling, communication management, power distribution, and thermal control. It also performs orbit and attitude control calculations, tele-command/telemetry processing, and autonomous fault diagnosis. This core communicates with peripherals via dedicated

CAN, UART, and SPI buses, and controls the FPGA fabric for data storage. The U54_2 core is dedicated to real-time flywheel control. Using a bare-metal program combined with an FPGA, it achieves high-frequency closed-loop control and status acquisition of the flywheel circuit, and reports data to the U54_1 core through shared memory. The U54_3 and U54_4 cores are, respectively, used for star tracker image processing. Each runs an independent image pipeline in bare-metal mode. The image acquisition is completed via DMA controlled by the FPGA, and attitude quaternions are solved and reported. This multi-core architecture achieves functional isolation and cooperative communication, ensuring real-time performance and reliability while realizing high integration of satellite platform management, attitude control, data storage, and other functions. To guarantee real-time performance, we established a budget-based task scheduling policy across the four U54 cores. The Worst-Case Execution Time (WCET) is budgeted to consume no more than 80% of the CPU utilization, leaving a 20% safety margin for system jitter and interrupt handling. The operational status of each application core is illustrated in Figure 10, and the software task requirements for each core are, respectively, summarized in Table 2.

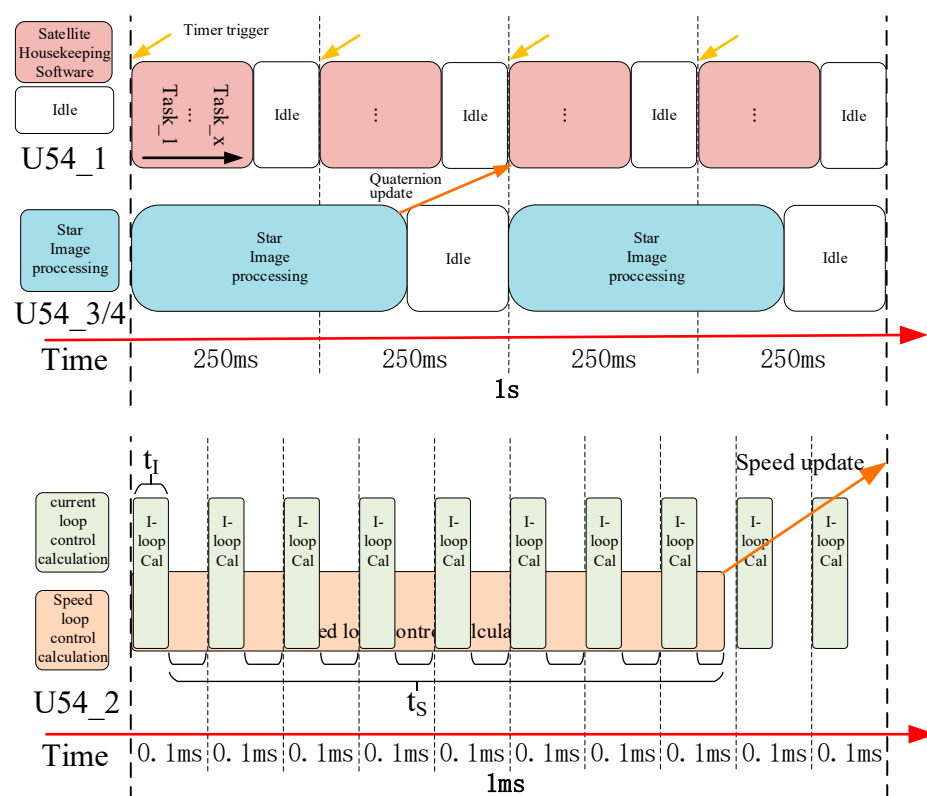


Figure 10. Timing diagram of application core software.

Table 2. Task WCET statistics.

Core	Task Function	Task Cycle/ Frequency	Execution Time (WCET)	CPU Utilization
U54_1	Satellite housekeeping & attitude control	250 ms (4 Hz)	≤200 ms	<80%
U54_2	Wheel control (current loop)	0.1 ms (10 kHz)	<0.04 ms	<80%
	Wheel control (speed loop)	1 ms (1 kHz)	<0.4 ms	
U54_3	Star tracker image processing	500 ms (2 Hz)	<400 ms	<80%
U54_4	Star tracker image processing	500 ms (2 Hz)	<400 ms	<80%

3.2. Program Reconfiguration Flow Design

The system boot process is divided into two stages. In the first stage, after satellite power-on, the compressed bootloader stored in the on-chip eNVM of the SoC is decompressed into the L2 LIM memory for execution. In the second stage, according to the software version corresponding to each U54 core, the bootloader loads the application program from external non-volatile memory, and eMMC is used preferentially. If eMMC fails or the stored content fails validation, the system automatically switches to SPI FLASH as the backup loading source. After the program image is moved to DDR, the bootloader starts each U54 core sequentially to complete the full-function initialization of the system. Through storage redundancy and version management, this design effectively improves the fault tolerance and autonomous recovery of onboard software in radiation environments. The system loading process is shown in Figure 11.

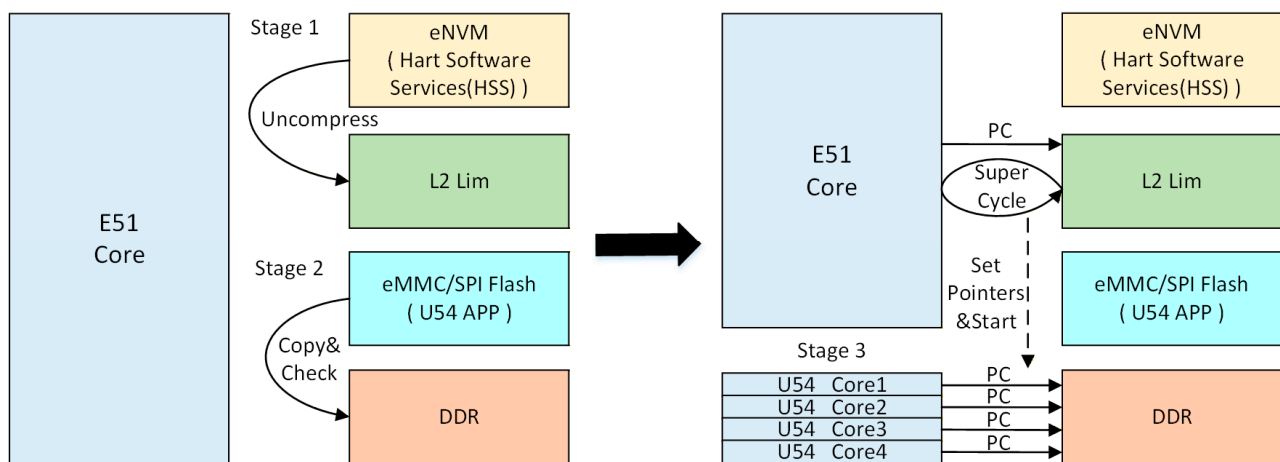


Figure 11. System loading process.

To address risks caused by on-orbit single-event effects, we adopt a single-program TMR storage architecture in program memory. The program storage architecture is shown in Figure 12. A multi-version program backup mechanism is established to retain reliable software recovery capability for on-orbit reconfiguration. Three versions are reserved for the satellite. Version 1 is the initial launch version, which is generally not updated to retain a fully tested and stable version. Versions 2 and 3 are used alternately for program upgrades. Since on-orbit program modifications are usually partial changes, with more than 95% of the program body unchanged, a full-image uplink is highly inefficient. Therefore, the open-source BSDIFF binary difference algorithm and LZMA compression algorithm are adopted in the program uplink scheme, which effectively reduces the uplink data volume from the megabyte level to the kilobyte level. A reliable fault rollback mechanism is also designed for the critical process of satellite on-orbit reconfiguration. During program upgrade, the target version is selected and updated via uplink. After all the uplinked data are verified correctly on the satellite, the version is replaced and indicated via telemetry. The ground can then modify the value of the Next Version Flag through tele-commands to set it to the successfully uplinked version. After an active reset, the satellite runs the new version. If the new version behaves abnormally, the system automatically reverts to the default version after reset, ensuring the operational safety of the satellite. The process of version upgrade switch is shown in Figure 13.

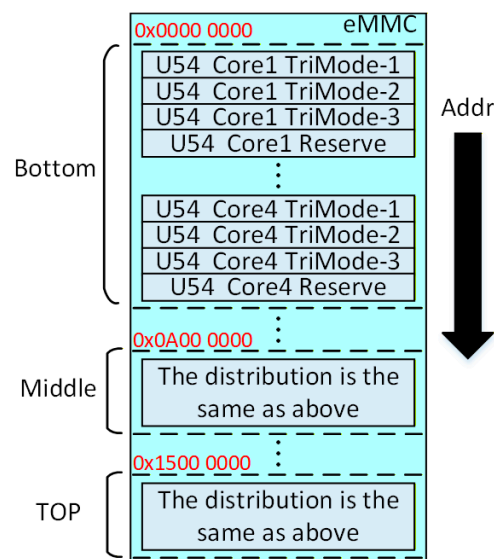


Figure 12. Program TMR storage architecture.

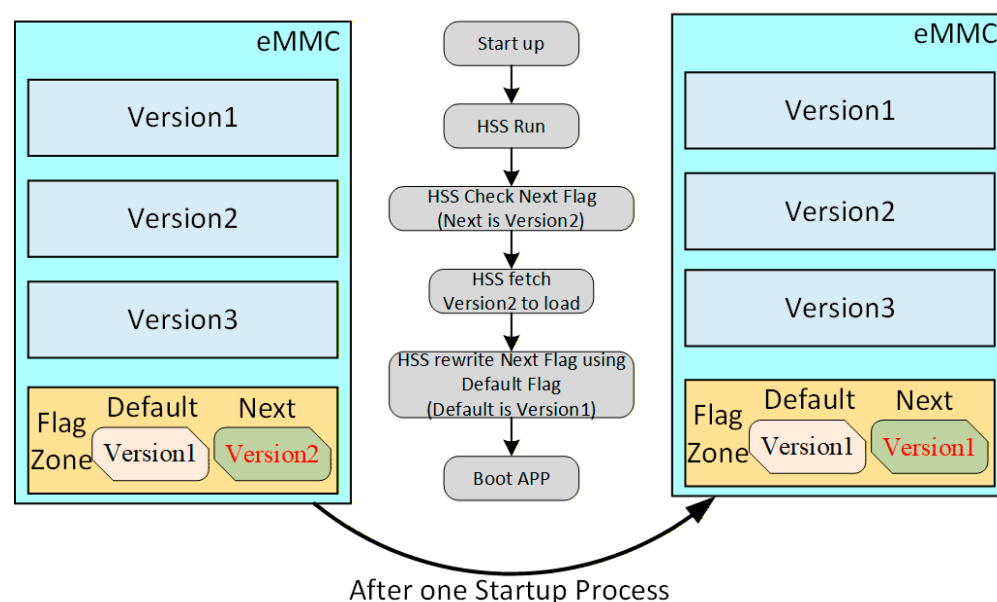


Figure 13. Version switch flowchart.

4. On-Orbit Performance Validation

The Jilin-1 Gaofen-05A satellite, equipped with the integrated satellite avionics designed in this paper, was successfully launched into its predetermined orbit at 13:30 on 15 June 2023, from the Taiyuan Satellite Launch Center aboard a Long March 2D (CZ-2D) carrier rocket. The initial orbital parameters are as follows: semi-major axis of 6923 km, inclination of 97°, eccentricity of 0.000214, and period of 5733 s. By November 2025, the satellite had been stably operating in orbit for 29 months, experiencing a total of 13,467 light–shadow cycles. During this period, the power system experienced zero abnormal power-down events, the redundant CAN bus switching success rate was 100% (252 switches in total), and the FPGA logic anomaly count was zero. During its on-orbit operation, the integrated satellite avionics has perfectly fulfilled all functions of satellite platform control with excellent performance indicators, fully verifying the feasibility and long-term on-orbit reliability of the designed integrated satellite avionics. The picture of the integrated satellite avionics is shown in Figure 14.

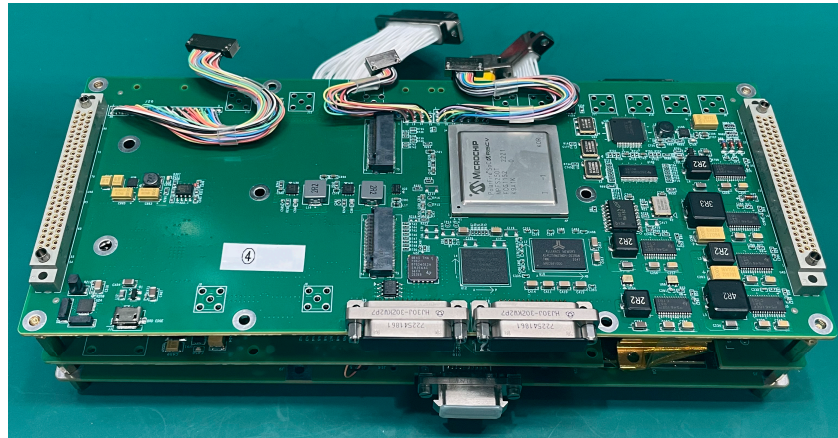


Figure 14. The integrated satellite avionics of Jilin-1 Gaofen-05A satellite.

4.1. On-Orbit Data Analysis of Power System

To verify the performance of the power system, we perform on-orbit data analysis on its bus voltage stability, solar array output characteristics, and total satellite power consumption. The test data indicate that all parameters of the power supply system meet the design expectations, the system operates stably and reliably, and can satisfy the energy demand of the satellite for long-term on-orbit operation.

Tests are performed on the bus voltage and battery pack voltage, where the designed index range of the bus voltage is 9 V to 12.3 V. A typical orbital arc on 3 August 2023 was selected for the test, and the variation trends of the bus voltage and storage battery voltage under the long-term operational conditions are shown in Figure 15a,b. The data shows that during the sunlight–shadow transition process, the bus voltage varies in the range of 11.4 V to 12.3 V (corresponding to a maximum depth of discharge of 26%), and the storage battery voltage varies between 11.5 V and 12.3 V. Both voltage levels remained consistently within the designed safety margin, exhibiting smooth profiles without any abnormal fluctuations. These results validate the capability of the power supply system to deliver continuous and stable power throughout the on-orbit mission. Specifically, the data confirms the effectiveness of the bus voltage regulation and the appropriateness of the battery charge–discharge management strategy. This successful on-orbit performance verifies the correctness of the power topology and its associated control logic.

Tests are also conducted on the output current of the solar array. Specifically, the output current of the solar array was monitored when the solar panels were in a sun-pointing attitude in the sunlight zone. The current telemetry curves are shown in Figure 15c, which show that there is no output in the shadow zone, and the output current is stably maintained between 6.2 A and 6.5 A without abnormal fluctuations, after entering the sunlight zone and stabilizing in the sun-pointing attitude. The on-orbit test data confirms the nominal functionality of the solar panel, which demonstrates stable and efficient power generation performance, with output characteristics fully meeting the satellite’s energy demands. These results further demonstrate the validity of the power system.

Finally, an on-orbit power consumption analysis of the satellite is conducted. The long-term power consumption design limits are specified as 30 W during solar minimum years and 40 W during solar maximum years. Based on real-time telemetry data of bus voltage and load current within the same orbital arc, the power consumption curves are derived, as shown in Figure 15d. The average long-term power consumption of the satellite is 33.4 W, which remains below the 40 W upper limit for solar maximum years. The curve is generally stable throughout the operation, with no abnormal fluctuations observed. These results indicate that all onboard loads operate normally, and the power management system

can achieve proper power distribution and regulation. In conclusion, the overall energy consumption of the satellite is well within the designed capacity of the system.

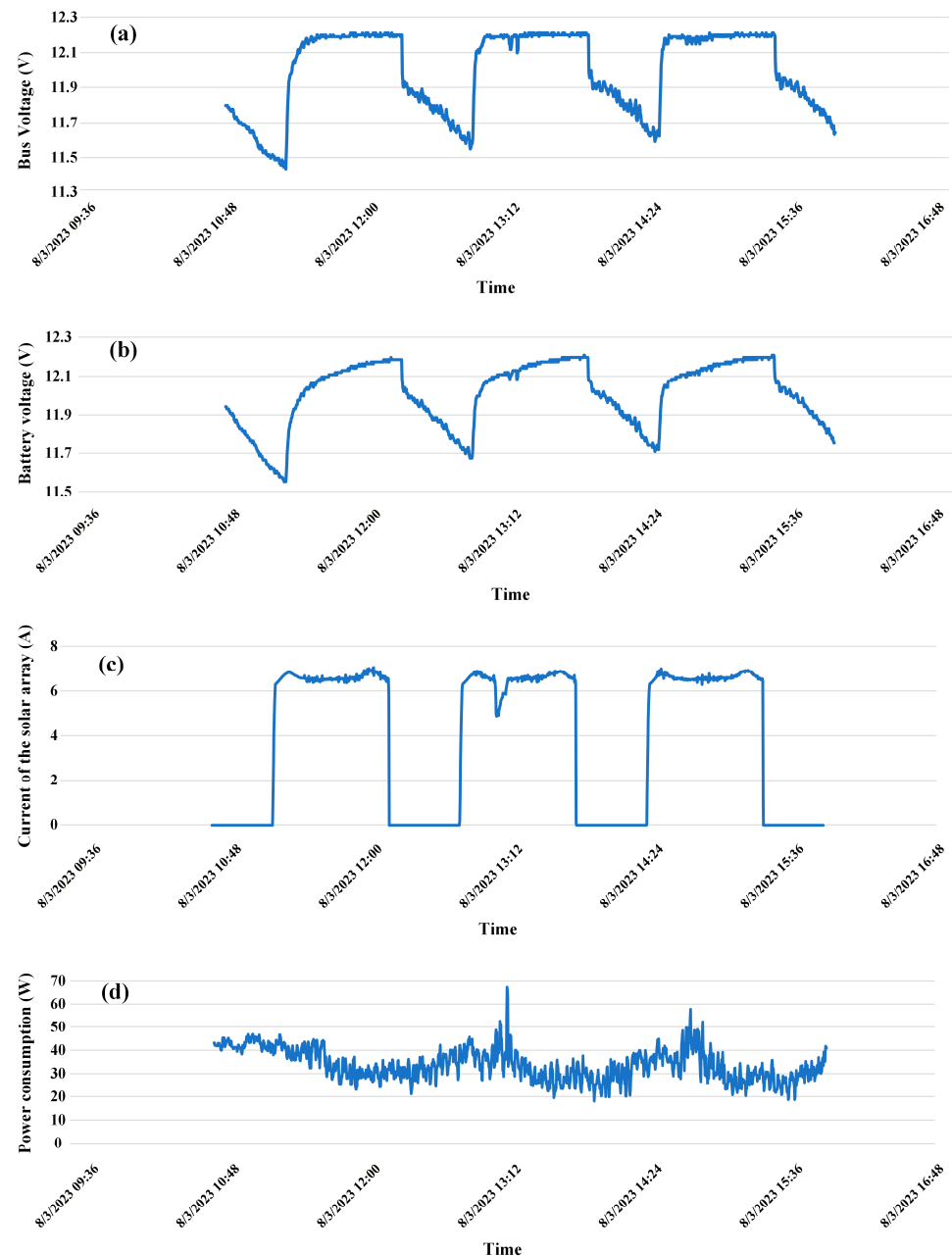


Figure 15. The on-orbit test data of power system. (a) The bus voltage. (b) The battery voltage. (c) The current of the solar array. (d) The power consumption of satellite.

All the above results confirm that the satellite power system achieves its design goals for bus voltage stability, solar array output, and power management, demonstrating excellent adaptability and stability across different operating modes. This validates the avionics system's architecture, component selection, and control strategies, ensuring long-term, reliable, and efficient on-orbit operation.

4.2. CPU Software Operation Status

The operational status of the onboard software is thoroughly evaluated. The satellite management program running on the U54_1 core functions properly, with all preset functions realized properly, and the overall system is running stably. The primary flywheel

control software on the U54_2 core operates continuously and reliably without failure when triggered by satellite management commands. The flywheel speed curve is shown in Figure 16. Meanwhile, the star tracker software executed on the U54_3 and U54_4 cores has maintained long-term, fault-free operation since orbit insertion, continuously transmitting high-precision attitude quaternion data to the satellite management software. The Star tracker quaternion output curve during a mission is shown in Figure 17.

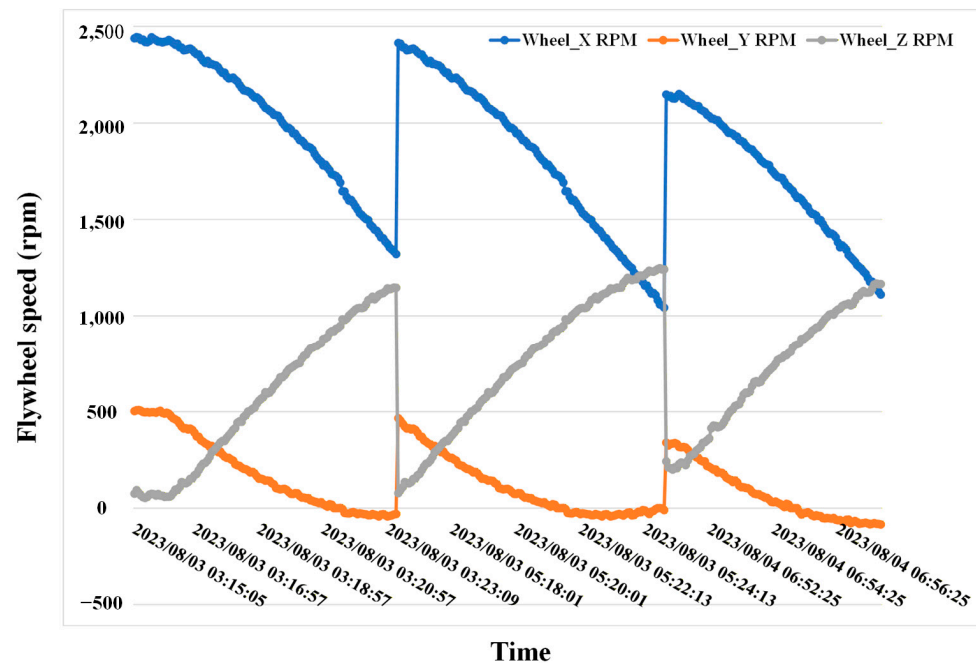


Figure 16. The flywheel speed diagram.

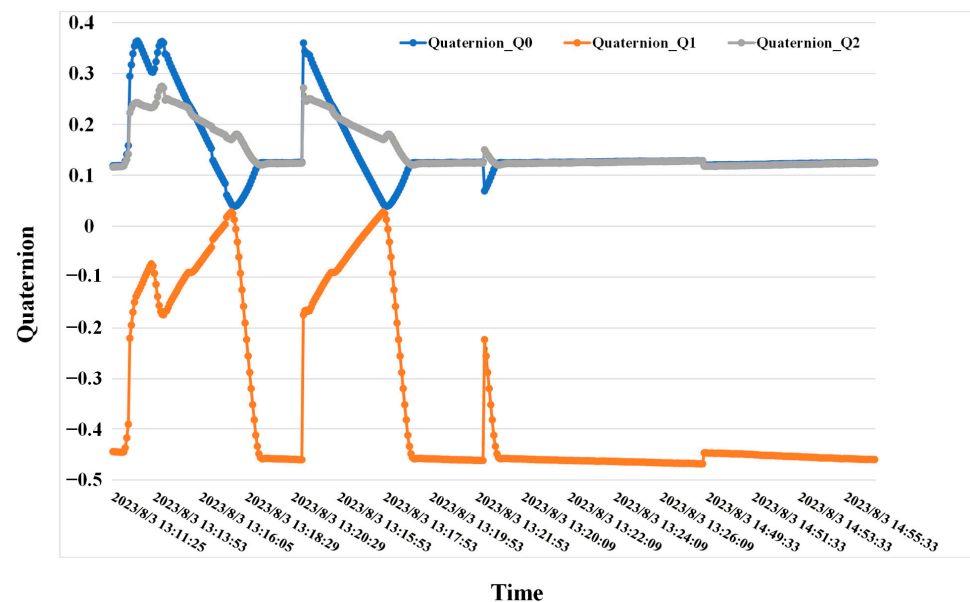


Figure 17. The Star tracker quaternion diagram.

4.3. Validation of X-Band TC&TM System

Regarding TC&TM performance, the downlink signal strength remained sufficient throughout the mission. During a specific orbital arc, the intermediate frequency signal strength (S/Φ) received by the ground station exceeded 70 dBHz, as shown in Figure 18, which is higher than the required threshold of 65.5 dBHz corresponding to the onboard

TC&TM downlink effective isotropic radiated power (EIRP) of -11 dBW. This confirms that the EIRP meets the design specification. During the satellite's extended on-orbit operation, both uplink and downlink signals for TC&TM have remained consistently stable, with over 10,000 commands transmitted successfully. These results comprehensively validate the operational stability and reliability of the X-band TC&TM system.

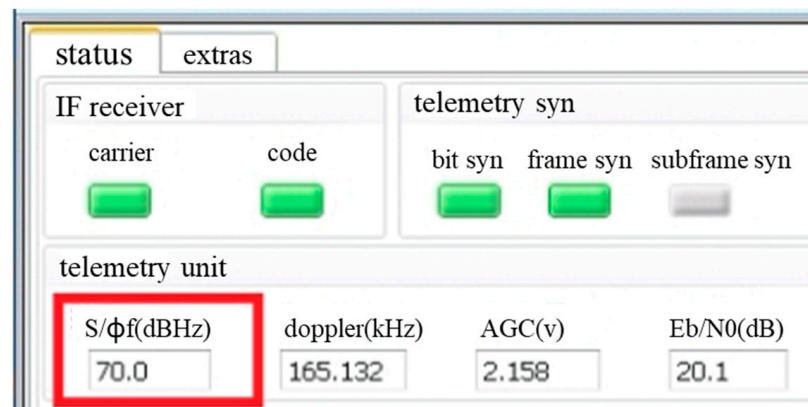


Figure 18. Ground station signal reception status.

During a typical satellite pass, the ground transmitted uplink signals. At the initial ingress stage, the X-band TC&TM system acquired a high Automatic Gain Control (AGC) and then immediately entered the lock mode (where '0' represents the locked state), maintaining a stable lock for approximately 8 min. As the satellite approached the egress stage, due to signal power attenuation and blockage, the system could no longer maintain a stable lock on the uplink signal. Throughout the entire pass, the AGC value remained stable with only minor fluctuations, indicating that the signal processing could properly keep the receiver's AGC. Figure 19 below shows the lock indication and AGC variation during this satellite pass. These results demonstrate that the uplink telecommand channel functioned normally and the receiving process was stable and reliable.

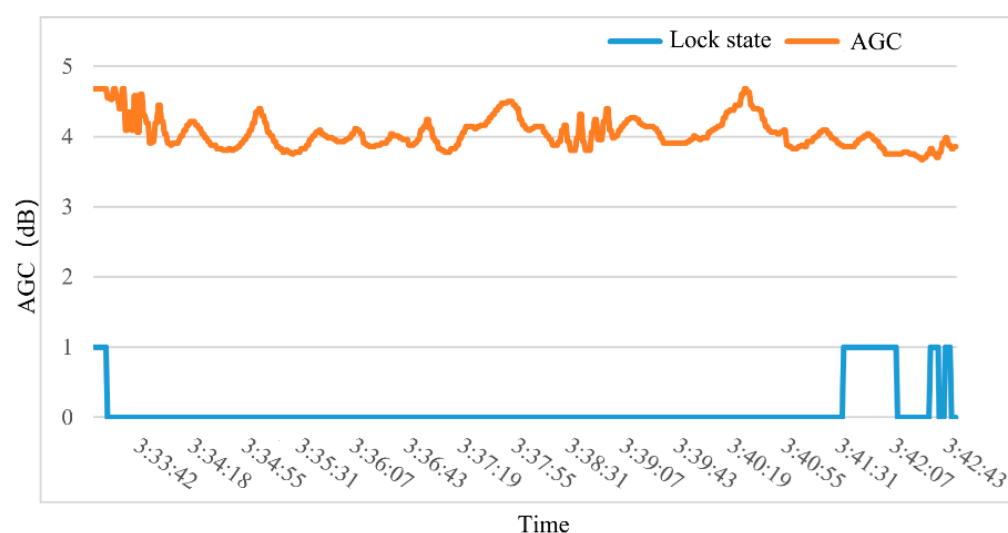


Figure 19. Lock state and AGC diagram.

All the above on-orbit telemetry data, system operating state records and long-term statistical operation records are consistent with the initial design indexes, and each performance conclusion drawn in this paper is strictly derived from actual measured in-orbit data

rather than theoretical speculation, which sufficiently verifies the rationality and superiority of the design proposed in this paper.

5. Conclusions

This paper presents a monolithic SoPC-based integrated satellite avionics that simultaneously achieves high reliability and low cost for LEO satellites. Through hardware–software co-design, all satellite avionics functions are integrated into a single SoPC with an AMP architecture combined with a Flash-based FPGA safety zone. The scheme adopts an enhanced dual-redundant CAN bus and an S3R power system, together with FPGA-implemented multi-level safety protection, to achieve highly reliable external communication and power supply at low cost. Furthermore, a hierarchical screening strategy for COTS components is adopted to systematically guarantee long-term on-orbit operational reliability. Compared with conventional design, the proposed integrated satellite avionics effectively reduces system volume, power consumption and complexity while balancing engineering cost and mission reliability.

By November 2025, the research design is validated by the successful on-orbit deployment and 29-month fault-free operation of the Jilin-1 Gaofen 05A satellite, with four key findings: (1) Feasibility of integration: All avionics functions were integrated into a SoPC and the system has operated without failure for 29 months, with all subsystems working in coordination. (2) Reliability of the power system: The 18650 battery-based power system demonstrated adequate cycling and long-term reliability, with bus voltage stabilized at 11.4–12.3 V. Furthermore, the average power consumption is as low as 33.4 W, demonstrating the outstanding low-power advantage of this design. (3) After 29 months of in-orbit operation and 13,467 light–shadow cycles, the system maintains stable operation with no power failures, 100% CAN bus switching success (252 operations) and zero FPGA logic abnormalities. This verifies the reliable fault tolerance of the proposed design even without radiation-hardened devices. (4) Stability of the AMP architecture: The AMP multi-core architecture operated continuously without exception, with all cores performing stable real-time control. The on-chip shared-memory communication provided high interconnect bandwidth and eliminated external bus delays, while the budget-based scheduling with timing redundancy fundamentally enhanced the system’s stability and determinism. The satisfactory on-orbit performance validates this monolithic SoPC-based design as an effective approach to achieving low-cost, high-reliability LEO satellite avionics and offers a valuable reference for future large-scale constellations.

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