electronics

MDPI

Article

A 20–43 GHz High-Dynamic-Range Amplifier with Current-Reused and Vertically Stacked Topology in GaAs Process

Zhen Ye [1], Jiyu Zhang [2], Liulin Hu [1] and Li Xu [2,*]

[1] Chengdu Ganide Technology Co., Ltd., Chengdu 610000, China
[2] School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 610000, China
* Correspondence: lixu@uestc.edu.cn

Abstract

This paper presents a current-reused vertically stacked (CRVS) topology for a high-dynamic-range amplifier (HDRA) implemented in a 0.1 μm GaAs pHEMT process, targeting wideband millimeter-wave (mm-wave) receiver front-ends. The proposed design breaks the inherent trade-off between noise figure (NF), linearity, and bandwidth, achieving simultaneous enhancement of transconductance efficiency, Miller effect suppression, and wideband matching. The fabricated prototype operates over a continuous 20–43 GHz bandwidth (covering K- and Ka-bands), demonstrating state-of-the-art performance: a flat gain of 24 ± 0.6 dB, a minimum NF of 2.2 dB, a maximum output 1 dB compression point (OP1dB) of 15.8 dBm and a low power consumption of 5 V/65 mA, with both input and output return losses better than −10 dB across the entire band. The results validate the effectiveness of the CRVS topology and highlight the competitiveness of GaAs pHEMT technology for high-performance wideband mm-wave front-ends, making the design suitable for applications including 5G/6G communication, satellite systems, and mm-wave test equipment.

Keywords: high-dynamic-range amplifier (HDRA); GaAs MMIC; current-reused and vertically stacked (CRVS) topology; millimeter-wave amplifier

1. Introduction

The rapid development of millimeter-wave (mm-wave) communication systems, including 5G networks, satellite communications, and ultra-wideband (UWB) applications, has imposed stringent requirements on radio frequency (RF) front-end amplifiers. Recent studies have highlighted that self-sufficient millimeter-wave and IoT systems strongly demand low-power, high linearity and wideband front-end amplifiers to achieve long-term autonomous operation [1]. However, conventional wideband amplifier topologies often suffer from fundamental performance trade-offs that prevent the simultaneous optimization of these key metrics [2–10].

Distributed amplifiers are widely adopted for ultra-broadband operation but typically suffer from high noise figure, large chip area, and high power consumption, making them unsuitable for power-constrained portable systems [3,4,11–13]. Balanced amplifiers provide good input/output matching and wide bandwidth but require bulky quadrature hybrids and consume twice the power of single-ended structures, leading to degraded efficiency and increased cost [5,6,14,15]. Darlington and cascaded common-source stages can improve gain and bandwidth but face severe noise–linearity trade-offs; low-noise

Check for updates

Academic Editor: Yosef Pinhasi

Received: 17 April 2026
Revised: 5 May 2026
Accepted: 12 May 2026
Published: 21 May 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

biasing usually degrades linearity, whereas high-linearity biasing elevates noise figure and power dissipation [7,8,16,17].

The selection of an appropriate semiconductor process is also crucial for RF circuit design. While CMOS technology offers high integration and low cost [18], its performance in millimeter-wave frequencies is often limited compared to GaAs and InP due to the relatively low cutoff frequency of transistors. InP technology features extremely high electron mobility and cutoff frequency, making it suitable for millimeter-wave and terahertz (THz) applications with excellent noise performance; however, InP manufacturing processes are prohibitively expensive, complex, and suffer from relatively low yield [19]. In contrast, GaAs technology remains the most mature and widely adopted solution for high-performance millimeter-wave low-noise amplifiers (LNAs).

To address the above challenges, this paper presents a fully integrated high-dynamic-range amplifier (HDRA) using a 0.1 μm GaAs pHEMT process. The proposed amplifier operates over the wide frequency band of 20–43 GHz and is intended for next-generation 5G systems, satellite communications, and mm-wave instrumentation. A novel current-reused and vertically stacked (CRVS) topology is proposed to break the traditional trade-off between noise figure and linearity. By synergistically combining current-reused and stacked device configurations, the design achieves ultra-low noise, high OP1dB, flat high gain, wide bandwidth, and low DC power consumption at the same time. The measured results show a minimum noise figure of 2.2 dB at 30 GHz, an OP1dB of 16 dBm from 35 GHz to 41 GHz, a flat small-signal gain of 24 ± 0.6 dB across the entire band, and a low power consumption of 5 V/65 mA.

The remainder of this paper is organized as follows. Section 2 describes the circuit topology and operating principle of the proposed CRVS amplifier. Section 3 presents fabrication, measurement setup, and experimental results, together with a comparison against the state of the art. Section 4 concludes this work and outlines future research directions.

2. Circuit Design and Theoretical Analysis

The design of mm-wave UWB circuits requires careful selection of appropriate topologies due to unique high-frequency characteristics. This work demonstrates that the proposed HDRA with CRVS topology (shown in Figure 1) provides a promising solution for mm-wave UWB systems, effectively overcoming traditional design trade-offs. The HDRA with CRVS topology not only achieves ultra-wide bandwidth but also demonstrates an excellent balance among key performance metrics, including noise figure, OP1dB linearity, gain flatness, and power consumption.

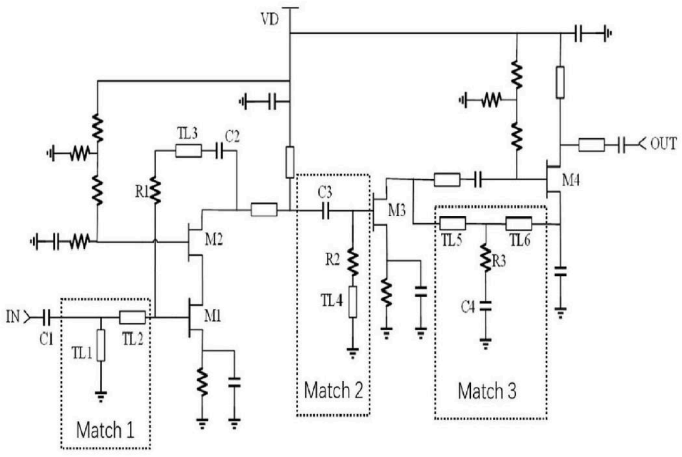


Figure 1. Schematic of the proposed HDRA.

The schematic is shown in Figure 1.

In this structure: (1) M_1 and M_3 are self-biased; (2) M_2 and M_1 share a common current path, while M_4 and M_3 share another.

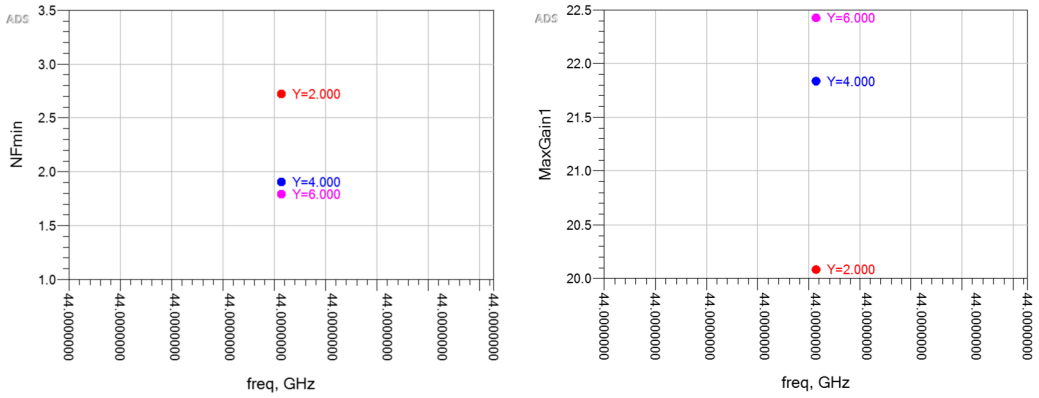
In traditional common-source amplifiers, input capacitance increases significantly due to the Miller effect [20]. However, the proposed CRVS could mitigate the Miller effect effectively, thereby extending bandwidth. As this circuit operates at frequencies exceeding 40 GHz, the CRVS effectively enhances high-frequency performance through the M_2 stage's suppression of M_1's feedback capacitance (notably C_{gd}) and similarly, through the M_4 stage's suppression of M_3's feedback capacitance. To quantitatively analyze this bandwidth extension capability, we examine the input admittance. In a traditional common-source amplifier, the input capacitance is expressed as $C_{in} = C_{gs} + (1+|A_v|)C_{gd}$. However, in the CRVS topology, the low input impedance of the common-gate stage (M_2) loads the common-source stage (M_1). The voltage gain of the first stage M_1 can be approximated as:

$$A_{v1} \approx -g_{m1} \cdot \frac{1}{g_{m2}} \approx -1 \tag{1}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. M_1 and M_2 have identical dimensions. M_1 and M_2 share the same current and exhibit nearly identical gate–source voltages (the simulated $|V_{GS1} - V_{GS2}|$ is below 20 mV across all bias and process corners), so according to the long-channel transconductance expression $g_m = \sqrt{2\mu Cox(W/L)ID}$, we obtain $g_{m1} \approx g_{m2}$. Consequently, the Miller multiplication factor $(1+|A_v|)$ is reduced to approximately 2, which is significantly lower than that of a standalone common-source stage. This suppression of the equivalent input capacitance shifts the dominant pole to a higher frequency, theoretically justified by:

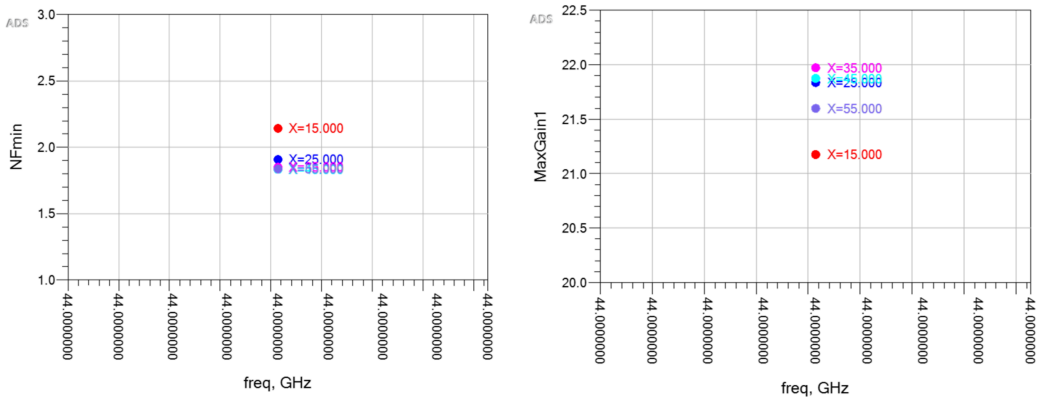
$$\omega_{p,in} = \frac{1}{R_S[C_{gs1} + C_{gd1}(1 + g_{m1}/g_{m2})]} \tag{2}$$

The choice of transistor sizing is crucial because it directly determines gain, noise figure and power consumption simultaneously. In particular, the first stage requires careful consideration because it must achieve high gain while maintaining a low noise figure and low DC power. Therefore, in this work in both the process of the transistor sizing selection and the input matching network implementation, the M_1/M_2 pair was treated as a combined unit. Since the first stage is not constrained by output-power requirements, the gate length was first fixed at X = 25 μm and the maximum gain (MaxGain) and minimum noise figure (NFmin) were simulated for gate-finger numbers Y = 2, 4, and 6. For the design of broadband amplifiers, due to the characteristic that gain decreases at high frequencies and noise increases at high frequencies, the transistor performance must be evaluated at the highest operating frequency. Considering a margin above the 20–43 GHz operating band, 44 GHz was selected as the evaluation point. To achieve a system NF below 3 dB, NFmin should preferably stay below 2 dB. As shown in Figure 2, the 2 × 25 device exhibits an unsatisfactory NFmin, while the 4 × 25 and 6 × 25 devices show comparable NFmin and only ~0.5 dB difference in MaxGain. Therefore, the 4 × 25 device is preferred for low-power design. To further validate this choice, the gate-finger number was then fixed at Y = 4 and the gate length was swept from X = 15 to 55 μm in 10-μm steps; the resulting NFmin and MaxGain are plotted in Figure 3, which confirms that X = 25 μm provides the best compromise between high gain, low noise figure, and low DC power.



(**a**) (**b**)

Figure 2. NFmin and MaxGain at 44 GHz versus the gate-finger number Y, for a fixed gate length X = 25 μm. (**a**) NFmin@44 GHz; (**b**) MaxGain@44 GHz.



(**a**) (**b**)

Figure 3. NFmin and MaxGain at 44 GHz versus the gate length X (15, 25, 35, 45, 55 μm), for a fixed gate-finger number Y = 4. (**a**) NFmin@44 GHz; (**b**) MaxGain@44 GHz.

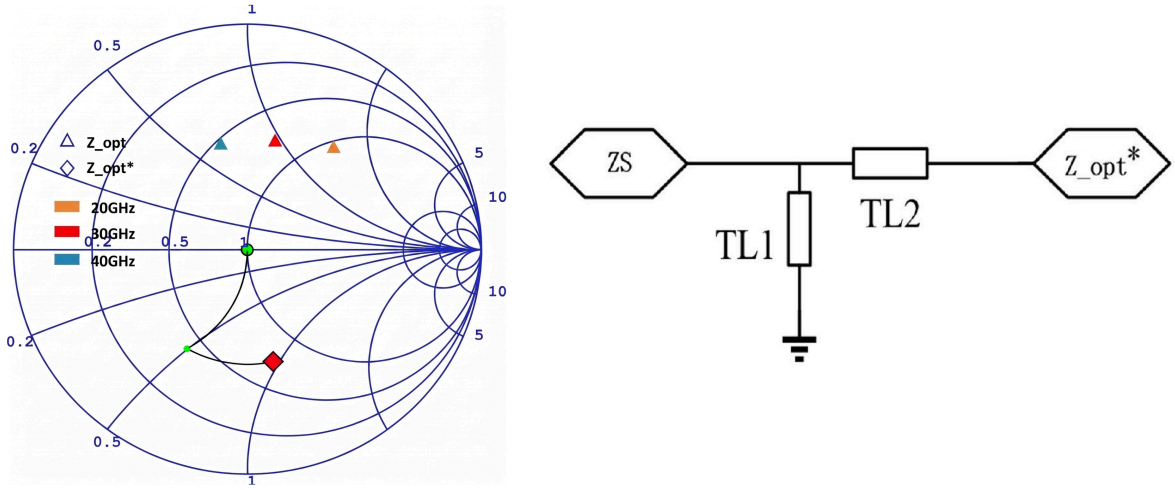
For the proposed M_1/M_2 pair, 4 × 25 μm CPW pHEMTs were used. The noise matching was initially optimized at the band-center frequency of 30 GHz, which is the geometric reference for the 20–43 GHz multi-octave band. Three characteristic frequencies (20, 30, and 40 GHz) were used to verify the noise circle convergence on the Smith chart (Figure 4a). A compact L-section noise-matching network, consisting of a series transmission line TL_1 and a shunt grounded stub TL_2 (Figure 4b), was synthesized between the standard 50 Ω source impedance Z_S and the conjugate of the optimum noise impedance Z_{opt}* = 35.8 – j46.8 Ω. The line dimensions were initialized using the LineCalc tool of Keysight ADS2017 and subsequently fine-tuned by gradient-based optimization in ADS, so that the noise matching is preserved across the entire 20–43 GHz band (denoted as Match 1 in Figure 1).

Unlike traditional cascaded structures consuming independent bias currents, CRVS integrates the common-gate device (M_2) vertically on common-source device (M_1), sharing the same DC current path, therefore maximizing transconductance efficiency (g_m/I_D).

At this stage, noise factor (NF) is dominated by channel thermal noise ($\overline{i_{nd}^2}$) of input transistor M_1. By multiplexing the bias current, M_1 can operate at a higher current density without increasing power consumption, which, according to long-channel theory, effectively minimizes the equivalent noise resistance R_n:

$$R_n \propto \frac{\gamma}{g_{m1}} = \frac{\gamma}{\sqrt{2\mu C_{ox}(W/L)_1 I_D}} \quad (3)$$

where γ denotes channel thermal noise factor, μ denotes the carrier mobility, C_{ox} is the gate oxide capacitance, and I_D stands for the shared bias current. This formula demonstrates that maximizing I_D through current multiplexing directly enhances g_{m1}, thereby reducing the input reference noise and establishing a lower noise baseline for the entire system.



(**a**) (**b**)

Figure 4. Variation in the matching network impedance and its implementation for the M_1–M_2 transistor pair. (**a**) Optimum noise source impedance Z_{opt} on the Smith chart at 20, 30, and 40 GHz. (**b**) Implementation of the noise-matching network for the M_1/M_2 pair.

Notably, the input DC-blocking capacitor C_1 was designed with a sufficiently large value (about 6 pF in this work) in the corresponding frequency range to minimize interference with the RF matching network. Furthermore, an RLC negative feedback network (comprising R_1, TL_3, and C_2 in Figure 1) was incorporated, which significantly improved gain flatness and circuit stability while maintaining optimal noise performance. This feedback structure also provided additional bandwidth extension.

Both M_3 and M_4 are made using 4×35 μm transistors in CRVS. This novel structure maximizes current utilization efficiency through sharing current paths between M_2/M_4 and M_1/M_3.

$M_3 - M_4$ stage cascading after the $M_1 - M_2$ stage not only increases circuit gain, but also provides a critical advantage on system level: reverse isolation. In the millimeter-wave band, feedback through C_{gd} typically renders the input impedance Z_{in} highly sensitive to variations on load (the load-pulling effect).

By employing a cascaded topology, the high reverse isolation (low S_{12}) of CRVS acts as a buffer, ensuring optimal noise matching at the sensitive first stage (M_1–M_2) remains stable across the entire 20–43 GHz bandwidth and independent of the nonlinear behavior of the output power stage. Meanwhile, the stacked voltage swing capability of M_3–M_4 contributes to enhancing output power ($P_{1\mathrm{dB}}$), breaking the traditional trade-off between sensitivity and linearity.

Consequently, the first stage dominates the noise performance while the second stage dominates the linearity ($P_{1\mathrm{dB}}$), effectively maximizing the amplifier's dynamic range ($DR \propto P_{1\mathrm{dB}} - NF_{sys}$). To verify the linearity of the proposed amplifier, the input-referred third-order (IIP3) and second-order intercept (IIP2) points were simulated; as shown in Figure 5 below, both indices confirm that the circuit maintains good linearity across the operating band.

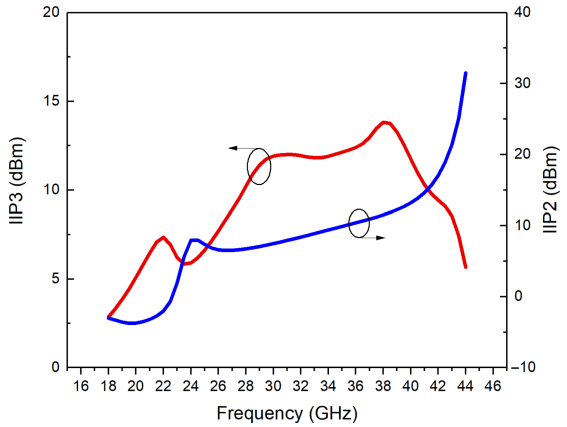


Figure 5. Simulated IIP3 and IIP2.

To meet ultra-wideband requirements, the interstage matching network (Matching 2 in Figure 1) was designed with dual functionality: the DC-blocking capacitor C_3 and grounded transmission line TL_4 not only provide interstage impedance matching but also form an LC network for bandwidth extension. From a transmission line theory perspective, this inter-stage matching network can be modeled as a section of an artificial transmission line. The parasitic output capacitance of the first stage (C_{out1}) and the input capacitance of the second stage (C_{in2}) are absorbed into the synthetic characteristic impedance Z_0 of the matching network:

$$Z_{0,inter} = \sqrt{\frac{L_{TL4}}{C_{out1} + C_{in2}}} \tag{4}$$

By carefully tuning the inductance of TL_4 and the coupling capacitor C_3, the structure forms a high-pass filter response that compensates for the gain roll-off of the transistors at higher frequencies. This effectively synthesizes a flat gain response across the multi-octave bandwidth. Similarly, in Matching 3 (Figure 1), transmission lines TL_5 and TL_6 serve dual purposes—functioning as series branches for M_3 and M_4 while combining with capacitor C_4 to create another LC matching network. Additionally, resistors R_2 and R_3 are incorporated to enhance overall circuit stability. The simulated stability factors K and μ across the entire band are shown in Figure 6, where K > 1 and μ > 1 hold over the full 20–43 GHz range, confirming that the amplifier is unconditionally stable.

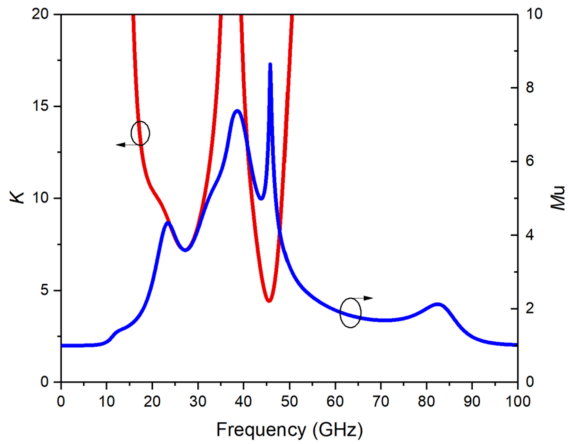


Figure 6. Simulated stability factors K and μ of the proposed amplifier across the full 20–43 GHz operating band.

3. Experimental Results

The MMIC HDRA was fabricated using a 0.1-μm GaAs pHEMT process. Figure 7 shows the die micrograph with dimensions of 1.97 × 1.3 mm. The layout is compact, reducing the chip area by at least one-third compared to conventional designs. The circuit operates on a single +5 V supply (V_D). M_1 and M_2 are biased at +2 V and +2.5 V drain voltages respectively, while M_3 and M_4 are biased at +1.7 V and +2.8 V. All gates are biased at −0.4 V. The total current consumption is below 65|mA.

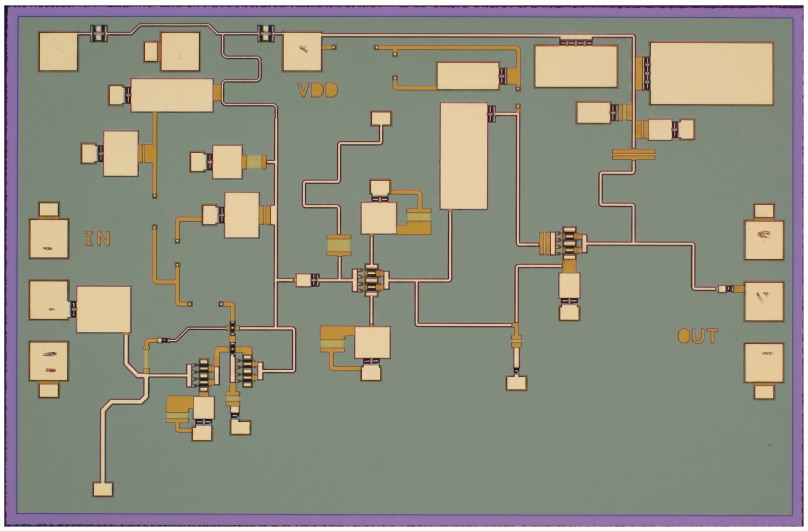
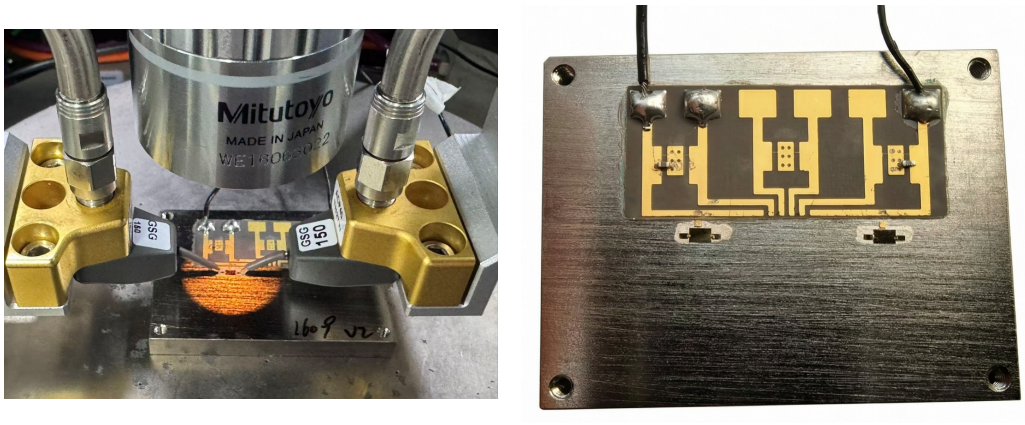


Figure 7. Microphotograph of the fabricated MMIC HDRA.

The on-wafer measurements were performed using a N5245B vector network analyzer (Keysight Technologies, Inc., Santa Rosa, CA, USA) connected to a probe station, shown in Figure 8a. Ground-Signal-Ground (GSG) probes with a 150-μm pitch were utilized to contact the chip pads. To measure amplifier performance, the chip is mounted on a PCB board and fixed onto an aluminum–nickel plated metal plate with conductive adhesive, shown in Figure 8b. Due to the high frequency, the input and output pads of the HDRA chip are connected to two 50-ohm straight-through chips via gold bonding wires, respectively, so as to consider the inductive effects equivalent to gold wires in practical applications.



(**a**) (**b**)

Figure 8. Photograph of the probe station used in this test and the test fixture. (**a**) Photograph of the probe station used in this test. (**b**) Photograph of the test fixture.

The measured small-signal gain achieves a flat response of ≈24 dB across 20–43 GHz, with variation within ±0.6 dB. A small but consistent gain offset of approximately 1–2 dB

is observed between the simulated and the measured S21 curves (Figure 9). This deviation is mainly attributable to: (i) non-ideal grounding through the back-side via array, which introduces additional source-degeneration inductance; and (ii) statistical process variations in the foundry pHEMT model. Meanwhile, the group delay varies from 65.32 ps to 114.1 ps across the operating band of 20–43 GHz, with a group delay variation of only 48.78 ps, which is suitable for UWB and broadband communication applications.

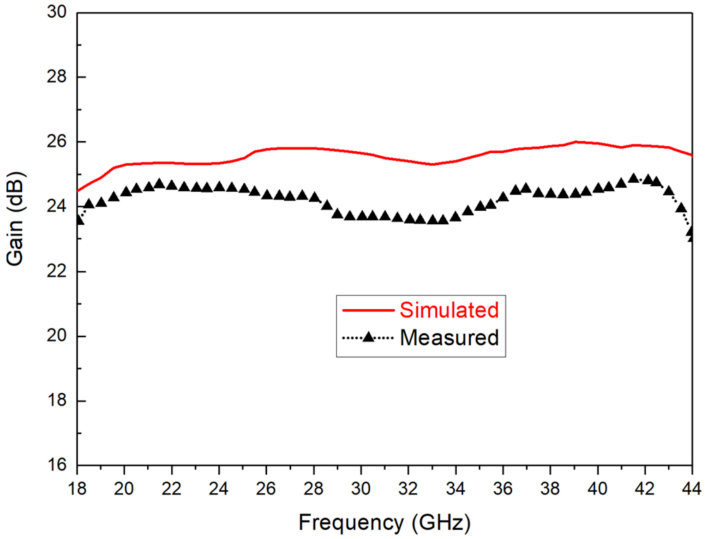


Figure 9. Simulated and measured gain of the HDRA at 25 °C.

Input and output return losses (S_{11}, S_{22}) remain below −10 dB (typically −15 dB), as shown in Figure 10. Good chip return loss is very important for signal transmission quality.

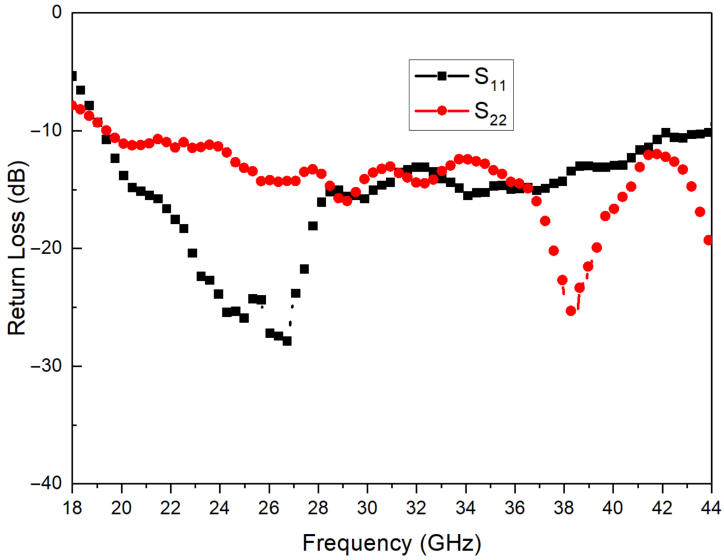


Figure 10. Measured input and output return loss (S_{11} & S_{22}) of the HDRA at 25 °C.

Figure 11 presents the noise and power performance. The typical noise figure is 2.5 dB (min 2.2 dB at 30 GHz). The output P_{1dB} reaches 15.8 dBm at 35–41 GHz, with a typical value of 15 dBm across the band. The results indicates that this work successfully breaks the traditional trade-off between noise figure and linearity.

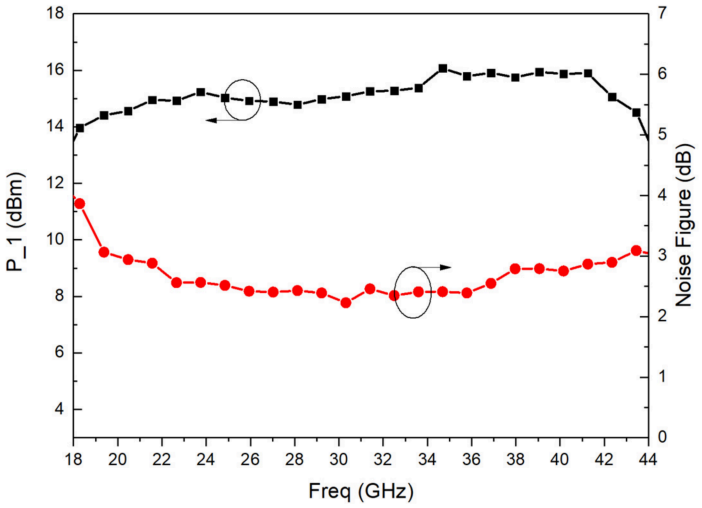


Figure 11. Measured output power (P_{1dB}) and noise figure (NF) of the HDRA 25 °C.

The measured small-signal gain at three temperatures (−55 °C, +25 °C, +85 °C) shows a good gain temperature coefficient with a gain spread of less than 2.5 dB across the full industrial-grade temperature range (shown in Figure 12). This confirms that the proposed CRVS topology preserves its noise–linearity advantage under temperature variations and is suitable for real-world environments.

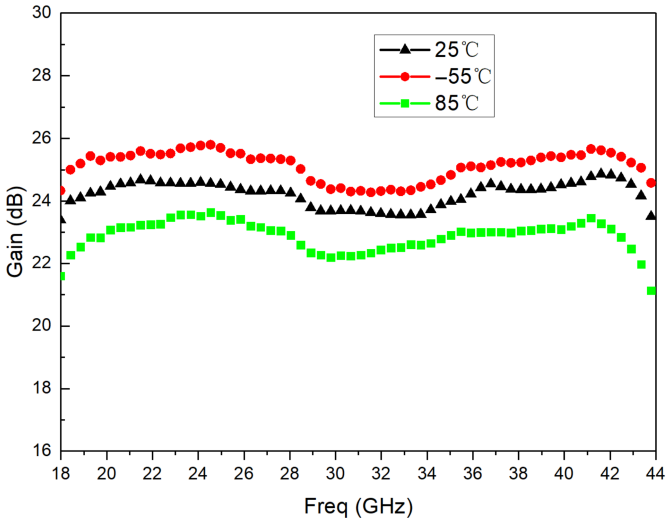


Figure 12. Measured gain fluctuation curve of the HDRA under three temperatures.

Table 1 presents a comprehensive performance comparison between the proposed 0.1 μm GaAs-based high-dynamic-range amplifier (HDRA) and state-of-the-art millimeter-wave (mm-wave) low-noise amplifiers (LNAs) reported in the literature, including both GaAs and scaled CMOS/SOI implementations.

To evaluate the overall performance efficiency, we adopt the widely recognized figure of merit (FoM) definition for broadband LNAs:

$$FoM = \frac{Gain[abs] \cdot OP1dB[mW] \cdot BW_{3dB}[GHz]}{P_{DC}[mW] \cdot (NF-1)[abs]} \quad (5)$$

Compared with the referenced designs, the proposed HDRA exhibits significant improvements in gain flatness, noise performance, linearity, and power consumption. Specifically, it outperforms the 0.15 μm GaAs LNA [21] in both gain and noise figure (NF), while also surpassing the 45 nm SOI [22] and 65 nm CMOS [23] LNAs in NF, linearity, and

gain flatness. When compared to the broadband GaAs LNA [7], which achieves a FoM of 11.4, the proposed work demonstrates a substantially higher FoM of 64.7, highlighting its superior trade-off among gain, bandwidth, noise, linearity, and power consumption. These results highlight the inherent advantages of GaAs pHEMT technology for mm-wave LNAs, particularly in achieving high gain, low noise, and high linearity simultaneously, making the proposed HDRA well-suited for high-performance wideband receiver applications.

Table 1. Comparison with state-of-the-art mm-wave LNAs.

Reference	Year	Tech.	Freq (GHz)	Gain (dB)	NF (dB)	P_{1dB} (dBm)	S_{11}/S_{22} (dB)	*FOM*
[21]	2015	0.15 µm GaAs	18–40	15.8 ± 2	3.5 (typ)	—	$\leq -9.4/-12$	–
[22]	2018	45 nm SOI	22–44	19 ± 1	4.7 (typ)	0 @ 28 GHz	$\leq -3/-15$	–
[23]	2021	65 nm CMOS	22–34	19 ± 3	4 @ 26G	2.8 @ 28 GHz	$\leq -10/-5$	–
[7]	2024	0.15 µm GaAs	0.5–30	23 ± 2	3.8 (typ)	6	$\leq -5/-5$	11.4
This Work	2026	0.1 µm GaAs	20–43	24 ± 0.6	2.2 (min)	15.8 (max)	≤ -10	64.7

4. Conclusions

This work presents a high-performance, ultra-wideband high-dynamic-range amplifier (HDRA) implemented in a 0.1 µm GaAs pHEMT process for millimeter-wave receiver front-ends. A novel current-reused vertically stacked (CRVS) topology is proposed to simultaneously address the fundamental trade-offs between noise figure, linearity, and bandwidth. The measured prototype achieves a continuous 20–43 GHz bandwidth, a flat gain of 24 ± 0.6 dB, a minimum noise figure of 2.2 dB, and a maximum OP1dB of 15.8 dBm, outperforming state-of-the-art CMOS, SOI, and GaAs LNAs in key metrics. The results validate the effectiveness of the CRVS architecture and demonstrate the advantages of GaAs pHEMT technology for high-performance wideband millimeter-wave applications.

For future work, two directions are identified to further advance this research:

Frequency extension: Scale the proposed topology to higher frequency bands (e.g., V- and E-band) while maintaining low noise and high linearity to support next-generation 6G communication systems.

Front-end integration: Integrate the HDRA with on-chip matching networks, switches, and control circuits to realize a fully integrated, reconfigurable millimeter-wave receiver front-end.

Author Contributions: Z.Y.: Writing—original draft, Writing—review and editing, Resources, Investigation, Methodology, Formal analysis. J.Z.: Writing—original draft, Writing—review and editing, Formal analysis. L.H.: Writing—original draft, Writing—review and editing, Supervision, Project administration. L.X.: Writing—original draft, Writing—review and editing, Supervision, Project administration. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Natural Science Foundation of China, grant number 62071102.

Data Availability Statement: The datasets used and analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of Interest: Authors Zhen Ye and Liulin Hu were employed by the company Chengdu Ganide Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript: HDRA—high-dynamic-range amplifier; MMIC—Monolithic Microwave Integrated Circuit; GaAs—Gallium Arsenide; pHEMT—pseudomorphic High Electron Mobility Transistor; CRVS—current-reused and vertically stacked; LNA—low-noise amplifier; NF—noise figure; P1dB—1 dB compression point; OP1dB—output 1 dB compression point; IIP2/IIP3—Input-referred Second-/Third-order Intercept Points; UWB—ultra-wideband; mm-wave—Millimeter Wave; CMOS—Complementary Metal-Oxide-Semiconductor; SOI—Silicon-on-Insulator; FD-SOI—Fully Depleted Silicon-on-Insulator; InP—Indium Phosphide; FoM—figure of merit; EM—Electromagnetic; RF—radio frequency; T/R—Transmit/Receive; CPW—Coplanar Waveguide; CW—Continuous Wave; GSG—Ground-Signal-Ground; PCB—Printed Circuit Board; ADS—Advanced Design System; PVT—Process, Voltage, and Temperature.

References

1. Citroni, R.; Mangini, F.; Frezza, F. Efficient integration of ultra-low power techniques and energy harvesting in self-sufficient devices: A comprehensive overview of current progress and future directions. *Sensors* **2024**, *24*, 4471. [CrossRef] [PubMed]
2. Gray, P.R.; Hurst, P.J.; Lewis, S.H.; Meyer, R.G. *Analysis and Design of Analog Integrated Circuits*, 6th ed.; Wiley: Hoboken, NJ, USA, 2021.
3. Ni, D.H.; Chen, J.W.; Yin, H.B.; Zeng, C.; Lu, Y.; Chen, K. Design and Implementation of a DC-20 GHz Ultra Broadband Distributed Low Noise Amplifier. In Proceedings of the 2024 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Chengdu, China, 28–30 August 2024.
4. Li, Q.L.; Han, J.Y.; Fan, X.T.; Xu, Y. A DC to 70 GHz Distributed Low Noise and Medium Power Amplifier. In Proceedings of the 2023 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Qingdao, China, 14–17 May 2023.
5. Zhan, Z.T.; Chen, P.; Yu, L.Q.; Zheng, Z.; Xia, J.; Zhang, G.; Yu, Y.; Zhu, X.-W.; Hao, Z.-C.; Chen, J.; et al. A Theoretical Method to Optimize Load-Modulation Behavior for a 62.5–72.5 GHz Asymmetrical Load Modulated Balanced Amplifier in 100-nm GaAs. In *IEEE Transactions on Microwave Theory and Techniques*; IEEE: Piscataway, NJ, USA, 2026; pp. 1–14.
6. Kang, L.; Wu, A.M.; Chen, W.H.; Chen, X. C–Ku-Band RF-Input Load Modulated Balanced Amplifier MMIC Utilizing Broadband Saturation Efficiency Enhancement Technique. *IEEE Trans. Microw. Theory Tech.* **2025**, *73*, 914–925. [CrossRef]
7. Yuan, Y.; Yuan, B.; Li, J.X.; Wang, Z.; Zeng, J.; Yu, Z. A Broadband Cascode Low-Noise Amplifier Using Transformer Feedback and Darlington Techniques. *IEEE Trans. Circuits Syst. II Express Briefs* **2024**, *71*, 41–45. [CrossRef]
8. Hu, J.; Ma, K.; Mou, S.; Meng, F. Analysis and Design of a 0.1–23 GHz LNA MMIC Using Frequency-Dependent Feedback. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1497–1501. [CrossRef]
9. Li, M.; Zeng, Z.; Wei, H.T. A design of a wideband balanced limited low noise amplifier. In Proceedings of the 2019 IEEE 13th International Conference on ASIC(ASICON), Chongqing, China, 29 October–1 November 2019.
10. Uchida, H.; Takatsu, S.; Nakahara, K.; Katoh, T.; Itoh, Y.; Imai, R.; Yamamoto, M.; Kadowaki, N. Ka-band multistage MMIC low-noise amplifier using source inductors with different values for each stage. *IEEE Microw. Guid. Wave Lett.* **1999**, *9*, 71–72. [CrossRef]
11. Nikandish, G.; Medi, A. A 40 GHz Bandwidth Tapered Distributed LNA. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2018**, *65*, 1614–1618. [CrossRef]
12. Bhagavatula, V.; Taghivand, M.; Rudell, J.C. A compact 24–54 GHz CMOS band-pass distributed amplifier for high fractional bandwidth signal amplification. In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Tampa, FL, USA, 1–3 June 2014.
13. Meng, F.; Liu, C.; Hu, J.; Mou, C.; Ma, K. Design and Analysis of a 0.01-to-6 GHz 31 dBm-P1dB 31.5%-PAE Distributed Power Amplifier in 0.25-μm GaAs Technology. *Chin. J. Electron.* **2021**, *30*, 549–555.
14. Chang, M.; Rebeiz, G.M. A 26 to 40 GHz Wideband SiGe Balanced Power Amplifier IC. In Proceedings of the 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, HI, USA, 3–5 June 2007.
15. Yang, G.; Guo, Y.; Xu, R. An 18–40 GHz ultra broadband low noise amplifier MMIC. In Proceedings of the 2008 International Conference on Microwave and Millimeter Wave Technology, Nanjing, China, 21–24 April 2008; Volume 2, pp. 865–867.

16. Su, Y.C.; Huang, K.-H.; Chang, H.-Y. A Ka-Band Low Noise Amplifier Using R-L-C Feedback Technique in E-Mode 0.15-μm GaAs pHEMT Process. In Proceedings of the 2024 IEEE Asia-Pacific Microwave Conference (APMC), Bali, Indonesia, 17–20 November 2024.
17. Chen, S.; Chen, Z.; Li, B.; Jiang, H. A 24–41 GHz GaN Low-Noise Amplifier with Cascode Structure and Multi-Stage Load. In Proceedings of the IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications, Guangzhou, China, 27–29 November 2022.
18. Mayeda, J.C.; Lopez, J.; Lie, D.Y.C. Highly-Efficient Broadband Medium Power Amplifier Design in 22 nm CMOS FD-SOI for mm-Wave 5G. In Proceedings of the 2020 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, USA, 26–28 May 2020; pp. 1–4.
19. Kim, S.C.; An, D.; Lee, B.-H.; Lee, M.-K.; Shin, D.-H.; Rhee, J.-K. Wideband and High Gain Cascode Amplifier Using Metamorphic HEMT for Millimeter Wave Applications. In Proceedings of the 2006 European Microwave Integrated Circuits Conference (EuMIC), Manchester, UK, 10–13 September 2006; p. 371.
20. Razavi, B. *RF Microelectronics*, 2nd ed.; Prentice-Hall: Upper Saddle River, NJ, USA, 2012; Chapter 5.
21. Banerjee, P.; Majumder, A. Computer-aided-design of an 18–40 GHz MMIC low noise amplifier using RLC and series inductive feedback. In Proceedings of the 2015 IEEE MTT-S International Microwave and RF Conference (IMaRC), Hyderabad, India, 10–12 December 2015.
22. Chauhan, V.; Floyd, B. A 24–44 GHz UWB LNA for 5G Cellular Frequency Bands. In Proceedings of the 2018 11th Global Symposium on Millimeter Waves (GSMM), Boulder, CO, USA, 22–24 May 2018.
23. Chen, X.; Li, L.; Cheng, D.; Fan, X. A 22–34 GHz Wide-Band Low Noise Amplifier with 22 dB Gain and 4 dB NF. In Proceedings of the 2021 IEEE MTT-S International Wireless Symposium (IWS), Nanjing, China, 23–26 May 2021.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.