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Generalized Positive/Negative Floating Impedance Multiplier Circuit and Its Application

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Abstract

Passive components in integrated circuits occupy significant areas and increase production costs, driving the demand for compact alternatives. This study presents a generalized, electronically controllable positive/negative floating impedance multiplier implemented in TSMC 180 nm CMOS technology. To achieve a compact layout, the architecture utilizes custom-designed operational transconductance amplifiers (OTAs). The circuit operates on a lossless principle, scaling resistance, capacitance, and inductance values within a wide multiplication range of −100 to +100 using only a single base element. Comprehensive LTspice simulations including PVT, Monte Carlo, THD, and noise analyses verify the design's stable operation, low distortion, and favorable noise characteristics across various filter configurations. Furthermore, practical feasibility is validated through SPICE simulations using commercial LM13700 OTA, confirming consistent behavior for real-world applications. The proposed active topology occupies a compact core area of only 5831 μm^2. By scaling down large passive components, this design decreases the overall system-level footprint, providing a versatile and area-efficient solution for tunable analog IC applications. It should be noted that the reported 5831 μm^2 corresponds to the active core only, while the effective system-level area benefit depends on the selected base impedance and the target application.

Keywords: impedance multiplier; capacitance multiplier; OTA; LM13700

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1. Introduction

As technology progresses, digital circuits are garnering increased attention in contrast to analog circuits; nevertheless, analog signals retain their inherent natural characteristics [1]. Analog signals are processed using analog circuits, where required impedance and capacitance values are typically large. Biomedical filter applications, Phase Locked Loops (PLLs), and sub-hertz applications generally operate at very low frequencies, necessitating high-value passive elements [2]. However, a large chip area incurs significant costs for the integration of these high-value passive elements [3]. To overcome this limitation, a plethora of active circuit elements have been employed in the design of analog circuits [4]. Capacitance multiplier and active inductance simulator circuits are among the primary components utilized for this purpose [5].

Beyond merely reducing the physical footprint of passive components, generalized impedance multipliers hold substantial potential for a wide range of integrated circuit (IC) challenges [6]. For instance, positive capacitance and inductance multipliers can easily emulate the massive time constants required in sub-Hz biomedical sensor interfaces without sacrificing silicon area [7]. Furthermore, the negative impedance multiplication capability is highly sought after for parasitic cancelation techniques [8]. Negative capacitors and resistors can be strategically connected to high-impedance nodes to neutralize unwanted parasitic elements, thereby extending the high-frequency bandwidth of amplifiers and compensating for inherent ohmic losses in oscillator designs [9,10]. Additionally, compact capacitance multipliers are highly beneficial in minimizing the area of loop filters within PLL systems [11]. Therefore, an electronically tunable, floating, and generalized positive/negative impedance multiplier provides a versatile building block for diverse analog signal processing applications.

Impedance multiplier circuits reported in the literature employ a variety of active building blocks such as CCII, CFOA, VCII, VDBA, OTRA, VDTA, CCCDTA, and OTA. These designs differ in terms of configuration (floating or grounded), electronic tunability, functionality (capacitance and/or inductance multiplication), and impedance type (positive or negative). A comparative summary of these previously reported circuits is provided in Table 1.

Table 1. Comparison of impedance multiplier circuits.

Ref.	Type of Impedance	Floating/Grounded	Type of Multiplier (Positive/Negative)	Electronically Tunable	Active Elements	Passive Elements (F/G)
[2]	C	Grounded	Positive	Yes	1 MO-VDTA	1/0
[3]	C	Grounded	Positive	Yes	1 CCCDTA	1/0
[5]	L, C	Floating	Positive	No	3 CCII	0/4
[6]	R, C	Grounded	Both	Yes	1 CFOA, 2 OTA	0/1
[8]	C	Grounded	Positive	Yes	1 ECCII, 1 DVB	1/0
[10]	C	Grounded	Both	No	2 VCII	2/1
[12]	R, C	Floating	Both	Yes	2 OTA, 2 CCII	0/1
[13]	L	Grounded	Both	Yes	1 VCII+, 1 OTA	1/1
[14]	C	Grounded	Positive	No	1 ICFOA	1/2
[15]	C	Grounded	Negative	No	1 CFOA	2/1
[16]	C	Grounded	Positive	No	2 CFOA	1/1
[17]	C	Grounded	Positive	No	2 CFOA	1/2
[18]	C	Grounded	Positive	Yes	1 FB-VDBA	2/0
[19]	C	Grounded	Positive	No	2 CFOA	2/2
[20]	C	Grounded	Both	Yes	1 E-VCII	1/0
[21]	C	Grounded	Positive	Yes	1CFDITA	2/1
[22]	C	Grounded	Both	Yes	1 OTRA, 1 VF	4/0
[23]	C	Grounded	Positive	Yes	1VDTA	1/0
[24]	C	Grounded	Positive	Yes	1 CCIIITA	0/1
[25]	FDNR, L, C	Floating	Both	No	3 CFOA	3/0
[26]	C	Grounded	Both	Yes	2 CFTA	1/2
[27]	C	Grounded	Positive	Yes	1 CFDITA	2/0
[28]	C	Floating	Positive	Yes	3 LT1228	1/0
This Work	**R, L, C**	**Floating**	**Both**	**Yes**	**3 OTA**	**0/1**

In the literature, active impedance synthesis is widely utilized to overcome the severe silicon area limitations of large passive components. Traditional approaches predominantly rely on impedance transformation networks, such as Gyrator-C architectures for active inductors (AIs) and Antoniou Generalized Impedance Converters (GICs) [29–31]. While these structures are effective in simulating on-chip inductors for RF applications or tuning frequency responses, they fundamentally operate as impedance inverters. Unlike gyrators

and Antoniou circuits that alter the inherent phase characteristics of the base element to simulate a different type of reactance, the generalized impedance multiplier proposed in this study acts as an impedance scaler. It preserves the electrical nature and phase angle of the base impedance. This characteristic provides a significant structural advantage for designing area-efficient on-chip compensation circuits without introducing unwanted phase shifts.

This study proposes a generalized impedance multiplier circuit capable of realizing resistance, capacitance, and inductance multiplication. The design consists of three CMOS-based OTAs and a single base impedance element, offering lossless operation without the need for external passive components. Its OTA-based structure enables both positive and negative impedance multiplication with electronic controllability. The circuit's performance was evaluated through non-ideal analyses, including parasitic effects, followed by comprehensive LTspice simulations covering process-voltage-temperature (PVT) variations, frequency response, and time-domain behavior. The proposed design was further applied to low-pass, high-pass, and band-pass filter implementations in LTspice. Additionally, frequency-domain simulations were conducted for each impedance type using the LM13700 IC, a commercial equivalent of the OTA employed in the proposed circuit.

The remainder of the paper is organized as follows: Section 2 presents the proposed generalized impedance multiplier. Section 3 analyzes its non-ideal behavior. Section 4 details the circuit simulations. Section 5 applies the capacitance multiplication to low-pass, band-pass, and high-pass filters. Section 6 validates the impedance multiplication through simulations with the LM13700 IC. Finally, Section 7 compares the performance of the proposed design with existing circuits in the literature.

2. Proposed Impedance Multiplier Circuit

The block diagram of the proposed electronically tunable floating impedance circuit, which relies on three operational transconductance amplifiers (OTAs), is illustrated in Figure 1. This circuit can be utilized for positive multiplication with the configuration depicted in Figure 1. To achieve negative multiplication, the arrangement shown in Figure 2 is obtained by merely interchanging the connections of positive and negative output terminals in the circuit illustrated in Figure 1.

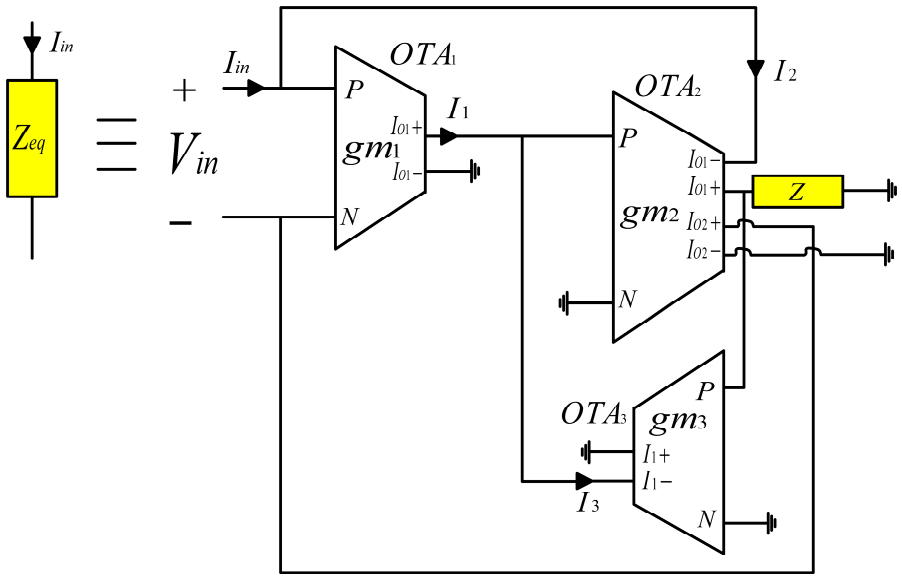


Figure 1. The proposed impedance circuit for positive multiplication.

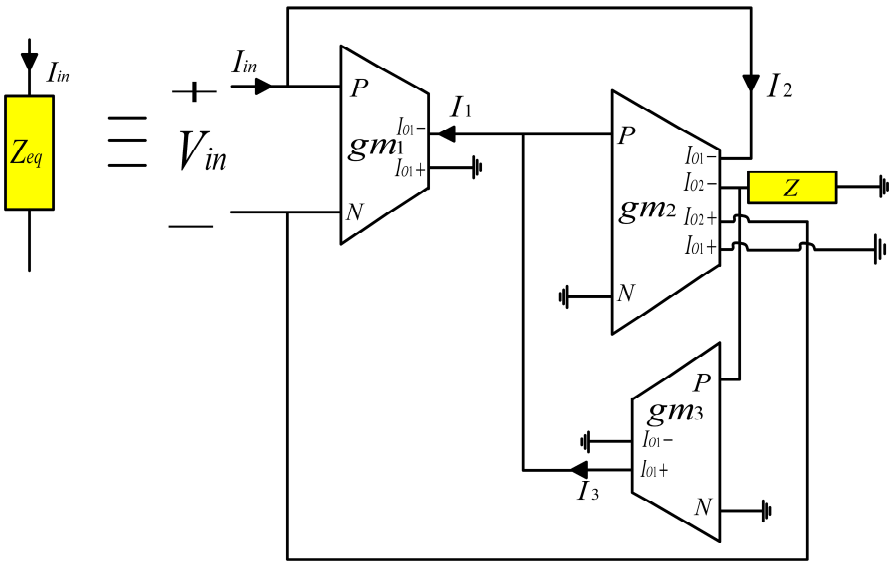


Figure 2. The proposed impedance circuit for negative multiplication.

In Figures 1 and 2, gm_1, gm_2, and gm_3 represent the transconductance parameters of OTAs, respectively. The output currents I_1, I_2, and I_3, belong to the first, second and third OTAs, respectively. The positive and negative output currents of OTAs are denoted as I_{O+} and I_{O-}, respectively. The base impedance to be multiplied is denoted as Z, while Z_{eq} signifies the resultant floating impedance obtained from this multiplication. For the positive impedance multiplier circuit illustrated in Figure 1, Z_{eq} is determined as follows:

$$I_{O+} = -(I_{O-}) = gm_i(V_{Pi} - V_{Ni}) \tag{1}$$

$$I_1 = I_3 \tag{2}$$

$$gm_1(V_{in}) = gm_3(V_Z) \tag{3}$$

$$V_Z = I_{in}(Z) \tag{4}$$

$$\frac{V_{in}}{I_{in}} = Z_{eq} = \frac{gm_3}{gm_1}Z \tag{5}$$

Similarly, for the negative impedance multiplier circuit provided in Figure 2, Z_{eq} is calculated as follows:

$$Z_{eq} = -\frac{gm_3}{gm_1}Z \tag{6}$$

After obtaining the general multiplication equations based on the base impedance Z, the equations for resistor, capacitor, and inductor are derived as follows:

If Z is chosen as R, for positive multiplication:

$$Z_{eq} = R_{eq} = \frac{gm_3}{gm_1}R \tag{7}$$

For negative multiplication:

$$Z_{eq} = R_{eq} = -\frac{gm_3}{gm_1}R \tag{8}$$

If Z is chosen as C, for positive multiplication:

$$Z_{eq} = \frac{1}{SC}\frac{gm_3}{gm_1} \tag{9}$$

$$C_{eq} = C\frac{gm_1}{gm_3} \tag{10}$$

If Z is chosen as C, for negative multiplication:

$$Z_{eq} = -\frac{1}{SC}\frac{gm_3}{gm_1} \tag{11}$$

$$C_{eq} = -C\frac{gm_1}{gm_3} \tag{12}$$

If Z is chosen as L, for positive multiplication:

$$Z_{eq} = SL\frac{gm_3}{gm_1} \tag{13}$$

$$L_{eq} = L\frac{gm_3}{gm_1} \tag{14}$$

If Z is chosen as L, for negative multiplication:

$$Z_{eq} = -SL\frac{gm_3}{gm_1} \tag{15}$$

$$L_{eq} = -L\frac{gm_3}{gm_1} \tag{16}$$

The CMOS circuit implementation of the Multi-Output OTA (MO-OTA) is shown in Figure 3. The transconductance gain (g_m) of MO-OTAs is obtained as depicted in (17).

$$g_m = B\sqrt{k_n I_{BMO}\left(\frac{W}{L}\right)_I} \tag{17}$$

Here, B denotes the ratio of the widths of the current mirrors (e.g., $(W_{M7}/W_{M6}) = (W_{M8}/W_{M5}) = B$), I_{BMO} represents the bias current, and $\left(\frac{W}{L}\right)_I$ expresses the ratio of the dimensions of the MOSFETs connected to the P and N input terminals.

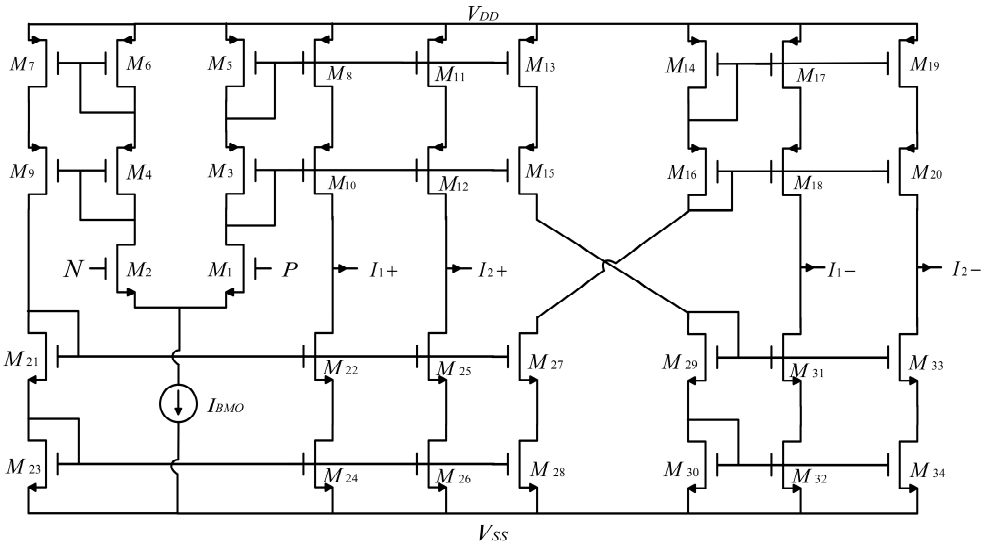


Figure 3. CMOS-based realization of the MO-OTA.

A cascode output stage is adopted in the OTA design to significantly increase the output impedance and, consequently, the overall DC gain. High DC gain is essential for the correct operation of the proposed impedance multiplier circuits. It ensures that the non-

ideal gain error factor (β) remains close to unity, which is critical for minimizing magnitude and phase deviations, particularly when operating at high multiplication factors (K).

3. Parasitic Analysis

In practical implementations, an OTA deviates from ideal behavior. Ideally, its output current is linearly proportional to the input voltage difference with infinite gain. However, due to internal limitations, the OTA exhibits finite gain, modeled by a gain error factor ($\beta < 1$):

$$I_{out} = \beta g_m (V_P - V_N) \tag{18}$$

Finite output resistance, limited voltage swing, and loading effects cause this deviation, which becomes more pronounced at high frequencies. Furthermore, the transconductance (g_m) is frequency-dependent and decreases with increasing frequency. This can be expressed by a single-pole transfer function:

$$g_m(s) = \frac{g_m}{1 + \frac{s}{\omega_p}} \tag{19}$$

where ω_p denotes the pole frequency that determines the bandwidth of the OTA. This model indicates that the OTA suffers from gain reduction at high frequencies, thereby influencing the overall frequency response of the designed circuit. Therefore, during circuit analysis, both the OTA's gain non-ideality (β) and its limited frequency response (ω_p) should be considered. These two non-ideal effects play a crucial role in determining the impedance expression and restricting the operating frequency range of the circuit.

The parasitic impedances of the proposed positive impedance multiplier circuit are provided in Figure 4.

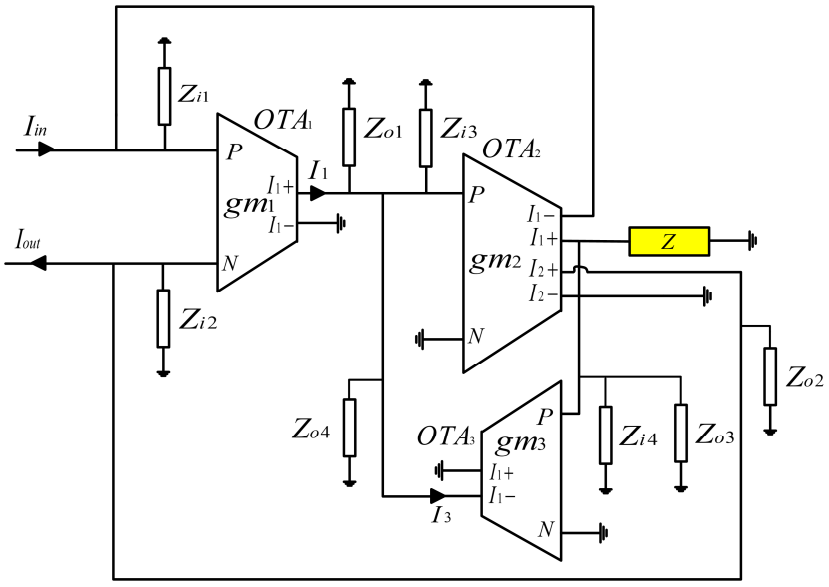


Figure 4. The proposed positive impedance multiplier circuit, along with its parasitic impedances.

In Figure 4, the input and output parasitic impedances are represented as Z_i and Z_o, respectively. The parasitic impedances consist of parasitic resistors and capacitors that are parallel to each other. The structure of the input and output impedances is as follows: $Z_i = R_i \parallel X_{Ci}$, $Z_o = R_o \parallel X_{Co}$. Here, R_i and C_i represent the input parasitic resistance and capacitance, while R_o and C_o represent the output parasitic resistance and capacitance.

The ideal input and output impedances of OTAs are infinite; however, in real-world conditions, the input resistance and capacitance are determined as 100 MΩ and 50 fF,

respectively. The output resistance and capacitance are set at levels of 1 MΩ and 100 fF, respectively [32,33].

The impedances of Z_{i1}, Z_{i2}, Z_{i3}, Z_{o1}, Z_{o2} and Z_{o4} are considered negligible owing to their exceedingly high-impedance values.

$$I_1 \cong \beta_1 g_{m1}(s) V_{in} \tag{20}$$

$$V_Z \cong I_{in}(Z(s) \parallel Z_{i4}(s) \parallel Z_{o3}(s)) \tag{21}$$

$$\beta_1 g_{m1}(s) \times V_{in} \cong \beta_3 g_{m3}(s)(I_{in}(Z(s) \parallel Z_{i4}(s) \parallel Z_{o3}(s))) \tag{22}$$

Equation (22) can be rearranged to obtain the input impedance (Z_{eq}), as shown in Equation (23).

$$\frac{V_{in}}{I_{in}} = Z_{eq}(s) \approx \frac{\beta_3 g_{m3}(s)}{\beta_1 g_{m1}(s)} (Z(s) \parallel Z_{i4}(s) \parallel Z_{o3}(s)) \tag{23}$$

In addition to the base impedance Z, the admittance Y_{par} obtained through the generalized impedance multiplier circuit, which also includes the parasitic effects and non-ideal behaviors of the proposed design, is given in Equation (24).

$$Y_{par}(s) = \frac{1}{Z(s)} + G_{tot} + s\, C_{tot} \tag{24}$$

$$C_{tot} = C_{i4} + C_{o4} \tag{25}$$

$$G_{tot} = \frac{1}{R_{i4}} + \frac{1}{R_{o4}} \tag{26}$$

$N(s)$ and $D_{\text{full}}(s)$ represent the numerator and denominator polynomials, respectively, of the function that expresses the equivalent impedance Z_{eq} obtained from the proposed circuit, including the non-ideal effects, as given below.

$$Z_{eq}(s) = \frac{N(s)}{D_{full}(s)} = \frac{\beta_3 g_{m3}(s)}{\beta_1 g_{m1}(s)} \frac{1}{Y_{par}(s)} \tag{27}$$

$$g_{m1}(s) = \frac{g_{m1}}{1 + \frac{s}{\omega_{p1}}},\ g_{m3}(s) = \frac{g_{m3}}{1 + \frac{s}{\omega_{p3}}} \tag{28}$$

$$N(s) = \beta_3 g_{m3} \omega_{p3} \left(s + \omega_{p1}\right) = b_1 s + b_0 \tag{29}$$

$$b_1 = \beta_3 g_{m3} \omega_{p3}, \qquad b_0 = \beta_3 g_{m3} \omega_{p3} \omega_{p1} \tag{30}$$

$$D_{full}(s) = \beta_1 g_{m1} \omega_{p1} \left(s + \omega_{p3}\right) Y_{par}(s) \tag{31}$$

$$Y_{par}(s) = Y_0 + Y_1 s + Y_2 s^2 \tag{32}$$

$$a_0 = \beta_1 g_{m1} \omega_{p1}\, \omega_{p3}\, Y_0 \tag{33}$$

$$a_1 = \beta_1 g_{m1} \omega_{p1} \left(Y_0 + \omega_{p3} Y_1\right) \tag{34}$$

The lower and upper operating frequency limits of the generalized impedance multiplier circuit are given in Equations (35) and (36), respectively.

$$f_L \approx \frac{1}{2\pi} \frac{a_0}{a_1} = \frac{1}{2\pi} \frac{\omega_{p3} Y_0}{Y_0 + \omega_{p3} Y_1} \tag{35}$$

$$f_H \approx \frac{1}{2\pi} \frac{b_0}{b_1} = \frac{\omega_{p1}}{2\pi} \tag{36}$$

The analysis of the operating frequency range of the proposed impedance multiplier circuit has been extended as follows for the cases where the base impedance is resistive, capacitive, or inductive.

First, when the base impedance is a resistance R and its admittance is G, the operating frequency ranges of the proposed circuit are obtained as follows.

$$Y_0 = G_{tot} + G, \quad Y_1 = C_{tot}, \quad Y_2 = 0 \tag{37}$$

$$f_L^{(R)} \approx \frac{1}{2\pi} \frac{\omega_{p3}\,(G_{tot} + G)}{(G_{tot} + G) + \omega_{p3} C_{tot}} \tag{38}$$

$$f_H^{(R)} \approx \frac{\omega_{p1}}{2\pi} \tag{39}$$

When the base impedance is a capacitance C, the new operating frequency ranges are obtained as follows.

$$Y_{par}(s) = G_{tot} + s(C_{tot}), \text{ with } C_{tot} = C + C_{i4} + C_{o4} \tag{40}$$

$$Y_0 = G_{tot}, \quad Y_1 = C_{tot}, \quad Y_2 = 0 \tag{41}$$

$$f_L^{(C)} \approx \frac{1}{2\pi} \frac{\omega_{p3}\, G_{tot}}{G_{tot} + \omega_{p3} C_{tot}} \tag{42}$$

$$f_H^{(C)} \approx \frac{\omega_{p1}}{2\pi} \tag{43}$$

Finally, in the extension of the operating frequency analysis, the following frequency ranges are obtained for the base impedance being an inductance L.

$$Y_{\text{par}}(s) = G_{\text{tot}} + sC_{\text{tot}} + \frac{1}{sL} = \frac{s^2 LC_{\text{tot}} + sLG_{\text{tot}} + 1}{sL} \tag{44}$$

$$Z_{\text{eq}}(s) = \frac{b_1 s + b_0}{\beta_1 g_{m1} \omega_{p1} (s + \omega_{p3})} \frac{1}{C_{\text{tot}} s^2 + G_{\text{tot}} s + \frac{1}{L}} \tag{45}$$

$$f_L^{(L)} \approx \frac{1}{2\pi} \frac{\frac{1}{L}}{G_{\text{tot}} + \omega_{p3} C_{\text{tot}}} \tag{46}$$

$$f_H^{(L)} \approx \frac{1}{2\pi} \min\left(\frac{b_0}{b_1}, \omega_{p1}, \omega_{p3} \right) \tag{47}$$

The operating frequency range of the proposed impedance multiplier circuit is determined by the non-ideal characteristics of the OTAs and the nature of the connected load. For a resistive load ($Z = R$), the low-frequency limit depends on the combined conductance of the OTA output and the load ($G_{tot} + 1/R$), while the high-frequency limit is mainly governed by the OTA's transconductance pole (ω_{p1}) and gain non-ideality (β), yielding a wide bandwidth. With a capacitive load ($Z = 1/sC$), the low-frequency cutoff is set by G_{tot}, whereas the high-frequency boundary is again dictated by the OTA pole frequencies, confining proper operation to below the OTA's intrinsic bandwidth. For an inductive load ($Z = sL$), the low-frequency limit arises from the resonance between the inductance and total capacitance (C_{tot}), while the high-frequency limit remains constrained by the OTA's frequency-dependent transconductance. Overall, the usable bandwidth is defined by the combined effects of OTA non-idealities, pole frequencies, and the reactive nature of the load.

4. Simulation Results

The impedance multiplier circuit proposed herein, based on 0.18 µm CMOS technology, has been simulated utilizing the LTspice program. The transistor dimensions for the OTAs employed in the presented circuit are detailed in Table 2. The supply voltages for the OTAs are set as $V_{DD} = 1.8$ V and $V_{SS} = -1.8$ V. The widths of transistors $M_7 - M_{20}$ in Table 2 are individually determined based on the type of impedance to be multiplied. The utilization of the B coefficient in the simulations of impedance multiplier will be elucidated. The input and output impedances of the OTAs were computed using LTspice program, yielding 555.23 MΩ and 2.37 MΩ, respectively.

Table 2. The transistor dimensions for the OTAs.

Transistors	W	L
M_1–M_2	2 µm	0.36 µm
M_{21}–M_{34}	4 µm	0.36 µm
M_3–M_6	2.5 µm	0.36 µm
M_7–M_{20}	$B \times 2.5$ µm	0.36 µm

The simulations of impedance multiplier circuits have been examined under three categories, namely resistance, capacitance, and inductance. Positive and negative multiplication simulations are provided for each category.

4.1. Resistance Multiplier Circuit Simulation

As depicted in Equation (7), if the base impedance is chosen as resistor, the proposed circuit will operate as a resistance multiplier. In both positive and negative multiplication circuits, the base resistor is chosen as $R = 1$ KΩ.

The positive resistance multiplier circuit is obtained by replacing Z with the base resistor (R) in the circuit given in Figure 1. In Table 2, parameter B represents the transistor scaling factor. Accordingly, the widths of transistors M_7–M_{20} are set to 10 µm for OTA_2 and OTA_3 $(B = 4)$, and 2.5 µm for OTA_1 $(B = 1)$.

The bias current for electronic control of the impedance multiplier is given by Equation (17) and denoted as I_{BMO}. The bias currents for OTA_1, OTA_2, and OTA_3 are represented as I_{BMO1}, I_{BMO2}, and I_{BMO3}, respectively. For a given multiplication factor K, the magnitude and phase responses of the positive resistance multiplier are shown in Figures 5 and 6. The OTA bias currents were selected according to the corresponding K values, as summarized in Table 3.

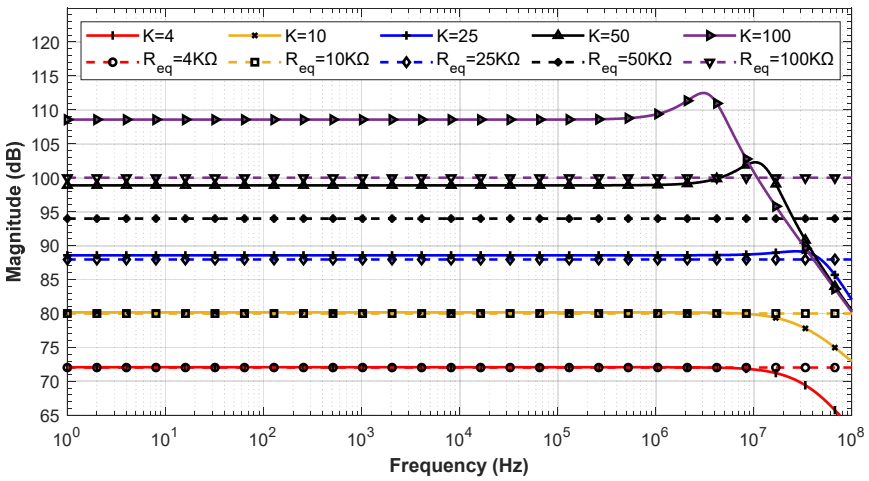


Figure 5. Magnitude response of the positive resistance multiplier circuit.

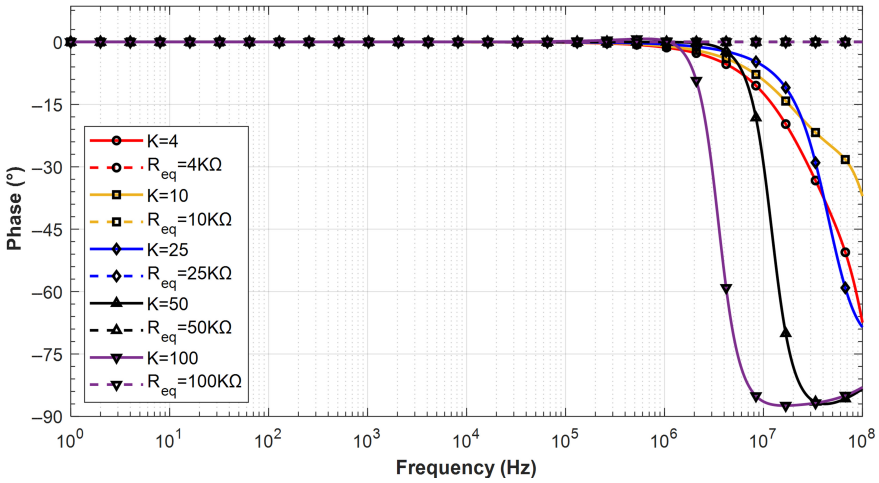


Figure 6. Phase response of the positive resistance multiplier circuit.

Table 3. Simulation results of the positive resistance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
4	100	100	100	0–118 MHz	0.05
10	16	100	100	0–72 MHz	0.22
25	6.4	250	250	0–49 MHz	0.69
50	1.6	250	250	0–12 MHz	4.94
100	0.4	250	250	0–3.5 MHz	7.4

The current resulting from the time-domain multiplication for the positive resistance multiplier circuit with a base resistor of 1 KΩ and $K = 10$ is depicted in Figure 7. The applied voltage source across the resistor is 10 mV peak-to-peak with a frequency of 1 kHz.

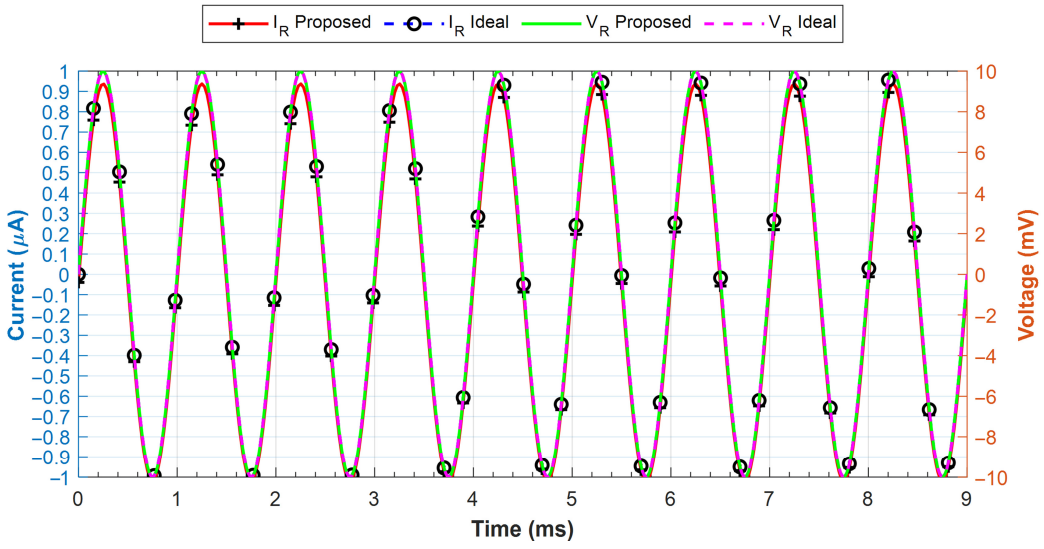


Figure 7. Time-domain analysis of the positive resistance multiplier circuit.

Magnitude and phase responses of the negative resistance multiplier circuit for different K values are provided in Figures 8 and 9, respectively. In the magnitude response simulations of the negative resistance multiplier circuit, the bias current values of the OTAs were selected according to different K values, as presented in Table 4.

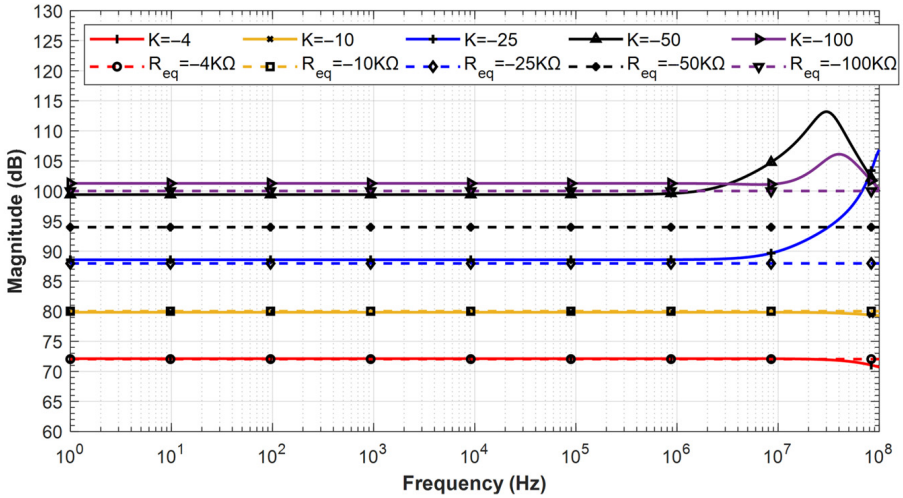


Figure 8. Magnitude response of the negative resistance multiplier circuit.

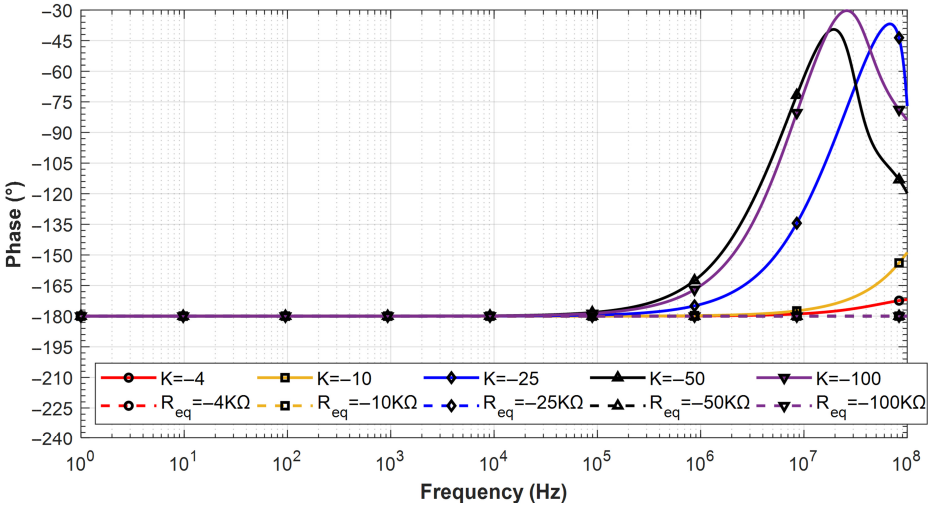


Figure 9. Phase response of the negative resistance multiplier circuit.

Table 4. Simulation results of the negative resistance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
−4	100	100	100	0–120 MHz	0.15
−10	16	100	100	0–98 MHz	0.23
−25	6.4	250	250	0–81 MHz	0.68
−50	1.6	250	250	0–24 MHz	5.45
−100	0.4	250	250	0–28 MHz	1.25

4.2. Capacitance Multiplier Circuit Simulation

The proposed positive capacitance multiplier circuit is obtained when the base impedance is chosen as a capacitance (C) using the connections shown in Figure 1, as expressed in Equations (9) and (10). In Table 2, the parameter B represents the transistor scaling factor that determines the width ratio among the OTAs. Accordingly, the widths of transistors M_7–M_{20} are set to 2.5 µm for OTA_2 and OTA_3 (B = 1) and 10 µm for OTA_1 (B = 4).

Magnitude and phase responses of the positive capacitance multiplier circuit for different K values are provided in Figures 10 and 11, respectively. In the magnitude

response simulations of the positive capacitance multiplier circuit, the bias current values of the OTAs were selected according to different K values, as presented in Table 5.

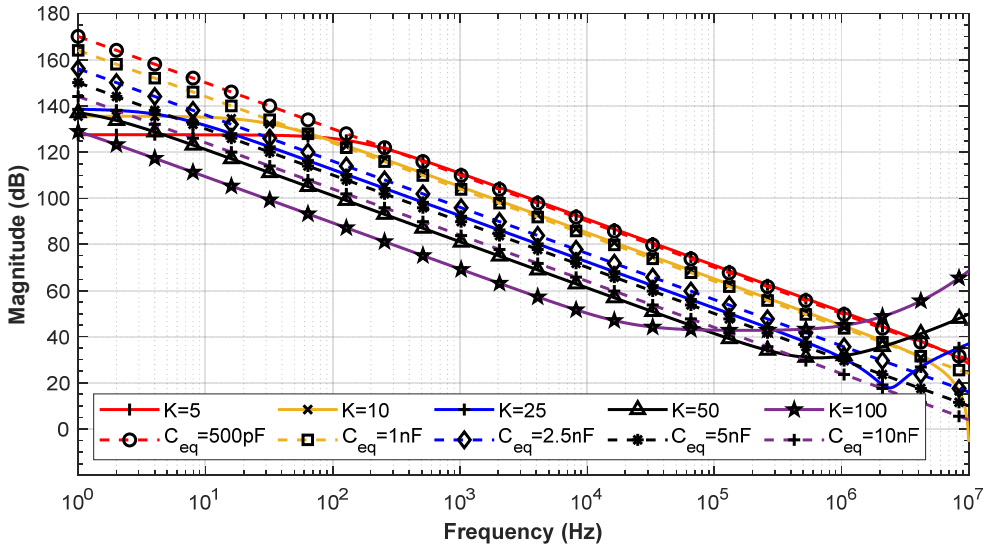


Figure 10. Magnitude response of the positive capacitance multiplier circuit.

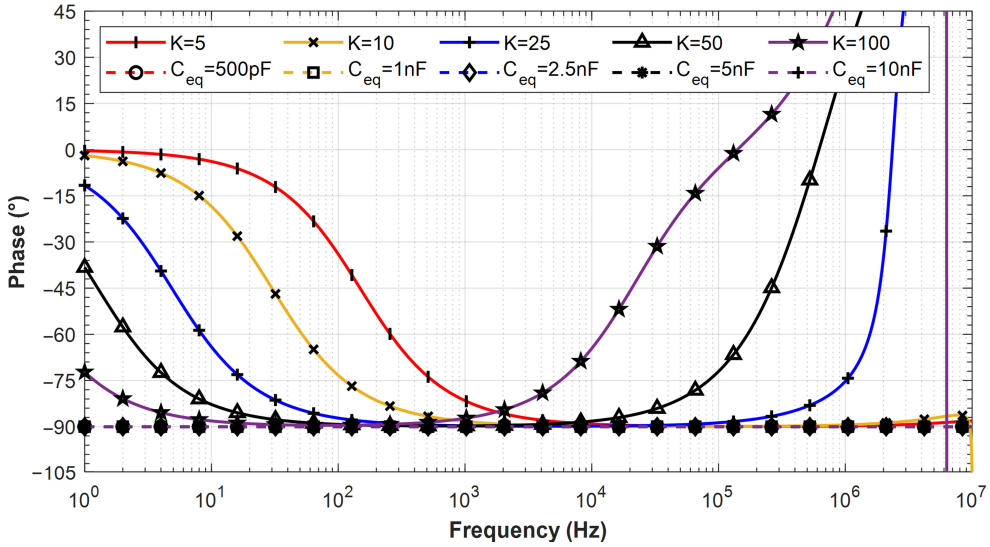


Figure 11. Phase response of the positive capacitance multiplier circuit.

Table 5. Simulation results of the positive capacitance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
5	125	80	80	200 Hz–20 MHz	1.31
10	125	20	20	25 Hz–12 MHz	1.80
25	125	3.2	3.2	up to 2 MHz	6.98
50	125	0.8	0.8	up to 627 kHz	9.89
100	125	0.2	0.2	up to 60 kHz	16.68

The current resulting from the time-domain multiplication for the positive capacitance multiplier circuit with a base capacitor of 1 nF and K = 10 is depicted in Figure 12. The applied voltage source across the capacitor is 1 mV peak-to-peak with a frequency of 1 kHz.

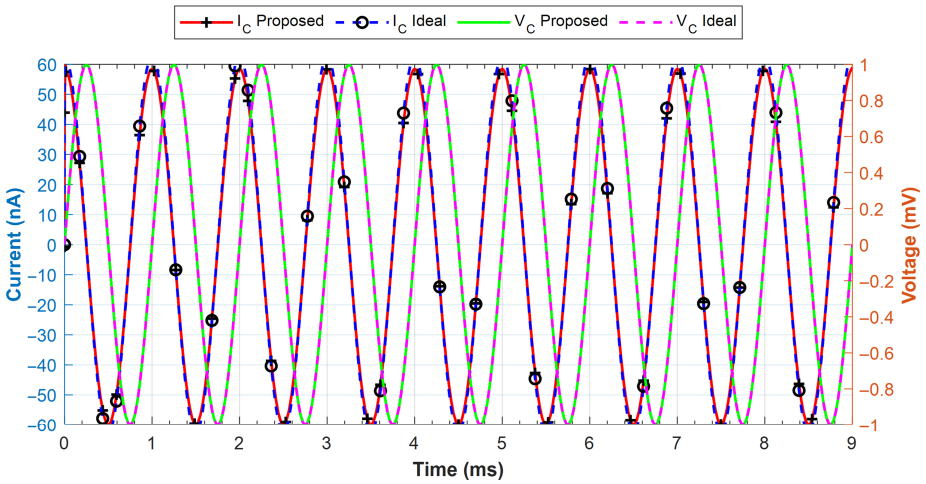


Figure 12. Time-domain analysis of the positive capacitance multiplier circuit.

Magnitude and phase responses of the negative capacitance multiplier circuit for different K values are provided in Figures 13 and 14, respectively. In the magnitude response simulations of the negative capacitance multiplier circuit, the bias current values of the OTAs were selected according to different K values, as presented in Table 6.

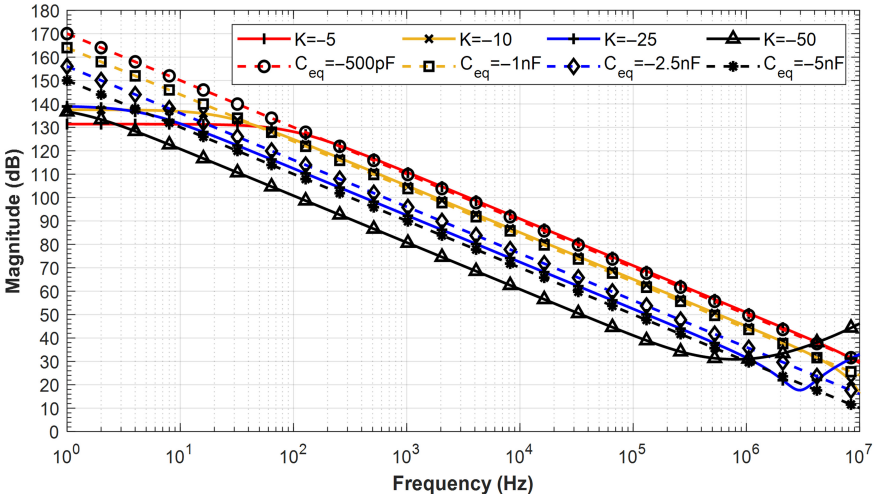


Figure 13. Magnitude response of the negative capacitance multiplier circuit.

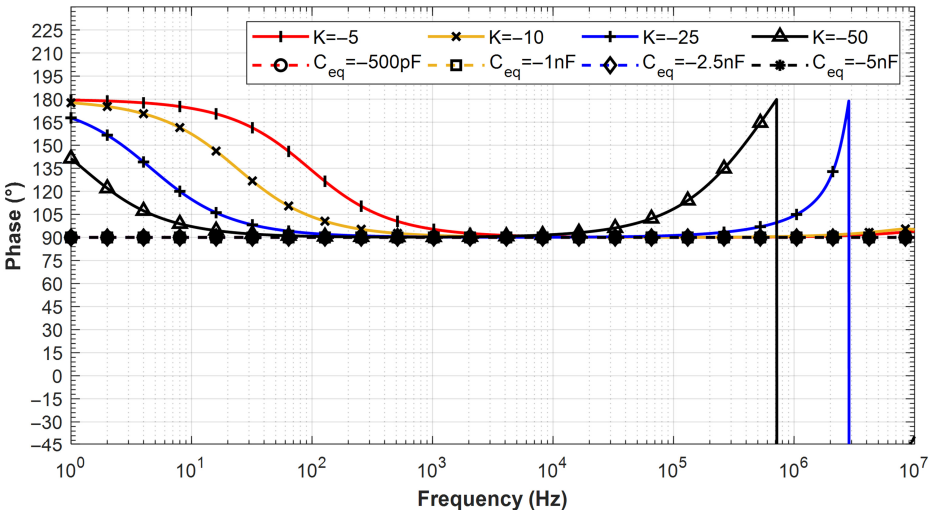


Figure 14. Phase response of the negative capacitance multiplier circuit.

Table 6. Simulation results of the negative capacitance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
−5	125	80	80	100 Hz–20 MHz	0.1
−10	125	20	20	130 Hz–12 MHz	1.26
−25	125	3.2	3.2	up to 2 MHz	4.80
−50	125	0.8	0.8	up to 0.5 MHz	13.1

4.3. Inductance Multiplier Circuit Simulation

The proposed positive inductance multiplier circuit is obtained when the base impedance is selected as inductance (L), using the connections shown in Figure 1, as expressed in Equations (13) and (14). In Table 2, the parameter B represents the transistor scaling factor that defines the width ratio among the OTAs. Accordingly, the widths of transistors M_7–M_{20} are set to 10 µm for OTA_2 and OTA_3 (B = 4), and 2.5 µm for OTA_1 (B = 1).

Active inductor (AI) circuits offer advantages in terms of integrability, tunability, and compact chip area, but due to the presence of active components, they exhibit higher noise levels, reduced linearity, and increased power consumption compared to passive inductors. Conversely, passive inductors provide low noise, excellent linearity, and zero power consumption, but their on-chip integration is challenging and requires a large silicon area. Therefore, AI circuits being particularly suitable for integrated circuit, RF, filter, and biomedical applications, where tunability and compactness are of primary importance.

The bias currents of both OTAs are chosen as 500 µA, and the load capacitance C_L is selected as 350 pF to obtain an inductance value of 1 mH as depicted in Figure 15.

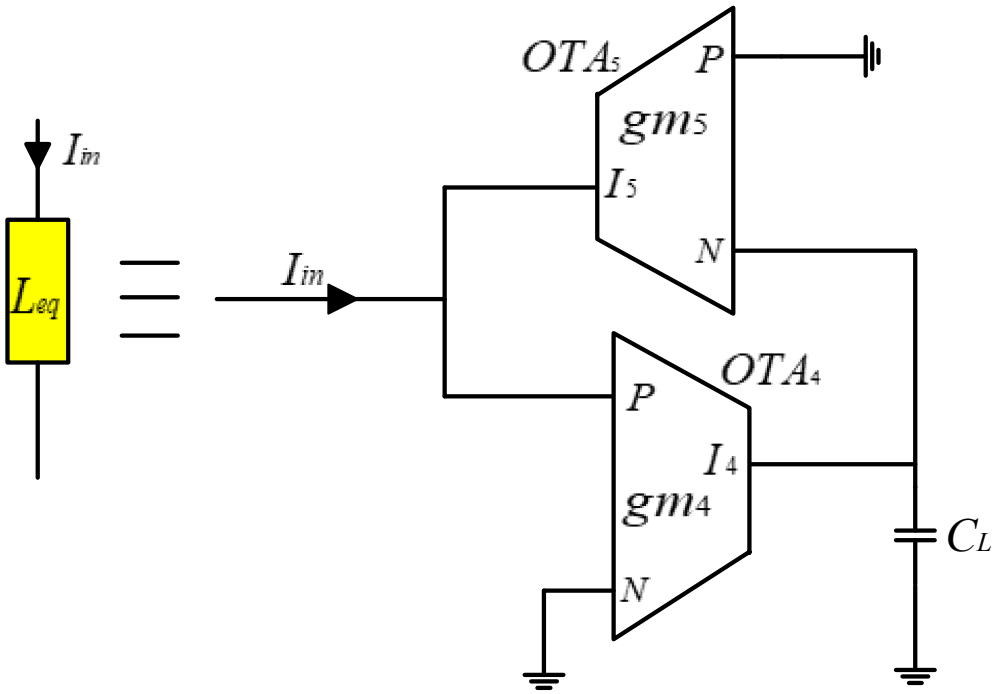


Figure 15. Base AI circuit [34].

Magnitude and phase responses of the positive inductance multiplier circuit for different K values are provided in Figures 16 and 17, respectively. In the magnitude response simulations of the positive inductance multiplier circuit, the bias current values of the OTAs were selected according to different K values, as presented in Table 7.

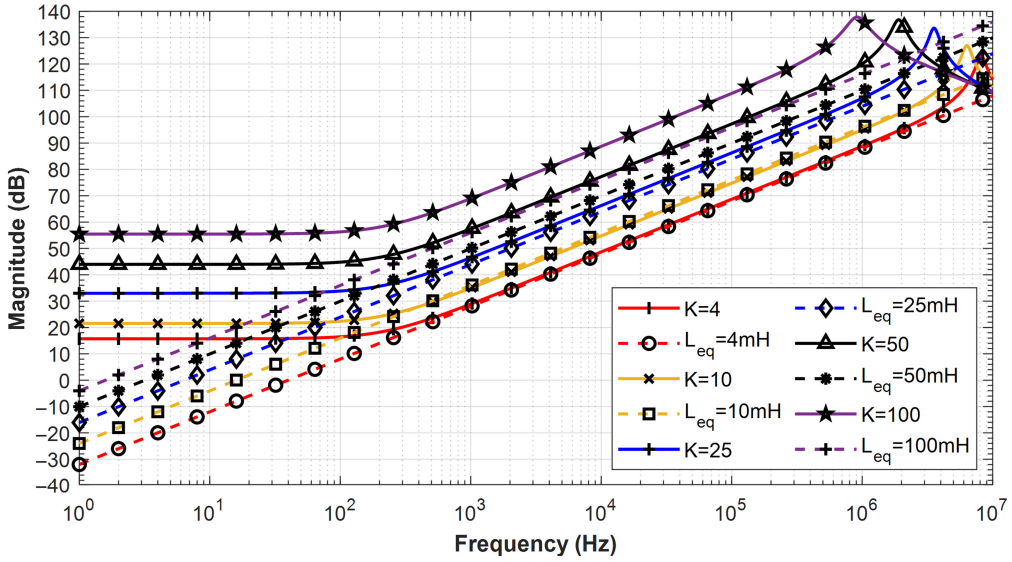


Figure 16. Magnitude response of the positive inductance multiplier circuit.

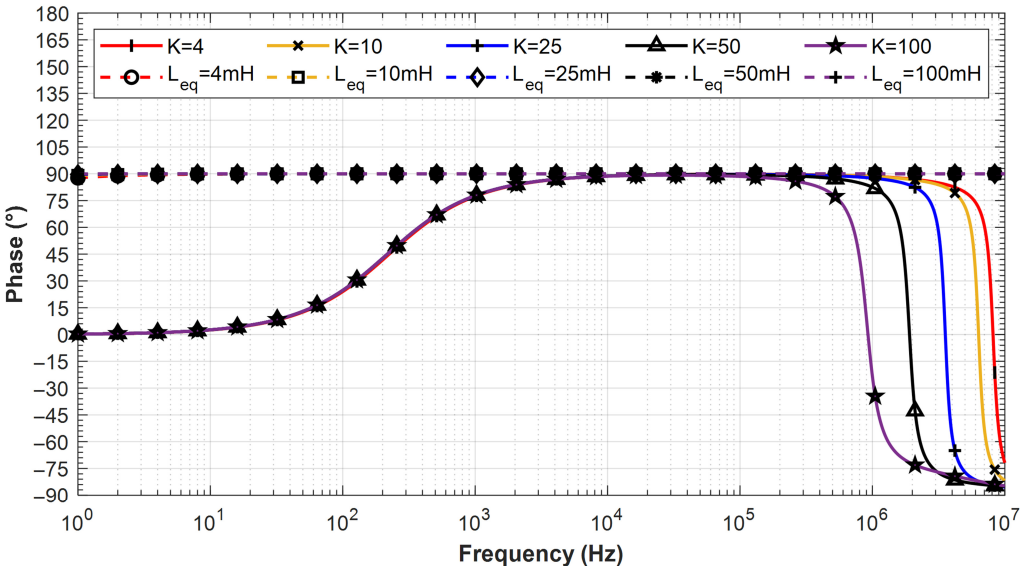


Figure 17. Phase response of the positive inductance multiplier circuit.

Table 7. Simulation results of the positive inductance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
4	200	200	200	285 Hz–4 MHz	1.00
10	32	200	200	250 Hz–3.7 MHz	1.63
25	5.12	200	200	300 Hz–2.8 MHz	2.70
50	1.28	200	200	180 Hz–1.4 MHz	8.06
100	0.32	200	200	210 Hz–0.5 MHz	13.42

The voltage resulting from the time-domain multiplication for the positive inductance multiplier circuit with a base inductor of 1 mH and K = 4 is depicted in Figure 18. The applied current source across the inductor is 100 µA peak-to-peak with a frequency of 10 kHz.

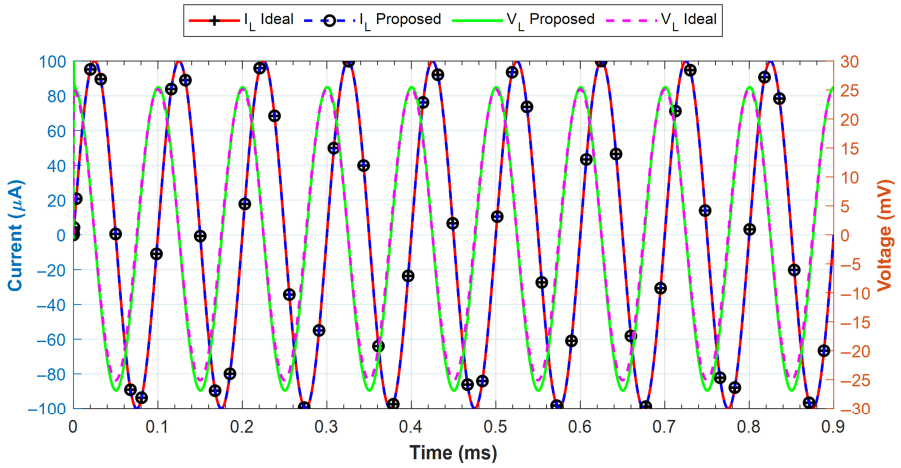


Figure 18. Time-domain analysis of the positive inductance multiplier circuit.

Magnitude and phase responses of the negative inductance multiplier circuit for different K values are provided in Figures 19 and 20, respectively. In the magnitude response simulations of the negative inductance multiplier circuit, the bias current values of the OTAs were selected according to different K values, as presented in Table 8.

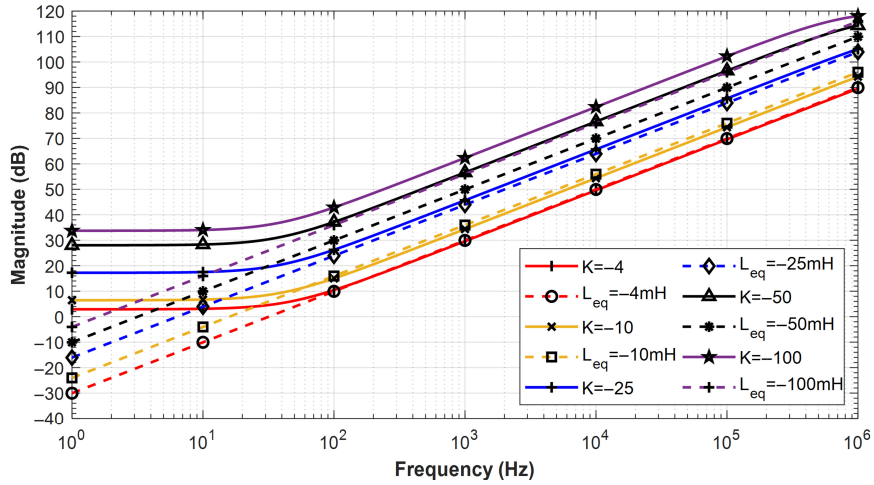


Figure 19. Magnitude response of the negative inductance multiplier circuit.

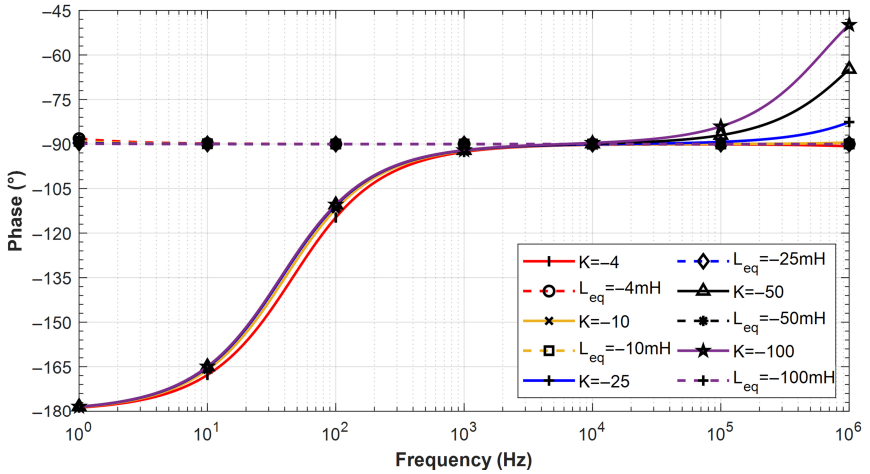


Figure 20. Phase response of the negative inductance multiplier circuit.

Table 8. Simulation results of the negative inductance multiplier circuit for different K values.

K	I_{BMO1}(µA)	I_{BMO2}(µA)	I_{BMO3}(µA)	Operating Frequency	Magnitude Error Ratio (%)
−4	200	200	200	90 Hz–4.5 MHz	1.03
−10	32	200	200	85 Hz–4 MHz	2.84
−25	5.12	200	200	70 Hz–3.2 MHz	2.75
−50	1.28	200	200	60 Hz–1.6 MHz	9.52
−100	0.32	200	200	40 Hz–1 MHz	8.38

5. Filter Applications

The low-pass, high-pass, and band-pass filters shown in Figure 21 were simulated utilizing the proposed positive capacitance multiplier circuit. The Bode plots of these circuits are provided in Figures 22–24, respectively. Here; R_{LP} = 0.5 KΩ, C_{LP} = 10 nF, R_{BP} = 0.25 KΩ, C_{BP} = 10 nF, L_{BP} = 2.5 mH, R_{HP} = 1 KΩ, C_{HP} = 10 nF. In all filter simulations, a positive capacitance multiplier circuit was utilized, with a base capacitor of 1 nF and K = 10 selected.

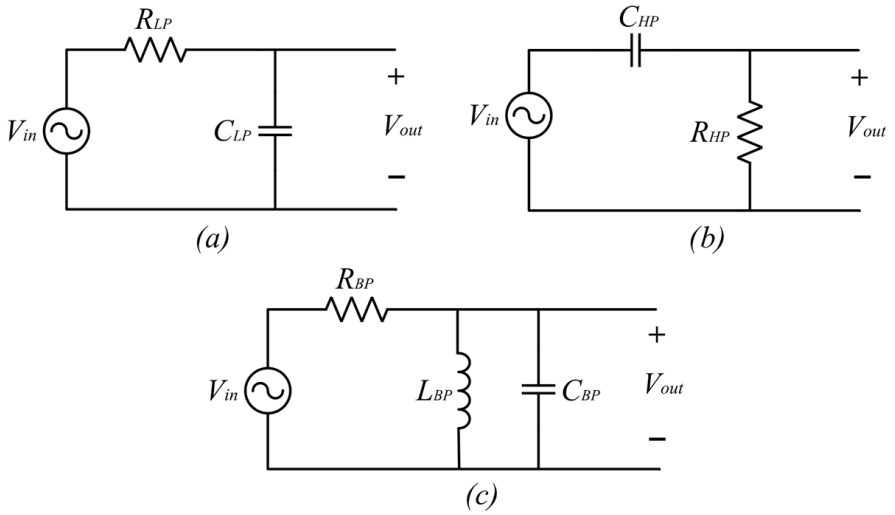


Figure 21. The (**a**) low-pass, (**b**) high-pass, and (**c**) band-pass filters utilized in Bode plot analysis.

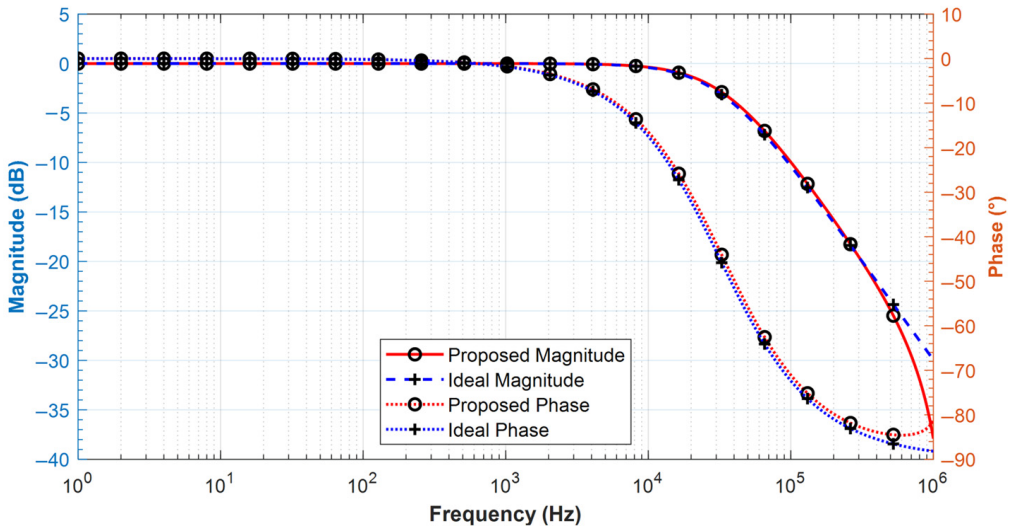


Figure 22. Magnitude and phase response of low-pass filter.

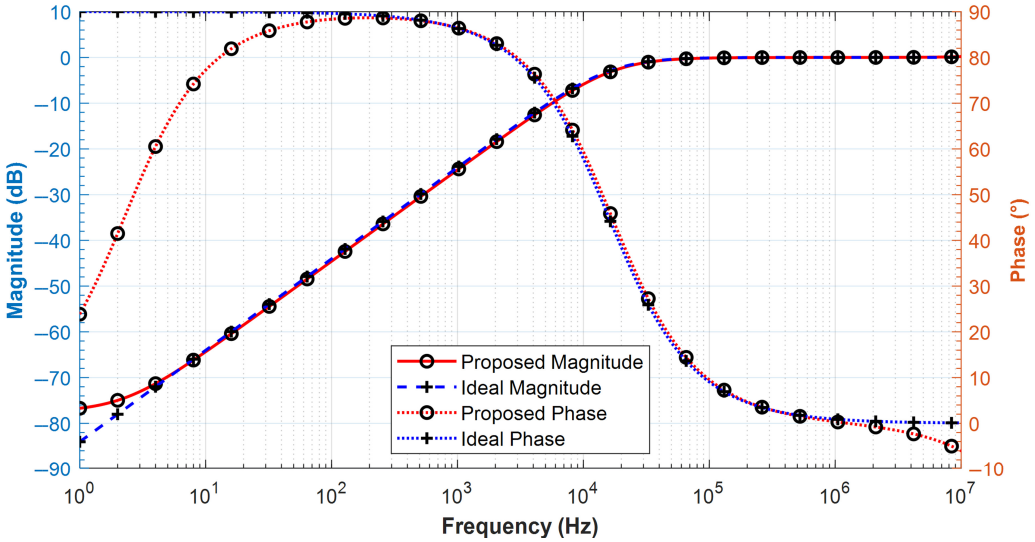


Figure 23. Magnitude and phase response of high-pass filter.

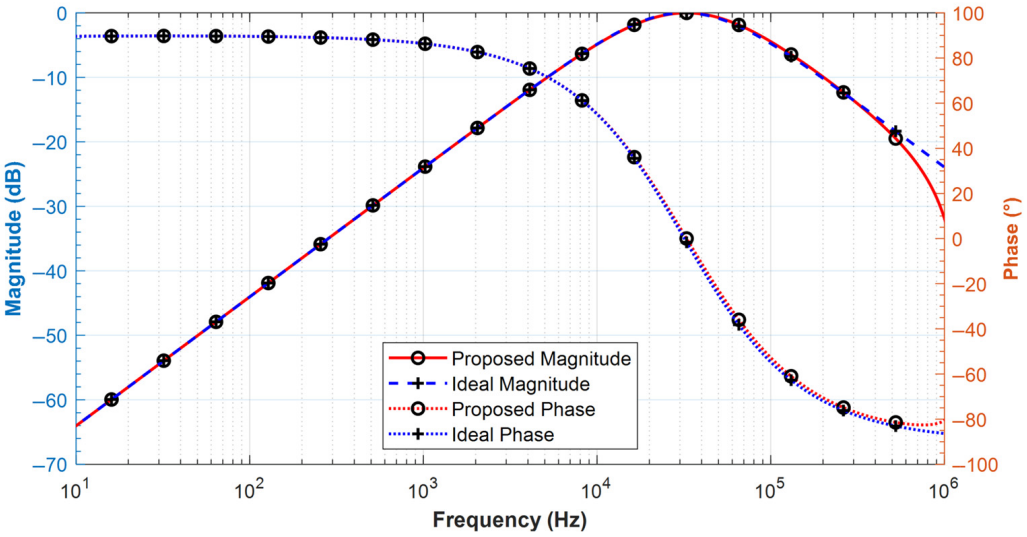


Figure 24. Magnitude and phase response of band-pass filter.

The transfer function H(s) of the voltage-mode band-pass filter is given in Equation (48), as shown in Figure 21c.

$$H(s) = \frac{V_{BP}}{V_{in}} = \frac{s\frac{1}{R_{BP}C_{BP}}}{s^2 + s\frac{1}{R_{BP}C_{BP}} + \frac{1}{L_{BP}C_{BP}}} \tag{48}$$

The resonant frequency (f_0) and quality factor (Q) associated with the band-pass filter are calculated as follows:

$$f_0 = \frac{1}{2\pi\sqrt{L_{BP}C_{BP}}} \tag{49}$$

$$Q = R\sqrt{\frac{C_{BP}}{L_{BP}}} \tag{50}$$

The component values were chosen as $R_{BP} = 0.25\,\text{K}\Omega$, $C_{BP} = 10\,\text{nF}$ and $L_{BP} = 2.5\,\text{mH}$ to achieve a resonant frequency of $f_0 = 31.83\,\text{KHz}$ and a quality factor of $Q = 0.5$.

The PVT analysis of the band-pass filter designed using the proposed positive capacitance multiplier circuit is shown in Figure 25, examining its frequency response under temperature and supply voltage variations. In this study, the capacitance multiplication fac-

tor is set to K = 10, scaling a 1 nF base capacitor to 10 nF. Temperature tests were performed at −40 °C, 25 °C, and 125 °C, while supply voltages varied by ±10% around nominal values. Figure 26 presents the circuit's performance across different process corners (FF, TT, SS). Monte Carlo simulations were also conducted with ±5% variations in MOSFET dimensions, bias currents, and base capacitance to assess robustness against device mismatch and process fluctuations. The results confirm stable capacitance scaling and overall frequency response under all tested conditions.

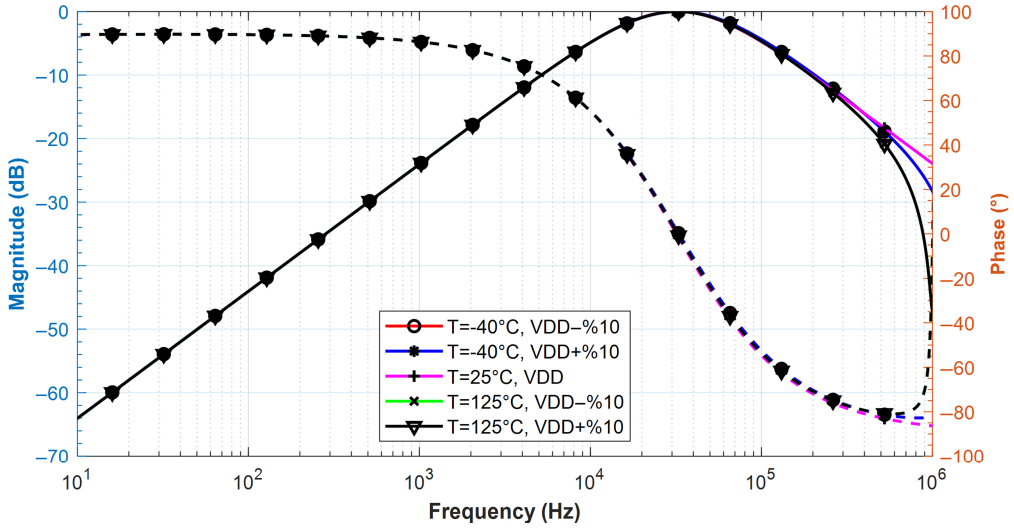


Figure 25. Band-pass filter magnitude and phase responses under temperature and supply voltages variations.

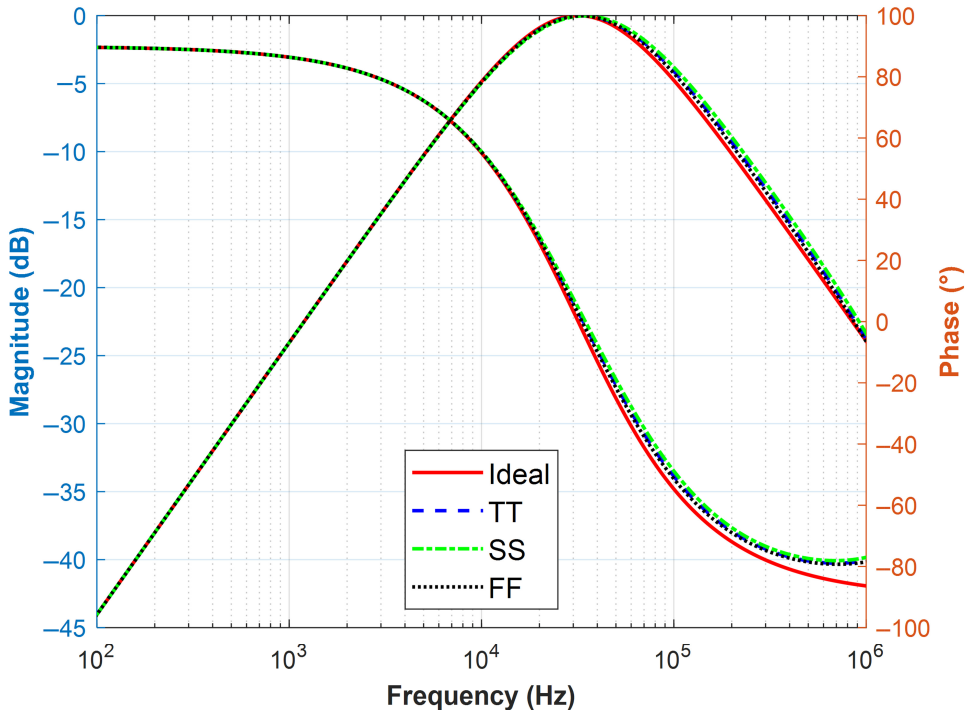


Figure 26. Band-pass filter magnitude and phase responses under process variations.

The proposed capacitance multiplier circuit has been subjected to a Monte Carlo simulation with 1000 runs, considering a ±5% tolerance for transistor dimensions, bias currents, and base capacitors. The results are presented in Figure 27.

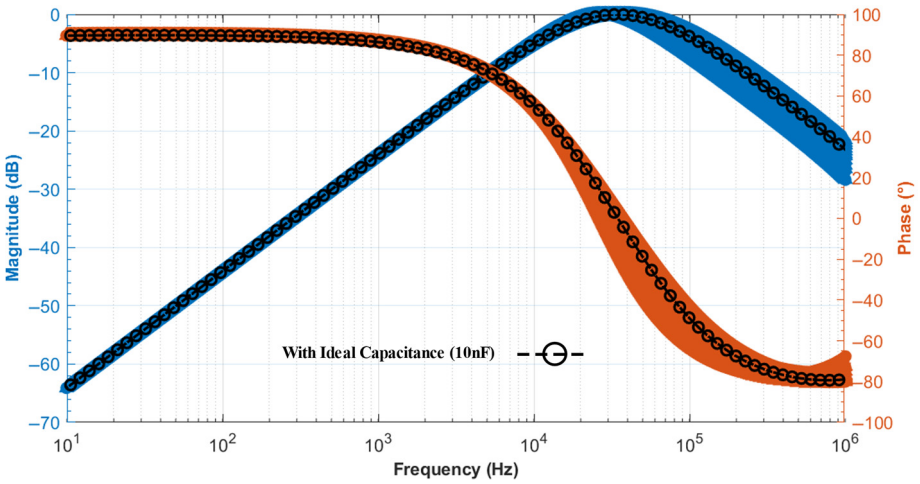


Figure 27. Band-pass filter magnitude and phase responses under Monte Carlo test.

Table 9 summarizes the Total Harmonic Distortion (THD) and noise performance of the proposed core circuit for different impedance multiplier configurations, with THD calculated based on the first 20 harmonics. All analyses were conducted for a multiplication factor of K = 10. The base inductance of 1 mH was realized using two OTAs biased at 500 µA with a 350 pF capacitor, enabling the inductive multiplication function.

Table 9. THD results of the core circuit for different multiplier configurations.

Multiplier Type	Base Element	K	IBMO/IB	Input Source	Base Impedance Realization	THD (%)	Total Noise (μV_{RMS})
Resistance	1 KΩ	10	100 µA/16 µA.	1 mV_{pp}, 1 kHz (voltage)	-	0.043	57.03
Capacitance	1 nF	10	20 µA/125 µA	1 mV_{pp}, 1 kHz (voltage)	-	0.096	971.03
Inductance	1 mH (2 OTAs + 350 pF)	10	200 µA/32 µA	100 μA_{pp} , 1 kHz (current)	OTA-based realization	0.430	54.769 * 575.06 **

* Core circuit. ** All circuits (with inductance simulator).

Noise performance, reported as total RMS values in Table 9, was evaluated over a 1 Hz–10 MHz frequency range to capture wideband characteristics. For the inductive multiplier, the results include both the core circuit noise and the combined contribution of the base inductance simulator, presented separately in Table 9.

6. Commercial OTA-Based Simulation Study

The commercial applicability and topological portability of the proposed generalized impedance multiplier were verified through SPICE simulations using the LM13700 OTA. The primary objective of this Commercial Off-The-Shelf (COTS)-based implementation is solely to validate the robustness of the proposed mathematical topology and to prove its functional workability using commercially accessible components. The detailed schematic of this COTS simulation setup is presented in Figure 28. In this design, the g_m of the OTA is linearly controlled by an external DC bias current (I_{ABC}). Bode analyses were conducted for resistance, capacitance, and inductance multiplication configurations with a target multiplication factor of K = 10. The base impedance values were set to 1 kΩ, 1 nF, and 1 mH, respectively. The LM13700 was powered by a ±18 V supply. For the resistance and inductance configurations, I_{ABC} was set to 1 mA for OTA_2 and OTA_3, and 100 µA for OTA_1. Conversely, for the capacitance multiplication, I_{ABC} was set to 100 µA for OTA_2 and

OTA_3, and 1 mA for OTA_1. The resulting magnitude and phase responses, which strictly confirm the expected theoretical impedance multiplication characteristics, are presented in the following figures.

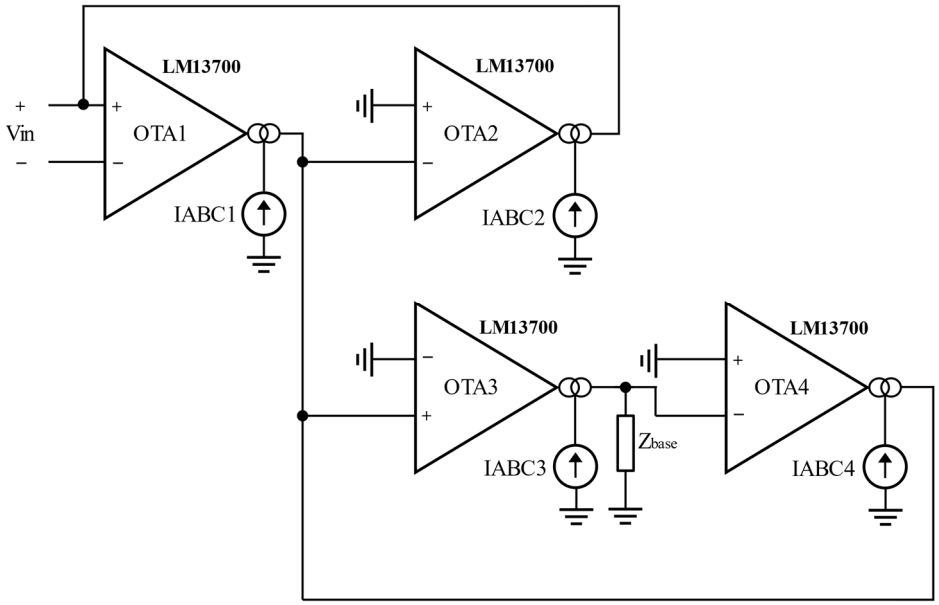


Figure 28. Schematic diagram of the proposed impedance multiplier implemented with LM13700 OTA for COTS-based verification.

As shown in Figures 29–40, the proposed impedance multiplication circuits exhibited correct operation within defined frequency ranges. Positive resistance multiplication functioned accurately up to approximately 1.7 MHz, while the negative resistance configuration remained stable up to around 1.4 MHz. For capacitance multiplication, the positive configuration operated reliably from 10 kHz to 3.5 MHz, whereas the negative capacitance case was stable between 10 kHz and 2 MHz. In the inductance multiplication setup, the positive inductance circuit functioned from 100 Hz to 400 kHz, and the negative inductance configuration exhibited valid impedance behavior between 100 Hz and 300 kHz.

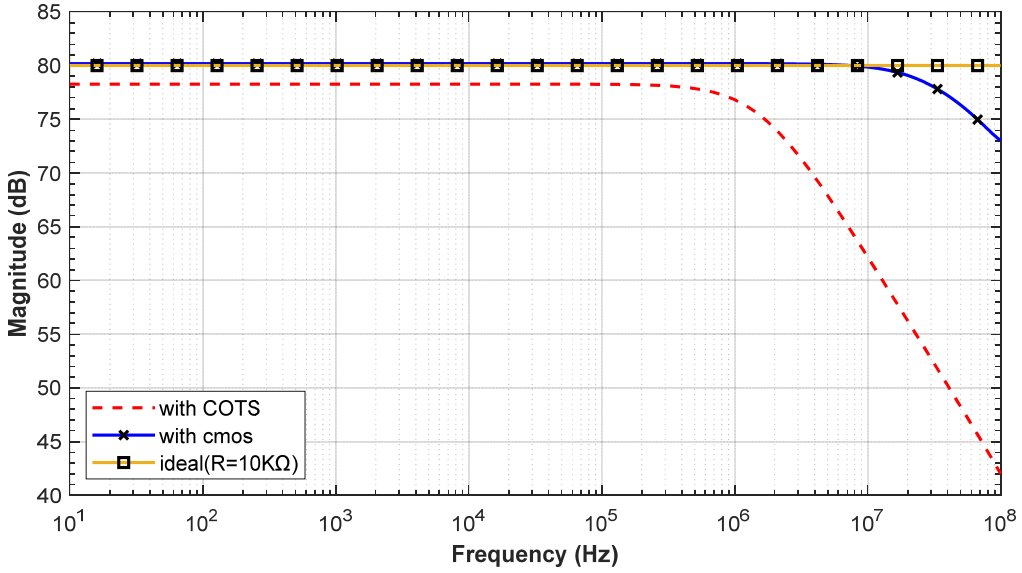


Figure 29. Magnitude response of the proposed circuit for positive resistance multiplication.

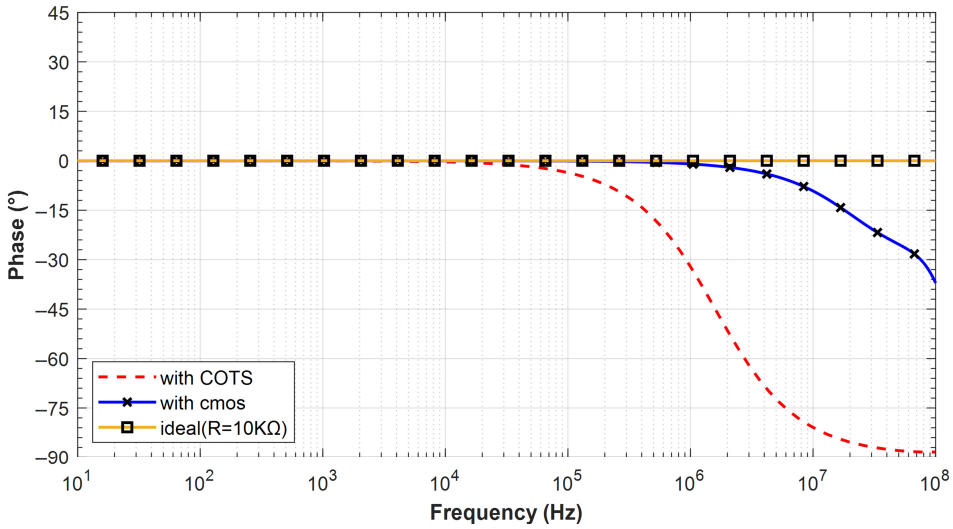


Figure 30. Phase response of the proposed circuit for positive resistance multiplication.

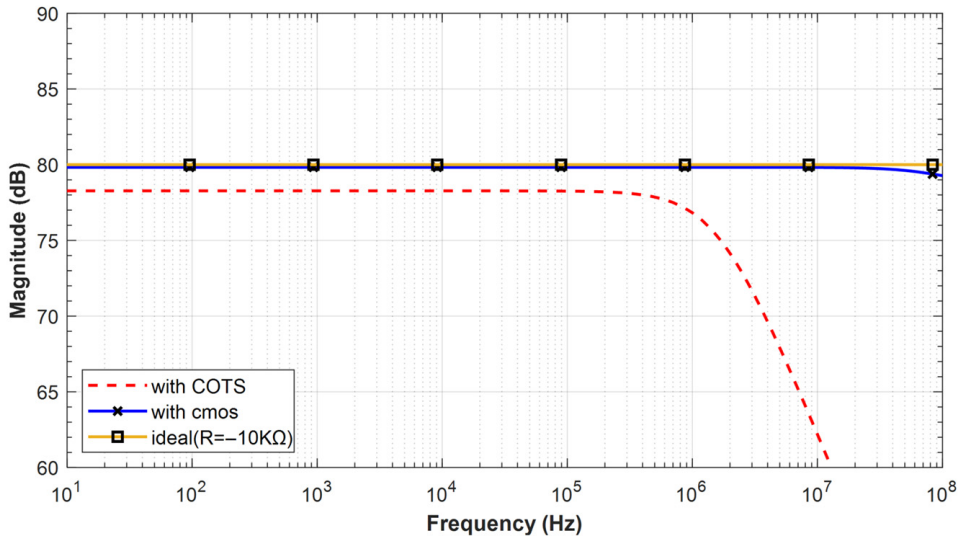


Figure 31. Magnitude response of the proposed circuit for negative resistance multiplication.

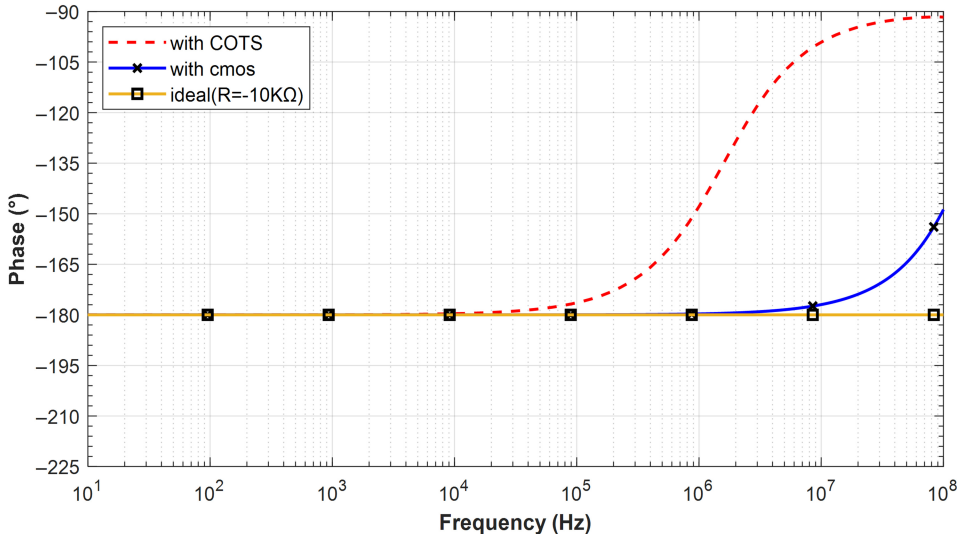


Figure 32. Phase response of the proposed circuit for negative resistance multiplication.

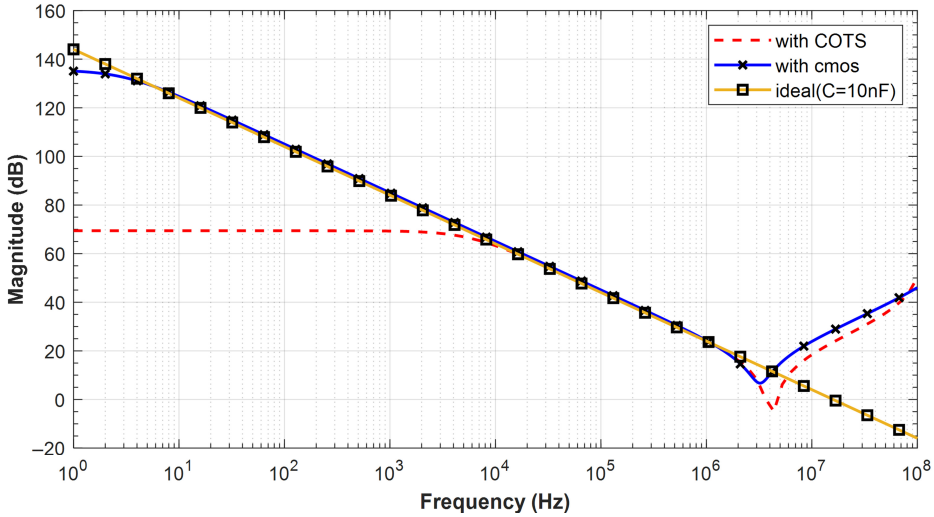


Figure 33. Magnitude response of the proposed circuit for positive capacitance multiplication.

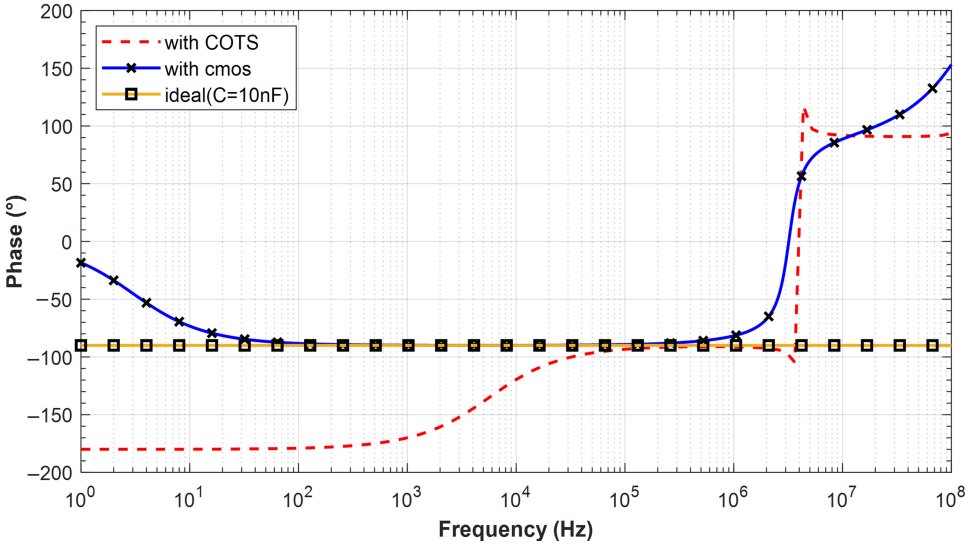


Figure 34. Phase response of the proposed circuit for positive capacitance multiplication.

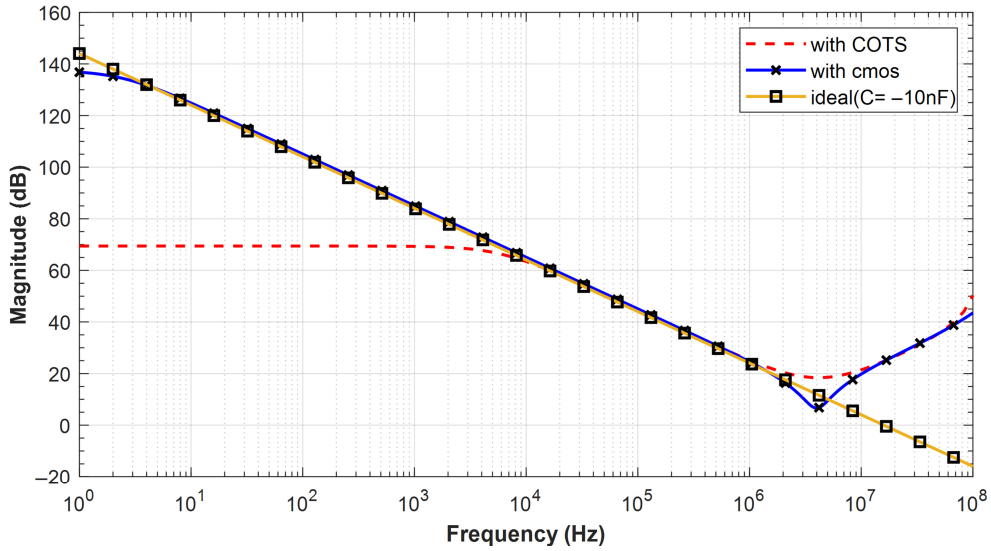


Figure 35. Magnitude response of the proposed circuit for negative capacitance multiplication.

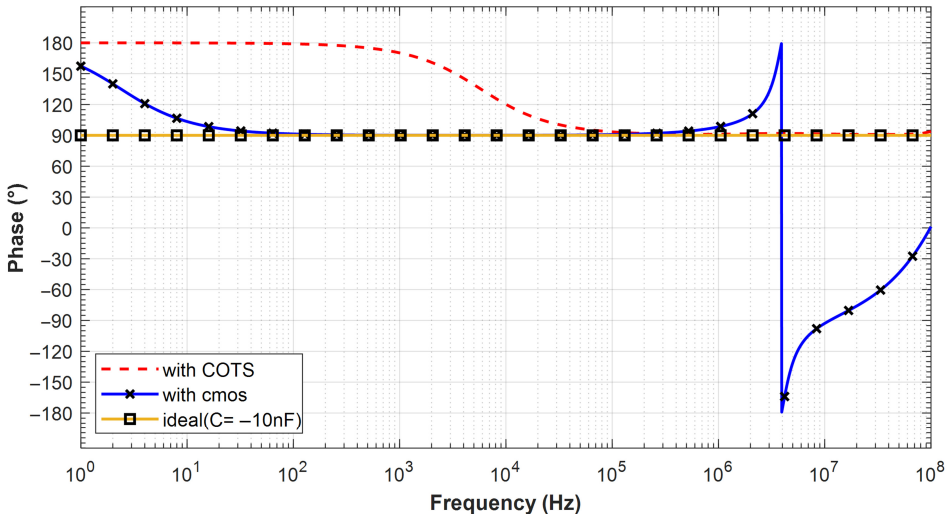


Figure 36. Phase response of the proposed circuit for negative capacitance multiplication.

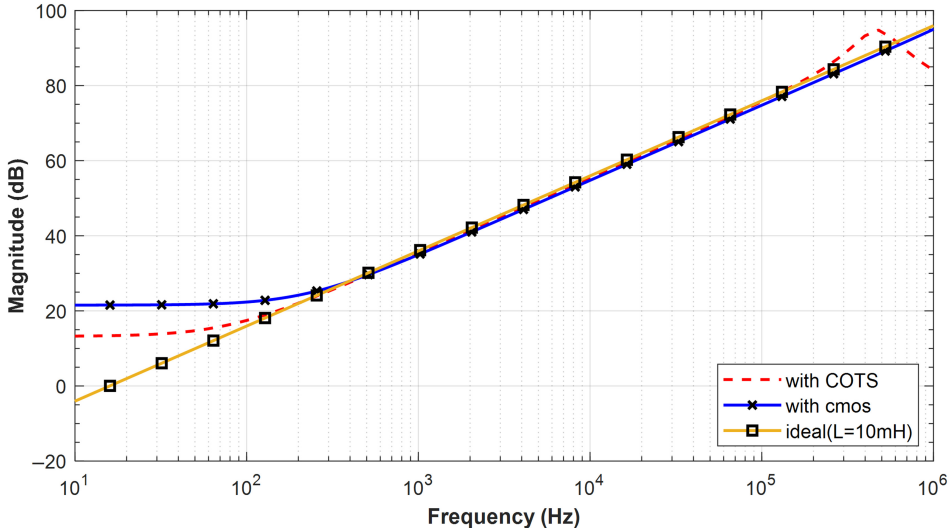


Figure 37. Magnitude response of the proposed circuit for positive inductance multiplication.

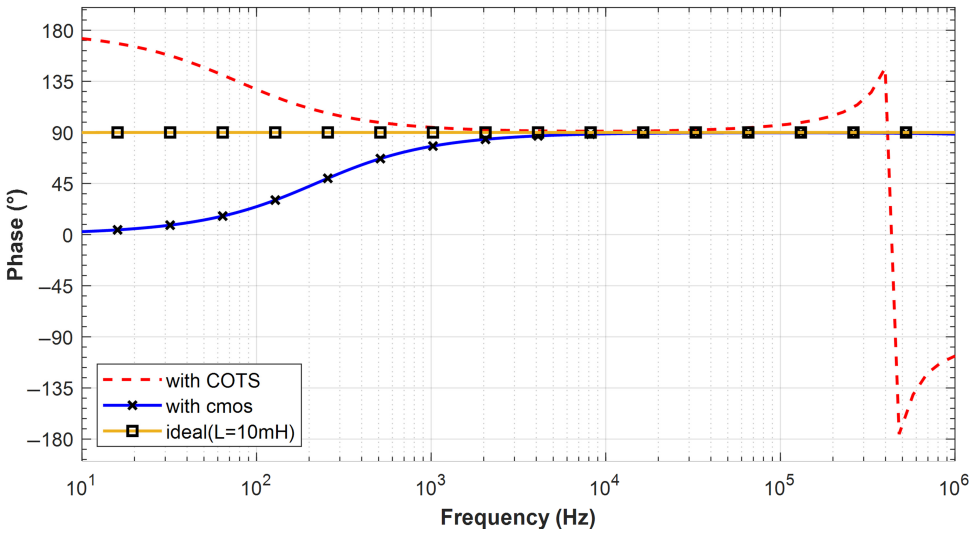


Figure 38. Phase response of the proposed circuit for positive inductance multiplication.

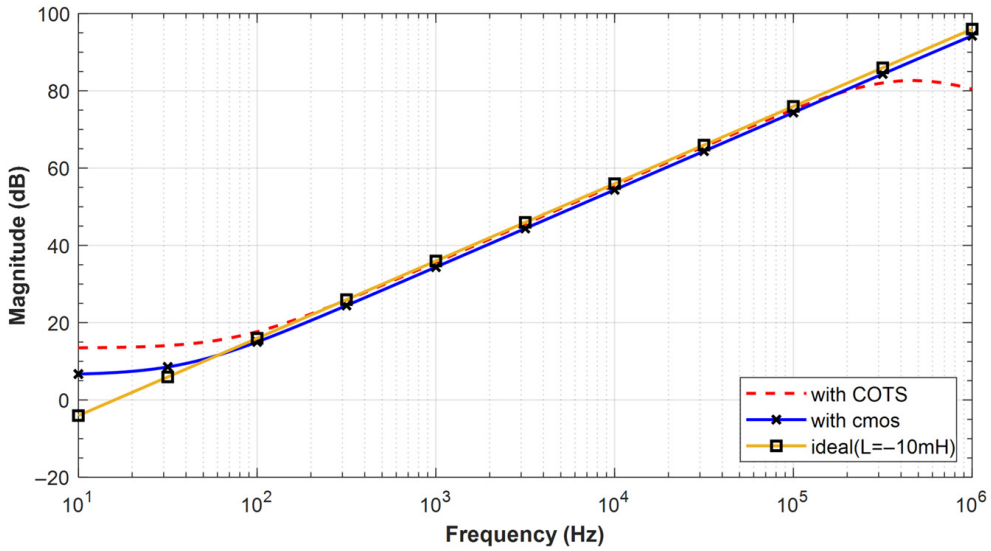


Figure 39. Magnitude response of the proposed circuit for negative inductance multiplication.

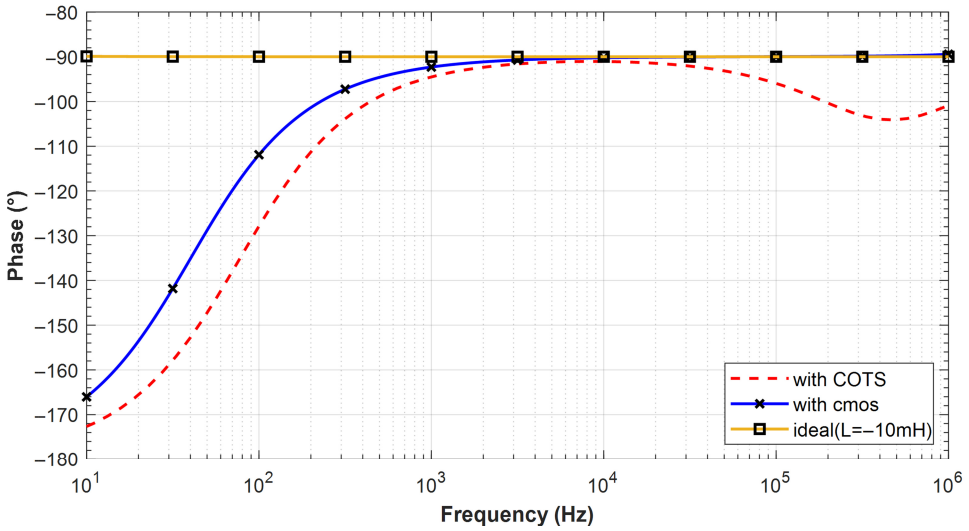


Figure 40. Phase response of the proposed circuit for negative inductance multiplication.

7. Discussion

Table 10 presents a comparison between the proposed capacitance multiplier and those available in the literature. In this study, we employed the TSMC 180 nm PDK. To implement the on-chip capacitors, the high-density 2.0 fF/μm^2 dual Metal-Insulator-Metal (MIM) capacitor offered by the TSMC process was preferred. This selection minimized the overall layout footprint of the proposed circuit without compromising the capacitive requirements.

Accordingly, a passive capacitance of 1 nF occupies an area of approximately 0.5 mm^2, while a 10 nF capacitance requires a massive area of approximately 5 mm^2. Instead of utilizing a conventional 10 nF passive capacitor, the proposed design achieves the same equivalent capacitance by combining a 1 nF base capacitor (0.5 mm^2) with the active impedance multiplier circuit (5831 μm^2). Consequently, the total occupied area is reduced to only 0.5058 mm^2. This quantitative evaluation demonstrates that the proposed structure provides an area saving of approximately 89.9% compared to its purely passive counterpart. At this point, it is crucial to emphasize that the area-related advantage of the proposed circuit is twofold: it provides a compact active core implementation (5831 μm^2) that competes favorably with existing literature, while simultaneously delivering effective area savings for passive components at the system level. The layout design of the proposed

impedance multiplier circuit, generated using the Electric VLSI software (version 9.07), is presented in Figure 41.

Table 10. Comparison of resistance multiplier circuits in terms of their performance.

Ref.	Supply Voltage	Power Consumption	Operating Frequency	Multiplication Factor	Supported Impedance Types	IC Area *	Technology	*FoM*
[6]	∓ 5 V	NA	2 Hz − 7 MHz	400	R, L, C	NA	With COTS	NA
[9]	∓0.9 V	17.6 µW	10 kHz − 10 MHz	NA	R, L, C	NA	0.18 µm	NA
[12]	NA	NA	NA	360	R, L, C	NA	With COTS	NA
[25]	∓1.25 V	3.3 mW	100 kHz − 10 MHz	100	R, L, C	NA	0.18 µm	27.27×10^{11}
[35]	∓0.9 V	NA	100 Hz − 10 MHz	NA	R, L, C	NA	0.18 µm	NA
This Work	**∓1.8 V**	**1.6 mW**	**118 MHz**	**−100/+100**	**R, L, C**	**5831 µm^2**	**0.18 µm**	**44.25×10^{12}**

* Base impedance layout area is not included. COTS: Commercial Off-The-Shelf. NA: Not Available.

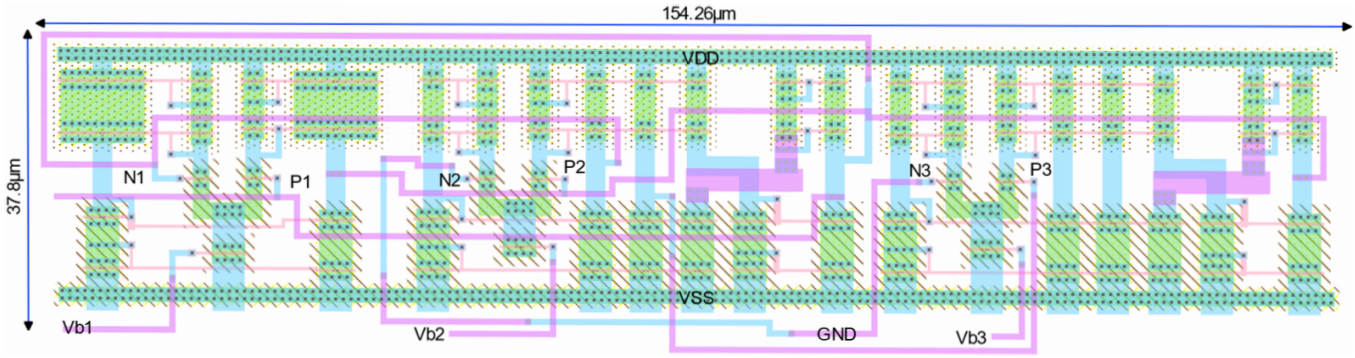


Figure 41. Layout of the proposed impedance multiplier circuit.

The following equation presents the *FoM* parameter calculation for the circuit we proposed, as compared to other studies in the literature. Here, K_{max} represents the maximum multiplication factor, f_{max} denotes the maximum operating frequency, K_T indicates the total number of signal types that can be multiplied, Z_T refers to the total number of impedance types that can be multiplied and P is the power consumption.

$$FoM = \frac{K_{max} \times F_{max} \times K_T \times Z_T}{P} \quad (51)$$

Tables 10–12 present a technical comparison of prior works on resistance, capacitance, and inductance multipliers, respectively, alongside the FoM results calculated using Equation (51). Since the physical layout area is not factored into the FoM in Equation (51) and recognizing that several prior works lack complete implementation metrics, this FoM comparison serves as supportive evidence of the proposed circuit's versatility and compactness, rather than definitive proof of absolute superiority. To ensure a fair and precise evaluation, the performance metrics reported in each table, including operating frequency and multiplication factor, are isolated strictly for the specific impedance mode being analyzed. While the 'Supported Impedance Types' column highlights the full functional versatility of each referenced circuit by indicating whether a design serves as a generalized R/C/L multiplier, the numerical data presented in a given table exclusively reflects its performance for that table's specific impedance category.

Table 11. Comparison of capacitance multiplier circuits in terms of their performance.

Ref.	Supply Voltage	Power Consumption	Operating Frequency	Multiplication Factor	Supported Impedance Types	IC Area *	Technology	*FoM*
[3]	∓0.9 V	0.6 mW	10 kHz − 10 MHz	30/150	C	14,000 μm^2	0.18 μm	2.5×10^{12}
[5]	∓1.25 V	1.26 mW	NA	1000	L, C	NA	0.18 μm	NA
[10]	∓1.65 V	1.5 mW	10 MHz	−50/ + 50	C	NA	0.35 μm	6.66×10^{11}
[15]	∓ 12 V	NA	4 kHz − 1 MHz	2001	C	NA	With COTS	NA
[18]	∓0.75 V	7.4 mW	NA	NA	C	NA	0.25 μm	NA
[20]	∓0.3 V	67 nW	80 Hz − 40 kHz	100	C	NA	0.18 μm	5.97×10^{13}
[21]	∓1.25 V	NA	10 kHz − 3 MHz	30	C	755 μm^2	0.18 μm	NA
[25]	∓1.25 V	3.3 mW	100 kHz − 10 MHz	100	R, L, C	NA	0.18 μm	27.27×10^{11}
[26]	∓0.75 V	NA	10 kHz − 100 MHz	−20/ + 20	C	NA	0.13 μm	NA
[36]	∓0.6 V	1.6 mW	4.5 MHz	500	C	NA	0.13 μm	1.41×10^{12}
[37]	∓ 10 V	NA	6 MHz	51	L, C	NA	With COTS	NA
This Work	**∓1.8 V**	**1.6 mW**	**20 MHz**	**−50/+50**	**R, L, C**	**5831 μm^2**	**0.18 μm**	**3.75×10^{12}**

* Base impedance layout area is not included. COTS: Commercial Off-The-Shelf. NA: Not Available.

Table 12. Comparison of inductance multiplier circuits in terms of their performance.

Ref.	Supply Voltage	Power Consumption	Operating Frequency	Multiplication Factor	Supported Impedance Types	IC Area *	Technology	*FoM*
[5]	∓1.25 V	1.26 mW	NA	1000	L, C	NA	0.18 μm	NA
[6]	∓ 5 V	NA	2 Hz − 7 MHz	400	R, L, C	NA	With COTS	NA
[9]	∓0.9 V	17.6 μW	10 kHz − 10 MHz	NA	L	NA	0.18 μm	NA
[12]	NA	NA	NA	360	L	NA	With COTS	NA
[25]	∓1.25 V	3.3 mW	100 kHz − 10 MHz	100	R, L, C	NA	0.18 μm	27.27×10^{11}
[35]	∓0.9 V	NA	100 Hz − 10 MHz	NA	R, L, C	NA	0.18 μm	NA
[37]	∓ 10 V	NA	6 MHz	51	L, C	NA	With COTS	NA
This Work	**∓1.8 V**	**1.6 mW**	**4 MHz**	**−50/+50**	**R, L, C**	**5831 μm^2**	**0.18 μm**	**75×10^{10}**

* Base impedance layout area is not included. COTS: Commercial Off-The-Shelf. NA: Not Available.

8. Conclusions

This study presented the design, analysis, and applicability of a generalized impedance multiplier capable of performing resistance, capacitance, and inductance multiplication with electronic controllability and lossless operation. Non-ideal effects of the OTAs were analyzed to assess practical performance. Simulation results indicate that the maximum operating frequency is primarily limited by the OTA bandwidth, with higher OTA gains reducing the frequency due to the constant gain–bandwidth product, while the minimum frequency is influenced by the base impedance and OTA non-idealities. The circuit achieves operating frequencies up to 120 MHz, depending on the type of impedance. The multiplication factor, K, of the designed impedance multiplier circuit is governed by the ratio of the g_m parameters of the utilized OTAs, which provides electronic controllability. For a desired multiplication target, as long as the g_m values are selected to avoid excessively amplifying the intrinsic parasitic effects of the OTAs, the proposed circuit operates stably within its applicable frequency range. The ideally infinite input and output impedances of the OTAs further help in restricting these parasitic contributions. However, it is important to delineate the practical operational range of the circuit. While the circuit supports multiplication factors from −100 to +100, the practically recommended operating ranges differ based on a maximum acceptable magnitude-error threshold of 10%. For positive multiplication, the circuit exhibits stable performance up to K = 100 for resistance, and up to K = 50 for capacitance and inductance. In negative multiplication configurations,

the stable range extends up to K = −100 for resistance and inductance but is restricted to K = −25 for capacitance. Extreme configurations beyond these recommended limits approach or exceed the 10% error threshold and should be carefully evaluated depending on the target application.

Comprehensive evaluations show high linearity, with THD values of 0.043%, 0.096%, and 0.43% for resistive, capacitive, and inductive multiplications, respectively, and low RMS noise levels of 57.03 μV, 971.03 μV, and 54.77 μV. The capacitance multiplication feature was validated via low-pass, band-pass, and high-pass filter simulations with a multiplication factor of K = 10. Band-pass filter implementations under PVT variations and Monte Carlo analyses demonstrated stable and reliable operation. Simulations using the commercial LM13700 OTA confirmed the circuit's practical feasibility, with impedance multiplication behavior matching theoretical expectations across a wide frequency range.

The proposed design operates at ±1.8 V with a power dissipation of 1.6 mW and occupies a compact active core area of 5831 μm^2. By using this compact core to scale down large passive components, the circuit achieves considerable area savings at the system level. The reported 5831 μm^2 corresponds to the active core only, and the total system-level area benefit depends on the selected base impedance and the target application. These results demonstrate that the generalized impedance multiplier offers a versatile and functionally broad topology with a balanced performance profile. It is well-suited for integration into compact and electronically tunable analog ICs where wide-range impedance scaling is prioritized. Future work may explore its application in complex analog systems and adaptive filter architectures.

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Abbreviations

The following abbreviations are used in this manuscript:

AI	Active Inductor
COTS	Commercial Off-The-Shelf
NA	Not Available
OTA	Operational Transconductance Amplifier
PLL	Phase Locked Loops
PVT	Process-Voltage-Temperature
THD	Total Harmonic Distortion

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