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Sub-6 GHz GaAs SPDT Switch Co-Designed with Shunt Inductor for ESD Protection

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Abstract: In this study, a single-pole double-throw (SPDT) switch for Sub-6 GHz application is designed. In particular, a shunt inductor is connected to the antenna port of the switch for ESD (electrostatic discharge) protection in RF (radio frequency) front end module. The shunt inductor not only serves as an ESD protection device, but also serves as a component of a parallel resonance circuit to suppress insertion loss of the switch. In addition, in order to secure the power handling capability, transistors turned off in the transmit (Tx) mode are implemented as quadruple-gate transistors. An SPDT switch is fabricated using GaAs pHEMT provided in the 500 nm GaAs BiFET process to verify the feasibility of the proposed switch structure. The operating frequency is set from 3 GHz to 5 GHz. The insertion loss and isolation measured in the Tx mode are lower than 0.35 dB and higher than 31.6 dB, respectively. The insertion loss and isolation measured in the Rx mode are lower than 0.32 dB and higher than 33.9 dB, respectively. The chip size including test pads is 0.890 × 0.875 mm^2.

Keywords: ESD; GaAs; isolation; resonance; single-pole double-throw (SPDT); switch

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1. Introduction

Recently, with the commercialization of 5G mobile communication, the development of RF integrated circuits (ICs) in n77 and n79 bands is also actively progressing [1–4]. In particular, switches, power amplifiers (PAs), and low-noise amplifiers (LNAs) are key circuits constituting RF front-end module (FEM) [5–7]. Among them, a switch is a circuit that is directly connected to an antenna, and insertion loss, isolation, and power handling capabilities are the main performance indicators [8–12]. If the insertion loss of the switch deteriorates, the output power of the transmitted signal decreases and the noise figure of the received signal increases. Also, if the power handling capability of the switch is low, the output power of the PAs is not fully transmitted to the antenna. Therefore, research to achieve the performance of such a switch is constantly being conducted.

In addition, as shown in Figure 1, the switch is directly connected to the antenna in the FEM. Therefore, the possibility of electrostatic discharge (ESD) through the antenna port of the switch should be considered when manufacturing the communication system using a FEM or operating the system. Therefore, it is necessary to obtain the reliability of the FEM by applying an ESD protection solution to the antenna port of the switch [13]. As shown in Figure 1, when an ESD protection solution is applied to the antenna port of the switch, the output of the PA and the input of the LNA are free from an additional ESD protection. For ESD protection in the switch, design techniques using diodes have

been introduced [14]. However, when using a diode as an ESD protection device, an additional design technique is required to remove the parasitic capacitance of the diode. As an example, in order to suppress the influence of the parasitic capacitance of the diode, a method of utilizing an additional LC tank has been proposed [15,16]. Shunt inductors can also be used as another ESD protection device in switches [13]. However, there is a problem that the use of shunt inductors for ESD protection deteriorates the performance of the switch. As such, the application of ESD protection techniques to RFICs is generally accompanied by deterioration in the performance of RFICs. As a result, there are often instances of the absence of ESD protection devices and circuits in the RFIC. Furthermore, even if the ESD protection technique is applied to the RFIC, it is common to apply the ESD protection technique after the design of the core circuit of the RFIC is completed. In other words, ESD protection techniques are generally designed somewhat independently of core circuits, and as a result, ESD protection devices and circuits are a major cause of deterioration of the performance of the RFIC.

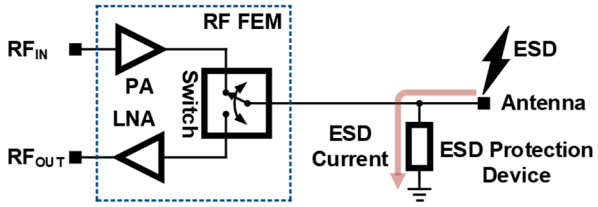


Figure 1. Conceptual block diagram of FEM with ESD protection solution.

In this study, we propose a co-design technique for switches and shunt inductors. Through the proposed co-design technique, shunt inductors are utilized for resonance in transmit (Tx) and receive (Rx) modes to suppress insertion loss as well as ESD protection. Because the shunt inductor of this study is co-designed with the matching network of the switch, performance degradation due to the shunt inductor can be successfully suppressed. In addition, in this study, unlike the typical LC tank technique, the capacitor for the LC tank is designed with parasitic capacitance generated by the switch itself, not an additional capacitor. Additionally, quadruple-gate transistors are asymmetrically used to secure power handling capabilities in the Tx mode.

In Section 2, the operation of the proposed single-pole double-throw (SPDT) switch using a shunt inductor for ESD protection is explained. In Section 3, simulation and measurement results are provided.

2. Proposed SPDT Switch with ESD Protection

First, a proposed ESD protection technique using a shunt inductor will be described. Then, the operation and design of the proposed switch with the shunt inductor will be provided.

2.1. ESD Protection Technique Using Shunt Inductor

In the proposed switch, a shunt inductor is connected to the antenna port. The shunt inductor serves as an ESD protection device. In general, considering the frequency components of the human-body-model (HBM) and the machine-model (MM) of ESD, the impedance of the RF inductor from the perspective of ESD is negligible. In order to conceptually examine the effectiveness of the proposed ESD protection technique through ESD model, the internationally standardized HBM of Figure 2 is considered.

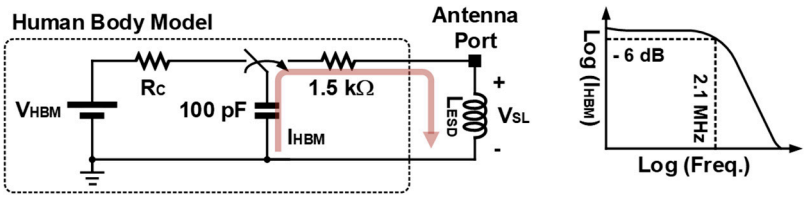


Figure 2. Human body model of ESD with shunt inductor: (**a**) schematic and (**b**) frequency response.

The HBM in Figure 2a consists of a charging resistor R_C, a 100 pF capacitor, and a 1.5 kΩ resistor. When the switch in Figure 2a is connected to RC, the 100 pF capacitor is charged with a charge equivalent to V_{HBM}. Then, if the switch is connected to the 1.5 kΩ resistor, the charge charged in the 100 pF capacitor is discharged through 1.5 kΩ resistor. Figure 2b shows the frequency response of the HBM ESD. The 6 dB bandwidth of the HBM ESD is from dc to 2.1 MHz, and 2.1 MHz is negligibly low compared to the operating frequency of a general RFIC.

In order to conceptually confirm the effectiveness of the proposed switch structure applying the ESD protection by connecting a shunt inductor between the antenna port and the ground, the shunt inductor, L_{ESD}, is connected to the output node of the ESD HMB as shown in Figure 2a. L_{ESD} operates as an inductive impedance for RF signals, but has a negligible impedance for an HBM ESD of 2.1 MHz, allowing ESD current to be easily shunted to the ground. For example, as shown in Figure 2, when I_{HBM}, the HBM ESD current, flows through the L_{ESD}, the shunt inductor, the voltage drop at the L_{ESD}, V_{SL}, is examined. Here, the frequency of the HBM ESD is set to 2.1 MHz and the L_{ESD} is set to 5 nH. Under such conditions, V_{SLpeak}, which is the peak V_{SL}, could be calculated as follows.

$$\left|V_{SL,peak}\right| = \frac{\omega L_{ESD}}{1.5k + \omega L_{ESD}} V_{HBM} = 4.4 \times 10^{-5} V_{HBM} \quad (1)$$

From the results, the $V_{SL,peak}$ reaches only 4.4 V when the V_{HBM} is 100 kV. Considering that a typical IC has a HBM ESD protection level of 2 kV or 8 kV, it has a sufficiently high ESD protection level when using a shunt inductor as an ESD protection device. This conclusion was successfully verified from previous studies through the measurement results of LNAs and PAs using shunt inductors or transformers as ESD protection devices [17,18]. In this study, the effectiveness of the proposed ESD protection technique is explained using HBM ESD, but previous studies have proven that shunt inductors have an ESD protection effect against MM ESD and as well as HBM ESD [17,18]. In this study, the width of the metal line constituting the L_{ESD} is 6 μm.

In summary, typical shunt inductor used in RFICs have negligible impedance in the frequency region of ESD HBM, which act as effective ESD protection devices. On the other hand, the shunt inductor in the general operation aspect of the RFIC provides useful impedance and could be used as a matching component for improving the performance of the RFIC. Therefore, in the proposed switch structure with ESD protection technique using L_{ESD}, the freedom to select L_{ESD} optimized for switch performance is easily secured even considering ESD survival level of the switch.

2.2. Operation of the Proposed SPDT Switch

Figure 3 shows the schematic of the proposed switch with ESD protection using L_{ESD}. For the Tx mode, V_C, which is a control voltage, is low, M_{TS} and M_{RX} are turned off, and M_{TX} and M_{RS} are turned on. Because M_{TX} serves to deliver Tx signals to the antenna port, M_{TX} is designed as a single-gate transistor to minimize power loss. In addition, M_{RS} is

designed as a single-gate transistor to remove the leakage current flowing into the Rx port in the Tx mode. M_{TS} and M_{RX}, which are transistors turned off in the Tx mode, are designed as quadruple-gate transistors in order to secure power handling capabilities in the Tx mode. In the Rx mode, M_{RX} and M_{TS} are turned on as opposed to the Tx mode. However, because M_{RX} and M_{TS} are designed as quadruple-gate transistors, the gate width is sufficiently secured to suppress power loss and improve isolation by reducing on-resistance. Here, because the quadruple-gate transistor has the effect of stacking four transistors, the ability to withstand power is improved, thereby improving the power handling capability of the switch. However, the structure in which four transistors are stacked could deteriorate the performance of the switch due to parasitic components caused by metal lines used to connect each transistor. On the other hand, quadruple-gate transistors have the almost same effect as the structure in which four transistors are stacked in terms of power handling capability. However, quadruple-gate transistors have the advantage of reducing parasitic components caused by metal lines compared to the structure in which four transistors are stacked.

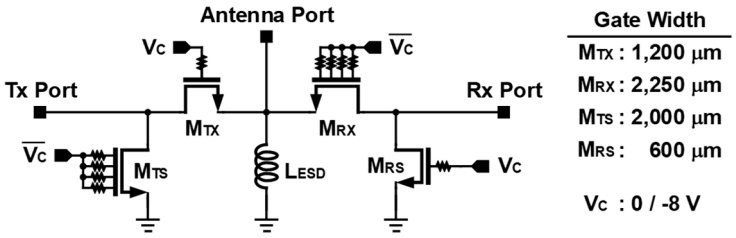


Figure 3. Proposed SPDT switch with ESD protection using a shunt inductor.

Figure 4 shows equivalent circuits in Tx and Rx modes. When each transistor is turned on and off, the transistors can be equivalent to on-resistances and off-capacitances, respectively.

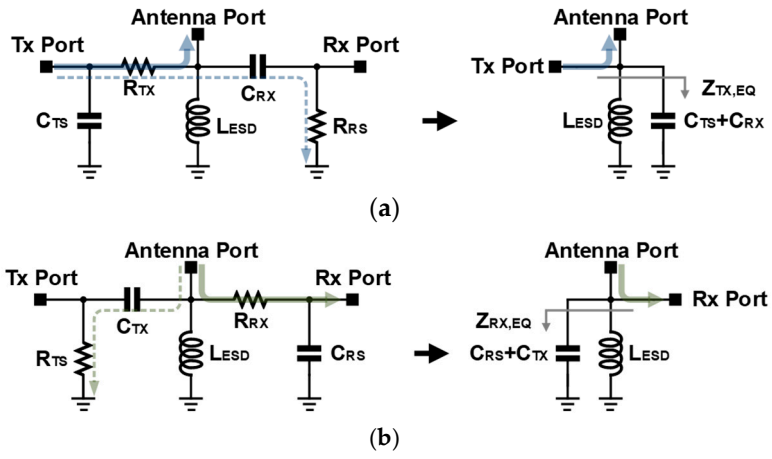


Figure 4. Equivalent circuits for (**a**) Tx mode and (**b**) Rx mode.

In the Tx mode, assuming that the on-resistance R_{TX} and R_{RS} are small enough, L_{ESD} and C_{TS} + C_{RX} become a parallel resonance circuit. If the resonance frequency of the resonance circuit matches the frequency of the Tx signal, the Tx signal is successfully transmitted to the antenna port. In addition to the resonance of L_{ESD} and C_{TS} + C_{RX}, if the R_{TX} is sufficiently small, insertion loss in the Tx mode could be suppressed. The R_{RS} serves to shunt the Tx signal flowing to the Rx port to the ground; therefore, if the R_{RS} is sufficiently small, isolation in the Tx mode could be secured.

Similarly to the Tx mode, in the Rx mode as well, the parallel resonance circuit forms a high impedance in the Rx signal frequency so that the Rx signal is successfully received at the Rx port. In addition to the resonance of L_{ESD} and C_{RS} + C_{TX}, if the R_{RX} is sufficiently small, insertion loss in the Rx mode could be suppressed. The R_{TS} serves to shunt the Rx signal flowing to the Tx port to the ground; therefore, if the R_{TS} is sufficiently small, isolation in the Rx mode could be secured.

Therefore, sufficiently lowering the on-resistance of the transistor and resonance play an important role in improving the performance of the switch. $Z_{TX,EQ}$ and $Z_{RX,EQ}$ in Figure 4 for considering the resonance characteristics can be expressed as follows.

$$Z_{TX,EQ} = \frac{j\omega L_{ESD}}{1 - \omega^2 L_{ESD} C_{EQ,TX}}, \quad Z_{RX,EQ} = \frac{j\omega L_{ESD}}{1 - \omega^2 L_{ESD} C_{EQ,RX}} \tag{2}$$

Here, $C_{EQ,TX}$ and $C_{EQ,RX}$ are C_{TS} + C_{RX} and C_{RS} + C_{TX}, respectively. In addition, in summary, it is ideal to match the resonant frequencies of each $Z_{TX,EQ}$ and $Z_{RX,EQ}$, f_{TX} and f_{RX}, with the operating frequencies of the signal.

$$f_{TX} = \frac{1}{2\pi\sqrt{L_{ESD} C_{EQ,TX}}}, \quad f_{RX} = \frac{1}{2\pi\sqrt{L_{ESD} C_{EQ,RX}}} \tag{3}$$

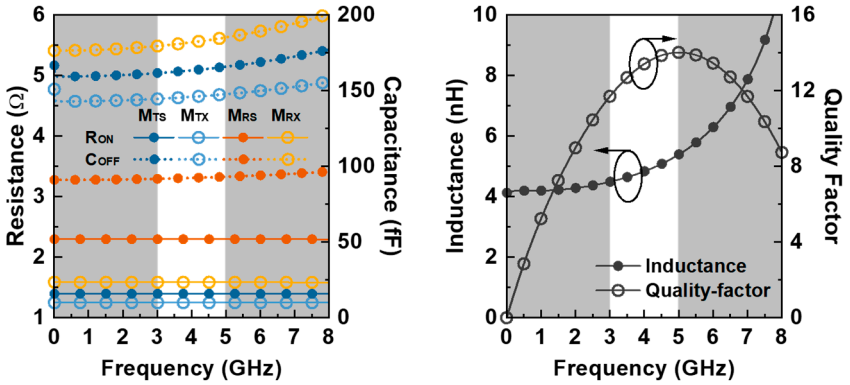
As a result, the L_{ESD} for ESD protection determines the operating frequency in each mode by resonance with $C_{EQ,TX}$ and $C_{EQ,RX}$ according to Tx and Rx modes, respectively. Considering the ideal operation of the SPDT switch, $C_{EQ,TX}$ and $C_{EQ,RX}$ should be the same in order for f_{TX} and f_{RX} to be the same. Therefore, $C_{EQ,TX}$ and $C_{EQ,RX}$ should be considered in determining the size of transistors.

In addition, when determining the size of the transistor, the on-resistance of the transistor should also be considered. In particular, R_{TX} and R_{RX} in Figure 4 directly affect insertion losses in Tx and Rx modes, respectively. In order to suppress insertion loss, the gate widths of M_{TX} and M_{RX} should be increased, but the increased gate width of the transistor increases C_{TX} and C_{RX}. The increased C_{TX} and C_{RX} increase $C_{EQ,RX}$ and $C_{EQ,TX}$, respectively, causing the switch to shift the operating frequency. The shift in the operating frequency could be corrected by reducing the inductance of the L_{ESD}. However, a decrease in L_{ESD} could cause a decrease in the frequency bandwidth of the switch. In conclusion, the size of the transistor should be carefully set by comprehensively considering operating frequency, bandwidth, insertion loss and isolation.

2.3. Design of the Proposed SPDT Switch

In order to verify the feasibility of the proposed switch to which the ESD protection technique is applied, a switch is fabricated using a 500 nm GaAs BiFET process. The 500 nm GaAs BiFET process provides HBT and pHEMT, and only pHEMT with a gate length of 500 nm is used for switch design. The operating frequency of the designed switch is set from 3 GHz to 5 GHz for application in the n77 and n79 bands.

The designed switch consists of a shunt inductor and four transistors as shown in Figure 3. Figure 5 shows the simulation results according to the frequency of the finally used transistors and L_{ESD}. Parasitic capacitances are extracted as capacitances between the drain and the source of the transistor when the transistor is in the off state. The L_{ESD} serves as an ESD protection device while also serving as an inductance of the parallel resonance circuit to prevent power loss. V_C is designed to be 0 V and −8 V. The V_C is applied to the gate through a resistor of 96 kΩ.



(**a**) (**b**)

Figure 5. Characteristics of the used devices: (**a**) transistors and (**b**) L_{ESD}.

In an ideal case, L_{ESD} is commonly used in Tx and Rx mode operations, so C_{TS} + C_{RX} and C_{RS} + C_{TX} in (3) should be the same, resulting in f_{TX} and f_{RX} being the same. However, C_{TS} + C_{RX} and C_{RS} + C_{TX} can be formed somewhat differently because not only off-capacitance but also on-resistance should be considered when determining the transistor. In particular, the on-resistance of M_{RS} and M_{TS} directly affects isolation in Tx and Rx modes, respectively. In this study, for convenience, IL_{TX} and IL_{RX}, which are insertion losses in each mode, are defined as follows.

$$IL_{TX} = 10\log\left|\frac{P_{TX}}{P_{ANT}}\right| dB, \quad IL_{RX} = 10\log\left|\frac{P_{ANT}}{P_{RX}}\right| dB \tag{4}$$

In IL_{TX}, P_{TX} is the power supplied from the Tx port, and P_{ANT} is the power delivered by the antenna port. Similarly, in IL_{RX}, P_{ANT} is the power supplied from the antenna port, and P_{RX} is the power delivered by the Rx port. Here, the P_{ANT}/P_{TX} and P_{RX}/P_{ANT} for the calculation of (4) may be calculated as follows.

$$\begin{aligned} for\ Tx\ mode: \frac{P_{TX}}{P_{ANT}} &= 1 + jR_L\left(\omega C_{EQ,TX} - \frac{1}{\omega L_{ESD}}\right) \\ for\ Rx\ mode: \frac{P_{ANT}}{P_{RX}} &= 1 + jR_L\left(\omega C_{EQ,RX} - \frac{1}{\omega L_{ESD}}\right) \end{aligned} \tag{5}$$

Here, R_L is the terminal impedance at each port, and in this study, R_L is assumed to be 50 Ω. In this study, the sizes of the transistors are determined to minimized the on-resistances of the transistors under the condition that both IL_{TX} and IL_{RX} are lower than 0.5 dB. For convenience of comparison, the simulation results of the designed switch are shown together with the measurement results in the next section.

3. Design Results

Figure 6 is a chip photograph of the fabricated switch. The overall chip size including test pads is 0.890 × 0.875 mm^2. The control voltage is applied through a bonding wire, and the RF signal is measured using a GSG probe.

Because the interconnection lines and inductor, including the GSG pads, are all optimized through electromagnetic (EM) simulation, deterioration of simulation accuracy due to parasitic components of passive devices and metal lines is suppressed. As a result, in this study, the simulation results show high similarity to the measurement results. For convenience of comparison between the simulation and the measurement results, the simulation and the measurement results are provided together. Measurement is performed on three samples. The variation between samples is negligible. In addition, the power loss caused by GSG pads is included in the performance of the switch without de-embedding. On

the other hand, power loss due to RF cables and connectors for measurement is carefully de-embedded.

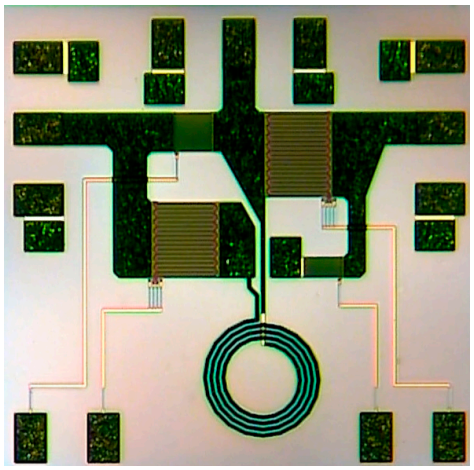
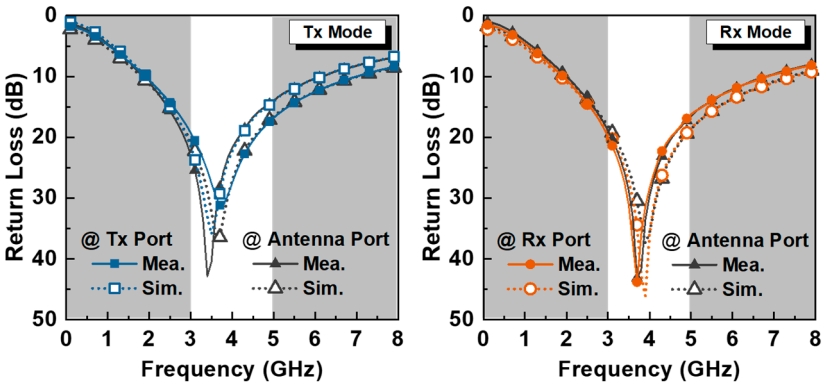


Figure 6. Chip photograph of the designed GaAs SPDT switch.

Figure 7 shows the return losses. At 3 GHz to 5 GHz, the measured return losses are greater than 14.0 dB and 16.2 dB in the Tx and Rx modes, respectively.



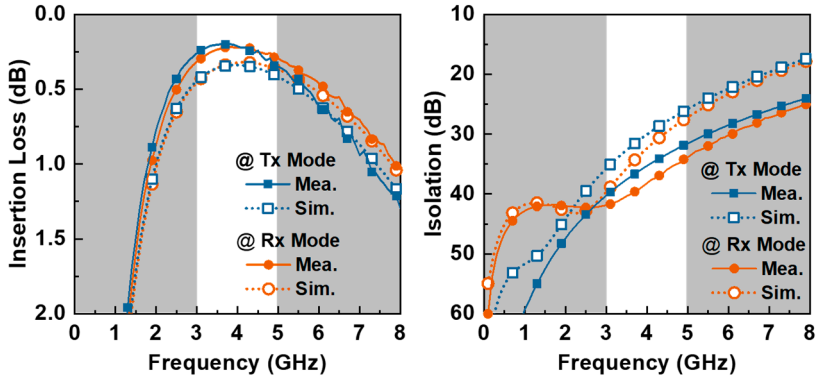
(**a**) (**b**)

Figure 7. Design results of return loss: (**a**) Tx mode and (**b**) Rx mode.

As shown in Figure 8, the measured insertion losses are less than 0.35 dB and 0.32 dB in the Tx and Rx modes, respectively. In particular, because both Tx and Rx modes can be equalized with parallel resonance circuits including L_{ESD}, the Tx and Rx modes showed similar measurement results. Isolations are measured higher than 31.6 dB and 33.9 dB in the Tx and Rx modes, respectively.

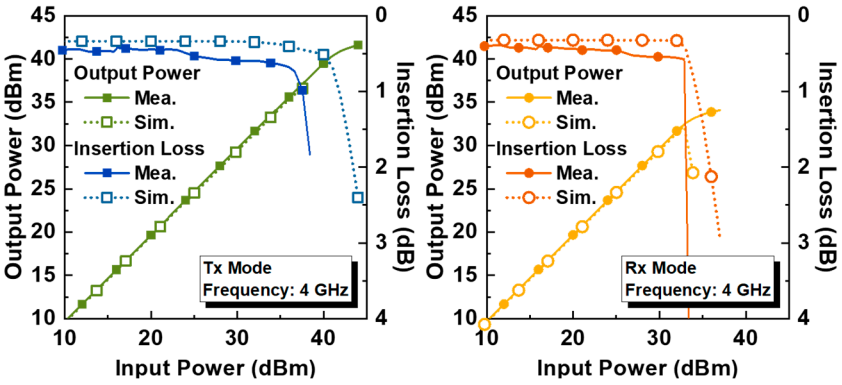
As shown in Figure 9, the output power according to the input power is measured at the center frequency of 4 GHz. The linearity of the Tx mode is measured relatively higher than that of the Rx mode. The measured input 1 dB compression points (IP_{1dB}s) at 4 GHz are 38.0 dBm and 33.0 dBm in Tx and Rx modes, respectively.

Table 1 shows the performance comparison of GaAs switches with an operating frequency of Sub-6 GHz. In Table 1, in the case of commercial products, because the performance is in the package state, the power loss by the package is included in the insertion loss. The performances of the proposed switch in the range of 3 GHz to 6 GHz as well as 3 GHz to 5 GHz, which is the target frequency, are also provided in Table 1. It can be seen that the switch in this study shows reasonable performance even though a shunt inductor for ESD protection is used.



(**a**) (**b**)

Figure 8. Design results of (**a**) insertion loss and (**b**) isolation.



(**a**) (**b**)

Figure 9. Design results of power handling capability: (**a**) Tx mode and (**b**) Rx mode.

Table 1. Performance summary and comparison of GaAs SPDT switches operating at sub-6GHz.

Reference	Tech.	Freq. (GHz)	Fractional Bandwidth (%)	Return Loss (dB)		Insertion Loss (dB)		Isolation (dB)		IP_{1dB} (dBm)		Chip Size (mm^2)
				Tx	Rx	Tx	Rx	Tx	Rx	Tx	Rx	
CEL'17 [19]	GaAs	2–6	100	>18		<0.4		>26		32 @ 6 GHz		-
Qorvo'18 [20]	GaAs	0.1–6	193	>15		<0.85		>17		35 @ 3 GHz		-
Skyworks'18 [21]	GaAs	0.1–6	193	>20		<0.6		>24		34 @ 2.45 GHz		-
WAMICON'23 [22]	500 nm GaAs	3–5	50	>15		<0.3		>32.7		>34.2 @ 3 GHz		0.83
MWTL'24 [23]	500 nm GaAs	3.3–5	41	>15.8		<0.53	<0.39	>36.4	>25.4	>40 (1)	-	0.84
This work	500 nm GaAs	3–5	50	>14.0	>16.2	<0.35	<0.32	>31.6	>33.9	38.0 (1)	33.0 (1)	0.78
		3–6	66.7	>10.3	>12.2	<0.62	<0.46	>28.5	>30.2			

(1) @ 4 GHz.

In this study, the proposed ESD protection technique was applied to the GaAs pHEMT switch for Sub-6 GHz applications. However, the proposed ESD protection technique using a shunt inductor can be easily applied to switches connected external antennas regardless of operating frequency and power handling capability. In particular, the proposed switch structure may also benefit emerging applications such as microwave sensing and non-contact detection [24,25].

4. Conclusions

In this study, we proposed an ESD protection technique of a switch constituting the RF FEM. For this, a shunt inductor was provided in the antenna port of the switch. In order to suppress the performance degradation caused by the shunt inductor, the inductor was co-designed with the matching network of the switch. Therefore, the shunt inductor serves as an ESD protection device while also serving as a component of a parallel resonance circuit to minimize the insertion loss of the switch. In addition, in order to secure power handling capabilities, transistors turned off in the Tx mode were designed as quadruple-gate transistors. The proposed switch was fabricated with GaAs pHEMT provided in the 500 nm GaAs BiFET process. For frequencies from 3 GHz to 5 GHz, the measured insertion losses were lower than 0.35 dB and 0.32 dB in the Tx and Rx modes, respectively. The measured isolations were higher than 31.6 dB and 33.9 dB in the Tx and Rx modes, respectively. The IP_{1dB} of the Tx mode was measured as 38.0 dBm at the operating frequency of 4 GHz.

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