

Review

Analysis of Edge Termination Techniques for Gallium Nitride Pseudo-Vertical p-n Diodes: Modeling Based on Technology Computer-Aided Design and Review of Current Developments

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Abstract: Edge termination techniques play a crucial role in enhancing the breakdown voltage (BV) and managing electric field distribution in GaN-based power devices. This review explores six key termination methods—field plate (FP), mesa, bevel, trench, ion implantation, and guard ring (GR)—with a focus on their performance, fabrication complexity, and insights derived from TCAD simulations. FP and trench terminations excel in high-voltage applications due to their superior electric field control but are accompanied by significant fabrication challenges. Mesa and bevel terminations, while simpler and cost-effective, are more suited for medium-voltage applications. Ion implantation and GR techniques strike a balance, offering customizable parameters for improved BV performance. TCAD simulations provide a robust framework for analyzing these techniques, highlighting optimal configurations and performance trade-offs. The choice of edge termination depends on the specific application, balancing BV requirements with manufacturing feasibility. This review offers a comprehensive comparison, emphasizing the critical role of simulations in guiding the selection and design of edge termination techniques for GaN power devices.

Keywords: gallium nitride; pseudo-vertical PN junction diode; breakdown voltage; electrical field crowding; edge termination technique



Academic Editors: Costas Psychalinos, Zhengran He, Victor Erokhin and Byung-Gyu Kim

Received: 27 February 2025

Revised: 14 March 2025

Accepted: 15 March 2025

Published: 18 March 2025

Citation: El Amrani, M.; Buckley, J.; Alquier, D.; Godignon, P.; Charles, M. Analysis of Edge Termination Techniques for Gallium Nitride Pseudo-Vertical p-n Diodes: Modeling Based on Technology Computer-Aided Design and Review of Current Developments. *Electronics* **2025**, *14*, 1188. <https://doi.org/10.3390/electronics14061188>

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1. Introduction

Gallium nitride (GaN) is a wide-bandgap semiconductor material known for its excellent material properties, including high electron mobility, high electron saturation velocity, high thermal conductivity, and a high critical electric field. These properties are becoming increasingly important in various applications [1,2]. As a result, GaN-based devices offer advantages such as a higher breakdown voltage, lower on-resistance, and reduced power losses. Vertical GaN power devices are particularly advantageous, as they provide low energy consumption, a high power density, a high operating frequency, and a high conversion efficiency, making them ideal for power electronic systems compared to silicon (Si) [3–5]. Higher breakdown voltages can be achieved by increasing the thickness of the drift layer without enlarging the overall device size. This approach also enables higher current handling, a smaller chip area, and better heat dissipation, which are beneficial for electronics and power systems [6–9]. Among these devices, GaN-based vertical P-i-N diodes, which feature high breakdown voltages, low on-resistance, and lower reverse

leakage currents, have been extensively studied, with significant progress reported [10–14]. However, destructive breakdown and premature avalanche breakdown can occur due to electric field crowding at various edges, including the P-N junction, depletion region, and electrode.

Recently, power devices with enhanced avalanche breakdown capabilities have been developed, allowing for higher breakdown voltages. Protection periphery techniques are commonly applied to reduce the electric field concentration at the device edges by controlling the depletion region of the junction. Several techniques, including field plates [15], ion implantation [16,17], plasma treatment [18], and mesa etching [19–23], have been implemented to mitigate the electric field at the edges of GaN P-i-N diodes, leading to higher breakdown voltages. These edge terminal techniques are effective in improving device performance without negatively influencing the on-state behavior, and they can be used in combination to optimize the device architecture. The purpose of this review is to investigate and compare the effects of different edge termination techniques on the breakdown voltage of GaN-based devices, with a strong emphasis on pseudo-vertical p-n diodes (PND) as test structures for fully vertical devices. Pseudo-vertical structures serve as an essential intermediate step in the development of true vertical GaN power devices, offering valuable insights into their electrical performance and optimization. By leveraging TCAD (Technology Computer-Aided Design) modeling, this study aims to refine edge termination strategies, ultimately contributing to the advancement of high-voltage GaN technologies. Edge terminations are essential for managing the electric field distribution at the device edges, as improper handling can lead to premature breakdown. Using TCAD simulations allows for precise modeling of electric field behavior and breakdown voltage under various edge termination conditions. By analyzing these simulations, this review aims to highlight the role of edge terminations in optimizing the breakdown voltage, providing insights into how different approaches can improve the performance and reliability of GaN power devices.

2. Edge Termination Techniques

To explore the effectiveness of these edge termination techniques in enhancing BV, Technology Computer-Aided Design (TCAD) Sentaurus Synopsys simulations were performed to analyze various mitigation methods, including field plates (FPs), ion implantation, mesa etching, bevel at different angles, guard rings (GRs), and adding of the trench termination. This section details the features and effectiveness of these approaches as demonstrated in recent advancements. Table 1 provides a comparative overview of the most commonly used methods, highlighting their operating principles, advantages, and limitations.

2.1. Prototype Device Structure and Parameters

Several GaN-based quasi-vertical p-n diode structures have been designed and calibrated without considering the presence of defects in the bulk GaN layers. As illustrated in the cross-sectional schematic in Figure 1a,b, the analyzed structure consists, from top to bottom, of a P-GaN layer with a thickness of 500 nm and a doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$, an N⁻-GaN drift layer with a thickness of 10 μm and a doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$, an N⁺-GaN layer with a thickness of 1 μm and a doping concentration of $5 \times 10^{18} \text{ cm}^{-3}$, a 1.5 μm buffer layer (AlGaIn/AlN), and a 50 μm silicon substrate. It is important to note that the breakdown mechanism remains largely the same between vertical and quasi-vertical structures in a non-punch-through (NPT) configuration as shown in Figure 1c [24–26]. The underlying physical processes, such as electric field distribution and avalanche multiplication, do not change significantly in either configuration as clearly

depicted in Figure 1d. The primary difference lies in the device geometry, which influences the on-state characteristics due to the current crowding effect in a pseudo-vertical structure [24]. Therefore, the choice of a quasi-vertical structure was made to optimize the electrical performances of this architecture while maintaining the same breakdown characteristics as a vertical configuration.

Table 1. Comparison of edge termination methods: operating modes, advantages, and disadvantages.

Edge Termination Technique	Operating Mode	Pros	Cons
Field Plate (FP)	Extends the electric field laterally, reducing peak field strength at the junction edge.	Enhances breakdown voltage, reduces surface charging effects, and improves reliability and performance.	Increased device capacitance, added parasitics, more complex design and fabrication.
Mesa	Physically etches a mesa structure to define the device's active area and control field distribution.	Simple and straightforward fabrication, effective for planar device designs.	Surface damage during etching, increased surface leakage current, lower long-term reliability.
Bevel	Creates an angled edge to spread electric field lines and reduce field crowding.	Reduces electric field intensity, improves breakdown voltage, and reduces risk of premature breakdown.	Requires precise angle control during etching, complex and delicate manufacturing process.
Trench	Etches deep trenches around the active region to modify field distribution and minimize field crowding.	High breakdown voltage, effective electrical isolation, minimizes surface leakage.	High etching complexity, potential for etch-induced lattice damage, added processing steps.
Ion Implantation	Introduces dopant or isolation ions to modify electrical properties and reduce surface traps.	Improves stability, reduces leakage currents, and enhances breakdown voltage and reliability.	Requires precise dose and energy control, potential for crystal lattice damage, complex post-implant annealing.
Guard Rings	Uses multiple concentric rings to distribute and control electric field lines at the device periphery.	Simple design, effectively reduces peak electric field intensity, and minimizes leakage.	Increases device footprint, requires additional lithography steps, more complex alignment needed.

In non-punch-through (NPT) structures, the narrow space charge extension within the highly doped p-GaN layer ensures that the breakdown voltage remains largely independent of the layer's thickness [27–31]. This characteristic allows for the implementation of a thinner p-GaN region in practical devices, thereby enhancing efficiency and minimizing material consumption. Accordingly, the simulation structure incorporates a thin p-GaN layer (0.5 μm) to reflect real-world device design considerations.

For reliable simulation outcomes, several physical phenomena must be carefully considered. Key physical models and parameters, including impact ionization coefficients, are summarized in Table 2 and will be applied throughout the simulations in this study [28–30]. For the structure described in this article, we assumed an ideal case with no surface leakage or other non-idealities in the bulk. With a drift doping of $1 \times 10^{16} \text{ cm}^{-3}$, the maximum breakdown voltage was found to be $\sim 1750 \text{ V}$, considering a peak field of 2.6 MV/cm (parallel-plane peak field, E_{pp}).

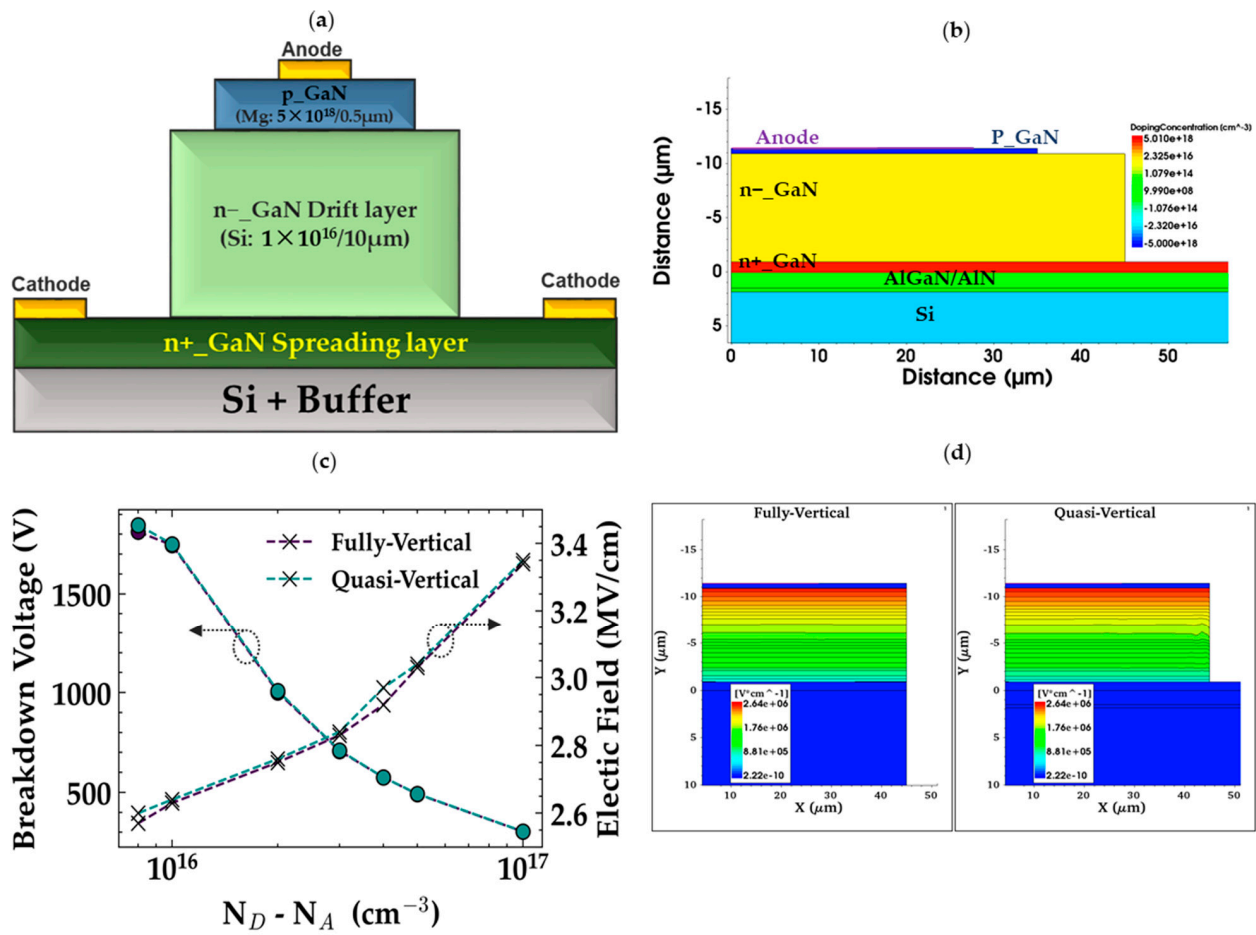


Figure 1. (a) Schematic cross-section of the pseudo-vertical p-n diode structure, illustrating the arrangement of key device layers including the p-type and n-type regions and contacts. (b) Simulated cross-section structure in TCAD, showing a detailed layer composition and geometry, used to investigate the breakdown characteristics of the device under different termination techniques. (c) The breakdown voltage and peak electric field in both quasi-vertical and fully vertical structures for different drift doping concentrations. (d) Electric field distribution at avalanche breakdown in both structures.

Table 2. Key simulation parameters implemented in TCAD.

Physical Phenomenon	Models	Parameters	Values
GaN bandgap	Temperature-dependent bandgap model (@0K)	Bandgap (E_g)	3.44 eV
		Electron affinity (χ)	4.1 eV
Incomplete ionization	Magnesium (p-doped)	Acceptor activation energy	200 meV
Mobility	Low-field doping-dependent Arora model	$\mu_{\min}$	$1500 \text{ cm}^2/\text{Vs}$
		$\mu_{\max}$	$160 \text{ cm}^2/\text{Vs}$
		Reference doping	$3 \times 10^{17} \text{ cm}^{-3}$
Impact ionization	Electron impact ionization coefficients	a_n	$4.48 \times 10^8 \text{ cm}^{-1}$
		b_n	$3.39 \times 10^7 \text{ cm}^{-1}$
	Hole impact ionization coefficients	a_p	$7.13 \times 10^6 \text{ cm}^{-1}$
		b_p	$1.46 \times 10^7 \text{ cm}^{-1}$
Radiative recombination	Radiative recombination constant	C_{rad}	$1.1 \times 10^{-10} \text{ cm}^3 \text{ s}^{-1}$
Auger recombination	Electron coefficient	A_n	$3 \times 10^{-31} \text{ cm}^6 \text{ s}^{-1}$
	Hole coefficient	A_p	$3 \times 10^{-31} \text{ cm}^6 \text{ s}^{-1}$

2.2. Metal Field Plates

Figure 2 illustrates a quasi-vertical p-n diode with a metal field plate located at its edge over the SiO₂ oxide. The electric field at the edge of the junction can be modulated by applying a bias voltage to the metal field plate [27]. Without bias voltage, the depletion region boundary follows the profile shown in case A. When a positive bias is applied to the field plate relative to the n-GaN drift layer, it attracts electrons toward the surface, reducing the depletion layer's extension along the surface, as depicted in case B. This increases the electric field at the junction, thereby lowering the breakdown voltage. Conversely, applying a negative bias repels electrons from the surface, expanding the depletion region along the surface, as shown in case C. This reduces the electric field at the p-n junction, resulting in a higher breakdown voltage [31].

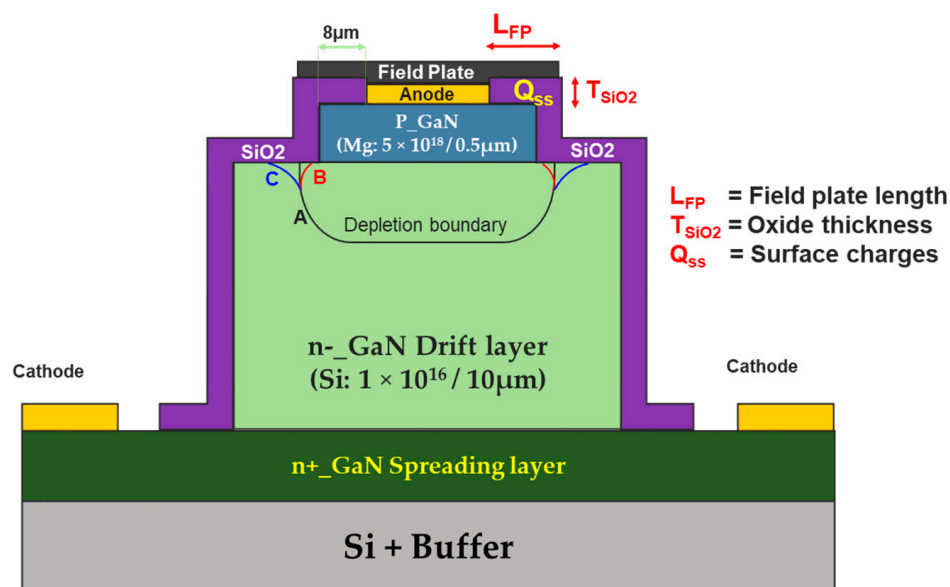


Figure 2. Schematic cross-section of the simulated structure in TCAD with field plate termination.

To identify key parameters and establish design guidelines for minimizing electric field crowding at the edges, the reverse breakdown characteristics of p-n diodes with field plate-based edge termination were analyzed. The simulated structure incorporates silicon dioxide (SiO₂) as the primary dielectric material, with a thickness (T_{SiO2}) ranging from 0.1 μm to 0.6 μm . The analysis further investigates the effects of varying the field plate length (L_{FP}) from 1 μm to 13 μm and the interface state density (Q_{ss}) from $5 \times 10^{11} \text{ cm}^{-2}$ to $1 \times 10^{14} \text{ cm}^{-2}$ on the breakdown voltage and electric field distribution.

As illustrated in Figure 3a, the breakdown voltage (BV) increases marginally with the length of the field plate (L_{FP}) up to 8 μm , showing the field plate has no effect on the breakdown below this dimension since the field plate is over the p⁺ anode region. A more pronounced increase of approximately 800 V is observed when the L_{FP} exceeds 10 μm , which aligns with the drift layer thickness. This trend is consistent across all passivation layer thicknesses. The substantial increase in BV can be attributed to the lateral expansion of the depletion region, which becomes comparable to the vertical depletion depth within the drift layer [10,31,32]. Moreover, the relationship between the passivation layer thickness (T_{SiO2}) and the breakdown voltage (BV) reveals that, for thicknesses below approximately 0.2 μm , the breakdown voltage increases as the passivation layer thickness increases, reaching a maximum value of approximately 1200 V. However, beyond this thickness, the breakdown voltage begins to decrease. As illustrated in Figure 3b, for a thin passivation layer, the electric field is suppressed at the junction edge and shifts toward the edge of the field plate. In contrast, for a thicker oxide layer, the field plate's influence on the electric field within the

GaN material is minimal, resulting in field crowding at the p-n junction edge. When the passivation layer thickness is $T_{\text{SiO}_2} = 0.2 \mu\text{m}$, the electric field is distributed approximately equally between the main junction edge and the field plate edge. This behavior occurs because, in the case of a thicker oxide layer, the field plates exert less influence on the electric field distribution within the GaN material, as evidenced by the one-dimensional (1-D) electric field distribution shown in Figure 3c, extracted at the p-n junction edge. In experimental devices, interface states arise from dangling bonds at the surface, which are inherently present. A high density of surface states can lead to increased leakage and a redistribution of the surface electric field [33]. To examine their effect, positive fixed charges at the GaN/Oxide interface were considered, with densities ranging from $5 \times 10^{11} \text{ cm}^{-2}$ to $1 \times 10^{14} \text{ cm}^{-2}$. The high density of surface states attracts electrons, forming a conductive surface channel that shorts the depletion region in the bulk and redistributes the electric fields. As a result, the BV starts decreasing when the Q_{ss} is above $1 \times 10^{12} \text{ cm}^{-2}$ due to the concentrated electric field at the GaN/Oxide interface, as shown in Figure 3d. This effect is more pronounced when the surface fixed charge (Q_{ss}) is high, leading to a more evenly distributed electric field and a lower BV. Therefore, minimizing Q_{ss} at the interface is critical to maintaining the effectiveness of the field plate edge termination.

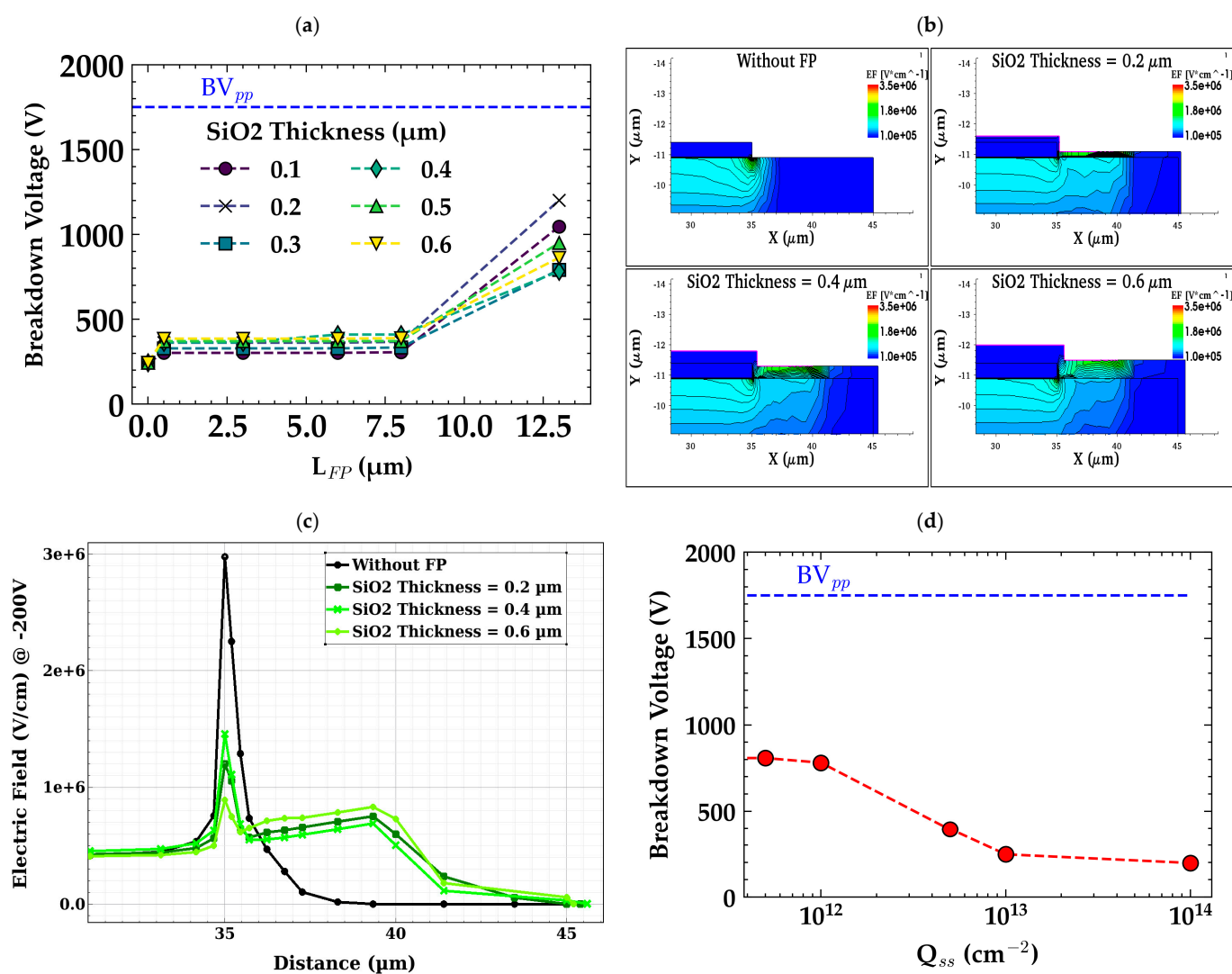


Figure 3. (a) The breakdown voltage vs. the field plate length L_{FP} for several SiO₂ thicknesses. (b) Electric field distribution at -200 V for different SiO₂ thicknesses. (c) Simulated 1-D electric field distribution cutline in the vertical GaN P-N diode for different SiO₂ thicknesses and without a field plate (red). (d) The breakdown voltage plotted against surface fixed charge (red) with a parallel plate BV in blue.

2.3. Mesa

As previously mentioned, electric field crowding at the edge of the p-n junction, which is strongly associated with impact ionization [28], reduces the junction breakdown voltage by intensifying the local electric field concentration. Therefore, mesa etching serves as an effective means of mitigating the electric field distribution from the p-n junction to the bulk. This technique, owing to its simplicity, is widely utilized in the vertical GaN PND process. It facilitates the achievement of a high breakdown voltage (BV) while maintaining both nondestructive and avalanche characteristics in PNDs [19,34]. To assess the effectiveness of this termination method, TCAD simulations were conducted, varying the mesa depth (D_M) from 0.5 μm to 8 μm (referring to the etching depth of the n-drift region), as shown in Figure 4. Additionally, the impact of the bending radius (R_B) at the mesa edges was investigated, with values ranging from 0.1 to 1 μm . Beyond that, the impact of the mesa length (L_M) is not explicitly reflected in the results. This omission arises because, beyond a certain threshold (8 μm), the L_M parameter no longer has a significant effect on the BV and the electric field distribution, as the lateral extension of the depletion layer becomes comparable to the vertical extension in the drift layer.

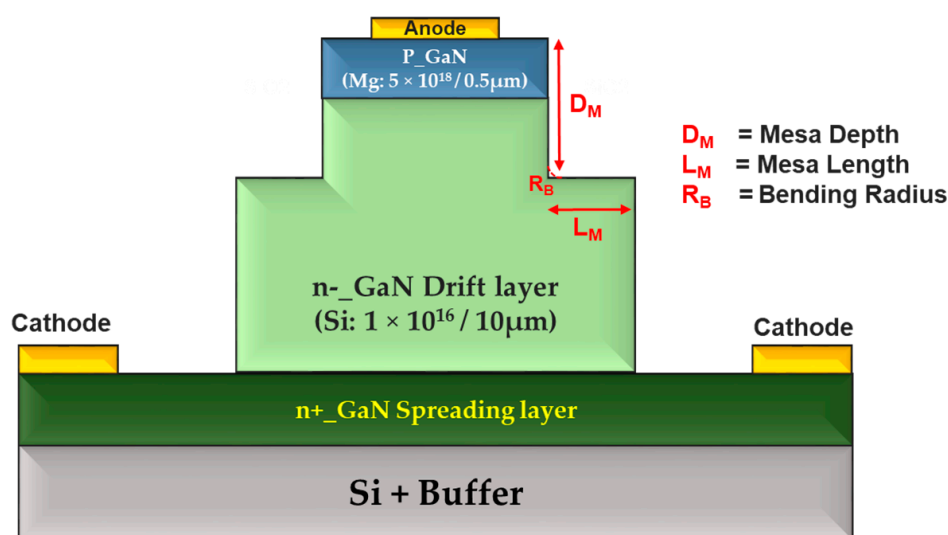


Figure 4. Schematic cross-section of the simulated structure in TCAD with mesa termination.

As depicted in Figure 5a, the breakdown voltage exhibits an almost linear increase with the depth of the mesa etching (D_M) at a low doping concentration ($\leq 1 \times 10^{16} \text{ cm}^{-3}$). As the etching depth increases, the breakdown voltage progressively approaches the ideal parallel-plane breakdown voltage. For deep etching, $D_M > 6 \mu\text{m}$, the device achieves a breakdown voltage of 1605 V, representing 92% of the ideal parallel-plane breakdown voltage device. However, at higher doping levels ($\geq 2 \times 10^{16} \text{ cm}^{-3}$), the breakdown voltage is more limited by the doping due to the reduced depletion extension in the n-GaN drift layer [29].

The electric field distribution at -200 V for the vertical PND was analyzed for mesa etching depths of $D_M = 0, 2, 4$, and 8 μm , as shown in Figure 5b. Notably, a significant reduction in the electric field at the junction, with decreased equipotential crowding, occurs at $D_M = 2 \mu\text{m}$, since the field peak is also displaced from the p-n junction to the bottom of the mesa. This phenomenon was previously discussed by H. Fukushima [19,20]. However, as the etching depth increases, the tip electric field at the edge diminishes, resulting in a more uniform electric field distribution [19]. Devices with deeper mesa etchings exhibit particularly uniform electric field distributions, especially around the edges. Additionally, the impact of the bending radius R_B at mesa corners was investigated

for a mesa depth of 3 μm . As shown in Figure 5c, the breakdown voltage (BV) increases with rounded corners, rising from 900 V to 1000 V. This positive effect can be attributed to the enhanced electric field distribution at the mesa corners [35], as previously explained in the context of trench gate MOSFETs [36,37]. These simulations underline the significance of incorporating rounded corners to improve voltage capability, despite the added complexity in the fabrication process.

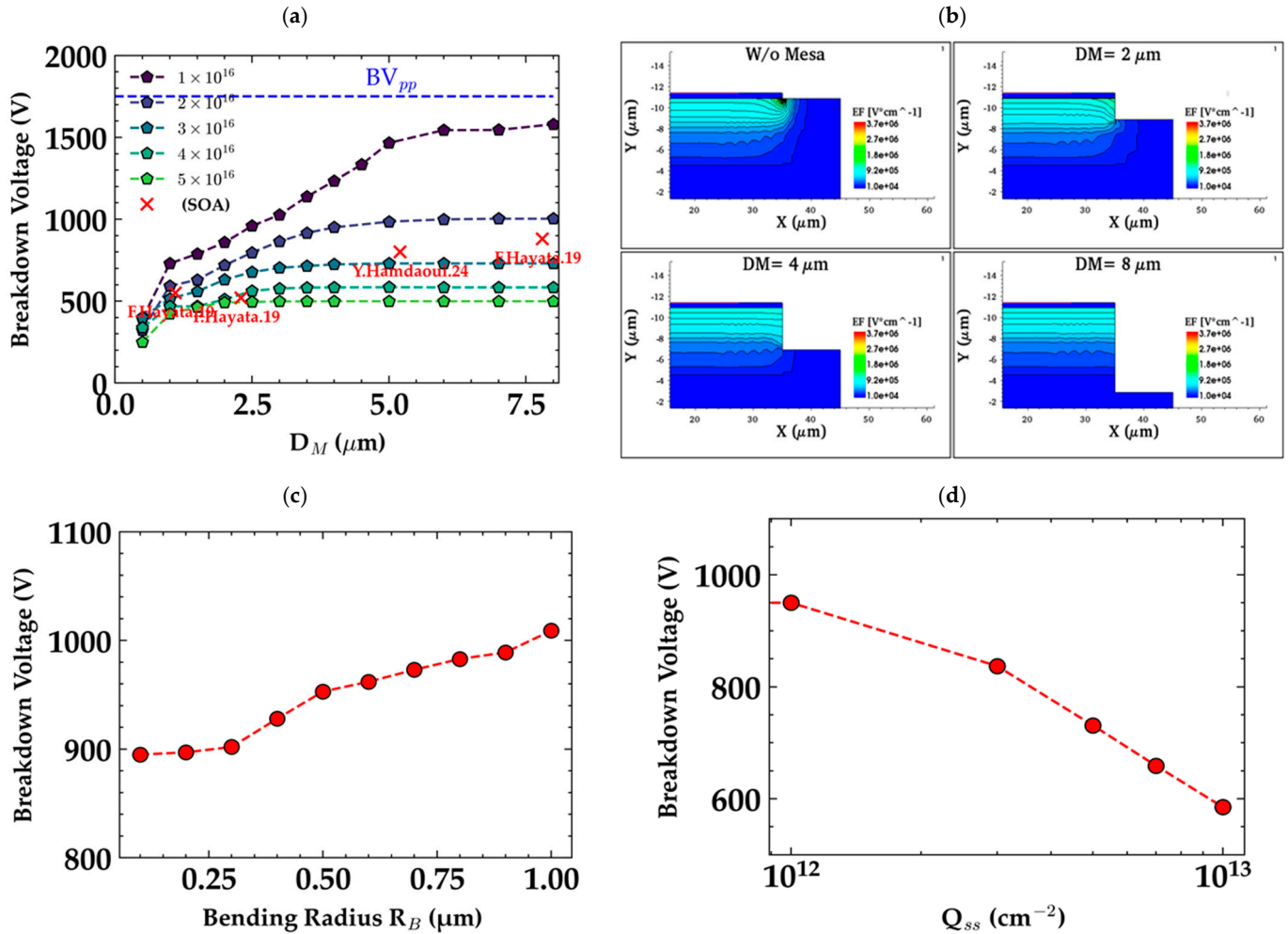


Figure 5. (a) Simulated breakdown voltage as a function of the mesa etching depth (D_M) compared to the state of the art (SOA) at different doping levels ($1\text{--}3 \times 10^{16} \text{ cm}^{-3}$). (b) The electric field distribution at -200V for several mesa etching depths D_M . (c) Breakdown voltage as a function of the bending radius (R_B) and (d) as a function of the surface fixed charges (Q_{ss}).

By comparing TCAD simulation results with experimental data (with a drift doping layer of $2\text{--}3 \times 10^{16} \text{ cm}^{-3}$) reported for the state of the art, as shown in Figure 5a, a good correlation can be observed. However, some discrepancies arise in certain cases, which can be attributed to interface state defects created during the mesa etching process. After mesa dry etching in GaN, interface states are formed due to plasma-induced damage, chemical modifications, and defect generation. These states trap carriers, affecting device performance through increased leakage and reduced mobility. Surface oxidation and nitrogen vacancies further degrade electrical properties. Post-etch treatments such as annealing and passivation can mitigate these effects, improving reliability. To investigate this effect, interface states were incorporated into the TCAD simulations, with a density ranging from $1 \times 10^{12} \text{ cm}^{-2}$ to $1 \times 10^{13} \text{ cm}^{-2}$, along with the implementation of a field plate with a D_M of 7 μm and a bending radius R_B of 1 μm , as illustrated in Figure 5d.

As observed, the electric field becomes increasingly concentrated at higher interface state densities exceeding $5 \times 10^{12} \text{ cm}^{-2}$, as previously seen in the previous section.

These results indicate that for mesa etching, a deeper etching depth results in a smaller and more distant electric field at the tip of the device edge relative to the center of the P-N junction. This leads to a more uniform electric field distribution within the device, reduces the likelihood of premature breakdown at the edge, and increases the breakdown voltage. Therefore, in designing a vertical mesa etching terminal structure, the mesa should be etched to a depth greater than the maximum depletion width to achieve a breakdown voltage approaching that of the ideal plane parallel structure [27].

2.4. Bevel Mesa

In addition to the conventional perpendicular mesa structure discussed in the previous section, a mesa structure with a negative bevel has been widely adopted to mitigate electric field crowding at the edge of the PN junction. In such design, the electric field at the edge exhibits a decreasing trend as the bevel angle θ is reduced from 90° . This adjustment causes the peak electric field to shift inwards within the device [21].

Several experimental studies have demonstrated that beveled mesa structures can achieve a breakdown voltage (BV) exceeding 3.3 kV with a low leakage current, outperforming the 3 kV BV observed in planar devices with steep mesas using the same field plate (FP) structure [38–43].

To investigate this further, TCAD simulations were conducted on pseudo-vertical p-n diodes with beveled mesa structures, as illustrated in Figure 6 [21]. To better understand the individual impact of each parameter, the simulations were divided into two parts. The first part excluded any passivation to assess only the intrinsic effects, while the second included fixed positive charges with a simple field plate to account for the influence of surface defect charges on the reverse performance of the p-n diode.

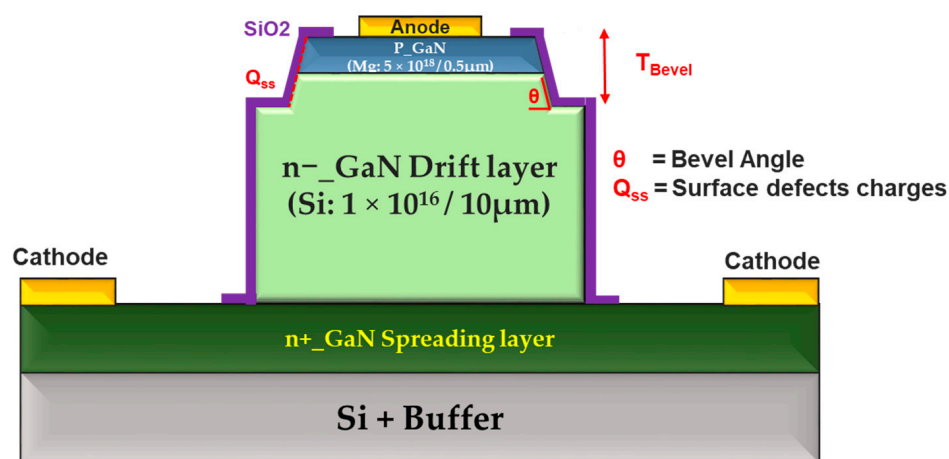


Figure 6. Schematic cross-section of the simulated structure in TCAD with bevel termination.

The bevel etch depth T_{bevel} is required to extend beyond the p-n junction boundary and, practically, should be as deep as possible. However, to account for fabrication limitations and simplify the analysis, a constant bevel etch depth of $2 \mu\text{m}$ was selected for all presented cases. It should be noted that with sufficiently low bevel angles, the etch depth could, in theory, be reduced to the thickness of the p-layer itself. In our study, the bevel angle was varied from 90° to 10° in 10° decrements, and subsequently to 8° , 5° , 3° , 1° , and 0.8° . To assess the impact of the drift doping, the doping densities were varied from $1 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{16} \text{ cm}^{-3}$.

As depicted in Figure 7a, the breakdown voltage (BV) of the bevel mesa structure exhibits two distinct trends based on the doping concentration of the n-GaN drift layer and the bevel angle (θ).

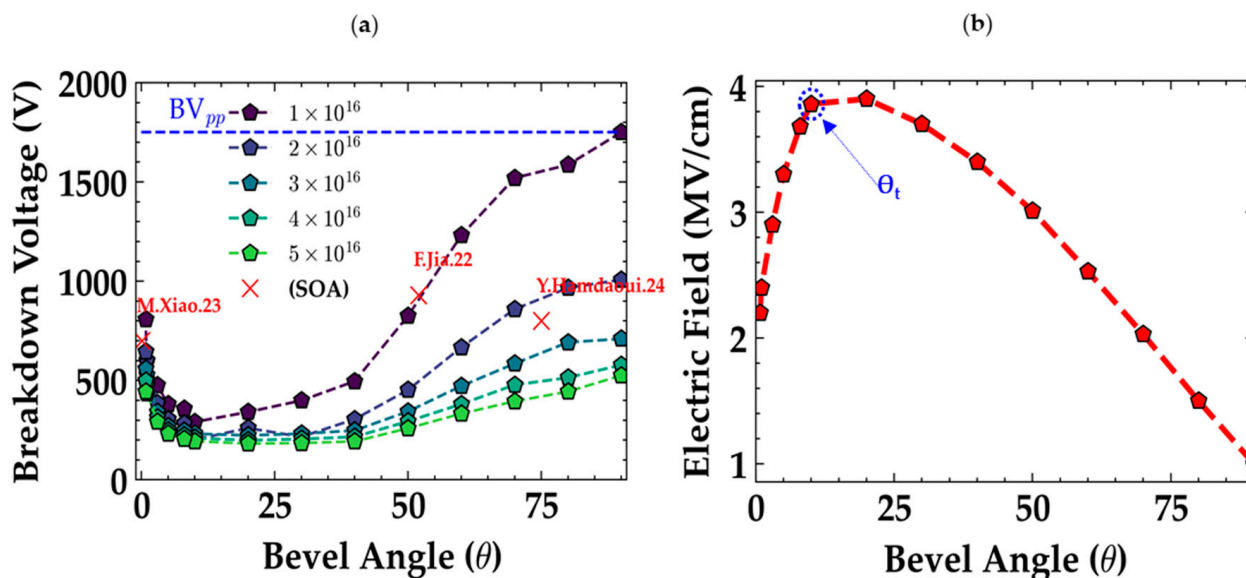


Figure 7. (a) Simulated breakdown voltage as a function of the bevel angle (θ) compared to the state of the art (SOA) at different doping levels ($1\text{--}5 \times 10^{16} \text{ cm}^{-3}$). (b) Peak field extracted from a horizontal cutline at a p-n junction versus a bevel angle (θ) at -300V ; the blue circle indicates the transition angle.

In the first trend, for bevel angles ranging from 90° to 10° , the breakdown voltage generally decreases for all doping concentrations, eventually stabilizing at approximately 300 V for smaller angles. However, at higher doping levels ($5 \times 10^{16} \text{ cm}^{-3}$), this decline is more pronounced, with the BV dropping to ~ 100 V at minimal angles. In the second trend, for ultra-small bevel angles (less than 10°), the BV starts to increase uniformly across all doping concentrations, reaching up to 850 V.

The optimal performance, characterized by a breakdown voltage of 1570 V, occurs at a bevel angle of 80° and a doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$. This configuration achieves approximately 91% of the ideal parallel-plane breakdown voltage. When compared to previously reported values in the state of the art, as shown in Figure 7a, the TCAD simulation results demonstrate strong consistency with these findings (with a drift doping layer of $2\text{--}3 \times 10^{16} \text{ cm}^{-3}$) [39,44–46]. However, some studies report higher breakdown voltages (BVs) at certain bevel angles. This discrepancy could be attributed to the inclusion of additional edge termination techniques alongside bevel termination, such as the use of a field plate with a simple passivation oxide or specifically SOG (spin-on-glass) passivation [39,40]. This could be further investigated through additional TCAD simulations.

To further analyze the impact of the negative bevel and its angle on device performance, the electric field distribution at the p-n junction was examined using a constant doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ in the n-GaN drift layer. Figure 7b shows the peak electric field at -300 V for bevel angles ranging from 90° to 0.8° . The electric field is concentrated at the edge of the main p-n junction, which is the critical point for breakdown within the device. The electric field (EF) for various bevel angles (θ) is extracted along a horizontal cutline at the p-n junction. Two distinct trends emerge, corresponding to the previously observed behavior of the breakdown voltage (BV). For bevel angles ranging from 90° to 10° , the electric field (EF) increases as θ decreases, resulting in a reduction in BV. However, for bevel angles smaller than 10° , the EF begins to decrease, leading to an increase in BV, as

shown in Figure 7a. At $\theta = 8^\circ$, the electric field at the edge starts decreasing, initiating the beveled edge termination mechanism. This angle is defined as the transition angle (θ_t) for the simulated p-n diode. The transition angle is significant because it represents the largest bevel angle where the edge field drops and marks the point at which the peak electric field shifts from the p-n junction edge to the bulk of the device. As θ decreases further below 8° , this transition becomes increasingly pronounced [21].

To assess the interface states effect, a $0.4 \mu\text{m}$ SiO_2 passivation layer was applied along the sidewalls, in conjunction with the introduction of interface states (Q_{ss}). Various densities of quasi-static surface states (Q_{ss}), ranging from $1 \times 10^{12} \text{ cm}^{-2}$ to $7 \times 10^{12} \text{ cm}^{-2}$, were incorporated at the GaN/ SiO_2 interface. Notably, in the absence of interface charges, the passivation layer, despite having a different dielectric constant than GaN, exerts a negligible influence on the electric field distribution both in the bulk and at the surface of the device. In this study, the bevel angle was fixed at 60° , with the doping concentration set to $2 \times 10^{16} \text{ cm}^{-3}$. Additionally, As illustrated in Figure 8a, the breakdown voltage decreases significantly from 640 V in the absence of fixed charges to less than 300 V with a Q_{ss} of $7 \times 10^{12} \text{ cm}^{-2}$. The presence of positive fixed charges on the beveled surface attracts electrons, thereby limiting the extension of the depletion region into the bulk, as previously discussed in the literature [15,21]. Consequently, the electric field, which was initially more evenly distributed due to the bevel termination, becomes significantly concentrated at the surface. This effect is evident in the electric field distribution at the GaN/ SiO_2 interface, as shown in Figure 8b. This results in the disruption of the low edge field previously achieved by the bevel termination, shifting the peak electric field to the surface and compromising the device's performance. This signals the onset of extrinsic breakdown and an increase in leakage current, which prevents the observation of avalanche breakdown. Thus, reducing Q_{ss} during the device's fabrication through surface and sidewall treatments is an important step to guarantee an effective bevel edge termination [45–48].

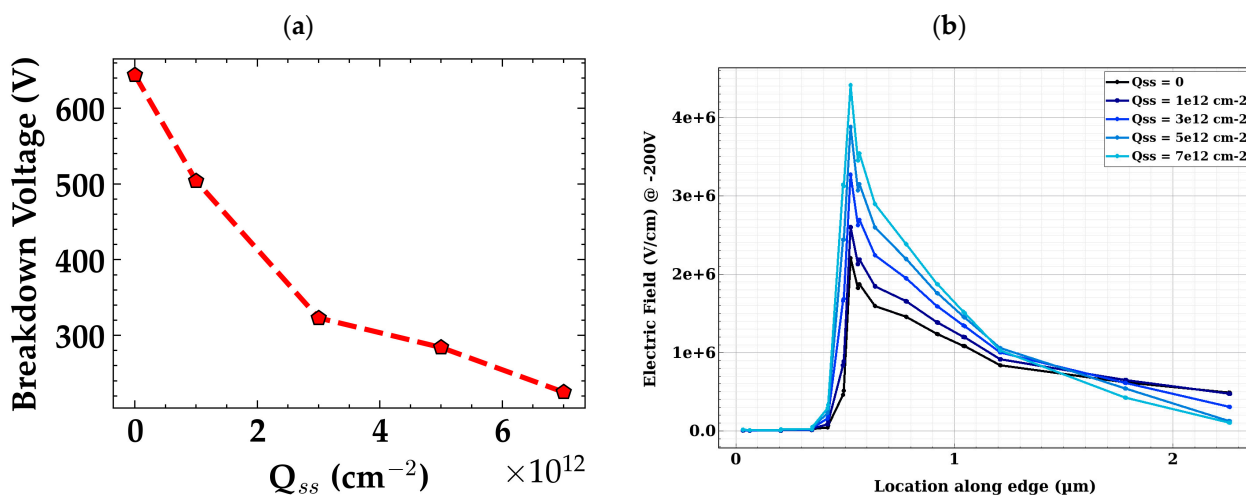


Figure 8. (a) Breakdown voltage as a function of the injected fixed charges at the edge–oxide interface. (b) The electric field profile along the edge at -200 V .

2.5. Trench Termination TT

Trench termination involves etching grooves or trenches around the edge of a device to create a controlled electric field distribution. This method effectively spreads the electric field at the junction between the semiconductor and the surrounding material, preventing the concentration of field lines at the edges that could lead to premature breakdown. The technique is particularly advantageous in GaN devices, where high-voltage performance is critical [35,49]. Various trench structures can be employed, including deeply etched trenches, laterally offset trenches, or stacked trench configurations, each tailored to specific

application requirements [35]. By carefully optimizing the trench geometry, the breakdown voltage and overall reliability of GaN-based devices can be significantly improved.

In this study, TCAD simulations were conducted on a pseudo-vertical PND featuring a rounded deep trench termination designed to control the electric field, as shown in Figure 9.

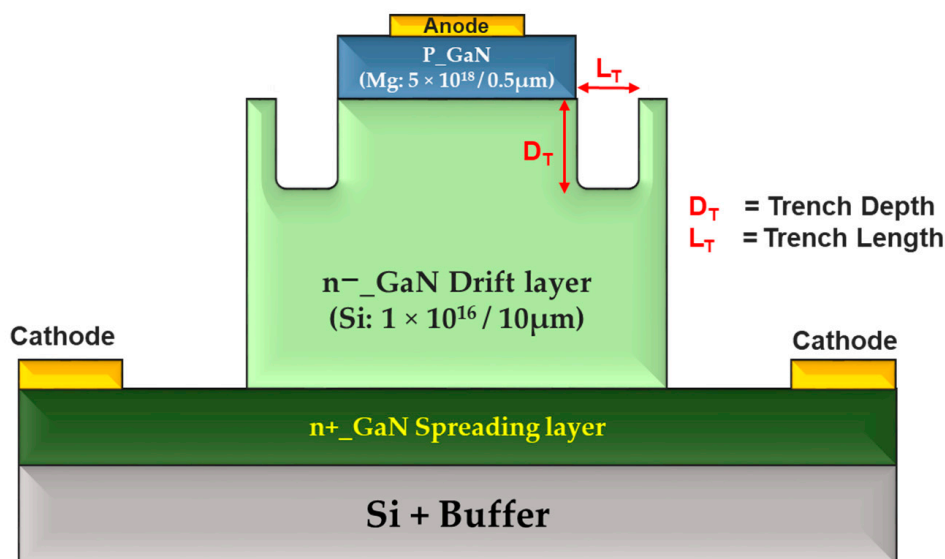


Figure 9. Schematic cross-section of the simulated structure in TCAD with trench termination.

Initially, the structure was investigated without any trench filling to evaluate the intrinsic effects of the trenches. The trench depth (D_T) was varied from 1 to 8 μm , and the trench length (L_T) was also varied from 1 to 8 μm . Results (not presented) showed an initial increase in breakdown voltage (BV) from 1 to 6 μm , beyond which no significant impact was observed. This behavior can be explained by the electric field shifting from the PN junction toward the bottom of the trench as the trench length increases. Once the trench length reaches a certain value (around 6 μm), the electric field becomes more evenly distributed, and further increases in trench length no longer significantly affect the breakdown voltage. The difference between trench and mesa termination can primarily be attributed to the variation in damage induced by the etching process on different geometries.

To achieve results that closely reflect practical scenarios, the trench was filled with a polymer material to mitigate the risk of air arcing and to prevent electric field crowding at the corners. Benzocyclobutene (BCB) was selected for this purpose due to its low dielectric constant of 2.65, as reported in [49,50]. Additionally, a simple field plate was incorporated into the simulation to further optimize the electric field distribution along the surface of the p-n diode, enhancing the overall device performance.

As explained in the previous section, the breakdown voltage (BV) increases strongly with a deeper trench (D_T). As the trench depth increases, the breakdown voltage progressively approaches the ideal parallel-plane breakdown voltage. For trench depths greater than 6 μm ($D_T > 6 \mu\text{m}$) and doping ($1 \times 10^{16} \text{ cm}^{-3}$), the device achieves a breakdown voltage of 1602 V, which represents approximately 92% of the ideal breakdown voltage of an ideal parallel-plane device.

Proceeding to the second phase of the study, the trench was filled with Benzocyclobutene (BCB) material. For this analysis, the trench depth (D_T) and length (L_T) were fixed at 6 μm each, and the n-GaN doping concentration was maintained at $1 \times 10^{16} \text{ cm}^{-3}$. As illustrated in Figure 10a, the incorporation of BCB significantly affects the electric field distribution within the device at -300 V . The low dielectric constant of BCB effectively reduces electric field crowding near the trench edges, contributing to a more uniform field distribution. This modification results in a substantial improvement in the breakdown

voltage compared to the real unfilled trench configuration, highlighting the efficiency of trench filling in alleviating surface electric field intensities and enhancing the device's overall performance.

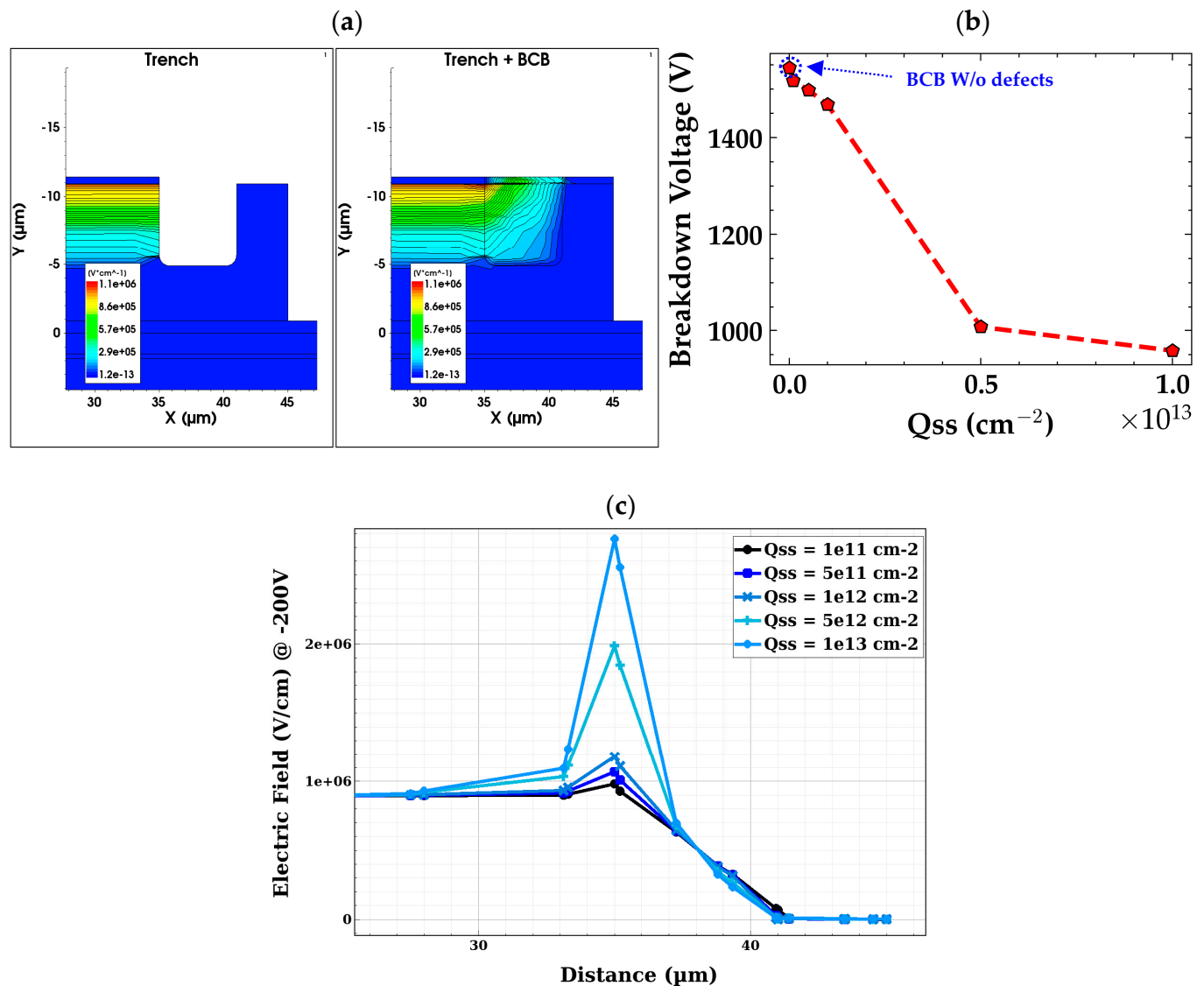


Figure 10. (a) The electric field distribution within the device at -300 V in two cases. (b) The breakdown voltage as a function of the surface fixed charges (Q_{ss}) with BCB. (c) The electric field profile along the GaN/oxide interface at -300 V.

To achieve more realistic results, the impact of interface states at the BCB/GaN interface was considered, as was performed for previously presented edge termination methods. Various densities of interface states Q_{ss} (ranging from 1×10^{11} cm⁻² to 1×10^{13} cm⁻²) were incorporated into the simulations to mimic real-world device conditions. As shown in Figure 10b, in the case of the trench with BCB, the BV significantly decreases at higher interface state densities ($>1 \times 10^{12}$ cm⁻²). Moreover, the presence of interface states substantially alters the electric field profile (cutline at -300 V), leading to a pronounced electric field concentration at the BCB/GaN interface, as shown in Figure 10c. These localized distortions in the electric field can adversely affect the voltage-handling capability of the device.

According to the simulation results, the selection of suitable materials and the adoption of advanced processing techniques to minimize interface state densities are crucial for fully harnessing the advantages of trench termination.

2.6. Ion Implantation

In addition to traditional edge termination techniques such as field plates, bevel mesa, and trench, ion implantation has emerged as a promising approach for controlling the electric field and preventing premature breakdown in vertical GaN power diodes. This stage involves the introduction of specific compensating species (e.g., O, H, and Zn) or inert species (e.g., Ar, N, He, and Kr) into the termination regions, creating deep-level traps that modify the electric field distribution and suppress surface breakdown [17,51–56]. Recently, ion implantation using species such as nitrogen (N) and hydrogen (H) has been explored for improving the performance of vertical GaN P-N diodes [16,47,57]. While ion implantation offers precise control over doping profiles, the mechanisms behind its effect are distinct from those of traditional techniques like bevel or planar mesa termination. Ion implantation can create regions of varying conductivity that effectively redistribute the electric field, mitigating the risks of breakdown. The mechanisms behind ion implantation terminations are multifaceted.

The vertical GaN PND structure under simulation, illustrated in Figure 11, builds upon the previously simulated pseudo-vertical structure by incorporating an innovative edge termination approach using a rectangular box of fixed negatively charged traps. In this simulation study, several parameters were varied to investigate their influence on the breakdown voltage (BV) performance: implant overlap (Ov), which refers to the degree of overlap between the implanted region and the main junction; implant length (Li), representing the lateral extension of the implant region; implant depth (Di), indicating the vertical penetration of the implanted species; and F-ion concentration, which is the density of fixed negatively charged traps introduced via F-ion implantation, studied to evaluate their effect on charge balancing and field modulation.

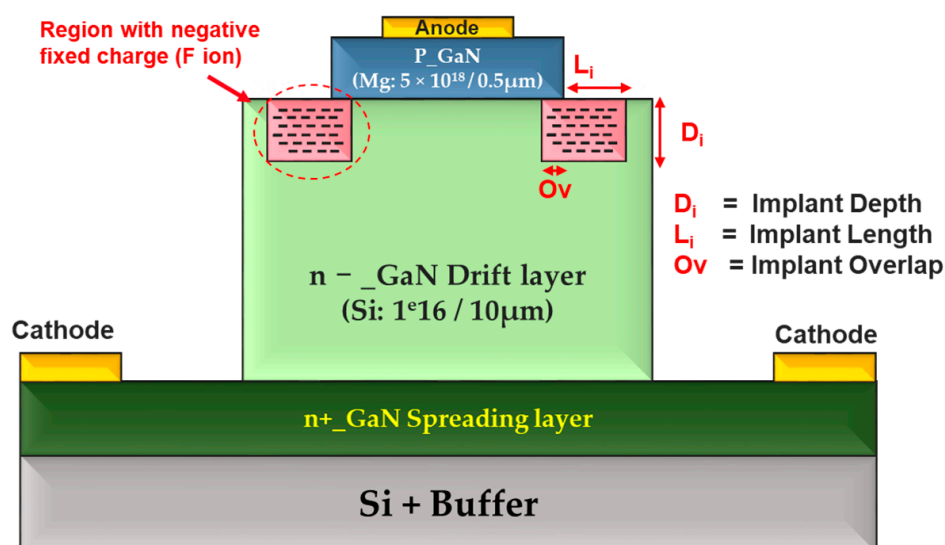


Figure 11. Schematic cross-section of the simulated structure in TCAD with ion implantation termination. A rectangular box with fixed negative charges is defined in the structure.

The impact of each parameter on the breakdown voltage (BV) is depicted in Figure 12. Note that the influence of the implant overlap (Ov) is not explicitly shown in the results because beyond a certain value (1 μm), the Ov parameter ceases to significantly affect the BV and the electric field distribution, as previously discussed in prior studies [51,55].

Consequently, to streamline the analysis and emphasize other influential factors, the implant overlap (Ov) parameter was fixed at a constant value of 1 μm for the simulations. This ensures that the observed effects on breakdown voltage (BV) are primarily due to

variations in implant length (Li), implant depth (Di), and F-ion concentration, allowing for a more focused examination of these parameters' roles in edge termination.

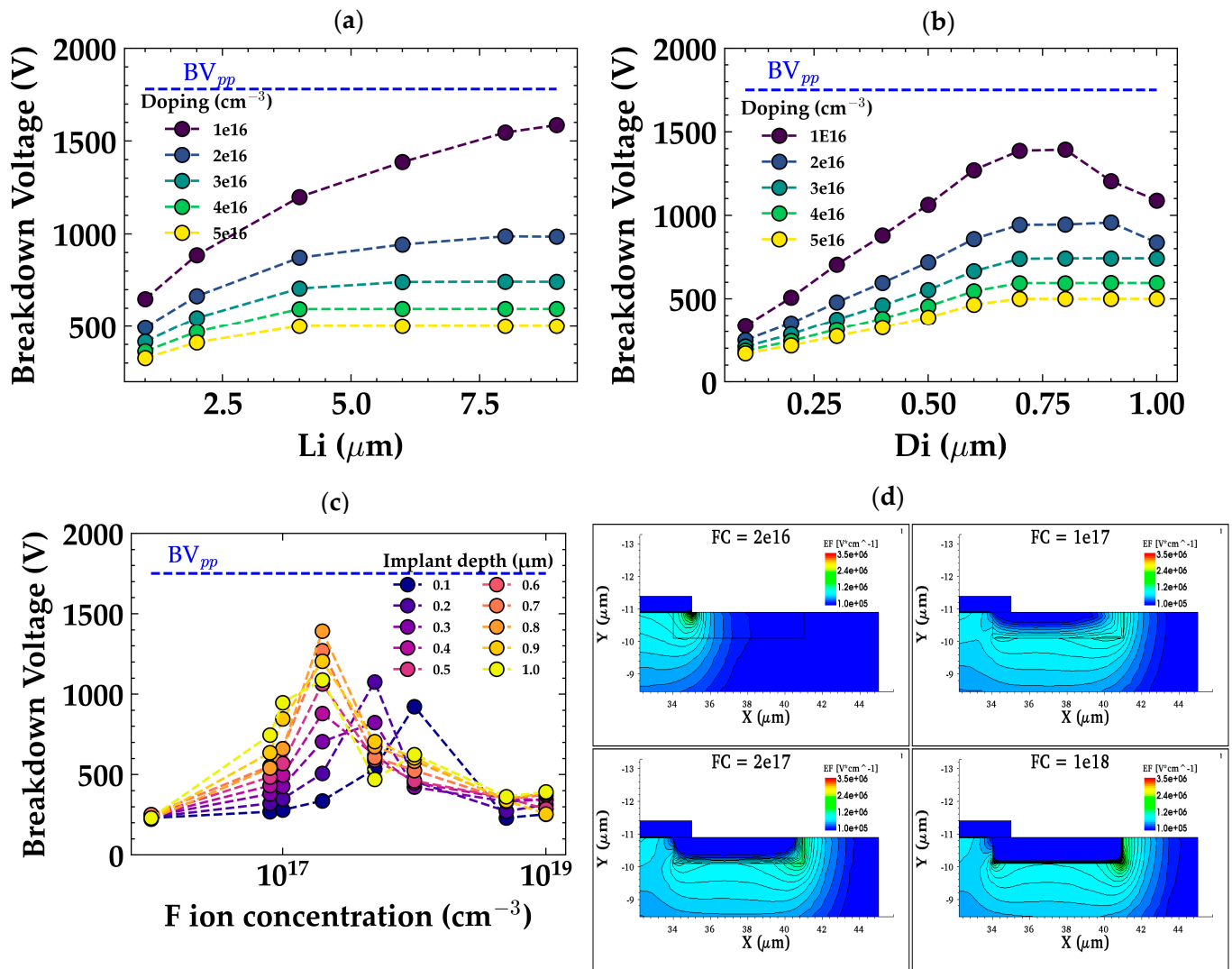


Figure 12. (a) Breakdown voltage as a function of implant width (Li) and (b) implant depth (Di) for several drift layer-doping levels. (c) Breakdown voltage versus F-ion concentration (FC) for various implant depths (Di). (d) Simulated electric field distribution as a function of F ion concentration (FC) at -200 V, with fixed Di and Li values of 0.8 μm and 6 μm , respectively.

Figure 12a illustrates the dependence of implant length (Li) on BV, with initial F-ion concentration and implant depth (Di) values set to $2 \times 10^{17} \text{ cm}^{-3}$ and 0.7 μm , respectively.

At low doping levels ($< 2 \times 10^{16} \text{ cm}^{-3}$), the BV increases as Li increases. This improvement is attributed to the lateral extension of the depletion layer into the implanted region, which shifts the electric field peak from the p-n junction to the edges of the implanted region. However, at higher Li values, the BV reaches a plateau because the lateral depletion extension becomes comparable to the vertical extension through the drift layer. At higher doping levels ($> 2 \times 10^{16} \text{ cm}^{-3}$), the BV exhibits a distinct behavior compared to lower doping levels. This difference is likely due to the doping-induced limitations, where BV becomes more constrained by the doping concentration than by the effects of the implant.

Figure 12b presents the impact of implant depth (Di) on breakdown voltage (BV) at various doping levels, while maintaining the fixed-charge concentration and implant length (Li) at $2 \times 10^{17} \text{ cm}^{-3}$ and 6 μm , respectively. The simulation results reveal two distinct trends: (i) at low doping levels, BV initially increases with Di, reaching a peak at

$D_i = 0.6 \mu\text{m}$, before starting to decline. The reduction in BV at deeper implantations can be attributed to the altered electric field distribution, as previously discussed in works such as [54,57]. This effect highlights the complex interplay between implantation depth and field management in low-doped devices. (ii) At high doping levels, unlike at lower doping levels, BV exhibits a single trend, increasing slightly with D_i until it stabilizes at $D_i = 0.6 \mu\text{m}$. This stabilization is primarily due to the limited depletion extension in the n-GaN drift layer [29] as discussed in the previous sections, which limits further improvement in BV beyond this implant depth. It is worth noting that the electric field distributions for these simulations are not shown, as they have been extensively analyzed in prior research [51,55]. However, the results emphasize the critical role of implant depth in determining BV, with $D_i = 0.6 \mu\text{m}$ emerging as an optimal value for both low and high doping scenarios.

Finally, the impact of fluorine concentration (FC) on breakdown voltage (BV) and electric field distribution was analyzed, as illustrated in Figure 12c. An increase in the F concentration for a given implantation dose (D_i) suggests the presence of an optimal negative fixed-charge concentration at a specific depth, which corresponds to the maximum BV. Furthermore, the optimal fixed-charge concentration decreases as the thickness of the negative fixed-charge region increases. Additionally, with increasing implantation depth, the reduction in BV becomes more significant as the F ion concentration (FC) rises.

The findings emphasize the critical role of optimizing both F ion concentration (FC) and implant depth (D_i) to enhance BV and reduce the electric field intensity at the p-n junction. Figure 12d shows the 2-D electric field distribution at -200 V . It is evident that at low F ion concentrations (FC), there is still significant electric field crowding around the edge of the p-n junction, with FC values below $5 \times 10^{16} \text{ cm}^{-3}$ in the implant region. In this case, the relatively low amount of negative fixed charges is insufficient to disperse the electric field away from the periphery of the main junction. However, at a higher F ion concentration of $>2 \times 10^{17} \text{ cm}^{-3}$, the electric field peak shifts from the main p-n junction to the outer edge of the implanted region, demonstrating the influence of the negatively fixed charges on the electric field distribution in the vertical GaN PND.

The BV demonstrated high sensitivity to variations in both FC and D_i , indicating the necessity of a balanced approach to these parameters. Simulations revealed that the optimal BV of 1410 V , reaching approximately 80% of the parallel-plane BV, was achieved at an FC of $2 \times 10^{17} \text{ cm}^{-3}$ combined with an implant depth of $0.8 \mu\text{m}$. This highlights the importance of precise FC regulation and carefully selected implant depths for effective edge termination. As the implant depth increased, the reduction in BV became more pronounced at elevated F concentrations. This interplay between implantation depth and charge concentration underscores the potential adverse effects of excessive concentrations at greater depths, which can disrupt the electric field distribution and compromise BV performance.

These results underscore the importance of precisely optimizing implantation parameters to achieve effective edge termination with uniform concentration in the implanted regions, ensuring reliable performance in high-voltage GaN devices. Similar behavior has also been observed in the analysis of junction termination extension (JTE) in Si and SiC technologies.

In conclusion, ion implantation is a versatile and effective edge termination technique for GaN devices, enabling precise control over breakdown voltage and electric field distribution. The results highlight the importance of optimizing key parameters such as implant depth, length, and fluorine concentration to achieve robust performance. By carefully balancing these factors, ion implantation can mitigate electric field crowding, enhance breakdown voltage, and improve device reliability. This makes it a promising solution for high-power and high-frequency GaN applications, where advanced edge termination is critical for achieving optimal performance.

2.7. Guard Rings

Transitioning to guard ring edge termination, this technique is a prominent method for managing electric fields at the device periphery, offering distinct advantages compared to other edge termination strategies [56–61]. Typically, field guard rings used in silicon are highly P-type-doped ($>1 \times 10^{19} \text{ cm}^{-3}$). However, integrating highly doped P-type rings in GaN is particularly challenging due to the difficulty of achieving p-type doping in GaN by implantation. Our approach aims to create moderately doped guard rings within the n-GaN drift layer using fluorine implantation, modeled by negative fixed charges as explained in the previous section.

Junction termination extension (JTE) offers field control by expanding the depletion region laterally through tailored doping profiles [23]. However, JTE often requires precise control over doping concentration and lateral diffusion, which can complicate fabrication. In contrast, guard rings can achieve effective edge termination with fewer design constraints, though they may require optimization of spacing and doping levels for maximum efficiency [61].

For this section, TCAD simulations using the same pseudo-vertical PND are employed to systematically investigate the impact of key design parameters on the performance of guard ring edge termination based on negatively fixed charges (F ions), as shown in Figure 13. These parameters include the spacing and width of the guard rings, the number of rings, and the F ion concentration (dose). Through these simulations, the influence of each parameter on critical device metrics, such as breakdown voltage (BV) and electric field distribution, is evaluated. The goal is to optimize the guard ring configuration to achieve robust and reliable edge termination, ensuring high-performance operation in GaN-based power devices.

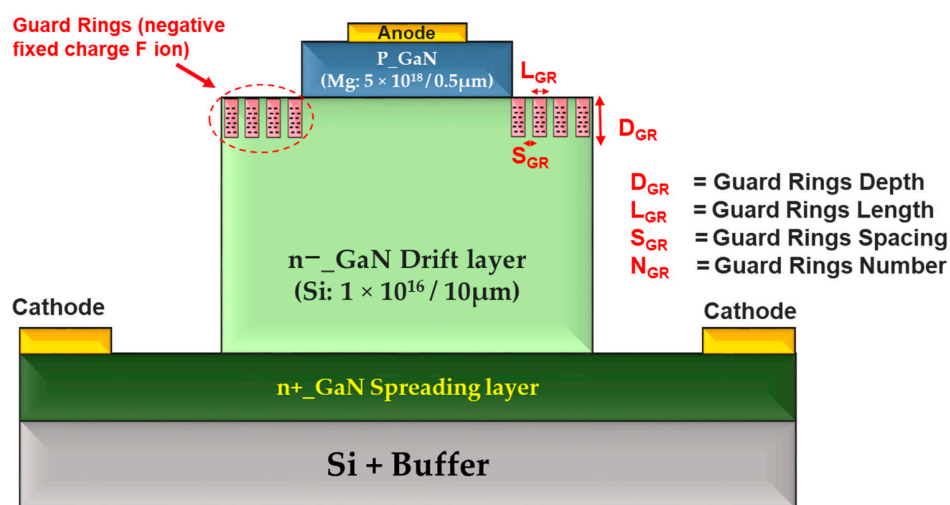


Figure 13. Schematic cross-section of the simulated structure in TCAD with trench termination.

Building on the findings from the ion implantation termination discussed in the previous section, as well as additional simulations incorporating guard ring (GR) edge termination, the optimal fluorine (F) ion concentration was determined to be $2 \times 10^{17} \text{ cm}^{-3}$. Consequently, this value is fixed and consistently applied in all simulations and results presented in this section. This approach establishes a standardized baseline for evaluating the influence of key guard ring parameters on device performance, including the guard ring depth (D_{GR}) ranging from 0.1 μm to 1 μm in 0.1 μm increments, guard ring length (L_{GR}) from 1 μm to 2.5 μm , spacing between adjacent guard rings (S_{GR}) from 0.5 μm to 2.5 μm , and the number of guard rings (N_{GR}) from 3 to 7.

Figure 14a illustrates the simulated breakdown voltage (BV) as a function of guard ring depth (D_{GR}), with constant parameters of $L_{GR} = 1 \mu\text{m}$, $S_{GR} = 1 \mu\text{m}$, and $N_{GR} = 3$. The results demonstrate that BV increases with D_{GR} , reaching an optimum value at a depth of $2 \mu\text{m}$, identified as the optimal depth for guard rings. Beyond this point, the BV reaches saturation and remains constant, emphasizing the importance of optimizing D_{GR} for maximum device performance [59]. Next, the effect of guard ring length (L_{GR}) was analyzed while keeping $D_{GR} = 2 \mu\text{m}$, $S_{GR} = 1 \mu\text{m}$, and $N_{GR} = 3$ constant as presented in Figure 14b. The results indicate a near-ideal parallel-plane BV of 1740 V , with less sensitivity to variations in L_{GR} compared to D_{GR} . This finding is consistent with observations in previous studies [59]. This behavior can be attributed to the equipotential nature of the guard ring length region, making L_{GR} a less critical parameter for electric field management.

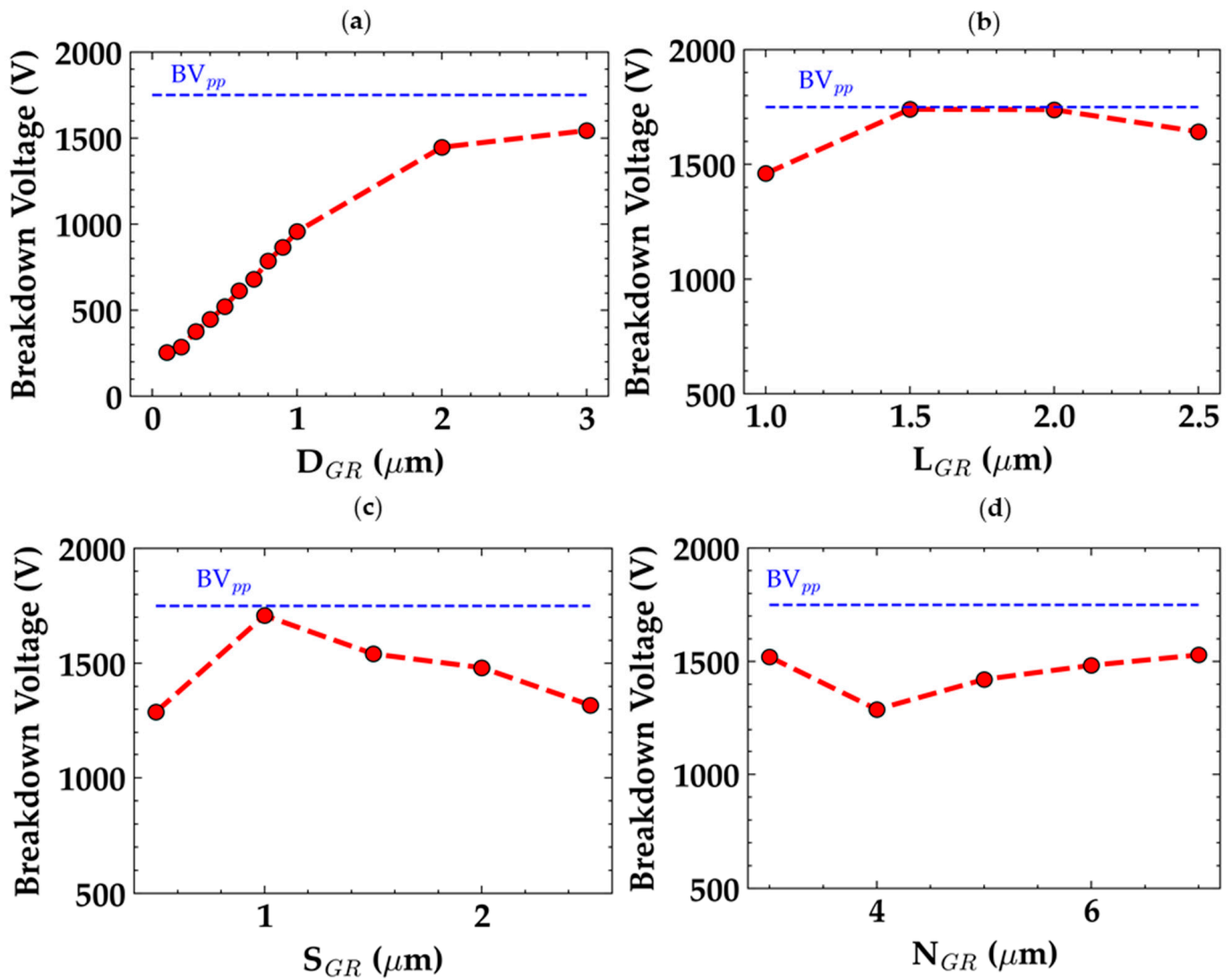


Figure 14. (a) Breakdown voltage as a function of guard ring depth (D_{GR}), (b) as a function of guard ring length (L_{GR}), (c) as a function of guard ring spacing (S_{GR}), and (d) as a function of the number of rings (N_{GR}).

In contrast, the impact of the spacing between adjacent guard rings (S_{GR}) was evaluated with constant $D_{GR} = 2 \mu\text{m}$, $L_{GR} = 1 \mu\text{m}$, and $N_{GR} = 4$. As shown in Figure 14c, two distinct trends emerge: (i) smaller S_{GR} values less than $1 \mu\text{m}$ result in reduced BV due to insufficient electric field spreading and a peak electric field concentration at the outer edge of the termination. (ii) Larger S_{GR} values beyond $1.5 \mu\text{m}$ lead to weaker electrostatic

coupling between adjacent rings, causing a higher peak electric field at the inner edge of the termination. An optimal electric field profile and enhanced BV are achieved for S_{GR} values between 1.0 μm and 1.5 μm , highlighting the importance of balanced spacing for effective edge termination and superior device performance. Finally, the influence of the number of guard rings (N_{GR}) was investigated, as shown in Figure 14d (with $D_{GR} = 2 \mu\text{m}$, $L_{GR} = 1 \mu\text{m}$ fixed). The results indicate that increasing the number of guard rings improves BV due to the enhanced lateral spreading of the electric field from the p-n junction edge to the bottom of the GR region. For three guard rings, the peak electric field is located at the outer edge of the termination. This peak is effectively suppressed as the number of rings increases. However, for $N_{GR} = 7$, the peak electric field shifts to the inner edge of the termination, with further increases in N_{GR} providing enhanced performance improvements. These findings align well with experimental results reported in [59].

In conclusion, the moderately doped guard ring (GR) edge termination has been found to be an effective technique for enhancing the breakdown voltage, achieving approximately 99% of the parallel-plane BV (~1740 V) in GaN devices by optimizing the electric field distribution. Key parameters such as guard ring depth (D_{GR}), length (L_{GR}), spacing (S_{GR}), and the number of rings (N_{GR}) play significant roles in achieving optimal device performance. The simulations revealed that D_{GR} and S_{GR} are critical for managing electric field peaks and maximizing BV, while L_{GR} has a less pronounced effect due to its equipotential nature. Increasing N_{GR} improves electric field spreading with enhanced BV. These findings highlight the necessity of precise parameter tuning to ensure robust and reliable edge termination for high-voltage GaN devices, making GR a scalable and efficient solution for advanced power electronics.

3. Conclusions

In conclusion, the various edge termination techniques—field plate (FP), mesa, bevel, trench, ion implantation, and guard ring (GR)—aim to improve breakdown voltage (BV) and optimize electric field distribution in GaN pseudo-vertical p-n diodes. However, the selection of the most suitable termination method is often influenced not only by performance considerations but also by fabrication complexity and cost as shown in Table 3.

Table 3. Comparison of edge termination techniques.

Edge Termination	Maximum BV	Complexity	Cost
Field Plate	1200	+	+
Mesa	1605	+	+
Bevel	1570	++	+
Trench	1602	+++	++
Ion Implantation	1410	++	++
Guard Ring (GR)	1740	+++	++

- Field Plate (FP) Termination: This method is highly effective in extending the high-voltage region and smoothing electric field transitions. However, it requires precise metallization steps and careful alignment of the field plates, which can add to the fabrication complexity.
- Mesa Termination: Mesa involves creating a stepped surface to direct electric fields away from the device edges. This method is relatively simple to fabricate using standard etching techniques, making it a cost-effective solution for many power devices. Its simplicity, however, may limit its performance in very high-voltage applications compared to other more advanced techniques.

- (c) **Bevel Termination:** Beveling the device edges helps to reduce electric field intensity at the corners, effectively preventing breakdowns. The fabrication of bevel edges requires precise angle control, which can be challenging. Bevel termination offers a good balance between performance and ease of fabrication, making it suitable for medium-voltage applications.
- (d) **Trench Termination:** Trench termination, especially when combined with materials like Benzocyclobutene (BCB), reduces electric field crowding and improves performance. Fabricating trenches with high precision is more complex and requires additional steps like trench filling and planarization, which increases fabrication costs and complexity. However, trench termination excels in high-voltage applications where field control is critical.
- (e) **Ion Implantation Termination:** This method modifies the edge termination with species like fluorine (F), which helps prevent premature breakdown. Ion implantation is a relatively straightforward process compared to trench termination but requires careful control of implantation depth and concentration. While the process is not as complex as trenching or field plating, the optimization of ion concentration and depth for maximum BV performance requires high precision, which can make this method more challenging from a production point of view than simpler techniques like bevel termination.
- (f) **Guard Ring (GR) Termination:** Guard ring termination distributes the electric field evenly around the device. While the concept is simple, optimizing guard ring parameters such as depth, length, spacing, and the number of rings can add fabrication complexity. It requires precise alignment of the guard rings, which increases manufacturing time and cost. However, it is a highly effective technique for high-voltage and high frequency applications, where the benefits in terms of field control justify the added complexity.

Each termination method offers unique advantages in terms of device performance, but the choice of technique often depends on the specific application, the required breakdown voltage, and the fabrication resources available. For high-performance devices where maximizing BV is critical, trench, field plate, and guard ring terminations are often preferred, despite their greater fabrication complexity. Conversely, mesa, bevel, and ion implantation terminations are more suitable for cost-effective designs where moderate performance is sufficient. In addition, other parameters such as avalanche breakdown capability must be taken into account. Guard rings and implantation edge terminations are known to be more efficient than MESA or field plates to maximize this parameter. However, it is important to note that our simulation results regarding edge termination techniques for GaN could be further improved with experimental validations and considerations for industrial scalability, ensuring that the methods are not only theoretically effective but also practically feasible for large-scale production.

Author Contributions: Conceptualization, M.E.A., J.B., P.G. and D.A.; methodology, M.E.A.; software, M.E.A.; validation, J.B., P.G. and D.A.; formal analysis, M.E.A.; investigation, M.E.A.; resources, J.B. and M.C.; data curation, M.E.A.; writing—original draft preparation, M.E.A.; writing—review and editing, J.B., P.G. and D.A.; visualization, M.E.A.; supervision, J.B. and D.A.; project administration, M.C. and J.B.; funding acquisition, M.C. and J.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Agence Nationale de la Recherche: ANR-22-CE05-0010.

Data Availability Statement: Data are contained within the article.

Acknowledgments: This work is part of the ELEGaNT project (ANR-22-CE05-0010).

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Fu, H.; Fu, K.; Chowdhury, S.; Palacios, T.; Zhao, Y. Vertical GaN Power Devices: Device Principles and Fabrication Technologies—Part I. *IEEE Trans. Electron Devices* **2021**, *68*, 3200–3211. [\[CrossRef\]](#)
2. Zhang, Y.; Dadgar, A.; Palacios, T. Gallium nitride vertical power devices on foreign substrates: A review and outlook. *J. Phys. Appl. Phys.* **2018**, *51*, 273001. [\[CrossRef\]](#)
3. Langpoklakpam, C.; Liu, A.-C.; Hsiao, Y.-K.; Lin, C.-H.; Kuo, H.-C. Vertical GaN MOSFET Power Devices. *Micromachines* **2023**, *14*, 1937. [\[CrossRef\]](#) [\[PubMed\]](#)
4. Roccaforte, F.; Greco, G.; Fiorenza, P.; Iucolano, F. An Overview of Normally-Off GaN-Based High Electron Mobility Transistors. *Materials* **2019**, *12*, 1599. [\[CrossRef\]](#) [\[PubMed\]](#)
5. Ding, X.; Zhou, Y.; Cheng, J. A review of gallium nitride power device and its applications in motor drive. *CES Trans. Electr. Mach. Syst.* **2019**, *3*, 54–64. [\[CrossRef\]](#)
6. Alquier, D.; Cayrel, F.; Menard, O.; Bazin, A.-E.; Yvon, A.; Collard, E. Recent Progresses in GaN Power Rectifier. *Jpn. J. Appl. Phys.* **2012**, *51*, 01AG08. [\[CrossRef\]](#)
7. Kachi, T. State-of-the-art GaN vertical power devices. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 16.1.1–16.1.4.
8. Zhang, Y.; Sun, M.; Piedra, D.; Azize, M.; Zhang, X.; Fujishima, T.; Palacios, T. GaN-on-Si Vertical Schottky and p-n Diodes. *IEEE Electron Device Lett.* **2014**, *35*, 618–620. [\[CrossRef\]](#)
9. Sun, Y.; Kang, X.; Zheng, Y.; Lu, J.; Tian, X.; Wei, K.; Wu, H.; Wang, W.; Liu, X.; Zhang, G. Review of the Recent Progress on GaN-Based Vertical Power Schottky Barrier Diodes (SBDs). *Electronics* **2019**, *8*, 575. [\[CrossRef\]](#)
10. Hatakeyama, Y.; Nomoto, K.; Kaneda, N.; Kawano, T.; Mishima, T.; Nakamura, T. Over 3.0 GW/cm² Figure-of-Merit GaN p-n Junction Diodes on Free-Standing GaN Substrates. *IEEE Electron Device Lett.* **2011**, *32*, 1674–1676. [\[CrossRef\]](#)
11. Bian, Z.; Zeng, K.; Chowdhury, S. 2.8 kV Avalanche in Vertical GaN PN Diode Utilizing Field Plate on Hydrogen Passivated P-Layer. *IEEE Electron Device Lett.* **2022**, *43*, 596–599. [\[CrossRef\]](#)
12. Kizilyalli, I.C.; Edwards, A.P.; Nie, H.; Bui-Quang, P.; Disney, D.; Bour, D. 400-A (Pulsed) Vertical GaN p-n Diode with Breakdown Voltage of 700 V. *IEEE Electron Device Lett.* **2014**, *35*, 654–656. [\[CrossRef\]](#)
13. Kizilyalli, I.C.; Edwards, A.P.; Nie, H.; Bour, D.; Prunty, T.; Disney, D. 3.7 kV Vertical GaN PN Diodes. *IEEE Electron Device Lett.* **2014**, *35*, 247–249. [\[CrossRef\]](#)
14. Xu, Z.; Detchprohm, T.; Shen, S.-C.; Nepomuk Otte, A.; Dupuis, R.D. Low Leakage and High Gain GaN p-i-n Avalanche Photodiode with Shallow Bevel Mesa Edge Termination and Recessed Window. *IEEE Trans. Electron Devices* **2024**, *71*, 3761–3768. [\[CrossRef\]](#)
15. Lee, S.-H.; Cha, H.-Y. Design of Trench MIS Field Plate Structure for Edge Termination of GaN Vertical PN Diode. *Micromachines* **2023**, *14*, 2005. [\[CrossRef\]](#) [\[PubMed\]](#)
16. Duan, Y.; Wang, J.; Xie, A.; Zhu, Z.; Fay, P. 1.7-kV vertical GaN p-n diode with triple-zone graded junction termination extension formed by ion-implantation. *E-Prime—Adv. Electr. Eng. Electron. Energy* **2023**, *6*, 100330. [\[CrossRef\]](#)
17. Sergei-Ion Implantation in GaN-01.pdf. Available online: <https://people.physics.anu.edu.au/~cxj109/Publications/Sergei-Ion%20Implantation%20in%20GaN-01.pdf> (accessed on 5 March 2024).
18. Fu, K.; He, Z.; Yang, C.; Zhou, J.; Fu, H.; Zhao, Y. GaN-on-GaN p-i-n diodes with avalanche capability enabled by eliminating surface leakage with hydrogen plasma treatment. *Appl. Phys. Lett.* **2022**, *121*, 092103. [\[CrossRef\]](#)
19. Fukushima, H.; Usami, S.; Ogura, M.; Ando, Y.; Tanaka, A.; Deki, M.; Kushimoto, M.; Nitta, S.; Honda, Y.; Amano, H. Vertical GaN p-n diode with deeply etched mesa and capability of avalanche breakdown. *Appl. Phys. Express* **2019**, *12*, 026502. [\[CrossRef\]](#)
20. Shi, S.; Wang, G.; Xiang, Y.; Guo, C.; Wang, X.; Pu, Y.; Li, H.; Li, Z. Investigation on Breakdown Characteristics of Various Surface Terminal Structures for GaN-Based Vertical P-i-N Diodes. *J. Appl. Math. Phys.* **2024**, *12*, 554–568. [\[CrossRef\]](#)
21. Zeng, K.; Chowdhury, S. Designing Beveled Edge Termination in GaN Vertical p-i-n Diode-Bevel Angle, Doping, and Passivation. *IEEE Trans. Electron Devices* **2020**, *67*, 2457–2462. [\[CrossRef\]](#)
22. El Amrani, M.; Buckley, J.; Katsounis, T.; Arguello, D.P.; El Rammouz, H.; Alquier, D.; Charles, M. Study of Leakage Current Transport Mechanisms in Pseudo-Vertical GaN-on-Silicon Schottky Diode Grown by Localized Epitaxy. *Crystals* **2024**, *14*, 553. [\[CrossRef\]](#)
23. Yates, L.; Gunning, B.P.; Crawford, M.H.; Steinfeldt, J.; Smith, M.L.; Abate, V.M.; Dickerson, J.R.; Armstrong, A.M.; Binder, A.; Allerman, A.A.; et al. Demonstration of >6.0-kV Breakdown Voltage in Large Area Vertical GaN p-n Diodes with Step-Etched Junction Termination Extensions. *IEEE Trans. Electron Devices* **2022**, *69*, 1931–1937. [\[CrossRef\]](#)
24. Zhang, X.; Zou, X.; Lu, X.; Tang, C.W.; Lau, K.M. Fully- and Quasi-Vertical GaN-on-Si p-i-n Diodes: High Performance and Comprehensive Comparison. *IEEE Trans. Electron Devices* **2017**, *64*, 809–815. [\[CrossRef\]](#)
25. Zhang, Y.; Piedra, D.; Sun, M.; Hennig, J.; Dadgar, A.; Yu, L.; Palacios, T. High-Performance 500 V Quasi- and Fully-Vertical GaN-on-Si pn Diodes. *IEEE Electron Device Lett.* **2017**, *38*, 248–251. [\[CrossRef\]](#)

26. HAL PDF Full Text. Available online: https://hal.science/hal-04436387v1/file/CSW-2023_Abstract_IEMN-Siltronic.pdf (accessed on 19 February 2025).
27. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer International Publishing: Cham, Switzerland, 2019; ISBN 978-3-319-93987-2.
28. Maeda, T.; Narita, T.; Yamada, S.; Kachi, T.; Kimoto, T.; Horita, M.; Suda, J. Impact ionization coefficients and critical electric field in GaN. *J. Appl. Phys.* **2021**, *129*, 185702. [\[CrossRef\]](#)
29. Sze, S.M. *Physics of Semiconductor Devices*, 3rd ed.; Wiley-Interscience: Hoboken, NJ, USA, 2007.
30. Cao, L.; Wang, J.; Harden, G.; Ye, H.; Stillwell, R.; Hoffman, A.J.; Fay, P. Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates. *Appl. Phys. Lett.* **2018**, *112*, 262103. [\[CrossRef\]](#)
31. Chung, S.K.; Han, S.Y. Design curves of breakdown voltage at field plate edge and effect of interface charge. *Microelectron. J.* **2002**, *33*, 399–402. [\[CrossRef\]](#)
32. Hatakeyama, Y.; Nomoto, K.; Terano, A.; Kaneda, N.; Tsuchiya, T.; Mishima, T.; Nakamura, T. High-Breakdown-Voltage and Low-Specific-on-Resistance GaN p-n Junction Diodes on Free-Standing GaN Substrates Fabricated Through Low-Damage Field-Plate Process. *Jpn. J. Appl. Phys.* **2013**, *52*, 028007. [\[CrossRef\]](#)
33. Engel-Herbert, R.; Hwang, Y.; Stemmer, S. Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces. *J. Appl. Phys.* **2010**, *108*, 124101. [\[CrossRef\]](#)
34. Fukushima, H.; Usami, S.; Ogura, M.; Ando, Y.; Tanaka, A.; Deki, M.; Kushimoto, M.; Nitta, S.; Honda, Y.; Amano, H. Deeply and vertically etched butte structure of vertical GaN p-n diode with avalanche capability. *Jpn. J. Appl. Phys.* **2019**, *58*, SCCD25. [\[CrossRef\]](#)
35. Zhang, Y.; Sun, M.; Liu, Z.; Piedra, D.; Hu, J.; Gao, X.; Palacios, T. Trench formation and corner rounding in vertical GaN power devices. *Appl. Phys. Lett.* **2017**, *110*, 193506. [\[CrossRef\]](#)
36. Baliga, B.J. *Advanced Power MOSFET Concepts*; Springer: Boston, MA, USA, 2010; ISBN 978-1-4419-5916-4.
37. Yamada, S.; Sakurai, H.; Osada, Y.; Furuta, K.; Nakamura, T.; Kamimura, R.; Narita, T.; Suda, J.; Kachi, T. Formation of highly vertical trenches with rounded corners via inductively coupled plasma reactive ion etching for vertical GaN power devices. *Appl. Phys. Lett.* **2021**, *118*, 102101. [\[CrossRef\]](#)
38. Nomoto, K.; Hu, Z.; Song, B.; Zhu, M.; Qi, M.; Yan, R.; Protasenko, V.; Imhoff, E.; Kuo, J.; Kaneda, N.; et al. GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ·cm²: A record high figure-of-merit of 12.8 GW/cm². In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 9.7.1–9.7.4. [\[CrossRef\]](#)
39. Shankar, B.; Zeng, K.; Gunning, B.; Martinez, R.P.; Meng, C.; Flicker, J.; Binder, A.; Dickerson, J.R.; Kaplar, R.; Chowdhury, S. Movement of Current Filaments and its Impact on Avalanche Robustness in Vertical GaN P-N diode Under UIS stress. In Proceedings of the 2022 Device Research Conference (DRC), Columbus, OH, USA, 26–29 June 2022; pp. 1–2. [\[CrossRef\]](#)
40. Shankar, B.; Bian, Z.; Zeng, K.; Meng, C.; Martinez, R.P.; Chowdhury, S.; Gunning, B.; Flicker, J.; Binder, A.; Dickerson, J.R.; et al. Study of Avalanche Behavior in 3 kV GaN Vertical P-N Diode Under UIS Stress for Edge-termination Optimization. In Proceedings of the 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 27–31 March 2022; pp. 2B.2-1–2B.2-4. [\[CrossRef\]](#)
41. Maeda, T.; Narita, T.; Ueda, H.; Kanechika, M.; Uesugi, T.; Kachi, T.; Kimoto, T.; Horita, M.; Suda, J. Design and Fabrication of GaN p-n Junction Diodes with Negative Beveled-Mesa Termination. *IEEE Electron Device Lett.* **2019**, *40*, 941–944. [\[CrossRef\]](#)
42. Hamdaoui, Y.; Michler, S.; Bidaud, A.; Ziouche, K.; Medjdoub, F. 1200-V Fully Vertical GaN-on-Silicon p-i-n Diodes with Avalanche Capability and High On-State Current Above 10 A. *IEEE Trans. Electron Devices* **2025**, *72*, 338–343. [\[CrossRef\]](#)
43. Jia, F.; Ma, X.; Yang, L.; Zhang, X.; Hou, B.; Zhang, M.; Wu, M.; Niu, X.; Du, J.; Liu, S.; et al. 930V and Low-Leakage Current GaN-on-Si Quasi-Vertical PiN Diode with Beveled-Sidewall Treated by Self-Aligned Fluorine Plasma. *IEEE Electron Device Lett.* **2022**, *43*, 1400–1403. [\[CrossRef\]](#)
44. Hamdaoui, Y.; Abid, I.; Michler, S.; Ziouche, K.; Medjdoub, F. Demonstration of avalanche capability in 800 V vertical GaN-on-silicon diodes. *Appl. Phys. Express* **2023**, *17*, 016503. [\[CrossRef\]](#)
45. Xiao, M.; Wang, Y.; Zhang, R.; Song, Q.; Porter, M.; Carlson, E.; Cheng, K.; Ngo, K.; Zhang, Y. Robust Avalanche in 1.7 kV Vertical GaN Diodes with a Single-Implant Bevel Edge Termination. *IEEE Electron Device Lett.* **2023**, *44*, 1616–1619. [\[CrossRef\]](#)
46. Zhang, Y.; Sun, M.; Wong, H.-Y.; Lin, Y.; Srivastava, P.; Hatem, C.; Azize, M.; Piedra, D.; Yu, L.; Sumitomo, T.; et al. Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes. *IEEE Trans. Electron Devices* **2015**, *62*, 2155–2161. [\[CrossRef\]](#)
47. Chang, Y.-F.; Liao, C.-L.; Zheng, B.-S.; Liu, J.-Z.; Ho, C.-L.; Hsieh, K.-C.; Wu, M.-C. Using Two-Step Mesa to Prevent the Effects of Sidewall Defects on the GaN p-i-n Diodes. *IEEE J. Quantum Electron.* **2015**, *51*, 1–6. [\[CrossRef\]](#)
48. Yang, Y.; Cao, X.A. Removing plasma-induced sidewall damage in GaN-based light-emitting diodes by annealing and wet chemical treatments. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* **2009**, *27*, 2337–2341. [\[CrossRef\]](#)
49. Krishna, D.V.; Panchal, A.; Sharma, E.; Dalal, S. Trench edge termination in a GaN-based power device. *Mater. Today Proc.* **2023**, *79*, 219–222. [\[CrossRef\]](#)

50. Théolier, L. *Conception de Transistor MOS Haute Tension (1200 Volts) Pour l'électronique de Puissance* Phdthesis; Université Paul Sabatier—Toulouse III: Toulouse, France, 2008.
51. Shiu, J.-Y.; Huang, J.-C.; Desmaris, V.; Chang, C.-T.; Lu, C.-Y.; Kumakura, K.; Makimoto, T.; Zirath, H.; Rorsman, N.; Chang, E.Y. Oxygen Ion Implantation Isolation Planar Process for AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* **2007**, *28*, 476–478. [[CrossRef](#)]
52. Maurya, V.; Alquier, D.; El Amrani, M.; Charles, M.; Buckley, J. Optimisation of Negative Fixed Charge Based Edge Termination for Vertical GaN Schottky Devices. *Micromachines* **2024**, *15*, 719. [[CrossRef](#)] [[PubMed](#)]
53. Ozbek, A.M.; Baliga, B.J. Planar Nearly Ideal Edge-Termination Technique for GaN Devices. *IEEE Electron Device Lett.* **2011**, *32*, 300–302. [[CrossRef](#)]
54. Ji, D.; Li, S.; Ercan, B.; Ren, C.; Chowdhury, S. Design and Fabrication of Ion-Implanted Moat Etch Termination Resulting in $0.7 \text{ m}\Omega \cdot \text{cm}^2/1500 \text{ V}$ GaN Diodes. *IEEE Electron Device Lett.* **2020**, *41*, 264–267. [[CrossRef](#)]
55. Liu, Y.; Yang, S.; Sheng, K. Design and Optimization of Vertical GaN PiN Diodes with Fluorine-Implanted Termination. *IEEE J. Electron Devices Soc.* **2020**, *8*, 241–250. [[CrossRef](#)]
56. Ohta, H.; Hayashi, K.; Horikiri, F.; Yoshino, M.; Nakamura, T.; Mishima, T. 5.0 kV breakdown-voltage vertical GaN p–n junction diodes. *Jpn. J. Appl. Phys.* **2018**, *57*, 04FG09. [[CrossRef](#)]
57. Fu, H.; Fu, K.; Alugubelli, S.R.; Cheng, C.-Y.; Huang, X.; Chen, H.; Yang, T.-H.; Yang, C.; Zhou, J.; Montes, J.; et al. High Voltage Vertical GaN p-n Diodes With Hydrogen-Plasma Based Guard Rings. *IEEE Electron Device Lett.* **2020**, *41*, 127–130. [[CrossRef](#)]
58. Guo, X.; Zhong, Y.; Zhou, Y.; Su, S.; Chen, X.; Yan, S.; Liu, J.; Sun, X.; Sun, Q.; Yang, H. Nitrogen-Implanted Guard Rings for 600-V Quasi-Vertical GaN-on-Si Schottky Barrier Diodes with a BFOM of $0.26 \text{ GW}/\text{cm}^2$. *IEEE Trans. Electron Devices* **2021**, *68*, 5682–5686. [[CrossRef](#)]
59. Wang, Y.; Porter, M.; Xiao, M.; Lu, A.; Yee, N.; Kravchenko, I.; Srijanto, B.; Cheng, K.; Wong, H.Y.; Zhang, Y. Implanted Guard Ring Edge Termination with Avalanche Capability for Vertical GaN Devices. *IEEE Trans. Electron Devices* **2024**, *71*, 1481–1487. [[CrossRef](#)]
60. Pu, T.; Younis, U.; Chiu, H.-C.; Xu, K.; Kuo, H.-C.; Liu, X. Review of Recent Progress on Vertical GaN-Based PN Diodes. *Nanoscale Res. Lett.* **2021**, *16*, 101. [[CrossRef](#)]
61. Cho, M.; Xu, Z.; Bakhtiary-Noodeh, M.; Detchprohm, T.; Daeumer, M.A.; Yoo, J.-H.; Shao, Q.; Laurence, T.A.; Key, D.; Hashimoto, T.; et al. 1.2-kV Vertical GaN PIN Rectifier with Ion-Implanted Floating Guard Rings. *IEEE Trans. Electron Devices* **2023**, *70*, 4578–4583. [[CrossRef](#)]

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