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A 12 dBm B1dB N-Path Notch Filter for Transmitter Leakage Suppression in Wideband Receiver

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Abstract: This paper proposes an N-path notch filter while offering high blocker power handling for co-address transmitter (TX) leakage suppression in a wideband receiver. The filter includes an impedance flip-flop over an adjustable transmission line in a block band, achieving a 12.3 to 13.6 dBm blocker 1 dB compression point (B1dB) and a 12.8 to 14 dBm 1 dB compression point (P1dB) in a 130 nm CMOS SOI process. This design effectively suppresses broadband interference in the receiving system and improves the dynamic range and linearity of the receiver (RX) channel. The filter consumes 186 to 242 mW in the 0.3 GHz to 0.6 GHz band and has an active chip area of 0.21 mm², providing maximum rejection >25 dB, with a passband third-order input intercept point (IIP3) of 22 to 25.2 dBm. The design of the adjustable transmission line structure is analyzed to reduce the insertion loss in terms of impedance and to achieve a 1.7 to 2 dB insertion loss shortfall over the RF tuning range.

Keywords: N-path filter; TX leakage; blocker; linearity; notch; impedance



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1. Introduction

As wireless communication rate technologies advance, the frequency bands supported by wireless devices have progressively expanded. In co-address transmitter (TX) and wideband receiver (RX) systems, TX leakage significantly compromises the dynamic range and sensitivity of the receiver channel. Traditional TX link front-end designs typically employ fixed-frequency filters, such as surface acoustic wave (SAW) and bulk acoustic wave (BAW) filters. However, the non-tunability of these filters necessitates an array of devices for multiband receivers, which increases system complexity.

In wireless transceiver systems, TX leakage levels reaching up to +12 dBm within an 800 kHz bandwidth can severely degrade receiver performance, as illustrated in Figure 1. This leakage imposes stringent requirements on receiver linearity and power handling. Furthermore, the reliance on multiple SAW filters in multiband radio systems adversely affects noise performance.

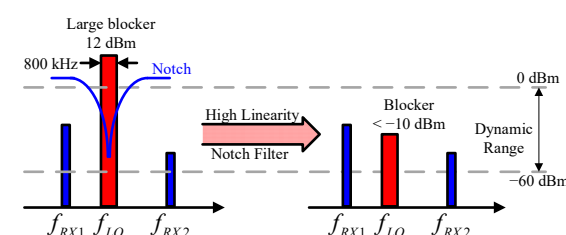


Figure 1. A large blocker causes saturation of the RX system and notch filter.

To overcome these limitations, tunable filters have emerged as a promising alternative to replace fixed-frequency filters. Filter solutions are categorized into conventional passive filters and active filters. Passive resonators can be implemented in traditional passive filter solutions in other ways, such as film bulk acoustic wave resonators (FBARs), which can achieve high-linearity filtering effects, but the frequency is not adjustable, limiting the range of filter use [1]. Passive filters are combined in the passive filter with other parts of the transceiver front end. The combination of the amplifier and the low-pass filter on the printed circuit board (PCB) achieves broadband filtering with precise impedance matching, resulting in a larger bandwidth and better fallback efficiency [2]. RF switches are combined with on-chip integrated transmission lines to reduce insertion loss, but the out-of-band rejection is not large enough to satisfy multiband communication selectivity requirements [3]. Active filters are in the spotlight because of their tunability and high level of integration. Various on-chip active filter technologies, including Q-enhanced, g_m -C, and N-path filters, have been explored. Q-enhanced filters offer high-Q narrowband filtering capabilities but face challenges with integration and frequency stability [4]. Active feedforward filtering mitigates TX leakage by downconverting the TX signal, applying low-pass filtering, and upconverting the signal. However, these systems are limited by the stringent requirements for phase and amplitude matching [5,6]. N-path filters have gained significant attention among tunable active filters due to their high Q-factor, tunability, low power consumption, and compact on-chip size. Despite their advantages, the linearity constraints of N-path filters remain a critical limitation for broader applications [7].

N-path filters provide a viable solution for developing SAW-less broadband multiband transceiver front-end systems. However, the linearity of these filters is fundamentally constrained by their design as switched-capacitor (SC) circuits composed of switches and capacitors [8,9]. As the amplitude of the input signal increases, strong nonlinear effects emerge in the N-path filter, compromising the sensitivity and potentially disrupting the functionality of the transceiver system. Large input signal voltage effects degrade the filter performance [7,10]. These effects collectively degrade the filter's ability to maintain high linearity under large signal conditions.

Researchers have proposed innovative designs to address these challenges and enhance the linearity of TX rejection band reject filters (BRF) [11]. One approach integrates an eight-phase bandpass filter with a BRF, allowing independent tuning to attenuate TX leakage as high as +10 dBm [12]. While this method significantly improves the BRF linearity, it limits the passband bandwidth, rendering it suitable primarily for narrowband reception applications. This trade-off underscores the ongoing challenge of achieving high linearity without compromising bandwidth in N-path filter designs.

This paper presents the design of a reconfigurable notch filter to suppress TX leakage in wireless transceiver systems. The proposed filter employs a hybrid architecture that combines an impedance-transformed shunt N-path filter with a series N-path BRF to mitigate TX leakage effectively. The proposed notch filter demonstrates a block compression point (B1dB) capable of achieving up to +12 dBm passband receiver linearity and notch block power. This performance significantly improves the isolation between transceiver channels, enhancing overall system linearity and mitigating interference. A detailed analysis explores the trade-offs between insertion loss, bandwidth, and linearity, providing valuable insights into the design optimization of reconfigurable notch filters for high-performance transceiver applications.

This paper is organized as follows: Section 2 derives the basic impedance characteristics of N-path filters. Section 3 shows the proposed N-path BRF architecture. Section 4 describes the complete circuit implementation structure. Section 5 gives the proposed filter's measurement results. The conclusion is given in Section 6.

2. Basic Design of N-Path Notch Filter

Figure 2a illustrates the fundamental operation of the N-path BRF, which consists of a high-pass filter connected in series with a switch. This configuration shifts the high-pass filtering characteristics to the local oscillator (LO) frequency, generating the desired notch response. The mechanism effectively extends the high-pass filter's utility to the target frequency band defined by the LO. Figure 2b shows that the N-path bandpass filter (BPF) operates with clock signals driven by a non-overlapping eight-phase clock waveform featuring a 12.5% duty cycle. The switching elements are modeled as ideal switches with a small series resistance, R_{SW} , representing the on-resistance. This design assumption simplifies the analysis and highlights the impact of switching behavior on the overall filter characteristics [13,14]. Figure 2b shows that the N-path BPF and its clock waveforms are driven by a non-overlapping clock with an eight-phase 12.5% duty cycle. The switch is considered an ideal switch with a small series resistance R_{SW} , which is the on-resistance.

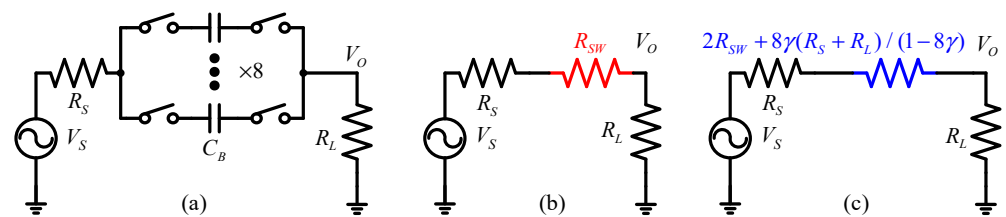


Figure 2. (a) Operation of N-path BRF. (b) f_{in} away from f_{LO} . (c) f_{in} equal to f_{LO} .

The input impedance of the system is defined as R_S . When a signal is applied, it passes through the series combination of the source resistance R_S and the switch on-resistance R_{SW} , with only one branch conducting at a time. Subsequently, the signal is connected in parallel with the eight ideal switches, as illustrated in Figure 3. Based on the derivation in other papers [15,16], the impedance equation for the N-channel band-stop filter can be obtained as:

$$Z_{in} = 2R_{SW} + R_L + (2R_{SW} + R_L + R_a) \frac{8\gamma}{1 - 8\gamma} // \gamma Z_{BB}(\omega - \omega_0) \quad (1)$$

where R_L is the load impedance, and $Z_{BB}(\omega - \omega_0)$ is the frequency-dependent base-band impedance.

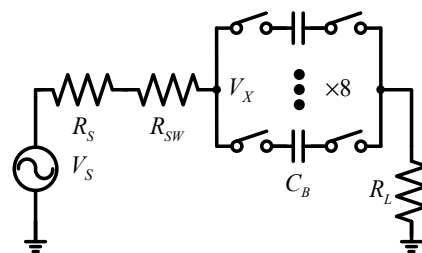


Figure 3. N-path filter with switched impedance equivalent modeling.

The conventional N-path BRF exhibits a large impedance at the center frequency of the notch, corresponding to low block linearity, while presenting matched impedance characteristics within the passband, as illustrated in Figure 4. Under identical input power conditions, the large impedance state at the center frequency produces a significant voltage amplitude across the signal. This elevated voltage amplitude is directly applied across the source and drain terminals of the N-path filter's switch. Consequently, this affects the V_{gs} of the MOS switch during both its on and off states, inducing nonlinearities in the filter's operation.

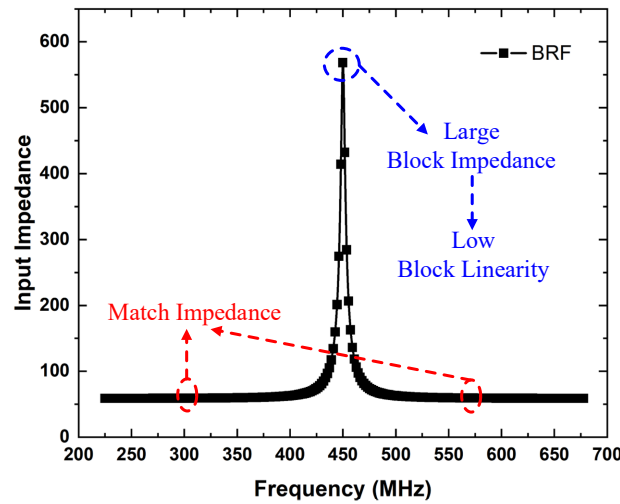


Figure 4. N-path BRF impedance characteristic curve at $f_{LO} = 450$ MHz.

3. Proposed N-Path Notch Filter Architecture

The circuit diagram of the proposed N-path BRF is presented in Figure 5. At any given moment, one of the eight paths is active, with the high level of the clock signal enabling the corresponding MOS switch, while the other paths remain inactive. The high-linearity notch filter is designed with a two-stage cascade structure. Stage I comprises an N-path BPF with quarter-wavelength impedance transformation, enabling the notch filter functionality. This stage establishes a low-resistance path to the ground within the blocking band, thereby enhancing linearity. Stage II utilizes a conventional N-path BRF to further increase the overall rejection depth of the system. The switches of the N-path filter are driven by an eight-phase clock signal with a 12.5% duty cycle, ensuring precise timing and operation of the filter stages.

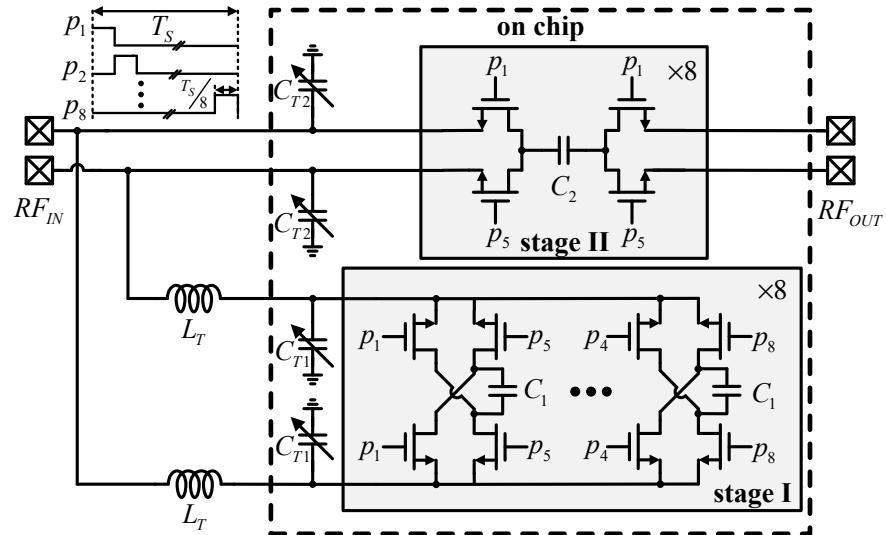


Figure 5. Schematic of the proposed N-path notch filter.

As illustrated in Figure 6, for SOI CMOS processes, the linearity of the N-path filter is constrained by the linearity of the MOS switches, which are designed to remain correctly on or off under clock control without accounting for switch-induced nonlinear distortion. With a 130 nm SOI CMOS process, the absolute value of V_{gs} must not exceed 2.5 V. For switches in the on state, the gate is subjected to a maximum voltage of $V_{DD} + V_B$, where a suitable DC bias V_B is applied to the source and drain of the switch. The maximum

positive swing of the input signal occurs when the on-state switch is critically closed and is given by:

$$V_{in,pos} = V_+ - V_B = V_{DD} - V_B - V_{TH}, \quad (2)$$

where V_{TH} is the threshold voltage of the MOS switch.

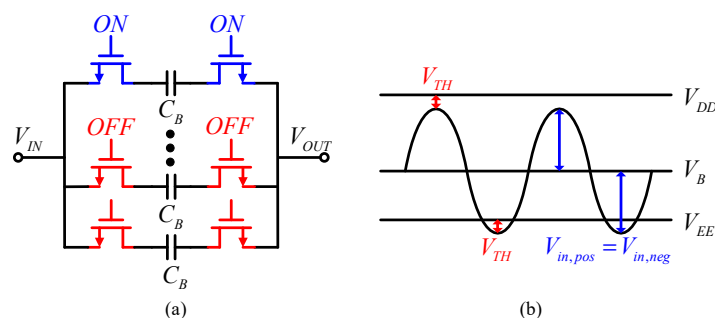


Figure 6. (a) N-path BRF schematic, (b) filter switch bias voltage.

Similarly, the maximum negative swing of the input signal occurs when the off-state switch is critically open and is given by:

$$V_{in,neg} = V_B - V_- = V_B - V_{EE} + V_{TH} \quad (3)$$

where V_{EE} represents the voltage when the clock output is '0', typically set to $V_{EE} = 0$. V_{EE} can be set to a negative voltage to improve linearity, as is further discussed in the subsequent sections. To ensure symmetrical voltage swings, the positive and negative swings should be equal, i.e., $V_{in,pos} = V_{in,neg}$. This condition leads to the equation:

$$V_B = \frac{V_{DD} + V_{EE} - 2V_{TH}}{2} \quad (4)$$

Thus, the maximum swing is as follows:

$$V_+ - V_B = \frac{V_{DD} - V_{EE}}{2} \quad (5)$$

the maximum blocking power of the circuit, without inducing significant nonlinearity, can be calculated as:

$$P_{in,max} = 10 \log \left[\frac{(V_{DD}/2)^2}{2R_{equ}} \right] \quad (6)$$

R_{equ} is the impedance of the filter input port at the blocking frequency.

An excessive input amplitude during the positive voltage half-cycle results in a variation in the switch-on impedance, thereby inducing nonlinear distortion in the switch when it is in the on state. The resistance of the switch exhibits a dependence on the input signal amplitude, as expressed in Equation (7) [17]. Conversely, during the negative voltage half-cycle, an excessively large input amplitude causes the switch-off impedance to decrease or, in some cases, leads to unintended switching behavior, where the switch erroneously turns on despite being in the off state. This phenomenon generates nonlinear distortion, which is primarily due to charge sharing between different paths.

$$R_{SW} = \frac{1}{\mu C \frac{W}{L} (V_{DD} - V_{in} - V_{TH})} \quad (7)$$

According to Equation (6), the maximum $P_{in,max}$ is obtained, with the ideal impedance characteristics of the band-stop filter, including low impedance in the stopband and

matched impedance in the passband; this is achieved by the impedance transformation of the quarter-wavelength transmission line. As with the impedance characteristics of the N-path BRF, the input impedance $Z_{in,sh}$ of the N-path BPF is given by Equation (8). Stage I of the filter exhibits a matched impedance within the passband and a low impedance within the stopband, for a single-ended eight-path bandpass filter $\gamma = \frac{8}{\pi^2} \sin^2 \frac{\pi}{8} \approx 0.1187$.

$$Z_{in,sh}(\omega) = R_{SW} + \left[(R_{SW} + R_S) \frac{8\gamma}{1 - 8\gamma} \right] // \gamma Z_{BB}(\omega - \omega_0) \quad (8)$$

The N-path BPF undergoes impedance transformation via a quarter-wavelength transmission line with an appropriately selected impedance, resulting in an impedance flip [18]. This transformation converts the input impedance from a matched impedance to a low impedance at the center frequency and from low impedance to a matched impedance as the frequency deviates from the center, as described in Equation (9):

$$\tilde{Z}_{in,sh}(\omega) = \frac{Z_0^2}{R_{SW} + \left[(R_{SW} + R_S) \frac{8\gamma}{1 - 8\gamma} \right] // \gamma Z_{BB}(\omega - \omega_0)} \quad (9)$$

The transformed input impedance Equation (9) is substituted into Equation (6), obtaining a notch filter with high blocking power.

Quarter-wavelength transmission lines are characterized by specific frequencies and impedance values. In the RF range of this design, the size of the on-chip quarter-wavelength transmission line is too large to be implemented, and it can be equated by the structure of CLC, as shown in Figure 7a, and the structure of LCL, as shown in Figure 7b.

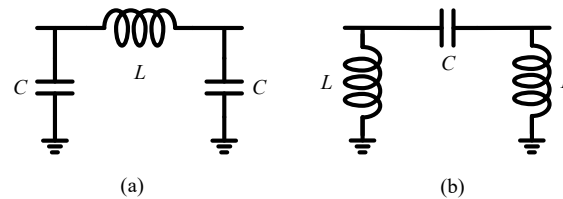


Figure 7. (a) CLC equivalent structure; (b) LCL equivalent structure.

The CLC structure equivalent to a quarter-wavelength transmission line used the least amount of inductor. The CLC structure quarter-wavelength transmission lines' specific frequencies were set to $f = 450$ MHz, and the transmission lines' specific impedances were set to $Z_{line} = 25 \Omega$. The inductance and capacitance parameters in their CLC equivalent structure are calculated by Equations (10) and (11), $L = 8.84$ nH, $C = 14.15$ pF.

$$L = \frac{Z_{line}}{2\pi f} \quad (10)$$

$$C = \frac{1}{2\pi f Z_{line}} \quad (11)$$

At this point the impedance characteristics of the notch filter can be rewritten as Equation (12), where Q_L is the Q value of the inductor in the CLC structure.

$$Z_{in,sh}(\omega) = \left[\left(R_{SW} + \left[(R_{SW} + R_S) \frac{8\gamma}{1 - 8\gamma} \right] // \gamma Z_{BB}(\omega - \omega_0) \right) \right] \left\| \frac{1}{j\omega C_{T1}} + j\omega L + \frac{\omega L}{Q_L} \right\| \left\| \frac{1}{j\omega C_{T2}} \right. \quad (12)$$

The quality factor of the inductor affects the impedance characteristics of the filter after it has been transformed by the CLC structure. First, for the reject band impedance, the base-band capacitor impedance $Z_{BB}(\omega - \omega_0)$ is approximately equal to the load impedance Z_B ,

and the reject impedance can be expressed as Equation (14). Next, the analyzed passband impedance can be expressed as Equation (15). From here, the resistance introduced by the finite inductor Q factor can actually be corrected by an increase in C_{T1} or a decrease in C_{T2} . Therefore, the quality factor does not limit the impedance of the filter's reject band or the linearity. However, this adjustment leads to a shift in the transmission line's characteristic frequency toward higher frequency.

$$Z_B \approx R_S \quad (13)$$

$$Z_{in,reject}(\omega) = \left[\left(R_{SW} + (R_{SW} + R_S) \frac{8\gamma}{1-8\gamma} \parallel \gamma Z_B \right) \parallel \frac{1}{j\omega C_{T1}} + j\omega L + \frac{\omega L}{Q_L} \right] \parallel \frac{1}{j\omega C_{T2}} \quad (14)$$

$$Z_{in,pass}(\omega) \approx \left(R_{SW} \parallel \frac{1}{j\omega C_{T1}} + j\omega L + \frac{\omega L}{Q_L} \right) \parallel \frac{1}{j\omega C_{T2}} \quad (15)$$

The simulation of the CLC uses an ideal inductor versus finite quality factor inductor equivalent structure with an ideal quarter-wavelength transmission line; the adjusted CLC structure is shown in Figure 8a, where it can be concluded that the CLC structure is approximately equivalent to a quarter-wavelength transmission line in 0 to 600 MHz, and equivalent deterioration of the impedance transformation at the band edges leads to an additional differential loss shortfall and poor equivalence at high frequencies due to its low-pass filtering characteristics. The adjusted CLC structure can correct the equivalent situation of the CLC structure, sacrifice low-frequency differential loss, and reduce high-frequency insertion loss substantially by affecting the capacitance on the low-impedance side, making an adjustable balance between low-frequency and high-frequency insertion loss. At the same time, the quality factor of the inductor affects the transmission line loss, which is reflected in the additional insertion loss of the filter, as shown in Figure 8b; as the Q value of the inductor decreases, the overall differential loss of the filter increases, and the characteristic frequency of the transmission line moves to lower frequency, resulting in asymmetry of the insertion loss on both sides of the operated frequency band, which requires a continued increase in C_{T1} and decrease in C_{T2} . The off-chip inductor with the appropriate quality factor is selected in forming a balance between size and differential loss. In this design, the value of the inductor Q factor is chosen to be 80.

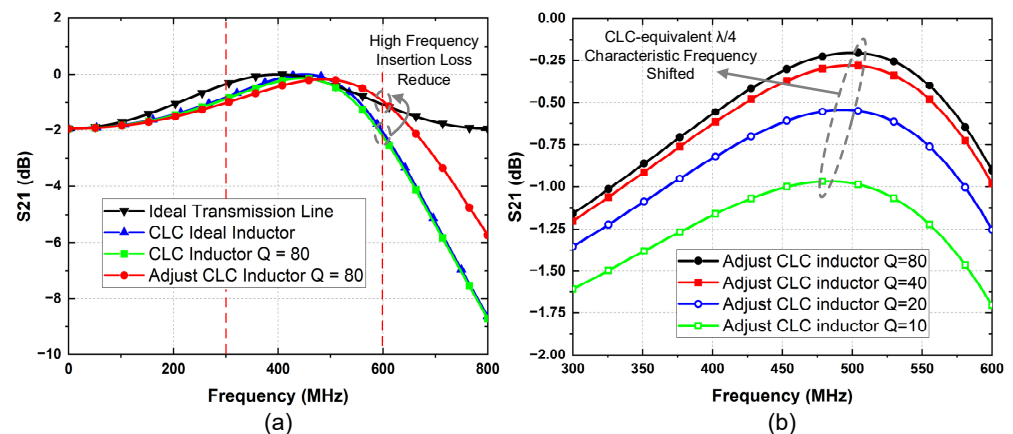


Figure 8. (a) The CLC structure Q factor influences inductors and adjusts the CLC structure. (b) Effect of different Q factors of inductor.

In this design, the RF range of 300 to 600 MHz, the transmission line's bandwidth influences the impedance conversion's effectiveness, particularly at the band's edges, where the conversion becomes less efficient. As the bandwidth increases, the insertion loss shortfall also becomes more significant. This impedance mismatch results in an increased insertion loss of the filter. To mitigate this issue, an adjustable transmission

line structure can be employed to compensate for the resulting shortfall in insertion loss. As shown in Figure 9, without modulating the transmission line structure, for the $C_{T1} = C_{T2}$ curve in the figure, the parasitic capacitance on the Stage II side is larger due to the parasitic factor, resulting in the $C_{T1} < C_{T2}$ curve in the corresponding figure; in this case, the insert shortfall at the edge of the filter band grows greater than 2 dB, and the filter loss increases. By adjusting the equivalent structure of the transmission line, it is possible to achieve the $C_{T1} > C_{T2}$ curve in the figure, where the insert shortfall at the edge of the filter band grows less than 0.3 dB. The proposed filter utilizes a matching impedance of 25Ω , which minimizes insertion loss at the lower transmission line impedances and increases insertion loss at the higher impedances. The overall insertion loss is influenced by parasitic capacitances inherent to the chip and the bandwidth of the transmission line. By appropriately adjusting the values of C_{T1} and C_{T2} , the insertion loss is effectively reduced.

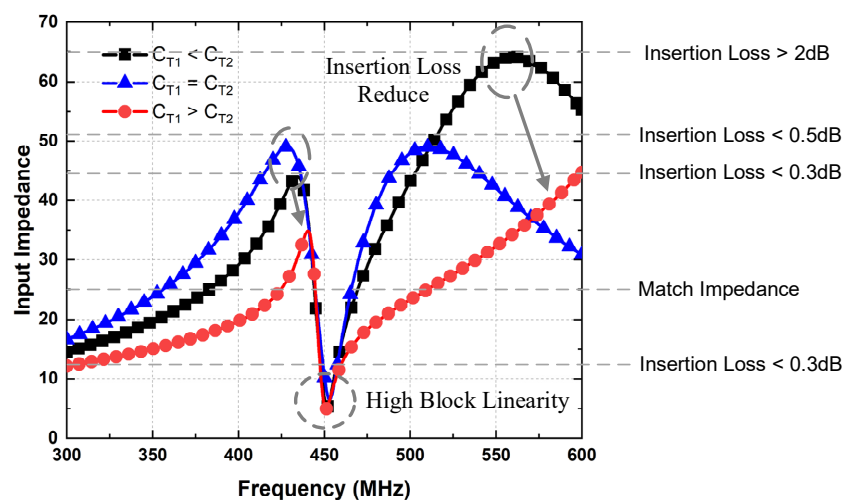


Figure 9. Inverted impedance curve of proposed notch filter at $f_{LO} = 450$ MHz.

4. Circuit Implementation

The schematic for the proposed filter is depicted in Figure 5. It features an eight-path notch filter with an in-band impedance flip-flop, driven by an eight-phase 12.5% duty cycle clock to achieve high linearity in blocker power rejection. High blocker power suppression is facilitated by a quarter-wavelength transmission line, which, combined with an N-path BPF in Stage I and an N-path BRF in Stage II, ensures a high rejection depth. Off-chip LC equivalents are utilized for the quarter-wavelength transmission lines to minimize chip area. The filter architecture includes an eight-path N-path BPF, an eight-path N-path BRF, two off-chip LC equivalent models, and an eight-phase 12.5% duty cycle clock generator.

4.1. N-Path Filter Architecture of Stage I and Stage II

A detailed schematic is presented in Figure 5. Within the BPF, off-chip quarter-wavelength transmission line transformation is employed, with the resultant impedance affecting both the blocking power and the depth of band rejection. All filter capacitance is realized using MIM capacitors. The N-path BPF and BRF switches utilize NMOS transistors with a low threshold voltage and a 2.5 V drain and source breakdown voltage to achieve high linearity. The rejection depth is enhanced by minimizing parasitic resistance in the switch and capacitor RF lines [18]. After conversion, the impedance in the blocking band is reduced to improve blocking linearity. Parasitic resistance in the switches also impacts the filter's insertion loss. The N-path filter's switch size W/L is equal to $240 \mu\text{m}/220 \text{ nm}$ and achieves an on-resistance of approximately 4Ω , which reduces passband insertion loss and

enhances notch rejection. The NMOS drain and source are biased with a 0.5 V voltage to optimize linearity.

4.2. Eight-Phase 12.5% Duty Cycle Clock Generator

The eight-phase 12.5% duty cycle clock generator schematic is shown in Figure 10. A single-ended sinusoidal clock input clock balun with $4 \times f_{LO}$ inputs is used to generate a symmetrical differential clock, LO+ and LO−. The clock balun is realized by a same-size inverter with a transmission gate that compensates for delays to minimize differential signal phase errors. The divide-by-four ring counter circuit, composed of D flip-flops, generates eight phase-shifted signals, each with a 50% duty cycle and a 12.5% phase shift between successive paths. The eight-phase, 12.5% duty cycle clock is derived from eight NAND gates [19]. Preceding the eight-phase clock, a duty cycle calibration module and a buffer circuit ensure accurate signal generation. The large filter switch size leads to larger output buffer size and increased clock dynamic power consumption.

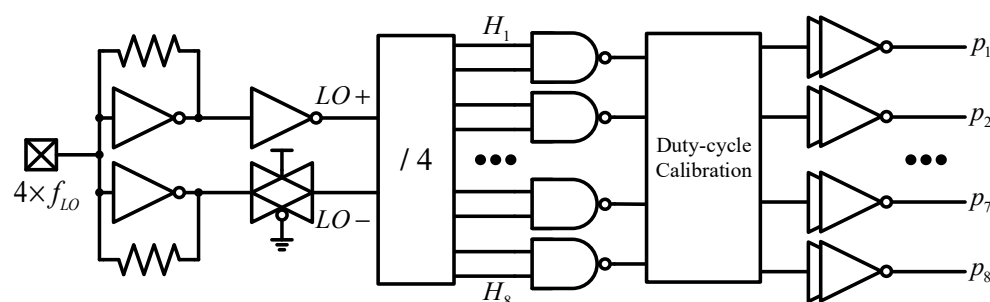


Figure 10. The schematic of the clock generator.

4.2.1. Divider

The divide-by-four ring counter uses a D flip-flop, as shown in Figure 11. The divide-by-four on the input signal $4 \times f_{LO}$ quadrature generates a frequency of f_{LO} and a 50% duty cycle signal; after eight D flip-flops, it generates an eight-phase 45° phase-shifted, 50% duty cycle from the intermediate signal. The D flip-flop consists of a differential clock-controlled transmission gate in series with an inverter to achieve the highest inversion speeds, in which the size of NMOS is $5 \mu\text{m}/120 \text{ nm}$, and the size of PMOS is $10 \mu\text{m}/120 \text{ nm}$. The eight-phase signal becomes eight NAND to generate an eight-phase, 45° phase-shifted, 12.5% duty cycle from the clock signals. Normally, adding an intermediate dummy d flip-flop is necessary to balance the phase error; clock phase differences affect the differential loss of filters.

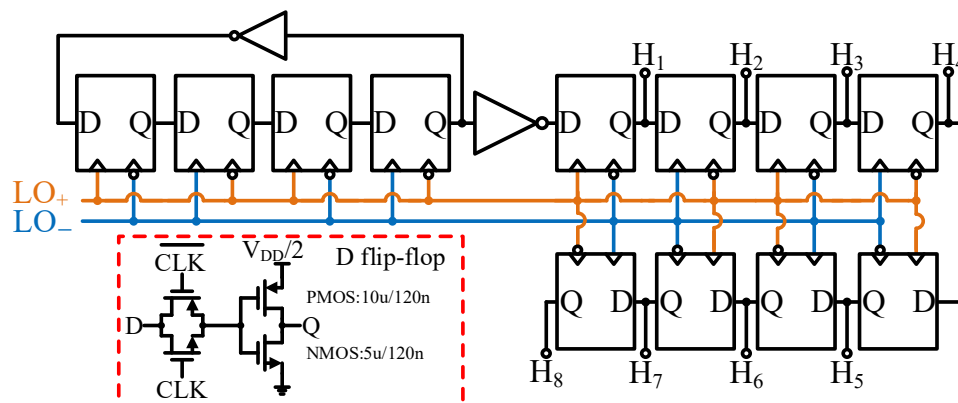


Figure 11. The divide-by-four ring counter circuit.

4.2.2. NAND and Duty Cycle Calibration

The NAND circuit is shown in Figure 12. In the NAND combination of two sets of crossed inverters, the size of NMOS is $5\ \mu\text{m}/120\ \text{nm}$ and the size of PMOS is $10\ \mu\text{m}/120\ \text{nm}$. Controlling the body voltage $V_{b\text{dn}}$ of NMOS and $V_{b\text{dp}}$ of PMOS in NAND adjusts the duty cycle of the output clock. The ideal clock duty cycle for an eight-path filter is 12.5%. A duty cycle that is too large can lead to filter aliasing; a duty cycle that is too small can lead to increased filter loss. The clock duty cycle is also adjusted by adjusting the bias voltage at the body end of the NMOS and PMOS in the duty cycle calibration circuit.

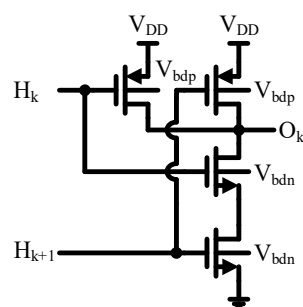


Figure 12. The NAND circuit.

4.3. Off-Chip LC Equivalent Model

In the frequency range of 300 to 600 MHz, the RF signal wavelength varies from approximately 1 m to 0.5 m. As a result, the size of the quarter-wavelength transmission line becomes impractically large, contributing significantly to both the design cost and chip area. To address this challenge, the simplest approach involves using off-chip lumped LC equivalents. For this purpose, a CLC network incorporating a single inductor is employed. Specifically, considering the inductive effect of bonding wires, an 8 nH wire-wound ceramic chip inductor with a Q factor of 80 is chosen to minimize passband loss. The inductance value is adjusted to modulate the transmission line's eigenfrequency, while the capacitances C_{T1} and C_{T2} in the CLC network are controlled on-chip through multiplier capacitor arrays. To achieve the desired filter performance, these capacitors have values ranging from 1 to 63 pF, adjustable in 1 pF steps.

5. Measurement Results

A high-linearity N-path notch filter is implemented using a 130 nm RFSOI process, and the die micrograph is depicted in Figure 13. The total chip area is $2.4 \times 2.4\ \text{mm}^2$, with the active filter area occupying $0.25\ \text{mm}^2$. To achieve the differential structure, two off-chip 1:1 balun (mini-circuits TC1-1-13MG2+) are used at the RF input and output ports. The chip is mounted in a QFN 40 package and tested on a PCB. Losses due to cables and PCB signal traces are de-embedded during measurement to ensure accurate results. The power consumption is measured to range from 186 to 242 mW within the 300 to 600 MHz RF range under a 12 dBm high TX blocker. The primary power consumption is attributed to the buffer, which drives large switches with an eight-phase nonoverlap 12.5% duty cycle clock.

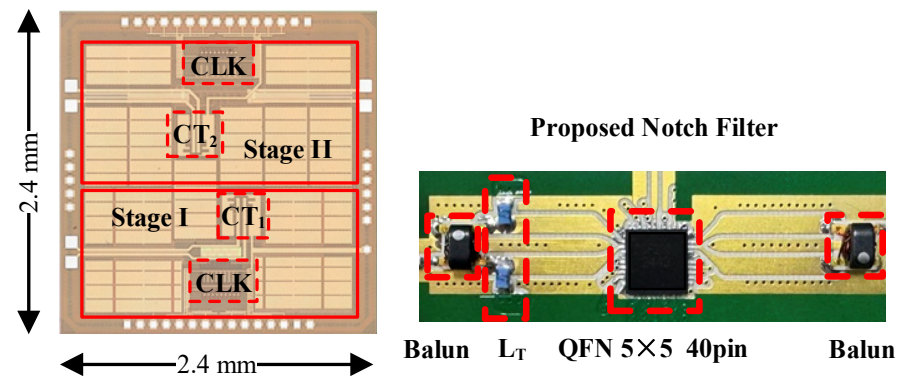


Figure 13. Chip micrograph and assembled board of the notch filter with CLC inductor L_T .

5.1. S-Parameters

The measured S_{21} of the proposed notch filter across the RF tuning range is shown in Figure 14a. To minimize the loss of receiver channel bandwidth, the 3 dB passband bandwidth of the proposed notch filter ranges from 3.5 to 4 MHz across the RF tuning range. The details of the measured and simulation results at $f_{LO} = 450$ MHz are provided in Figure 14b. For a QAM64 signal with a baseband bandwidth of 800 kHz, the filters achieve a rejection greater than 20 dB over the entire frequency range and zoom in through the details, with a maximum rejection exceeding 25 dB.

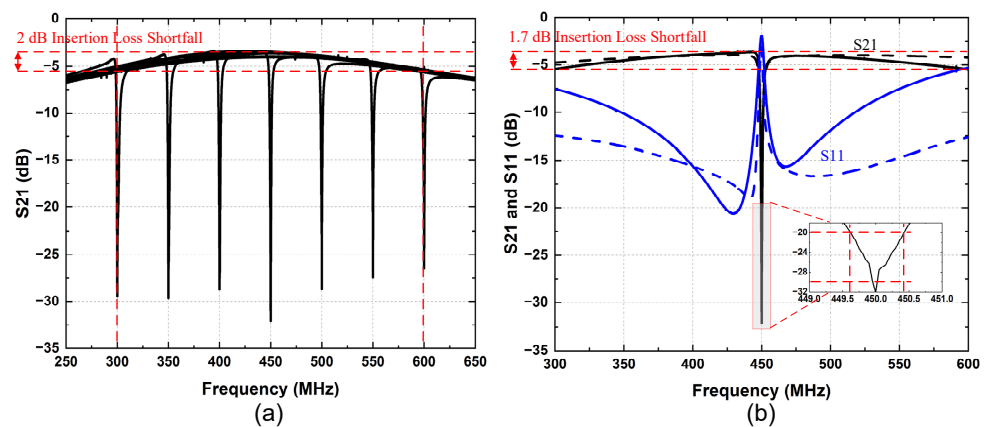


Figure 14. (a) Measured S_{21} of the proposed notch filter across the RF tuning range; (b) measured S_{21} and S_{11} at $f_{LO} = 450$ MHz. Some variations between measurements (solid) and simulations (dashed) were observed.

The frequency corresponding to the quarter-wavelength transmission line characteristic impedance is about 450 MHz to equalize the performance over the entire frequency band. The passband differential loss at the edge of the band increases by 2 dB due to the variation in the transmission line wavelength, which a more complex LC structure can reduce. However, it also requires the use of more off-chip inductance. The insertion loss shortfall reduces from 3.8 dB to 2 dB across 300 MHz to 600 MHz via adjustable C_{T1} and C_{T2} . The filter insertion loss is 3.6 to 5.4 dB at $f_{LO} = 450$ MHz with a 1.8 dB insertion loss shortfall. This insertion loss is acceptable for multiple SAW filters in a switched array configuration, as shown in Figure 14b.

5.2. Linearity and NF

A single tone at f_{LO} is used to measure B1dB. A single tone at $f_{LO} + 20$ MHz is used to measure P1dB in the passband. The third-order input-intercept-point (IIP3) profile is measured by injecting two-tone tests with a frequency at $f_{LO} + 20$ MHz and $f_{LO} + 21$ MHz.

The large block signal causes compression of the desired signal. The measured blocker B1dB is 12.3 to 13.6 dBm. The measured P1dB is 12.8 to 14 dB, and the IIP3 ranges between 22.3 and 25.2 dBm across the tuning range, as shown in Figure 15.

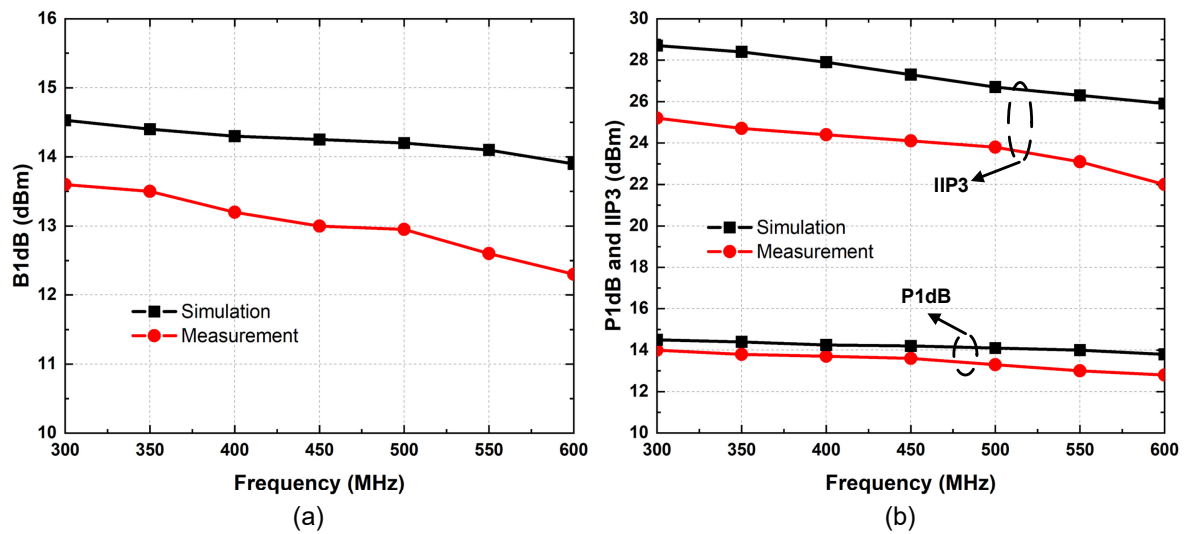


Figure 15. (a) Measured and simulation B1dB across the RF tuning range; (b) measured and simulation P1dB and IIP3 across the RF tuning range.

Figure 16a shows rejection for a bandwidth of 800 kHz versus block power at $f_{LO} = 450$ MHz. The notch depth was degraded by 1 dB for a 12 dBm block power, and the filter maintained >20 dB of rejection for a bandwidth of 800 kHz. In the RF tuning range, the min NF is 3.58 dB to 4.78 dB, as shown in Figure 16b. The NF at 600 MHz goes up by 1.2 dB. The blocker noise figure (BNF) is measured in the presence of a TX signal located at $f_{LO} = 450$ MHz and is plotted in Figure 17. The NF increases to around 9 dB with a 12 dBm TX leakage.

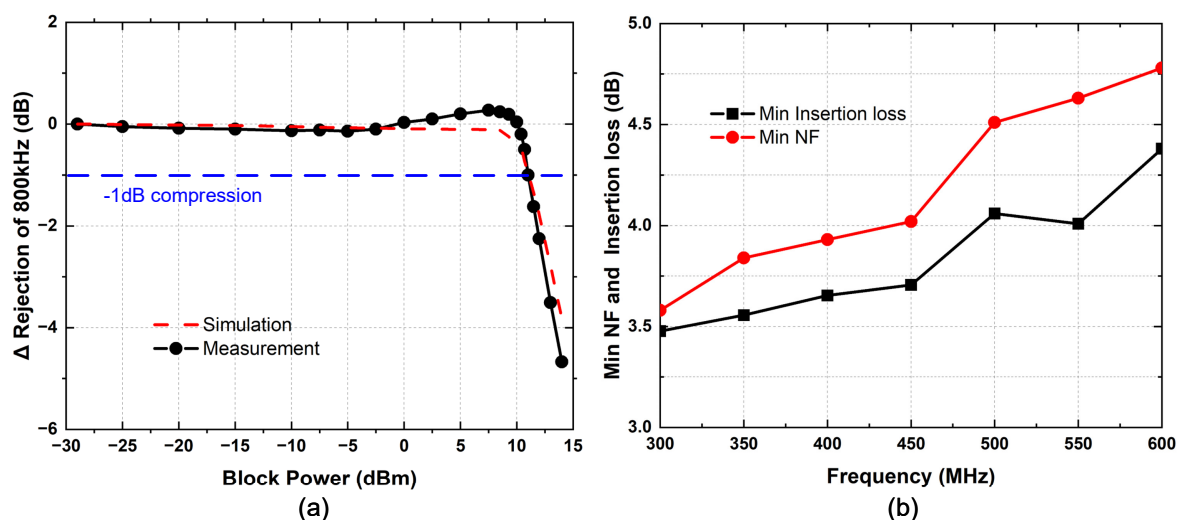


Figure 16. (a) Rejection versus block power at $f_{LO} = 450$ MHz; (b) measured min NF across RF tuning range.

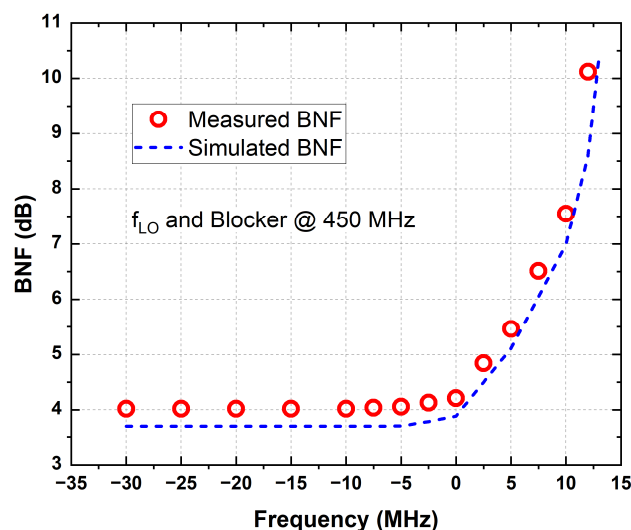


Figure 17. Measured and simulated BNF with a blocker located at 450 MHz.

Table 1 summarizes the power consumption at different frequencies when the proposed notch filter is tuned from 0.3 to 0.6 GHz. With a 12 dBm TX leakage, the clock power consumption is 186 to 242 mW over the tuning range. Table 1 shows that the switch buffers mainly consume power, which drives the large switches with eight-phase nonoverlap 12.5% duty cycle clocks. The buffer power consumption is proportional to the switch size, with smaller switch sizes leading to lower insertion loss.

Table 1. Power consumption table with 12 dBm TX leakage.

With 12 dBm TX Leakage	Frequency = 0.3 GHz	Frequency = 0.6 GHz
Clock Balun	7.2	9.1
Divider	5.1	8.5
NANDs and Duty Cycle Calibration	26.5	28.6
Buffers	147.2	195.8
Total	186	242

Table 2 summarizes the performance of the proposed notch filter and compares the measured results with state-of-the-art N-path-based passive notch filters. The filter linearity and maximum rejection are substantially improved compared to the conventional LNA shunt notch structure [19]. Compared to the N-path bandpass filter with a series notch architecture presented in [12], the proposed filter demonstrates advantages in both B1dB and P1dB, while also meeting the requirements of wideband receivers and reducing power consumption simultaneously. Compared with [20,21], the proposed filter exhibits improved B1dB and P1dB. It is comparable to that in [22] in terms of noise and rejection performance, but with a large improvement in passband IIP3. Furthermore, compared to the design in [16], which utilizes an N-path inverted shunt notch architecture, the proposed filter incorporates an adjustable transmission line structure. This design effectively reduces insertion loss by optimizing impedance and achieves a smaller insertion loss shortfall across the RF tuning range.

Table 2. Performance summary and comparison.

Reference	[19]	[20]	[21]	[22]	[12]	[16]	This Work
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	45 nm SOI	45 nm SOI	130 nm SOI
Topology	N-path LNA + Shunt Notch	N-path Neg. Trans-Res. Notch	LNTA + Dual-Band LC Notch	CS-LNA BPF+ FF Blocker Cancelling Notch	N-path BPF + Series Notch	N-path Inv. Shunt Notch	N-path Adjustable Inv. Shunt Notch + Series Notch
RF Range/GHz	1 to 1.6	0.2 to 1	0.7 to 2.2	1.35 to 2.7	0.2 to 3.6	0.9 to 1.1	0.3 to 0.6
BW/MHz	N/A	28 (20 dB BW)	N/A	>48	>80	12 to 25 (3 dB BW)	3.5 to 4 (3 dB BW) 0.8 (20 dB BW)
B1dB/dBm	−10 #	5 to 7	−18 to −6 #	>7.5	10 #	N/A	12.3 to 13.6
P1dB/dBm	N/A	N/A	>−40	N/A	4 #	>−10	12.8 to 14
IB IIP3/dBm	N/A	17 to 21.5	−14.5	4.8 to 5.8	22	22.6 *	22 to 25.2
Insertion Loss Shortfall/dB	<1 #	>4 #	>3 #	N/A	2 #	>3 #	1.7 to 2
DSB NF/dB	5	1 to 4	3.5 to 4.4	4.4 to 4.6	2.8 to 4.5	4 to 5	3.58 to 4.78
Max Rejection/dB	19	>50	>25	>23.8	41	23	27 to 32
Power Con./mW	30	17 to 21.5	11.7	21.2	183.3 to 303.5 ‡	6.18	186 to 242

* This chip works in N-Path mode. # Estimate from figure. ‡ With 9 dBm TX blocker.

6. Conclusions

This paper presents a blocker N-path notch filter for TX leakage suppression in a wideband receiver. The transmission line achieves an impedance flip within the block band to improve the linearity of blocker suppression. The adjustable CLC transmission line minimizes insertion loss shortfall in the tuning range. The filter achieves >25 dB rejection for a 12.3 to 13.6 dBm TX leakage blocker and 12.8 to 14 dBm P1dB. At the same time, the passband IIP3 of up to 22 to 25.2 dBm is realized, maximizing the dynamic range of the receiving channel. The design of the adjustable transmission line structure is analyzed to reduce the insertion loss in terms of impedance and to achieve 1.7 to 2 dB insertion loss shortfall over 300 to 600 MHz. Due to its high linearity, the TX leakage can be effectively filtered out in the front end of a broadband receiver, improving the receiver sensitivity.

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Abbreviations

The following abbreviations are used in this manuscript:

TX	Transmitter
RX	Receiver
B1dB	Blocker 1 dB compression point
P1dB	1 dB compression point
IIP3	Third-order input intercept point
SAW	Surface acoustic wave
BAW	Bulk acoustic wave
SC	Switched capacitor
BRF	Band reject filters
BPF	Bandpass filter
LO	Local oscillator
V _{gs}	Gate-to-source voltage
PCB	Printed circuit board
NF	Noise figure
BNF	Blocker noise figure

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