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A Design of High-Precision and Low-Noise High-Current Power Amplifier

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Abstract

Addressing the limitations of existing power amplifiers, particularly in terms of accuracy and noise performance, a high-voltage and high-current power amplifier has been developed. The input stage utilizes a rail-to-rail circuit structure, allowing the amplifier to deal with the full swing of input signals from the negative to the positive power supply. The output stage features an innovative class AB configuration with a bias structure, effectively reducing the crossover distortion typically associated with traditional circuits. This design improves linearity, achieving an output range that extends to the rails, while also enhancing the power supply rejection ratio and optimizing noise performance. Furthermore, over-temperature protection and current limiting circuits have been integrated to safeguard the system against permanent damage under extreme conditions. The power amplifier circuit was simulated and validated using Cadence 61 Spectre software. With a power supply of $\pm$30 V, the amplifier achieved an output current of 560 mA, a low-frequency gain of 138 dB, a bandwidth of 24 MHz, and a noise level of 4.8 nV/$\sqrt{\text{Hz}}$. The slew rate was measured at 14.2 V/µs. Compared to existing literature, significant advancements have been achieved in terms of gain, bandwidth, and noise performance.

Keywords: high current; power amplifier; rail-to-rail; class AB

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1. Introduction

In the field of operational amplifier chip design within China, research hotspots have primarily focused on Radio Frequency power amplifiers [1], audio power amplifiers [2,3], and general-purpose amplifiers [4], with relatively limited exploration into high-voltage, high-current output power amplifiers. Traditional operational amplifiers face limitations when driving high-voltage loads, while discrete component solutions suffer from bulky size and low energy efficiency. Integrated high-voltage, high-power amplifiers effectively resolve the technical challenges of traditional solutions in high-voltage, high-power driving. These chips feature high output voltage swing and large current output capability, enabling direct driving of high-impedance or high-power loads. This makes them highly valuable for critical applications in industrial control, automotive electronics, and other key fields [5]. To ensure operational reliability under complex conditions, these chips typically incorporate protection mechanisms like overload and overheat protection, further enhancing their suitability for industrial environments.

In the design of high-current power amplifiers, high output current and fast slew rate have been primary research focuses. Reference [6] employs a common-source gain stage with a constant current source load to increase circuit gain, while utilizing a Class

B push-pull common-drain amplifier to achieve high slew rate. Reference [7] employs P-channel Junction Field-Effect transistors as input differential pairs. The intermediate gain stage consists of a common-emitter configuration centered around a Darlington NPN transistor and a composite Darlington structure for the output stage. This structure achieves high output current and high conversion rates. Reference [8] utilizes a fully differential topology with source-driven common-base amplification. Achieve a balance between conversion rate, bias current, and noise. Although these power amplifiers demonstrate clear advantages in output current and slew rate, they simultaneously suffer from insufficient precision and elevated noise levels. Consequently, they are unsuitable for high-precision, low-noise applications.

Addressing these limitations, this paper proposes a high-precision, low-noise high-current power amplifier. The amplifier's input stage employs a rail-to-rail differential input structure. The output stage employs a Class AB configuration. Through an optimized floating current source structure, combined with a transconductance linear loop to provide bias for the output stage. This enhances the linearity and gain stability of the output stage. Additionally, protection circuits are incorporated to boost overall system stability and reliability. This power amplifier combines high-voltage, high-current output capability with high precision and low noise performance, demonstrating significant advantages in applications such as industrial inspection and medical equipment.

2. Circuit Design and Implementation

2.1. Overall Circuit Structure

This paper presents the design of a high-voltage, high-output current power amplifier utilizing high-voltage technology. The schematic diagram of the entire circuit is illustrated in Figure 1, encompassing the amplifier's core circuit module, over-temperature indication and shutdown module, as well as the current-limiting protection module. The amplifier comprises a rail-to-rail input stage and a high-current output stage, with bias circuitry supplying the drive current. Within the diagram, VIP and VIN denote input signal ports, OUT represents the output port, and the FLAG terminal serves as the over-temperature indication port.

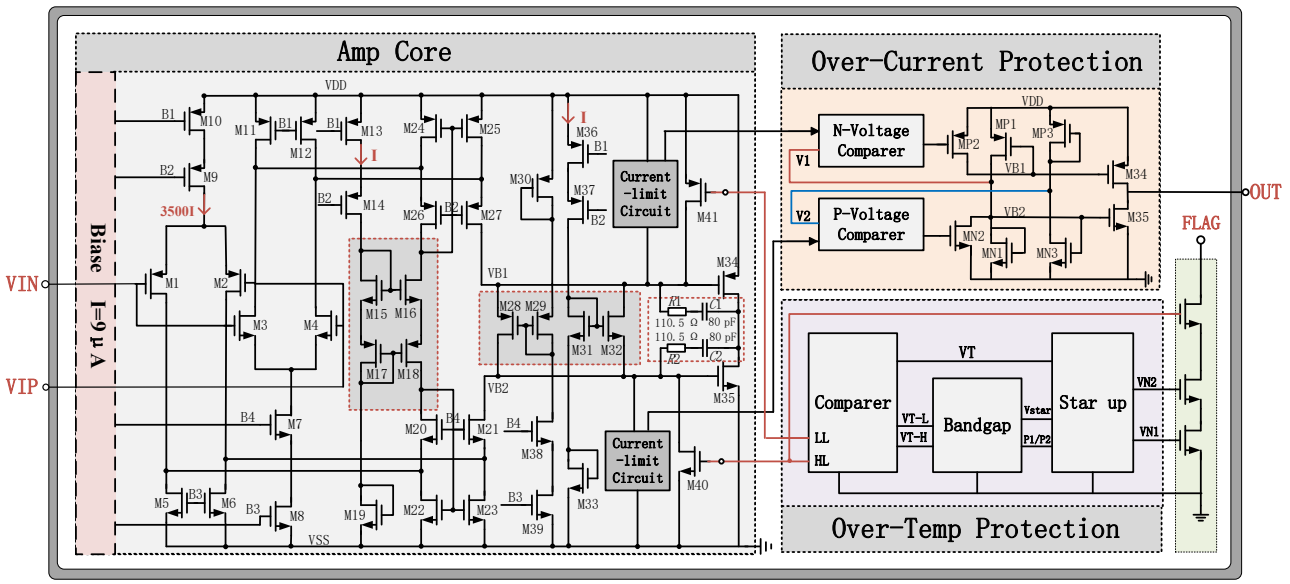


Figure 1. Overall circuit diagram.

2.2. Core Amplifier Circuit

2.2.1. Circuit Structure Design

The amplifier's core circuit consists of a bias network, input stage, and output stage. To ensure voltage withstand capability, the entire amplifier section employs Laterally Diffused Metal-Oxide-Semiconductor (LDMOS) transistors with 75 V drain-source breakdown voltage. This enables it to operate normally at supply voltages of 30 V and below. The dual-ended input-single-ended output two-stage power operational amplifier designed in this paper is shown in Figure 1.

Figure 1 shows a bias circuit employing a wide-swing cascode current mirror bias structure. This configuration effectively suppresses channel length modulation effects while precisely replicating the reference current to deliver stable bias voltage [9,10]. The input stage utilizes a rail-to-rail folded common-source common-gate amplifier circuit [11,12]. M1–M4 form a differential input pair consisting of one N-channel Metal-Oxide-Semiconductor Field-Effect Transistor(NMOS) and one N-channel Metal-Oxide-Semiconductor Field-Effect Transistor(PMOS) transistor connected in parallel. The rail-to-rail structure provides a wider common-mode input range. When the input voltage approaches the positive supply rail, the NMOS input transistor conducts. When the input voltage approaches the negative supply rail, the PMOS input transistor conducts. Under other voltage conditions, both pairs operate simultaneously. To achieve low-noise performance, the input transistor dimensions follow low-noise amplifier design principles, employing a large width-to-length ratio (shown in Table 1) to optimize noise characteristics. Intermediate transistors M20–M27 form a cascode structure, providing high output impedance and achieving a large open-loop gain.

Table 1. Key MOSFET parameters.

Tube	W/L	Tube	W/L
M1/M2	16×10^3	M3/M4	9.6×10^3
M27	720	M25	700
M21	320	M23	230

The output stage employs a Class AB push-pull configuration [13,14]. Class B output stages can achieve large swing with low quiescent current but exhibit significant crossover distortion [15]. Class A output stages eliminate crossover distortion but operate at lower efficiency. Class AB output stages offer a superior compromise. It achieves a large output swing by enabling the output to swing to VDD $-$ V_{DSsat} and VSS + V_{DSsat} through a combination of PMOS and NMOS transistors. Output power transistors M34 and M35 provide bidirectional current output capability. When biased at relatively low quiescent currents, they effectively reduce crossover distortion, making their biasing critical.

This paper proposes an optimized bias structure. An optimized floating current source is combined with a transconductance linear loop to jointly bias the output stage. Compared to traditional floating voltage source bias structures, this approach provides more stable bias for the output stage's quiescent current. While conventional floating current sources act directly on the output stage, this paper positions the floating current source before the Cascode cascade. This arrangement stabilizes the intermediate stage's quiescent operating point while establishing a defined DC operating point at the output stage's input.

In Figure 1, transistors M15–M18 form the floating current source, delivering a constant bias current to the output stage. The drain voltages of M16 and M18 can track the gate voltages of M34 and M35, preventing a drop in V_{DS} (drain-source voltage) due to variations in the output transistor gates. This prevents M16 and M18 from entering the linear region and failing to provide a constant current. However, a standalone floating cur-

rent source cannot precisely control the static current of the output power transistors. The transconductance feedback loop enables precise current proportionality control through voltage relationships. As shown in the figure, transistors M28 and M29, M30, and M34 form one transconductance loop to bias the gate voltage of M34, while M31, M32, M33, and M35 form another transconductance loop to bias the gate voltage of M35. Taking the transconductance loop formed by NMOS as an example, based on the voltage and phase equality, we have

$$V_{GS31} + V_{GS33} = V_{GS32} + V_{GS35} \tag{1}$$

In the formula, V_{GS31} represents the gate-source voltage of the M31 tube, and the same applies to the others. Substituting the current formula in the saturation region of the MOSFET gives

$$(V_{TH31} + \sqrt{\frac{I_{D31}}{\beta_{31}}}) + (V_{TH33} + \sqrt{\frac{I_{D33}}{\beta_{33}}}) = (V_{TH32} + \sqrt{\frac{I_{D32}}{\beta_{32}}}) + (V_{TH35} + \sqrt{\frac{I_{D35}}{\beta_{35}}}) \tag{2}$$

In the formula, V_{TH} represents the threshold voltage, and $\beta = \mu_n \cdot C_{ox} \cdot W/L$. Assuming that the MOSFETs are perfectly matched and the back-gate effect is ignored, the above formula V_{TH} can cancel out, and $\mu_n \cdot C_{ox}$ are equal. Then, we have

$$\sqrt{\frac{I_{D31}}{W_{31}/L_{31}}} + \sqrt{\frac{I_{D33}}{W_{33}/L_{33}}} = \sqrt{\frac{I_{D32}}{W_{32}/L_{32}}} + \sqrt{\frac{I_{D35}}{W_{35}/L_{35}}} \tag{3}$$

The formula reveals that precise control of the static current of tube M35 can be obtained by adjusting the width-to-length ratio of the four tubes and the current of tubes M31 to M33. Similarly, the static current of the M34 transistor can be controlled by the cross-conductor loop consisting of PMOS. Additionally, temperature variations affect carrier mobility and threshold voltage, thereby influencing I_D. According to Equation (3), current deviation directly impacts the current control accuracy of the transconductance loop. When temperature rises, excessive static bias current in the output transistor increases power dissipation. Conversely, when temperature drops, static current may become too low. This can cause distortion in the output transistor and compromise signal integrity. This paper partially mitigates the effects of temperature drift by introducing a composite bias structure. Simultaneously, it ensures current proportional accuracy. Figure 1 illustrates a Miller compensation structure formed by R1, R2, C1, and C2, along with a zero adjustment resistor, enhancing stability by increasing the phase margin. The resistance and capacitance values are shown in Figure 1.

2.2.2. Small-Signal Analysis

Since the output stage gain is approximately 1, the amplifier's overall gain is primarily contributed by the first stage. Based on Figure 1, the small-signal gain expression for the first stage is:

When only one pair of transistors work, take NMOS transistors as an example, and PMOS transistors are the same.

$$A_v = g_{m1,2} \cdot R_{outn} = g_{m1,2} \frac{g_{m27}\, r_{o27}\, r_{o25}\, r_{o4} \cdot g_{m21}\, r_{o21}\, r_{o23}}{g_{m27}\, r_{o27}\, r_{o25}\, r_{o4} + g_{m21}\, r_{o21}\, r_{o23}(r_{o25} + r_{o4})} \tag{4}$$

When two pairs of pipes work at the same time,

$$A_v = (g_{m1,2} + g_{m1,2}) \cdot \frac{R_{outnn} \cdot R_{outp}}{R_{outnn} + R_{outp}} \tag{5}$$

In the formula, $g_{m1,2}$ denotes the transconductance of M1 to M4. Similarly, g_{m27} and r_{o27} denote the transconductance and AC dynamic equivalent resistance of M27, and this convention applies to the remaining components. R_{outn} and R_{outp} signify the AC equivalent output impedance of NMOS pairs and PMOS pairs when operating autonomously. Table 1 provides the dimensional parameters of the main transistors.

The transfer function expression for a two-stage amplifier with Miller compensation is

$$H(s) = \frac{1 + \frac{s}{z}}{(1 + \frac{s}{w_{p1}})\left(1 + \frac{s}{w_{p2}}\right)} \tag{6}$$

Among these, the main pole located at the output node is

$$wp_1 \approx \frac{1}{(r_{o34}||r_{o35})\cdot(C_L + C_1)} \tag{7}$$

The secondary pole is contributed by the first-stage output node

$$w_{p2} \approx \frac{1}{(R_{outn}||R_{outp})\cdot C_{eq}} \tag{8}$$

The zero is generated by the feedforward path formed by the zeroing resistor and compensation capacitor:

$$z \approx \frac{1}{R_1 \cdot C_1} \tag{9}$$

Thus, the overall system's GBW expression is

$$GBW = |A_v| \cdot \frac{w_{p1}}{2\Pi} \tag{10}$$

In the formula, C_L is the load capacitance and C_{eq} is the total parasitic capacitance at the first-stage output node.

2.3. Protection Circuit

2.3.1. Design of Over-Temperature Protection Circuit

In operational amplifiers designed for high drive currents, the protection circuit plays a critical role in ensuring the circuit operates normally. The over-temperature protection function in this paper is implemented by the start-up circuit, bandgap reference, and hysteresis comparison circuit, as shown in Figure 2. A temporary low-voltage power supply(VCC), is generated to power the hysteresis comparison circuit. Q5 and Q6 are temperature-sensing transistors. VT serves as the temperature detection port, functioning as the non-inverting input of the hysteresis comparison circuit. VT-high and VT-low represent two temperature-dependent threshold voltages generated by the bandgap reference circuit. This voltage acts as the inverting input of the hysteresis comparison circuit. These two temperature thresholds correspond to the two thresholds defining the hysteresis characteristic [16,17].

Figure 2 illustrates a hysteresis comparison circuit based on positive feedback, where the hysteresis characteristic is generated by a Schmitt trigger. This hysteresis effectively prevents frequent switching caused by temperature fluctuations, enhancing the circuit's stability and reliability. At ambient temperature, the voltage at the VT terminal exceeds the reference voltage. Virtually no current flows from the FLAG terminal, indicating the over-temperature protection mechanism is inactive. As temperature rises, the voltage at the VT terminal falls below the reference voltage. The HL terminal outputs a high level, controlling the conduction of transistor M40 in Figure 1. By pulling down the gate voltage of transistor M35 to cut off its conduction. The same applies to the LL end, where the

amplifier is turned off at this point. At the same time, current flows out of the FLAG port, indicating excessive temperature. When the temperature slightly decreases, due to the positive feedback characteristic of the hysteresis comparator circuit, current continues to flow from the FLAG port. Only when the temperature drops to another lower threshold does the comparator flip, ceasing current flow from the FLAG port. Consequently, the amplifier resumes normal operation.

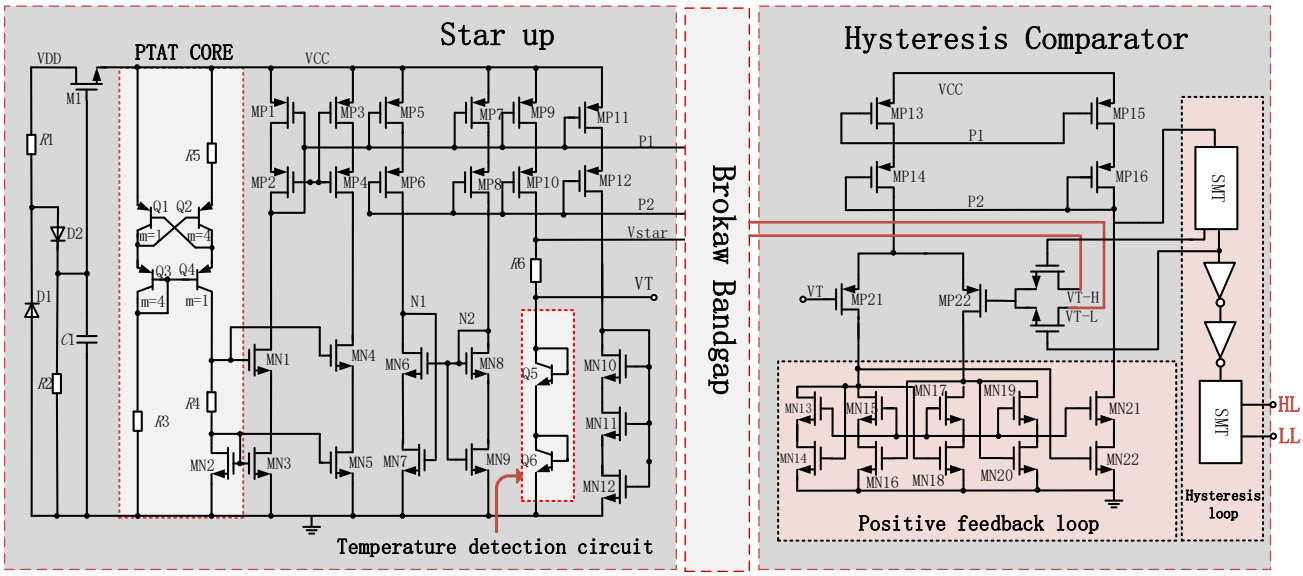


Figure 2. Hysteretic over-temperature protection circuit.

2.3.2. Design of Current Limiting Protection Circuit

The over-current protection function in this design is bidirectional, limiting both the current flowing out of and into the amplifier. The N-type and P-type voltage comparators in this design utilize a five-tube amplifier structure. To prevent over-tolerance of the MOS tubes and ensure the effectiveness of the current-limiting protection function, a measure is implemented at the output of the comparator. This measure involves clamping the output voltage of the MOS tubes using three diodes in series. This approach safeguards the enabling tubes (MP2 and MN2) from damage caused by exceeding the gate-source voltage threshold.

In Figure 1, since transistors M34 and MP1 have identical dimensions, they carry currents of equal magnitude. This current generates voltage V1 across MN1, which serves as the input to the N-channel voltage comparator. Finally, MP2 controls the gate voltage of the output transistor, thereby turning off the amplifier. This achieves the function of limiting the amplifier's output current. The protection mechanism for the current flowing into the amplifier operates identically, differing only in the types of sampling and control transistors used.

3. Circuit Simulation and Layout Design

3.1. Circuit Simulation Results

Based on the 180 nm process technology, an integrated high-voltage, high-current power amplifier was designed. Cadence 61 Spectre software was employed to simulate and validate the performance metrics of the power amplifier. The integrated circuit operates with dual power supplies. Post-simulation results were obtained under the following conditions: supply voltages of ±30 V, a common-mode level of 0 V, and a temperature of 25 °C, across different process corners.

Figure 3 shows the AC characteristic simulation results for the overall system. Under load conditions of 10 kΩ resistance and 100 pF capacitance, the system exhibits a small-signal low-frequency gain of 138.9 dB, a phase margin of 73°, and a unity-gain bandwidth product of 24 MHz.

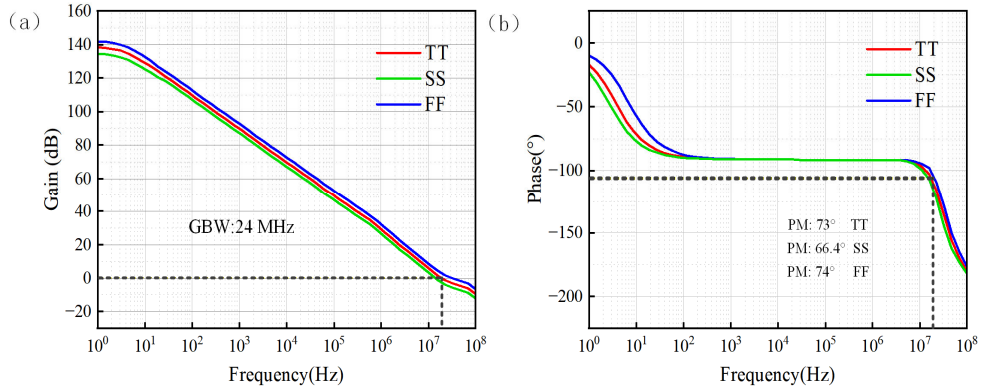


Figure 3. (**a**) Amplitude-Frequency characteristic; (**b**) Phase-Frequency characteristic.

Figure 4a illustrates the impact of varying load conditions on gain. When the load transitions from 10 kΩ to 20 kΩ, the gain variation remains below 4 dB. This demonstrates the amplifier's robust gain stability under load variations. Figure 4b shows the effect of temperature on gain. Across a wide temperature range, the gain under typical process conditions remains above 130 dB, meeting the application requirements for the target scenario.

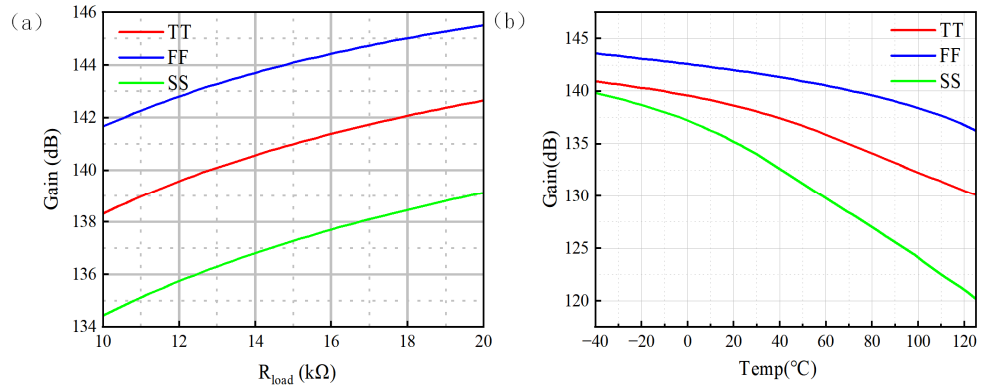


Figure 4. (**a**) Effect of different loads on gain; (**b**) Effect of different temperatures on gain.

Figure 5a,b, respectively, shows the simulated common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR). At low frequencies, the CMRR is 138 dB and the PSRR is 96 dB. This demonstrates the system's strong suppression capability against common-mode signals and excellent immunity to power supply voltage fluctuations.

Figure 6a shows the output voltage noise density plot. At nominal temperature, the output noise at 10 kHz is 4.8 $nV/Hz^{1/2}$. This low noise indicates a high signal-to-noise ratio, enabling transmission of even faint effective signals. After converting to logarithmic coordinates, the coner frequency of the flicker noise is determined to be 600 kHz. Figure 6b illustrates the temperature effect on noise. It is evident that when the temperature varies by 165 degrees, the noise changes by only 0.6 $nV/Hz^{1/2}$. This indicates that the noise is insensitive to temperature changes, demonstrating the system's excellent noise performance.

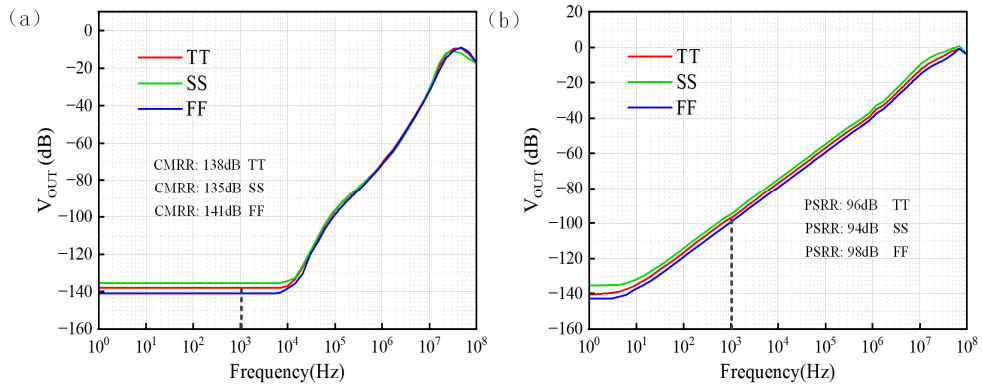


Figure 5. (**a**) Common mode rejection ratio; (**b**) Power supply rejection ratio.

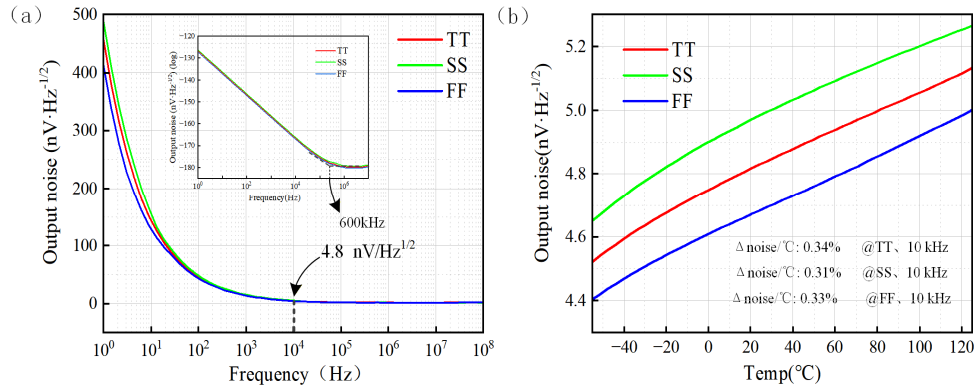


Figure 6. (**a**) Output voltage noise density; (**b**) Effect of different temperatures on noise.

Figure 7a shows the simulation results for the system's slew rate. Under load conditions of 10 kΩ resistance and 100 pF capacitance, with a 15 V square wave input and a rise time of 1 ns, the measured slew rate is 14.2 V/μs. This indicates a favorable transient response capability to input signals. Figure 7b presents the simulation of input offset voltage, with an offset voltage of 38 μV at room temperature.

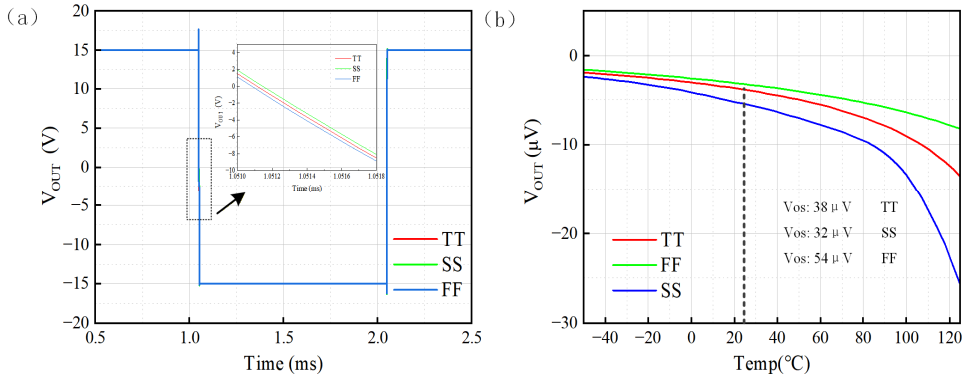


Figure 7. (**a**) Slew Rate; (**b**) Input offset voltage.

Figure 8a displays the simulation results for the system's over-temperature indication and shutdown function. During the heating process, when the temperature is below 152 °C, the FLAG pin exhibits no significant output current. Upon exceeding this threshold, the FLAG pin current jumps to 13.6 μA, indicating excessive temperature. The system then shuts down and ceases operation. When the temperature drops below 134 °C, the FLAG pin current decreases to the nA level, and the system resumes normal operation. The temperature hysteresis range is 18 °C. It can be observed that the system operates

normally within the temperature range of −40 °C to 134 °C. Upon exceeding 152 °C, the over-temperature protection function activates, ensuring the system remains undamaged. Figure 8b Simulated results for the current limiting protection function: With a load resistance of 10 Ω, the system's maximum output current was measured at 560 mA. Upon exceeding this value, the output current stabilizes at a constant level without further increase, protecting the system from damage due to excessive current. The overall static power consumption of the system is 0.9 W.

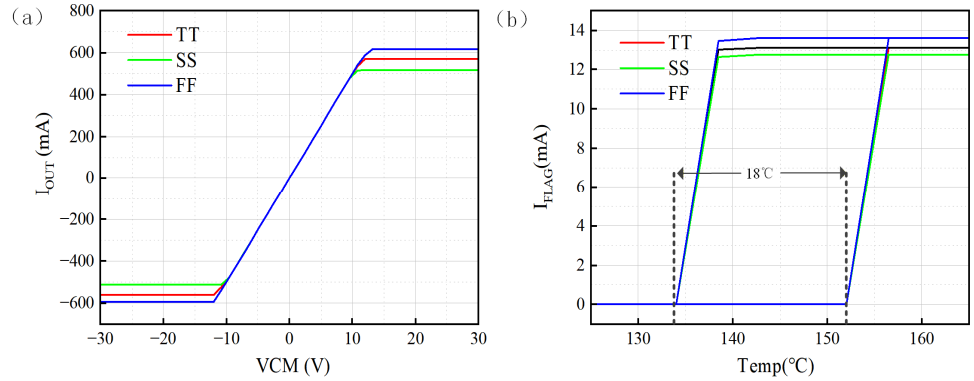


Figure 8. (**a**) Over-current protection function; (**b**) Over-temperature protection function.

Table 2 presents the comparison results of pre-simulation and post-simulation performance for the overall system. During the post-simulation process, parasitic parameters introduced by layout design (resistance and capacitance of metal interconnects, as well as parasitic capacitance of MOS devices) were extracted. The results demonstrate performance under practical application conditions including varying process angles, wide temperature ranges, and dynamic loads. Based on these conditions, the simulation results show that core performance metrics exhibit slight deviations compared to the pre-simulation. Due to the influence of parasitic parameters, the low-frequency gain decreases, the pole frequency shifts to the left, and consequently the bandwidth also decreases. The parasitic resistance introduced at the input transistor gate and the parasitic capacitance at the substrate introduce additional noise, causing a certain increase in noise amplitude. The presence of parasitic resistance in the output transistor reduces the output current and also affects the slew rate. However, all deviations remain within the engineering tolerance range for primary application scenarios. The overall system meets the target scenario requirements for signal amplification accuracy, noise suppression, high-current drive capability, and reliability.

Table 2. Front-to-Back simulation performance comparison.

Parameter	Open Loop Gain (dB)	Band-Width (MHz)	Output Current (mA)	Offset Voltage (μV)	Noise (nV/$\sqrt{Hz}$)	Slew Rate (V/μs)	Power
Pre-simulation	140	26	576	36.72	4.6	15.1	0.8
Post-simulation	138.9	24	560	38	4.8	14.2	0.9

Table 3 compares the parameters of this design with those of power amplifiers described in other literature. Reference [6] exhibits a higher slew rate but lower output current than this design. Reference [7] offers advantages in both output current and slew rate, yet suffers from insufficient bandwidth and gain. Reference [8] demonstrates superior slew rate performance but inferior noise performance compared to this design. Reference [18] features higher open-loop gain but exhibits poorer bandwidth and noise performance. Reference [19] exhibits lower offset voltage but falls short in bandwidth and slew rate

metrics. Reference [20] features low offset voltage but suffers from high noise and narrow bandwidth. Reference [21] delivers substantial output current with strong drive capability but introduces greater noise. Through comparison, the power amplifier described herein achieves higher precision, lower noise, and superior overall performance. Although these documents differ in their focus on process and parameter optimization, the table compares amplifiers of the same type operating under high-voltage, high-current conditions. This ensures the validity of the parameter comparisons.

Table 3. Performance parameter comparison.

Parameter	This Paper	[6]	[7]	[8]	[18]	[19]	[20]	[21]
Open-Loop Gain (dB)	138	97.9	95	138.6	142.7	125.6	97	100
Bandwidth (MHz)	24	3	9.6	3.089	1.9	4.98	1.6	20
Output Current (mA)	560	75	900	369	-	114.8	10^4	3000
Noise (nV/$\sqrt{\text{Hz}}$)	4.8	-	-	9.07	31.8	1.8×10^3	-	-
Offset Voltage (μV)	38	-	225	29.9	0.78	105	2000	10^4
Slew Rate (V/μs)	14.2	57	20	16.58	1.3	1.68	10	50

3.2. Layout Design

In layout design, strictly adhere to high-voltage process design rules. For the wide-swing current mirror in the bias circuit, a common-centroid symmetric layout scheme was adopted in the design. Dummy transistors were added on both sides of the matching transistors to enhance matching and reduce mismatch. The high-voltage gain section of the cascode and the high-voltage power section of the output stage were placed on opposite sides of the layout. The input matching transistors and the transconductance linear loop were positioned in the central portion of the layout. This layout creates a symmetrical structure with high-voltage regions on both sides and a low-voltage region in the center. This configuration improves matching precision and ensures signal integrity. Considering the significant heat generated by the output stage during system operation, the symmetrical layout guarantees consistent thermal conditions. Additionally, wide metal traces are employed to minimize thermal losses under high-current conditions. After comprehensively addressing the above considerations, the overall layout design was completed as shown in Figure 9. The total layout dimensions are 2500 μm × 2300 μm. The entire layout has passed Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification.

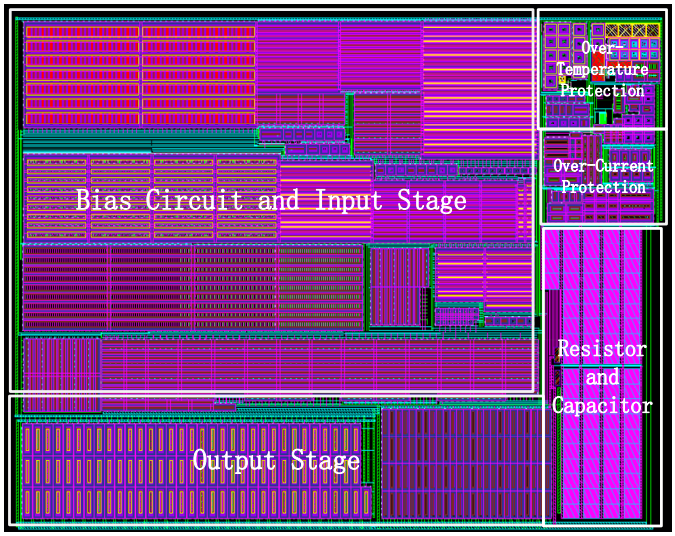


Figure 9. Overall layout.

4. Conclusions

This paper designs a high-voltage, high-output-current power amplifier that introduces an optimized structure for class AB bias, ensuring the stability and purity of the output signal. Simulation results demonstrate that this design significantly enhances gain and bandwidth performance while achieving high-voltage, high-current output, and effectively optimizes noise levels. The incorporation of on-chip over-temperature protection and current-limiting protection circuits enhances system reliability in complex operating environments. However, further improvements remain possible in both power consumption optimization and switching rate enhancement. Regarding the co-optimization of these two aspects, relevant studies have proposed solutions: Reference [22] employs two voltage-controlled current sources to achieve a low output quiescent current while adding additional control circuits to ensure a large output current during large-signal operation. This approach guarantees driving capability while reducing power consumption. Reference [23] introduces a novel parallel slew rate enhancer, significantly boosting conversion speed while optimizing settling time. This work provides crucial reference directions for subsequent optimizations in power consumption and conversion speed in this paper.

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