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Topology Optimization and Leakage Current Suppression of Photovoltaic Energy Storage Four-Leg Inverter Based on Independent Split Capacitor

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Abstract

Leakage current is a prevalent issue in non-isolated photovoltaic (PV) energy storage inverter systems, which not only induces additional power losses but also poses potential safety hazards and degrades system operational efficiency. To address this critical problem, this paper proposes an improved three-phase four-leg PV energy storage inverter topology integrated with independent split capacitors, based on the traditional three-level topology. First, an in-depth analysis of the leakage current generation mechanism is conducted, focusing on the impacts of common-mode voltage fluctuations and parasitic capacitance on leakage current paths. By establishing an equivalent mathematical model, a systematic comparative analysis is performed between the proposed topology and the traditional topology regarding key performance indicators, including leakage current suppression capability, DC-side neutral point potential stability, and power quality. Notably, the improved topology requires no additional control strategy design; under the same carrier modulation strategy and parameter configuration as the traditional topology, it can stably constrain the DC-side neutral point potential to fluctuate within an acceptable range. Experimental results demonstrate that the proposed topology reduces the peak leakage current to within 200 mA while maintaining the total harmonic distortion (THD) of the load-side current at a low level. These performance metrics comply with the relevant national and industry power quality standards for PV grid-connected systems, endowing the topology with high engineering practical value.

Keywords: non-isolated photovoltaic energy storage inverter; leakage current; topology improvement; three-phase four-leg

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1. Introduction

At the critical juncture of the global energy transition toward cleanliness and low carbon, photovoltaic (PV) energy storage systems have become the core carrier for renewable energy integration, with their operational safety and power quality directly affecting grid stability [1]. Medium-to-high voltage PV energy storage applications (such as commercial and industrial energy storage, microgrids) impose an urgent demand for inverters with "high voltage withstand capability, low losses, and resistance to three-phase imbalance." Benefiting from the significant advantages of multilevel topology in reducing switching voltage stress and the fourth arm in mitigating load imbalance, non-isolated three-level four-leg inverters have emerged as the mainstream solution in this field [2]. However, this

topology has inherent flaws: the parasitic capacitance between the PV array and the ground (typical value: 50–150 nF/kW [3]) forms leakage current paths under high-frequency common-mode voltage excitation; furthermore, fluctuations in the DC-side neutral point potential induced by four-leg control further amplify the common-mode loop gain, resulting in peak leakage current of the traditional topology far exceeding the 300 mA limit specified in China's NB/T 32004-2018 [4] and GB/T 20321-2023 [5] standards. This not only causes additional power losses and impairs grid power quality but also accelerates equipment insulation aging, posing a threat to personnel safety.

To address the leakage current challenge, the academic community has developed two primary technical approaches, "control optimization" and "topology improvement," both of which have significant limitations. At the control strategy level, reference [6] adopts unipolar SPWM technology to maintain a constant common-mode voltage (Vdc/2) and eliminates additional leakage current paths through freewheeling mode, achieving low leakage current RMS values of 11.09 mA (H9 topology)/11.73 mA (H10 topology). However, this scheme is only applicable to single-phase low-voltage systems, and the H10 topology incorporates 10 switching devices, resulting in high costs; reference [7] employs non-high-frequency-jump space vectors, realizing a leakage current RMS $\leq$ 4.95 mA that is independent of switching frequency and input voltage, with 60% of the power transmitted directly to improve efficiency. Nevertheless, it only has 19 effective space vectors, leading to high control complexity and requiring two additional inductors, which increases volume and cost; reference [8] proposes an optimized Discrete Pulse Width Modulation (DPWM) strategy that can reduce leakage current under unbalanced midpoint voltage conditions of three-level inverters, but it necessitates real-time adjustment of switching sequences, imposing stringent requirements on controller computing power; reference [9] designs an integrated modulation strategy for dual-parallel three-level inverters to suppress leakage current by coordinating the switching states of bridge arms, yet this scheme is only suitable for specific parallel topologies and lacks universality; reference [10] presents a leakage current suppression modulation scheme for split capacitor four-wire current-source inverters, which can reduce leakage current but fails to adapt to the charge–discharge characteristics of photovoltaic energy storage systems; reference [11] proposes a leakage current suppression scheme (optimized SVPWM with synchronous switching points to eliminate the 2Vdc/3 common-mode voltage), which requires no additional hardware and achieves significant suppression (especially at low speeds) without compromising control performance. However, it results in a slight increase in current harmonics, limited gain at high speeds, and relies on switching synchronization.

At the topology improvement level, most existing solutions achieve leakage current suppression at the cost of increasing the number of components: Reference [12] proposes a leakage current suppression scheme combining the H8 topology, dedicated modulation, and SiC devices. This scheme features accurate common-mode voltage control, compatibility with SiC devices for optimized lifespan, and high strategy flexibility. However, the CCMV-SV (Common-Mode Voltage Suppression Space Vector) is limited by the modulation index, additional components increase losses, SiC devices entail high costs, and extra filtering is required to suppress second harmonic components. Reference [13] presents a five-level inverter topology that reduces the leakage current RMS to 13.82 mA by stabilizing the common-mode voltage, but it requires 11 switching devices, leading to a more than 20% increase in conduction losses; reference [14] adopts a switched-capacitor impedance source structure, which enhances voltage gain while suppressing leakage current. Its four-leg configuration can adapt to three-phase unbalanced loads and reduces common-mode voltage transients, yet the charging and discharging of switched capacitors may introduce high-frequency leakage current components, necessitating additional capacitors/inductors

and increasing the topology volume; reference [15] uses four miniature film capacitors to achieve open-circuit and short-circuit immunity, minimize switching overlap time, and naturally balance inductor currents, thereby reducing leakage current sources. However, it is only applicable to current-source inverters, requires additional capacitors leading to higher costs, and has limited application scenarios; reference [16] designs a seven-level transformerless grid-connected inverter integrating boost and leakage current-limiting functions, achieving negligible peak leakage current. Nevertheless, it needs four additional capacitors and two diodes to construct the switched-capacitor unit, resulting in high topological complexity and a 35% cost increase; reference [17] adopts an input–output common-ground design to eliminate leakage current paths, with a unidirectional active buffer circuit isolating ripple power without electrolytic capacitors, improving long-term stability. However, this scheme is only suitable for single-phase systems, requires high-voltage-rated buffer capacitors, and may exhibit reduced leakage current suppression performance when scaled to three-phase topologies; reference [18] proposes a switched-boost four-leg inverter that maintains constant common-mode voltage using the fourth leg, enabling leakage current control at 18.4 mA. However, the DC side requires two inductors and one capacitor, which is unfavorable for system miniaturization; reference [19] designs a five-level transformerless topology based on capacitive voltage division that can completely eliminate leakage current, but it needs an additional inductor to limit capacitor charging current, reducing dynamic response speed; reference [20] only adds one diode, achieving complete leakage current elimination (RMS $\leq$ 0.7 mA) at low PV voltages and a 90% leakage current reduction at high voltages with only a 0.3% efficiency drop. However, when the PV voltage exceeds 480 V, the leakage current suppression effectiveness decreases to 50%, requiring coordinated control with boost and inverter switches; reference [21] presents a HERIC cascaded H-bridge inverter that suppresses leakage current through AC-side decoupling, but the cascaded structure increases control degrees of freedom, complicating neutral point potential balancing; reference [22] proposes a coupled inductor functional expansion damping scheme, embedding damping windings in parallel inverters to suppress common-mode leakage current. However, it requires redesigning the inductor structure, posing significant challenges for engineering implementation.

Furthermore, there exists a significant research gap in dedicated topologies for photovoltaic (PV) energy storage scenarios. Most existing solutions focus on grid-connected inverters, neglecting the coupling impact of DC-side voltage fluctuations on leakage current during the charge–discharge switching of energy storage systems. Common-ground topologies [23] eliminate common-mode voltage fluctuations through direct grounding, achieving excellent leakage current suppression performance. However, they are not suitable for floating PV systems or multi-string energy storage systems; boost–buck topologies [24] can adapt to low PV input voltages but often overlook the coupling relationship between leakage current and neutral point potential balancing. Although the nine-level transformerless boost inverter proposed in the reference significantly reduces leakage current, it requires complex fractional power transfer control, posing substantial challenges for engineering implementation; reference [25] presents a hybrid energy storage scheme combined with a ten-switch inverter, which improves power quality but lacks optimization for leakage current issues, resulting in limited applicability.

To address the aforementioned challenges, this paper focuses on the topological optimization of a four-leg photovoltaic (PV) energy storage inverter, aiming to achieve the goal of "high operational adaptability with minimal component increments without relying on additional complex control." Based on Kirchhoff's laws, a common-mode equivalent circuit of the traditional three-level four-leg topology is established, the leakage current expression is derived, and the coupling mechanism of parasitic capacitance, filter inductance, and

neutral point potential fluctuations on leakage current is quantitatively analyzed. This study systematically reveals the common flaws of existing solutions: control strategies rely on complex algorithms, topology improvements sacrifice cost and efficiency, and dedicated topologies have poor adaptability. An improved topology based on independent voltage-divider capacitors is proposed. This scheme only adds two independent voltage-divider capacitors (with capacitance much smaller than the main capacitors) on the DC side and connects the midpoint of the output filter capacitors to the midpoint of the voltage-divider capacitors. This design simultaneously constructs an active discharge path for common-mode current and avoids modulation failure that may be caused by direct grounding of the DC-side neutral point. Simulation and experimental verifications demonstrate the excellent performance of the improved topology in leakage current suppression.

The remainder of this paper is structured as follows: Section 2 establishes the common-mode model of the traditional topology and analyzes the leakage current mechanism; Section 3 elaborates on the proposed improved topology and its operating principle in detail; Section 4 verifies the effectiveness and superiority of the proposed topology through comparative simulations and experiments; Section 5 summarizes the entire paper.

2. Traditional Three-Level Three-Phase Four-Leg Photovoltaic Energy Storage Inverter Topology

The existence of the parasitic capacitance between the photovoltaic array and the ground forms a common-mode resonant circuit that generates leakage current, posing risks to the safety and stability of the system. The schematic diagram of leakage current generation is shown in Figure 1. In the figure, C_{pv} is the parasitic capacitance between the solar panel and the ground; u_{pv1} and u_{pv2} are the parasitic capacitance voltages of the positive and negative buses, respectively. C_1 and C_2 are the positive and negative bus voltage-dividing capacitors on the DC side; L is the bridge arm filter inductor; C is the filter capacitor; O is the midpoint of the positive and negative bus capacitors on the DC side; n is the neutral point of the load, and the current icm flowing from n to the ground is the leakage current.

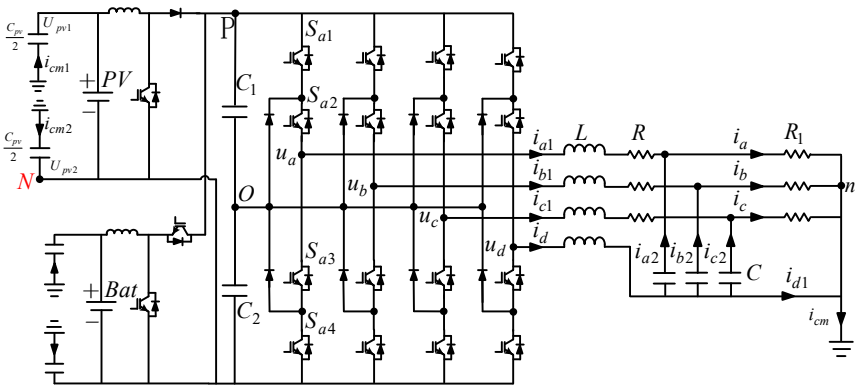


Figure 1. Schematic diagram of the traditional topology (*N* denotes the negative pole of the DC busbar).

Figure 1 shows the traditional three-level three-phase four-leg photovoltaic energy storage inverter topology [26], which will be referred to as the traditional topology later.

The inverter adopts a carrier modulation strategy as a whole. The fourth bridge arm uses a positive and negative sequence separation method, mainly to improve the symmetry of the output voltage under unbalanced load conditions, and finally strike a balance between the suppression effect and the assurance of system performance.

2.1. Mathematical Modeling and Analysis of Common-Mode Loop in Traditional Topology Structure

According to Kirchhoff's voltage law, the following equations can be listed:

$$\begin{cases} u_a = L\frac{di_{a1}}{dt} + i_{a1}R + i_aR_1 + u_{nN} \\ u_b = L\frac{di_{b1}}{dt} + i_{b1}R + i_bR_1 + u_{nN} \\ u_c = L\frac{di_{c1}}{dt} + i_{c1}R + i_cR_1 + u_{nN} \\ u_d = L\frac{di_d}{dt} + u_{nN} \end{cases} \tag{1}$$

u_a, u_b, u_c, u_d are the voltages from point O to N of the output of each bridge arm; i_{a1}, i_{b1}, i_{c1}, i_{d1} are the output currents of the bridge arms; i_a, i_b, i_c are the load currents; R_1 is a three-phase load; u_{nN} is the voltage of the neutral point on the load side relative to point N.

The formula for the midpoint voltage difference can be expressed as follows:

$$U_O = U_{PO} - U_{ON} \tag{2}$$

where P is the positive terminal of the DC bus, and N is the negative terminal of the DC bus.

The leakage current can be expressed as follows:

$$i_{cm} = i_{a1} + i_{b1} + i_{c1} + i_d = i_1 + i_d \tag{3}$$

The current of the capacitor branch is defined as follows:

$$i_2 = i_{a2} + i_{b2} + i_{c2} \tag{4}$$

The current of the three-phase load branch is defined as follows:

$$i_3 = i_a + i_b + i_c \tag{5}$$

The voltage difference u_{nN} between the neutral point n of the load end and point N can be expressed as follows:

$$u_{nN} = u_{pv1} = u_{pv2} \tag{6}$$

Since the parasitic capacitances of the positive and negative DC buses to the ground are the same, and the currents flowing through them are also the same, there are the following:

$$u_{pv} = u_{pv1} = u_{pv2} \tag{7}$$

Substituting Equation (7) into Equation (6), we can obtain the following:

$$u_{nN} = u_{pv} \tag{8}$$

From the topology of Figure 1, the following equations can be formulated:

$$\begin{cases} i_{cm} = i_{cm1} + i_{cm2} \\ i_{cm1} = i_{cm2} = \frac{C_{pv}}{2}\frac{du_{pv}}{dt} \end{cases} \tag{9}$$

Among them, i_{cm1} and i_{cm2} are the leakage currents generated by the parasitic capacitances of the positive and negative buses to the ground, respectively. It can be obtained from Equations (8) and (9):

$$u_{pv} = \frac{1}{C_{pv}}\int i_{cm}dt \tag{10}$$

Select point N on the DC bus side as the common-mode voltage reference point. The common-mode voltage is defined as the arithmetic mean of the voltages of the four-phase bridge arms output to point N. Then we can obtain the following:

$$u_{cm} = \frac{1}{4}(u_a + u_b + u_c + u_d) \tag{11}$$

By rearranging Equations (1)–(11), the common-mode voltage equation for the common-mode loop is obtained:

$$4u_{cm} = L\frac{di_{cm}}{dt} + i_3R_1 + i_1R + \frac{1}{C}\int i_d dt + \frac{4}{C_{pv}}\int i_{cm} dt \tag{12}$$

Based on Equation (12), the equivalent circuit of the common-mode loop for the inverter under the traditional topology is derived as shown in Figure 2.

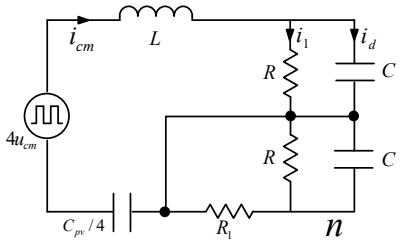


Figure 2. Traditional topological equivalent circuit diagram.

Based on Equation (12), the equivalent circuit of the circuit shown in Figure 1 is derived, and its specific form is presented in Figure 2. As indicated in Figure 2, the excitation source of this equivalent circuit is the common-mode voltage $4u_{cm}$. Without changing the original component parameters, the leakage current i_{cm} can be suppressed through two core methods: First, optimize the excitation mode and control strategy to reduce the slew rate of the common-mode voltage, thereby indirectly mitigating the leakage current. Second, modify the circuit topology based on the principles of the hardware circuit to achieve direct suppression of the leakage current.

2.2. Leakage Current Analysis of Traditional Topology

The simulation experiment is carried out on the MATLAB(R2022b)/Simulink platform. The parameter settings are shown in Table 1. According to the active power of about 50 nF~150 nF/kW, the parasitic capacitance value is 1 μF.

Table 1. Simulation parameter settings.

Parameter	Numerical Value
dc link pd	680 V
the reference output active power	125 kW
reference output reactive power	0 VAR
output voltage frequency	50 Hz
equivalent line resistance	0.1 Ω
filter inductance	150 μH
sampling frequency	16 kHz
smoothing capacitance	40 μF
parasitic capacitance	1 μF
single-phase resistance	4 Ω

To control variables, the simulation parameters for the subsequent optimized topology are set as shown in Table 1.

Under the traditional topology, the load-side current and voltage waveforms are shown in Figures 3 and 4, respectively. After the load-side current reaches a steady-state operating condition, Fast Fourier Transform (FFT) analysis is performed on the load-side voltage waveform, with the results presented in Figure 5. As can be clearly observed from Figure 5, the total harmonic distortion (THD) of the load-side voltage under this operating condition is 1.11%. This THD value objectively reflects the degree of voltage waveform distortion, providing a quantitative basis for evaluating the power quality of the traditional topology.

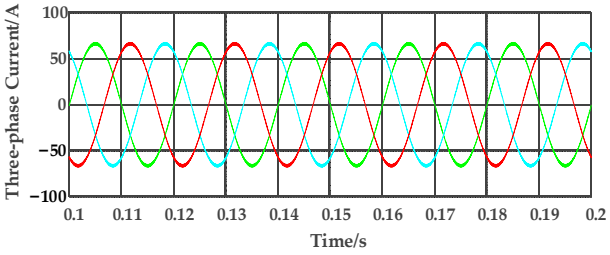


Figure 3. Traditional topology load-side current.

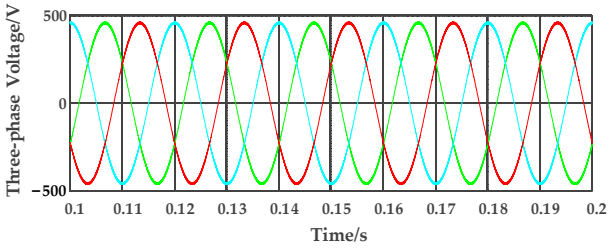


Figure 4. Traditional topology load-side voltage.

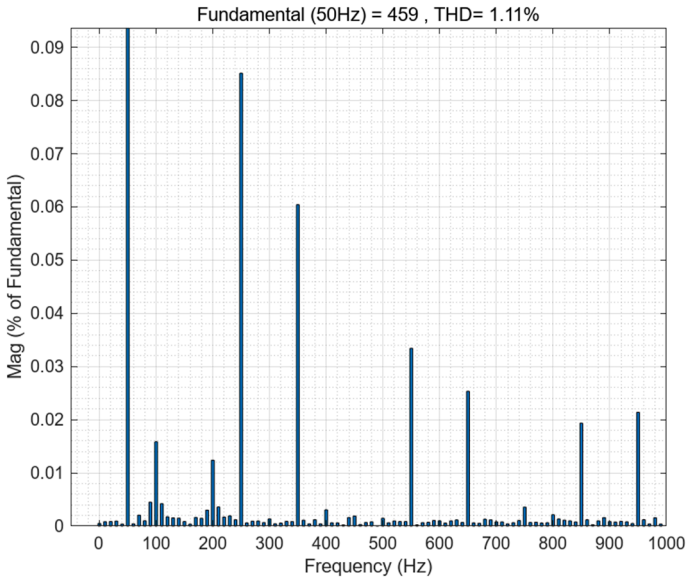


Figure 5. FFT Analysis of traditional topology.

Figure 6 shows the voltage difference waveform across the two DC-side voltage-dividing capacitors, and Figure 7 presents the leakage current waveform of this topology. A comprehensive analysis of the simulation results from Figures 3–7 indicates that, under the current control strategy, the fluctuation in the DC midpoint potential is maintained within 2 V. The suppression of leakage current is moderately effective, and the current distortion at the load end is relatively low. However, it should be noted that this strategy

still has significant drawbacks: the maximum leakage current reaches 20 A, exceeding the safe operating threshold and posing considerable safety hazards. Therefore, further optimization of the three-phase four-leg topology is required to achieve the coordinated suppression of leakage current and midpoint potential fluctuations, thereby improving the system's safety performance and operational stability.

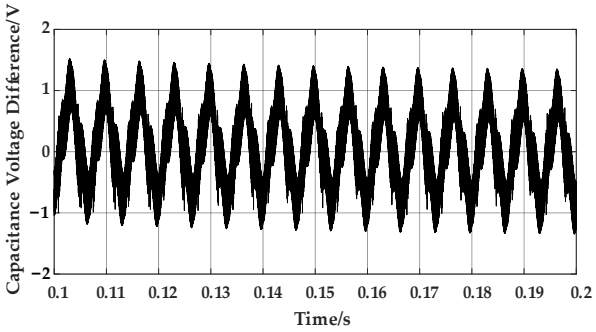


Figure 6. In the traditional topology, the voltage difference between the two capacitors on the DC side.

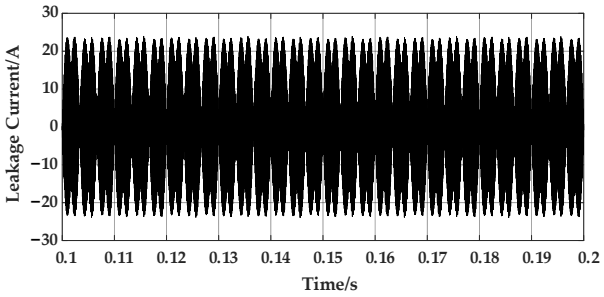


Figure 7. Leakage current of traditional topology.

3. Direct Midpoint Feedback Type I Topology

In the initial design, directly connecting the neutral point of the filter capacitor to midpoint O of the two DC-side voltage-dividing capacitors clamps the DC midpoint potential directly to zero, thus rendering the original modulation algorithm ineffective. To solve this problem, a current-limiting resistor R_2 is connected in series between the neutral point of the filter capacitor and midpoint O of the DC bus capacitors. The improved topology thus obtained is shown in Figure 8.

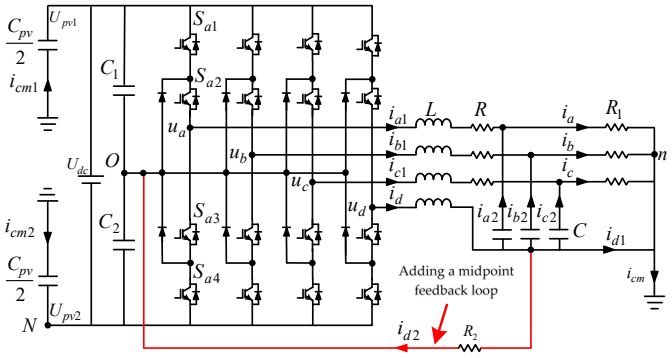


Figure 8. Middle-point feedback Type I topology schematic diagram.

Figure 8 illustrates the direct midpoint feedback Type I topology, hereinafter referred to as the midpoint feedback Type I topology.

3.1. Mathematical Modeling and Analysis of Common-Mode Loop with Midpoint Feedback Type I Topology Structure

For the midpoint feedback Type I topology illustrated in Figure 8, the leakage current loop equation is identical to Equations (1). Based on Kirchhoff's Voltage Law (KVL), the following equation can be derived for the midpoint feedback loop:

$$\begin{cases} u_a = L\dfrac{di_{a1}}{dt} + i_{a1}R - \dfrac{1}{C}\int i_{a2}dt + i_{d2}R_2 + U_{ON} \\ u_b = L\dfrac{di_{b1}}{dt} + i_{b1}R - \dfrac{1}{C}\int i_{b2}dt + i_{d2}R_2 + U_{ON} \\ u_c = L\dfrac{di_{c1}}{dt} + i_{c1}R - \dfrac{1}{C}\int i_{c2}dt + i_{d2}R_2 + U_{ON} \\ u_d = L\dfrac{di_d}{dt} + i_{d2}R_2 + U_{ON} \end{cases} \tag{13}$$

The leakage current can be further expressed as follows:

$$i_{cm} = i_a + i_b + i_c = i_1 + i_2 = i_1 + i_d - i_{d2} \tag{14}$$

Sorting out the above formulas, the following can be obtained:

$$4u_{cm} = L\frac{di_1}{dt} + L\frac{di_d}{dt} + i_1R + i_3R_1 + \frac{4}{C_{pv}}\int i_{cm}dt \tag{15}$$

$$4u_{cm} = L\frac{di_1}{dt} + L\frac{di_d}{dt} + i_1R - \frac{1}{C}\int i_2dt + 4i_{d2}R_2 + 4U_{ON} \tag{16}$$

Based on Equations (15) and (16), the equivalent common-mode loop topology of the inverter under the neutral point feedback Type I topology is derived, as illustrated in Figure 9.

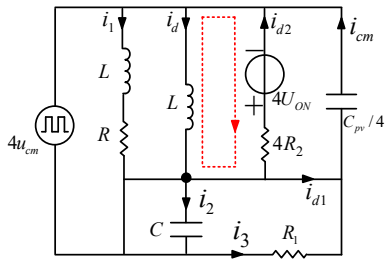


Figure 9. Equivalent circuit diagram of midpoint feedback Type I topology (The part marked by the red dashed arrow indicates the equivalent path of the added midpoint feedback loop).

In the equivalent circuit illustrated in Figure 9, the introduction of resistor R_2 theoretically alleviates the circulating current issue. Specifically, the current induced by the common-mode voltage $4u_{cm}$ is diverted into multiple shunt paths through this branch, further reducing the current in the leakage current branch and ultimately achieving leakage current suppression.

The appropriate selection of the resistance value of R_2 is crucial to circuit stability. If the resistance of R_2 is too high, the leakage current in the circuit will increase sharply. Conversely, if the resistance is too low, not only will the total harmonic distortion (THD) on the load side barely meet the power quality standards, but the system's ability to suppress circulating currents will also be significantly reduced. As illustrated in Figure 10, when R_2 is 3.5 Ω, an optimal balance is achieved between leakage current suppression and load current THD control. Therefore, the parameter configuration R_2 = 3.5 Ω will be adopted in subsequent simulation analyses.

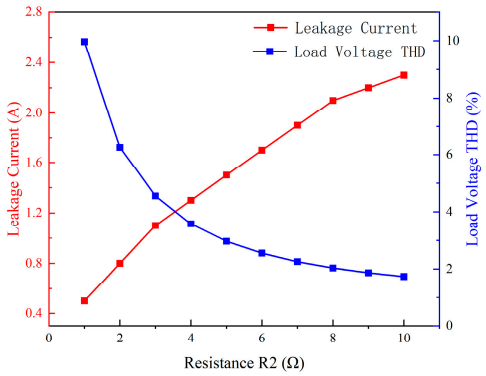


Figure 10. Effect of resistance R_2 on leakage current and its load current THD.

3.2. Leakage Current Analysis of Neutral Point Feedback Type I Topology

The simulation results of the midpoint feedback Type I topology are illustrated in Figures 11–13. Figure 11 shows the leakage current waveform of this simulation model, reflecting the dynamic variation characteristics of the leakage current during the topology's operation. Figure 12 presents the Fast Fourier Transform (FFT) analysis results of the load-side current after the system reaches stable operation, which can be used to evaluate the harmonic content of the load current. Figure 13 shows the voltage difference between the two DC-side voltage-dividing capacitors in the improved topology—an indicator that directly reflects the DC-side voltage balance.

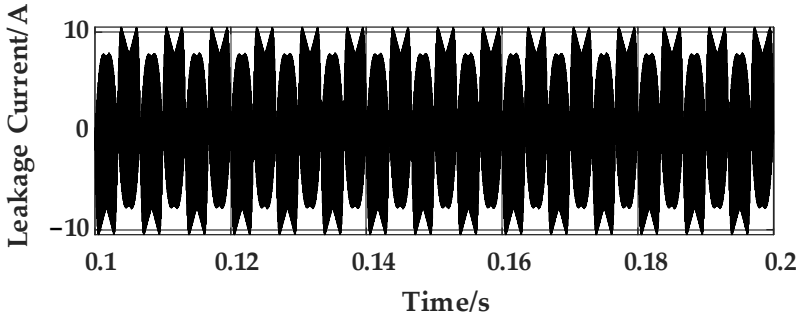


Figure 11. Leakage current of neutral point feedback Type I topology.

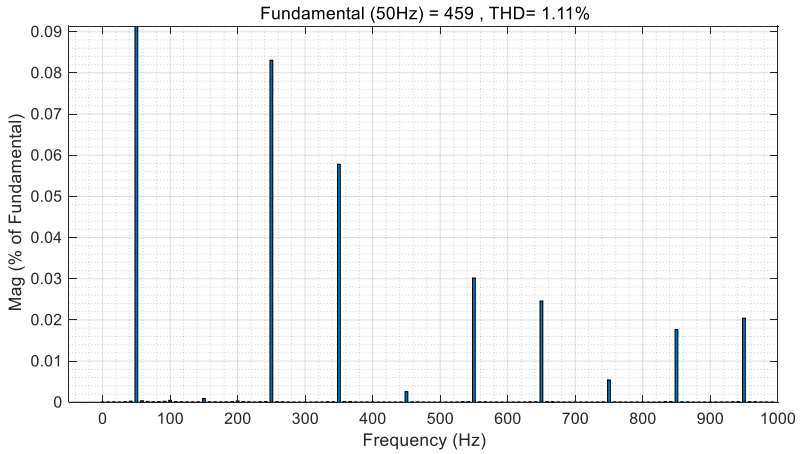


Figure 12. FFT analysis of midpoint feedback Type I topology.

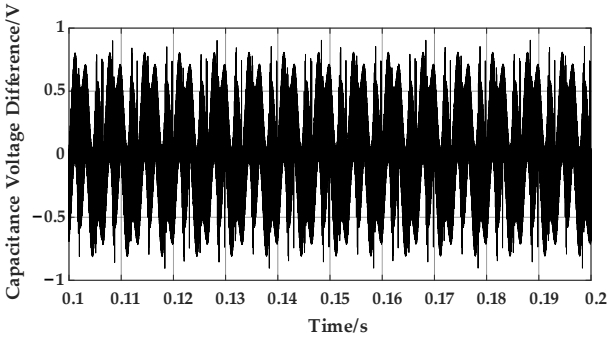


Figure 13. The voltage difference between the two capacitors on the DC side of the neutral point feedback Type I topology.

During stable operation, the peak leakage current of the system is approximately 10 A, which is still significantly higher than the international standard threshold of 0.3 A, thus requiring further optimization. In addition, there are two key issues: First, the fourth bridge arm branch only contains a single series inductor, resulting in excessively low branch impedance that directly causes DC backflow. Second, this backflow current interferes with the DC-side midpoint potential, leading to a shift in the midpoint potential of the two DC-side voltage-dividing capacitors. This, in turn, seriously impacts the stable and efficient operation of the system. In conclusion, the leakage current of the current topology fails to meet the national standard requirement of 0.3 A. Further improvements to the topology structure or the adoption of additional control strategies are required to address these issues.

4. Neutral Point Feedback Type II Topology Based on Independent Split Capacitor

This paper proposes a leakage current suppression structure based on independent split capacitors. In this structure, Capacitors C_1' and C_2' serve as independent split capacitors between the positive and negative DC buses, with their capacitance values much smaller than those of the main DC-side capacitors C_1 and C_2. The neutral point of the output filter capacitor is connected to midpoint O' of the DC-side independent split capacitors. This connection method avoids the risk of direct grounding of the DC-side midpoint while providing an additional shunt path for the leakage current branches, thereby achieving leakage current suppression. The specific configuration of this improved topology is illustrated in Figure 14.

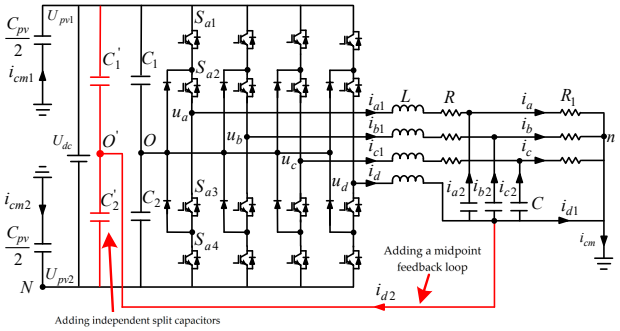


Figure 14. The midpoint feedback Type II topology structure.

Figure 14 illustrates the three-level four-leg photovoltaic energy storage inverter topology based on independent split capacitors, hereinafter referred to as the midpoint feedback Type II topology. Based on this topology, the corresponding equivalent circuit is shown in Figure 15.

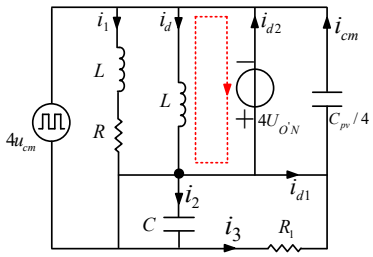


Figure 15. Neutral point feedback Type II topology equivalent circuit.(The part marked by the red dashed arrow indicates the equivalent path of the added midpoint feedback loop.)

As illustrated in Figure 15, compared with the traditional topology and the midpoint feedback Type I topology, the midpoint feedback Type II topology adds a new branch to the leakage current path. Theoretically, this branch plays a moderate role in suppressing leakage current. Meanwhile, the current is fed back to neutral point O' of the independent split capacitors, which does not affect the DC bus midpoint, thereby enhancing system stability.

4.1. Mathematical Modeling and Analysis of Common-Mode Loop with Midpoint Feedback Type II Topology Structure

For the midpoint feedback Type II topology illustrated in Figure 14, the leakage current loop equation is identical to Equation (1). Based on Kirchhoff's Voltage Law (KVL), the following equation can be derived for the midpoint feedback loop:

$$\begin{cases} u_a = L\dfrac{di_{a1}}{dt} + i_{a1}R - \dfrac{1}{C}\int i_{a2}dt + U_{O'O} + U_{ON} \\ u_b = L\dfrac{di_{b1}}{dt} + i_{b1}R - \dfrac{1}{C}\int i_{b2}dt + U_{O'O} + U_{ON} \\ u_c = L\dfrac{di_{c1}}{dt} + i_{c1}R - \dfrac{1}{C}\int i_{c2}dt + U_{O'O} + U_{ON} \\ u_d = L\dfrac{di_d}{dt} + U_{O'O} + U_{ON} \end{cases} \tag{17}$$

where $U_{O'O}$ denotes the voltage between the midpoint of the split capacitors and the midpoint of the bus capacitors. With point N uniformly adopted as the voltage reference point for the modeling equations, the voltages of $U_{O'O}$ and U_{ON} are superimposed and uniformly expressed as $U_{O'N}$, and the above equations are rewritten as follows:

$$\begin{cases} u_a = L\dfrac{di_{a1}}{dt} + i_{a1}R - \dfrac{1}{C}\int i_{a2}dt + U_{O'N} \\ u_b = L\dfrac{di_{b1}}{dt} + i_{b1}R - \dfrac{1}{C}\int i_{b2}dt + U_{O'N} \\ u_c = L\dfrac{di_{c1}}{dt} + i_{c1}R - \dfrac{1}{C}\int i_{c2}dt + U_{O'N} \\ u_d = L\dfrac{di_d}{dt} + U_{O'N} \end{cases} \tag{18}$$

The leakage current under this condition is given by Equation (14).

It is not difficult to derive the leakage current loop equation from Figure 14, which is completely consistent with Equation (15). By combining and organizing Equation (18), the midpoint feedback loop equation is obtained as shown in Equation (19).

$$4u_{cm} = L\frac{di_1}{dt} + L\frac{di_d}{dt} + i_1R - \frac{1}{C}\int i_2dt + 4U_{O'N} \tag{19}$$

At this time, the resonant frequency of the common-mode circuit can be obtained:

$$f_{res\_cm} = \frac{1}{2\pi\sqrt{L_1 \frac{C_f \frac{2}{3} C'}{C_f + \frac{2}{3} C'}}} \tag{20}$$

The independent split capacitor C' only affects the system's common-mode resonant frequency f_{res_cm}, while its interference with the differential-mode resonant frequency f_{res_dm} is negligible. Leveraging this characteristic, the capacitance range of the independent split capacitor can be constrained based on the requirements for common-mode resonance suppression. Through the reasonable selection of capacitor parameters, this method ensures that the system maintains high common-mode filtering performance while delivering higher power quality to the load side.

4.2. Calculation of Capacitance Value of Neutral Point Feedback Type II Topologically Independent Split Capacitor

A reasonable capacitance value for the independent split capacitor can effectively mitigate low-frequency oscillation of the bridge arm–side current and reduce the effective value of the line current. Next, the basis and principles for selecting the capacitance value are discussed.

The expression of the low-frequency component in the common-mode voltage source [27], the harmonic coefficient f(n), and the harmonic source frequency f_{res} in the Fourier expression of the common-mode voltage are as follows:

$$f(n) = \frac{6\sqrt{3}E_m}{4\pi U_{dc}} \frac{(-1)^{n+1}}{(3n-2)(3n-1)} \tag{21}$$

$$f_{res} = 3(2n-1)f \tag{22}$$

where n denotes the harmonic order; E_m is the phase voltage amplitude; u_{dc} represents the DC bus voltage; and f stands for the load-side frequency.

In engineering practice, it is generally accepted that when the harmonic component coefficient $f(n) < 0.001$, the influence of that harmonic order may be considered negligible. Based on this criterion, the minimum frequency of the harmonic source f_{res_min}, can be calculated. If the system's common-mode resonance frequency f_{res_cm}, exceeds fres_min, the circuit can avoid generating common-mode resonance. Concurrently, to ensure the system possesses high-frequency filtering capability, the common-mode resonance frequency must be less than half the switching frequency f_s (i.e., $f_{res\_cm} < 0.5\,f_s$). In summary, when the common-mode resonance frequency satisfies $f_{res\_cm} \in [f_{res\_min}, 0.5\,f_s]$, the circuit can both avoid common-mode resonance and achieve high-frequency filtering. Substituting the DC-side electromotive force E_m = 270 V and DC bus voltage U_{dc} = 680 V into Equation (21) yields the specific constraint range for the common-mode resonance frequency:

When $n \geq 7$,

$$(3n-2)(3n-1) > 328.4 \tag{23}$$

To satisfy the condition for neglecting harmonic components with coefficients $f(n) < 0.001$, a harmonic order of n = 7 is selected. Substituting it into Equation (22) yields the following: the minimum frequency f_{res_min} = 1.95 kHz for harmonic sources with sufficiently negligible amplitude impact. Combining this with the preceding switching frequency constraint $0.5\,f_s$ = 8 kHz, the effective range for the common-mode resonance frequency is further determined as $f_{res\_cm} \in$ [1.95 kHz, 8 kHz]. Analyzing the common-mode resonance frequency calculation formula (20), it is evident that the independent split capacitance value C' decreases as f_{res_cm} increases, ultimately approaching 9.32 μF.

Balancing engineering selection convenience with performance requirements, C' = 9 μF was selected for simulation analysis. This parameter ensures the circuit avoids common-mode resonance while effectively limiting the feedback current in the LC circuit.

4.3. Leakage Current Analysis of Neutral Point Feedback Type II Topology

The simulation results of the midpoint feedback Type II topology are illustrated in Figures 16–20. The physical quantities depicted in each figure and their analyses are as follows: Figure 16 presents the load-side current waveform, reflecting the dynamic response and steady-state characteristics of the load current; Figure 17 shows the load-side voltage waveform, which is used to observe the amplitude stability and waveform smoothness of the output voltage; Figure 18 displays the Fast Fourier Transform (FFT) analysis results of the load-side current after the system reaches stability, enabling quantitative evaluation of the total harmonic distortion (THD) to measure power quality; Figure 19 depicts the leakage current waveform, intuitively demonstrating the leakage current suppression effect of this topology; Figure 20 provides the voltage difference waveform between the two voltage-dividing capacitors on the DC side under the optimal topology scheme, which is used to analyze the balance of the midpoint potential on the DC side.

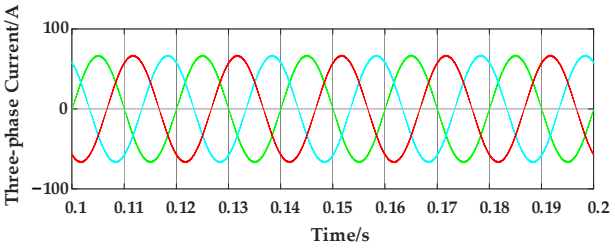


Figure 16. Load-side current waveform of neutral point feedback Type II topology.

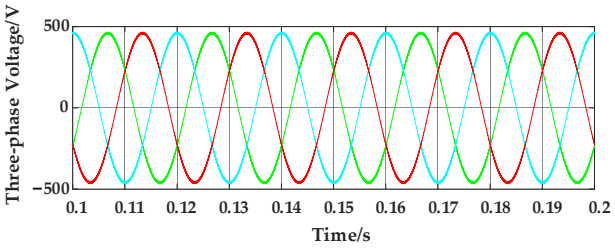


Figure 17. Neutral point feedback Type II topology load-side voltage waveform.

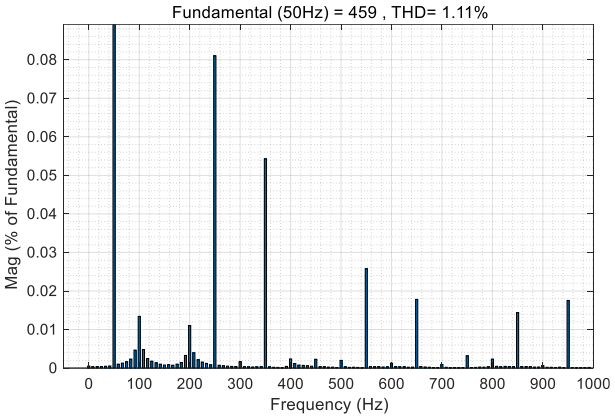


Figure 18. FFT analysis of load-side voltage of neutral point feedback Type II topology.

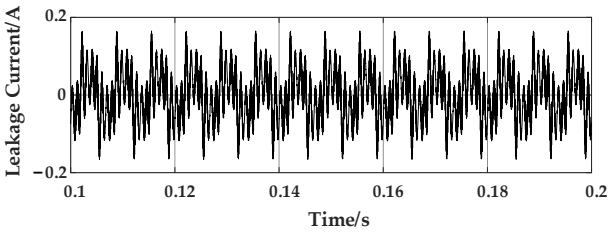


Figure 19. Neutral point feedback Type II topology leakage current waveform.

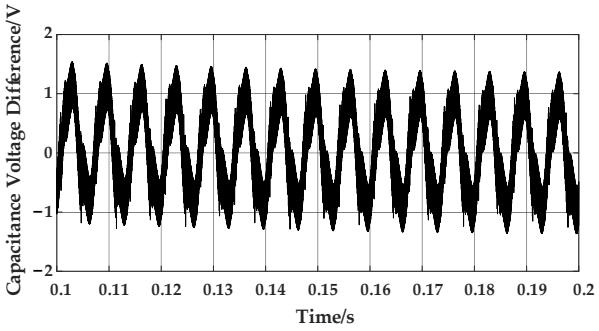


Figure 20. Voltage difference between two DC bus capacitors in neutral point feedback Type II topology.

As can be seen from Figure 18, the current distortion rate (i.e., total harmonic distortion, THD) of the load side under the midpoint feedback Type II topology is 1.11%, indicating that the output power quality meets the relevant standards.

According to China's energy industry standard NB/T 32004-2018 "Technical Specification for Photovoltaic Grid-Connected Inverters" and national standard GB/T 20321-2023 "Inverters for Off-Grid Wind and Solar Power Generation Systems", for inverters with a rated output of less than 30 kVA, the leakage current requirement is no more than 300 mA. As illustrated in Figure 19, the maximum leakage current of the midpoint feedback Type II topology is 165 mA, which meets the requirements of China's energy industry standard.

5. Analysis of Experimental Results

Building upon the validation of the aforementioned simulation results, this study further constructed a physical experimental platform with parameters consistent with those of the simulations to verify the practical operational performance of the optimized topology. Figure 21 presents the overall configuration of the three-level three-phase four-leg inverter experimental platform utilized in this research. Comprising a main circuit module, a control module, a sampling module, and a load module, the platform facilitates real-time monitoring of the topology's operational status and accurate data acquisition.

A detailed description of the equipment used in the experiment is as follows: the oscilloscope was manufactured by TektronixTektronix, model TDS 1012C-SC, with its headquarters located at 14150 SW Karl Braun Drive, Beaverton, OR 97077, USA; the voltage probe was a high-voltage isolation probe produced by CYBERTEK (Shenzhen ZhiYong Electronics Co., Ltd., Shenzhen, China), model DP615, and the company is situated at Unit A1702-1, No.1 Workshop, Longgang Tian'an Digital Entrepreneurship Park, No.441 Huangge Road, Longgang District, Shenzhen, Guangdong, China; the current probe was a current clamp manufactured by CYBERTEK (Shenzhen ZhiYong Electronics Co., Ltd.), model HCP8300, with the same company address as above; the photovoltaic simulation DC source adopted the solar array simulator of Parwa (Shenzhen Parwa Technology Company Limited), with a maximum output voltage of 600 V, and the company is located

at Floor 6, Block 5, Nangang Second Industrial Park, Xili Town, Nanshan District, Shenzhen, Guangdong, China.

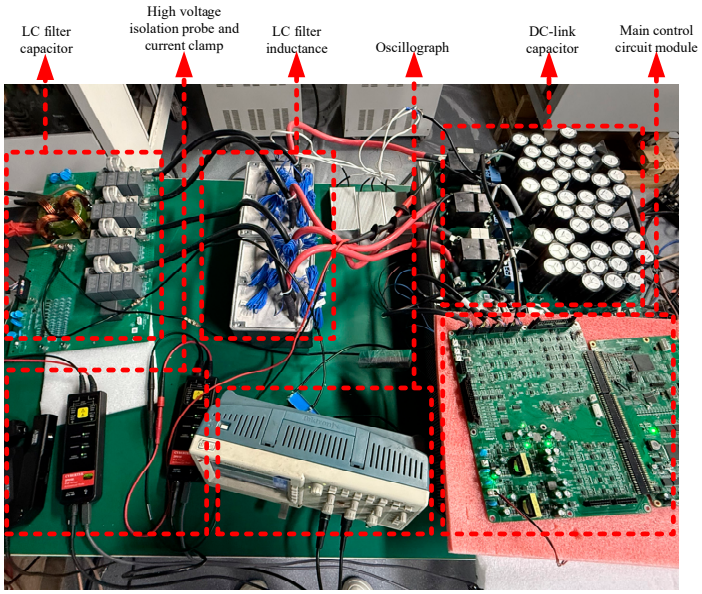
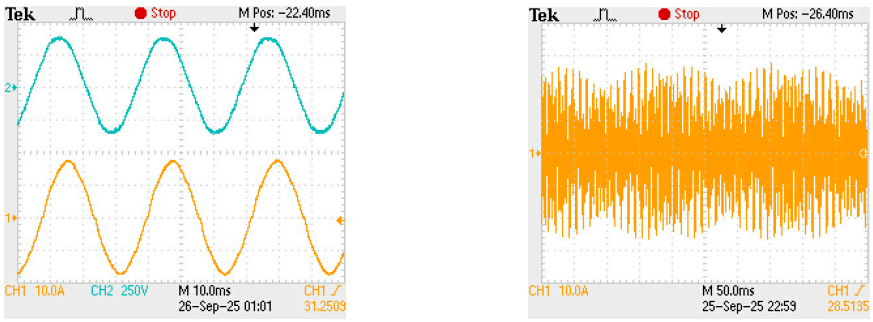


Figure 21. Overall Structure of the Three-Level Three-Phase Four-Leg Photovoltaic Energy Storage Inverter Experimental Platform.

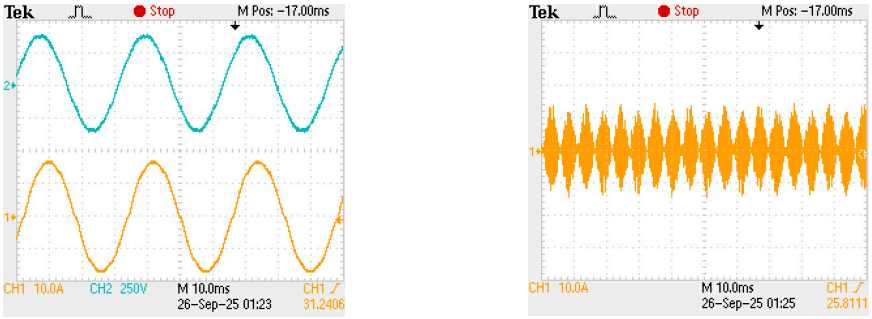
To verify the performance advantages of the proposed "three-level three-phase four-leg topology with independent split capacitors on the DC bus," a comparative experiment was designed. When the DC bus voltage is set to 600 V, the traditional three-level three-phase four-leg topology and the improved topology proposed in this paper adopt the same carrier modulation strategy for parallel experiments. Figure 22 presents the first set of experimental results of the traditional topology. Although the load-side line voltage of phases a and b and the phase a current waveform maintain sinusoidal characteristics, the peak leakage current of the traditional topology reaches as high as 26 A. This leakage current value far exceeds the safe operation threshold, which may damage equipment insulation and pose significant safety hazards to personnel. This highlights the major flaw of the traditional topology in leakage current suppression.



(**a**) (**b**)

Figure 22. (**a**) Traditional topology load line voltage (solid blue line) and its current waveform (solid orange line), (**b**) leakage current waveform.

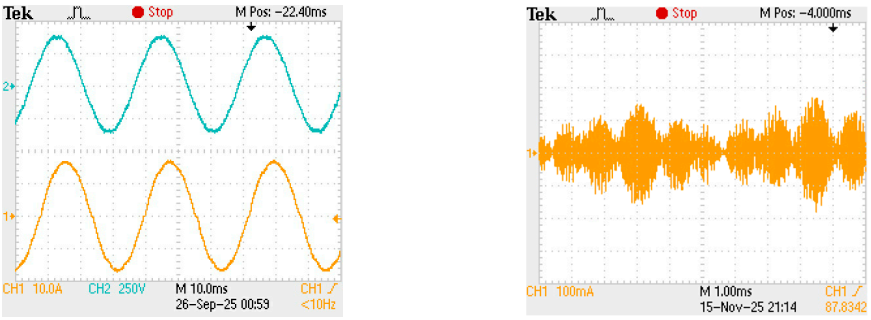
Figure 23 presents the waveforms of the phase a–b voltage and phase a current obtained from the experiment on the midpoint feedback Type I topology. At this point, the peak leakage current is approximately 14 A, which is significantly reduced compared with the traditional topology but fails to meet the engineering requirements.



(**a**) (**b**)

Figure 23. (**a**) Neutral point feedback Type I topology load line voltage (solid blue line) and its current waveform (solid orange line), (**b**) leakage current waveform.

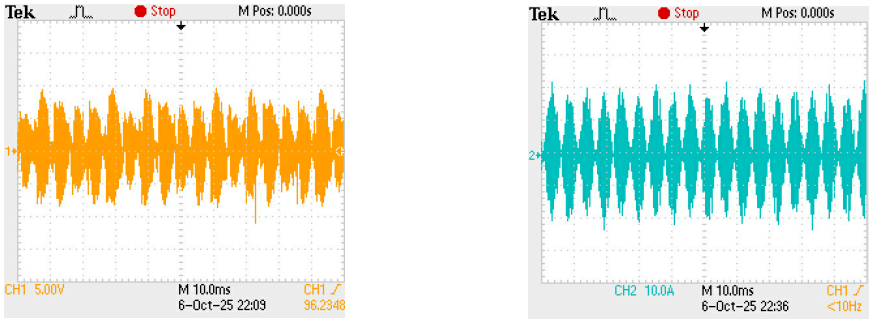
Figure 24 illustrates the experimental waveforms of the proposed "three-level three-phase four-leg inverter with independent split capacitors" under a DC bus voltage of 600 V, including the load line voltage waveform, load line current waveform, and leakage current waveform. As is clearly shown in Figure 24, both the load line voltage and line current waveforms are very close to standard sine waves with low distortion. At this point, the peak leakage current is approximately 185 mA, which is almost identical to the simulation result (165 mA). Considering that the simulation parameters are idealized and the difference is negligible, the experimental results basically meet the expectations.



(**a**) (**b**)

Figure 24. (**a**) The load line voltage (solid blue line) and its current waveform (solid orange line), (**b**) leakage current waveform of the neutral point feedback type II topology.

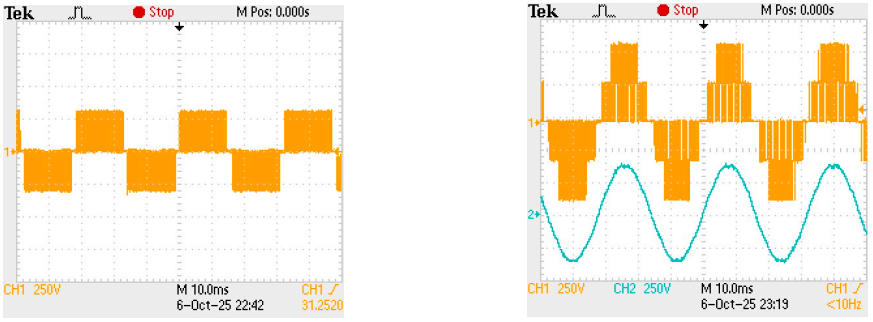
Building on the experimental results in Figure 24, further experiments and analyses were conducted on the midpoint feedback Type II topology. Figure 25 illustrates the voltage fluctuation waveform of the midpoint of the DC bus capacitors and the current waveform between the load-side point n and the midpoint of the split capacitors. The figure shows that the fluctuation amplitude of the midpoint potential of the DC bus capacitors is consistently within 10 V, indicating that this topology provides effective voltage balance control for the bus. In this experiment, the independent split capacitors consist of two 10 μF capacitors connected in series. Experimental data demonstrate that the peak current flowing from the load-side point n to the midpoint of the split capacitors is approximately 20 A. It should be noted that the independent split capacitors are connected in parallel with the DC bus capacitors in the circuit. This topology relies on the independent split capacitors to carry the load-side feedback current, effectively suppressing midpoint potential drift and thus ensuring the operational stability of the DC bus midpoint.



(**a**) (**b**)

Figure 25. (**a**) The neutral point fluctuation in the DC bus capacitor of the neutral point feedback type II topology, (**b**) the *n* point of the load side flowing into the neutral point current of the split capacitor.

Figure 26 illustrates the key output waveforms of the proposed "three-level three-phase four-leg inverter based on independent split capacitors," specifically including the output voltage waveform of Leg A, the output line voltage waveform of Legs A and B, and the load-side line voltage waveform of phases a and b. The experimental waveforms show that the line voltage of Legs A and B exhibits a typical five-level characteristic (i.e., five discrete voltage levels), which is consistent with the output voltage performance of the three-level topology. After processing by the output filter circuit, both the load-side line voltage of phases a and b and the corresponding line current waveform are close to the standard sinusoidal form with excellent smoothness, verifying the effectiveness of the filter scheme for this topology.



(**a**) (**b**)

Figure 26. (**a**) The output voltage waveform of the A bridge arm switch tube of the midpoint feedback type II topology, (**b**) the output line voltage waveform of the AB bridge arm of the switch tube (solid orange line) and the ab line voltage waveform on the output side (solid blue line).

Based on comprehensive simulation and experimental data, the peak leakage current performances of different topologies are as follows: the traditional topology has a simulated value of 24 A and an experimental value of 26 A; the midpoint feedback Type I topology has a simulated value of 11 A and an experimental value of 14 A; while the proposed midpoint feedback Type II topology has a simulated value of only 165 mA and an experimental value of 185 mA. The simulation and experimental results are largely consistent, verifying the accuracy of the analytical model. From the experimental data, it is clearly observed that the midpoint feedback Type II topology exhibits a significant leakage current suppression effect compared to the traditional topology. This advantage stems from the introduction of independent split capacitors: these capacitors provide an additional active discharge path for the common-mode leakage current. Without interfering with the system's original control logic or overall stable operation, the magnitude of the leakage current flowing to the ground is greatly reduced.

In conclusion, the "three-level three-phase four-leg topology with independent split capacitors on the DC bus" proposed in this paper achieves effective leakage current suppression through the synergistic action of the common-mode shunting effect provided by the independent split capacitors and the midpoint potential stabilization mechanism. At the same time, the voltage and current waveforms on the load side maintain good sinusoidal characteristics, meeting the power quality requirements. Particularly importantly, this topology can achieve an excellent balance between leakage current suppression performance and system operational stability without the need for designing additional control strategies, which fully verifies its technical feasibility and advantages for engineering applications.

6. Conclusions

Based on the traditional three-level three-phase four-leg inverter topology, this paper first analyzes the mechanism of leakage current generation. On this basis, a photovoltaic energy storage four-leg inverter topology integrated with independent split capacitors is proposed. By establishing an equivalent mathematical model, a comparative analysis of the performance differences between this topology and the traditional topology is conducted. The improved topology requires no additional control strategies. Under the same control strategy and parameter settings as the traditional topology, it can maintain stable fluctuations in the neutral point potential on the DC side, significantly enhancing leakage current suppression capability while ensuring system stability. Experimental results demonstrate that compared with the traditional topology, the topology based on independent split capacitors reduces the leakage current to within 200 mA and meets the power quality requirements regarding the total harmonic distortion (THD) of the load-side current. This topology still maintains a strong leakage current suppression capability under high-voltage conditions, and the total harmonic distortion (THD) of the current fully complies with relevant standards, demonstrating high engineering practical value.

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