

Article

150-GHz 28-nm CMOS Reflection-Type Phase Shifter Design Suitable for Low-Q Varactor

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Abstract

This paper presents the design and implementation of a D-band CMOS phase shifter based on a parallel reflective-load topology. Two phase-shifting architectures are explored, namely a 360° continuously tunable phase shifter and a 180° phase shifter combined with a phase inverter, enabling full 360° phase coverage. The circuit was simplified, and the number of bias lines was minimized to facilitate future array circuit implementation. In addition, a serial peripheral interface (SPI) circuit is implemented to simplify bias control and reduce the number of external connections during array chip packaging.

Keywords: reflective type phase shifter; D-band; CMOS

1. Introduction

Using higher carrier frequencies for wireless communication is becoming increasingly important for achieving high capacity and low latency. The wide bandwidth at these frequencies is ideal for ultra-fast data transmission, which is crucial for applications such as fixed wireless access and front/backhaul systems, both in urban and rural areas [1]. Research has focused on frequencies below 100 GHz, but due to certain limitations, the D-band is emerging as the new promising frequency range, aided by advances in measurement equipment and hardware technology. There is ongoing research into beamforming systems that use carrier frequencies up to the D-band, focusing on improving both efficiency and performance [2]. Extensive research has been conducted on the development of circuits for D-band beamforming, with the ultimate objective of implementing these circuits in array configurations and integrating them through advanced packaging techniques.

Although most CMOS-based designs have traditionally targeted frequencies below 100 GHz due to limited transistor f_T and f_{max} , the D-band (110–170 GHz) offers significantly wider bandwidth for next-generation wireless links. However, circuit implementation at these frequencies becomes increasingly challenging because of higher conductor losses, varactor quality degradation, and parasitic coupling. Despite these inherent CMOS loss limitations, we have successfully developed a novel circuit design technique to realize a high-performance phase shifter that effectively mitigates the high-frequency challenges.

One of the simplest approaches to implement phase shifting is using transmission delay lines. A 5-bit differential phase shifter employing a transmission delay line was demonstrated in [3], which utilized eight lumped-element cells and operated in the 120–146 GHz frequency range. Similarly, a 3-bit phase shifter based on an SPDT switch, coupler and filter network has also been presented [4]. Delay-line-based designs offer bi-directional operation and low DC power consumption. However, they suffer from significant insertion



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loss, lack of analog control capability, and substantial chip area overhead as the number of bits increases.

To address these limitations, a trombone-like structure has been proposed, where propagation distance is controlled through two parallel transmission lines periodically interconnected via a switch network [5]. While this technique provides improved chip area and flexibility in delay tuning, it still does not enable true analog phase control and requires many switches, which significantly increases the complexity of DC biasing.

The vector-sum phase shifter topology has recently emerged as one of the most widely adopted approaches for high-frequency phase shifting. In this architecture, variable-gain amplifiers are used to control the gain states, while careful device sizing and biasing enable precise phase control. Compact vector-sum phase shifters implemented in BiCMOS technology and operating at D-band and higher frequencies have been presented [6,7]. Additionally, at 60 GHz, techniques have been proposed to minimize impedance variations resulting from phase and gain tuning, thereby reducing phase and gain errors [8]. Despite these advantages, vector-sum phase shifters inherently require many transistors, leading to increased DC power consumption and a high biasing complexity. Without a dedicated serial peripheral interface (SPI), controlling these bias states becomes impractical, and the large number of control lines also complicates system packaging.

Achieving a wide phase-shifting range using RTPS topology at high frequencies is one of the primary challenges in phase shifter design. Conventional approaches to extend the phase range often rely on cascading multiple phase-shifter stages or incorporating phase inverters. For instance, a 250-nm InP HBT implementation demonstrated a full 360° phase shift using two cascaded RTPS stages [9], while designs in 90-nm SiGe BiCMOS and 0.12- μm SiGe process employed two cascaded stages combined with a one-bit phase inverter [10,11]. Although effective, these methods increase chip area, insertion loss, and DC power consumption, making them less suitable for compact and energy-efficient systems.

This work presents a reflection-type phase shifter architecture that achieves continuous 360° phase control using a single phase-shifter core. A passive phase inverter is utilized to minimize DC power consumption and reduce bias-line complexity, while a parallel reflective-load technique is introduced to extend the phase control range. The proposed approach enables a compact, low-loss, and power-efficient solution for D-band phase shifter integration.

2. Proposed Phase Shifter Overview Configuration

In this study, two versions of phase shifters were designed using parallel load termination which is shown in Figure 1.

The first approach, which enables a full 360° phase shift, utilizes only a Lange coupler and a load termination without polarity selection, thereby minimizing chip area while providing a wide phase-shifting range. Additionally, this circuit requires only a single bias line, allowing for bias control without an SPI (Serial Peripheral Interface) circuit in a packaged implementation, which simplifies the overall design.

The second approach, which provides a 180° phase shift, consists of a two-way divider, a switch amplifier, a phase inverter, a two-way combiner, a Lange coupler, and a load termination. Compared with the first approach, this configuration achieves stable 180° phase shifting even with variations in the designed inductance values and offers low loss characteristics. In this architecture, the two-way divider and switch amplifier select the desired phase of the signal, either 0° or 180° , which is then fed into the Lange coupler and subsequently phase-shifted by the load termination. Since two control signals are applied to the switch, an N-channel array implementation would require $2N$ bias lines. To

overcome this limitation, SPI (Serial Peripheral Interface) control is adopted for biasing, while the varactor bias is applied manually.

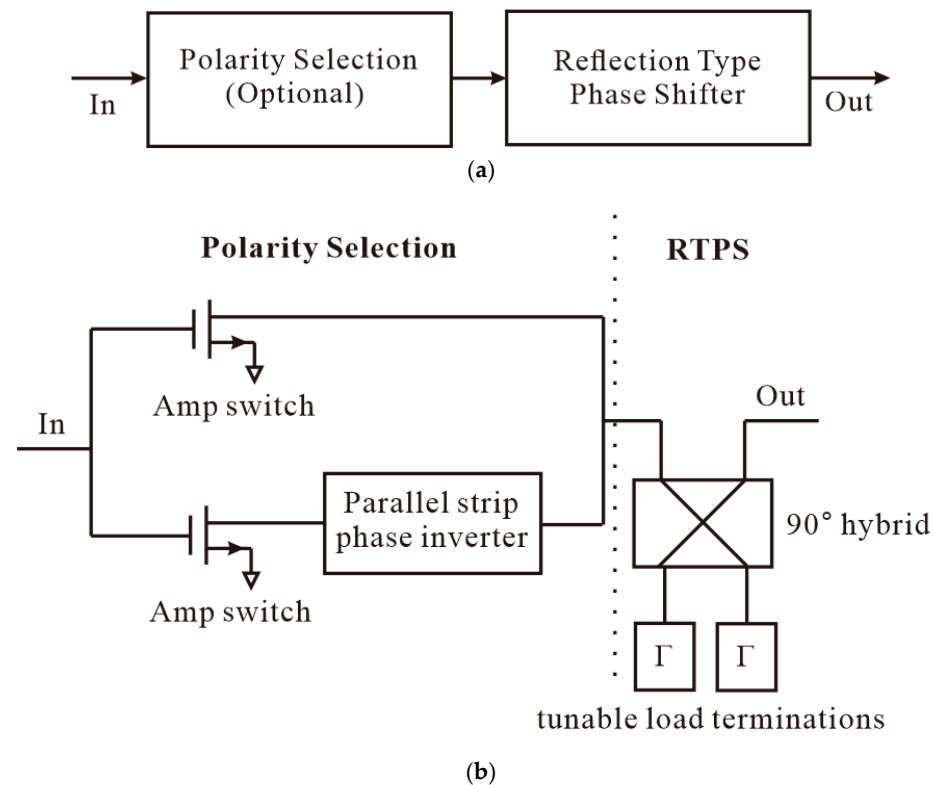


Figure 1. Block diagram of the proposed phase shifter: (a) overall architecture and (b) detailed configuration.

3. Design of Circuit Elements

3.1. Tunable Load Termination

To achieve a wide and continuous phase-shifting capability in D-band phase shifters, various load termination topologies were investigated. Conventional designs are limited by the intrinsic quality factor of the varactor and its relatively small capacitance tuning ratio ($C_{\max}/C_{\min}$), which makes big insertion losses and loss variation caused by impedance change fundamentally restrict the achievable phase-shifting range and in high-frequency applications.

A simple capacitive-load topology, where a single varactor serves as a load termination, provides only about 40° of phase tuning range, rendering it unsuitable for 360° phase shifting. The LC reflective-load topology improves the range slightly by adding a series inductor in front of the varactor; however, its phase-shifting capability rapidly degrades at higher frequencies, and its performance is highly sensitive to inaccuracies in the inductance and capacitance modeling, often resulting in instability.

The CLC- π reflective-load topology, which is widely used in phase shifters, achieves a marginally larger tuning range than the LC topology. Independent control of each varactor within the CLC- π structure can further extend the range, but this requires additional bias lines and significantly increases design complexity, making it less attractive for compact, high-frequency integration.

To overcome these limitations, a parallel LC reflective-load topology was adopted, as shown in Figure 2. This structure employs two LC load terminations connected in parallel with intentionally different inductance values. The inductors are realized using high-impedance transmission lines, allowing precise inductance control and ensuring stable high-frequency operation. By carefully selecting the inductance difference, a trade-off

between gain and tuning range is established: A small inductance difference yields a wide tuning range exceeding 360° but results in relatively lower gain, and a larger inductance difference achieves higher gain at the cost of a reduced tuning range of approximately 180° . This approach provides flexibility to optimize phase shifter performance depending on the target system requirements.

The tuning mechanism of the parallel-LC topology can be summarized as follows: When the varactor capacitance is at its minimum, a series resonance occurs between L_1 , which is derived from the θ_1 transmission line, and C_v . For intermediate capacitance values ($C_{\min} < C_v < C_{\max}$), the L_1 - C_v network becomes inductive, while the L_2 - C_v network becomes capacitive, creating a parallel resonance condition. When the capacitance reaches its maximum ($C_v = C_{\max}$), a series resonance forms between L_2 and C_v .

Although the proposed approach achieves a wide phase-shifting range, it suffers from increased insertion loss and amplitude imbalance due to varactor loss, especially at low bias voltages where the varactor resistance is higher. To mitigate these effects, the matching network was carefully optimized to align the phase rotation axis with the center of the Smith chart, minimizing amplitude variation across the tuning range.

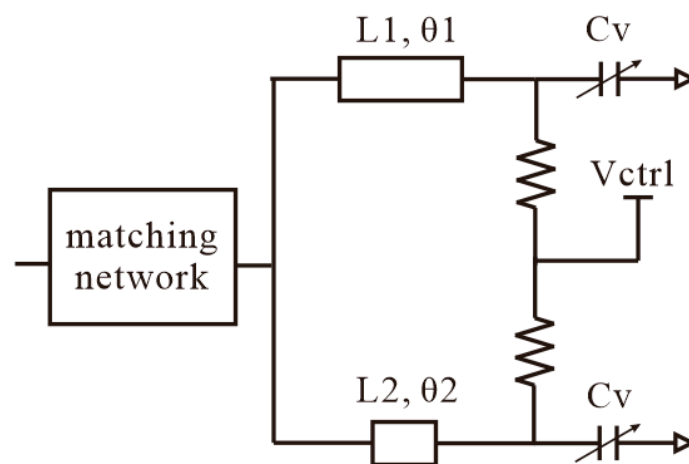


Figure 2. Detailed configuration of tunable load termination.

3.2. Phase Inverter

A parallel-strip phase inverter shown in Figure 3 is implemented using a signal-ground crossover structure to achieve a compact and bias-free phase inversion. The inverter exhibits an insertion loss of 4.9 dB at each port at 150 GHz, with amplitude variation kept below 0.3 dB across the 140~170 GHz band and a phase error of approximately 2.5° per 10 GHz. Compared with active phase-shifting approaches, the passive inverter offers inherently wide bandwidth and reduces DC power consumption by minimizing the number of required bias lines. Furthermore, unlike line-delay-based phase-shifting techniques, this design achieves lower amplitude variation and smaller footprint, as shorter transmission lines are sufficient to realize the desired phase shift. The phase difference is controlled by adjusting the dimensions of the ground slot, while gain balance is fine-tuned through the optimization of line width. This makes the proposed inverter well-suited for compact, low-power millimeter-wave and sub-terahertz front-end systems.

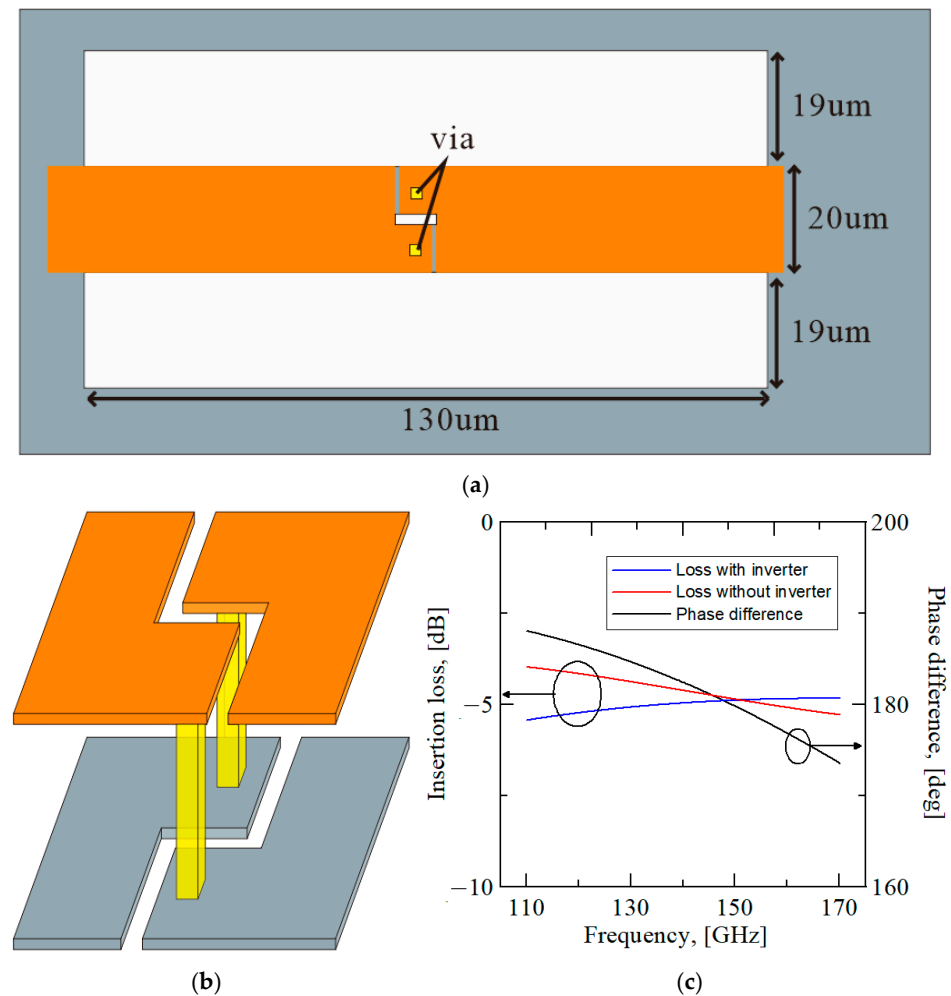


Figure 3. Overall layout of parallel-strip phase inverter (a), detailed cross-over section (b), and EM-simulated S-parameter (c).

3.3. Amp Switch

A single-stage common-base amplifier topology is employed for the switch, enabling compact design and simple bias control. The switch achieves input matching better than -20 dB (S_{11}) at 150 GHz and provides an on-off ratio exceeding 15 dB. In a standalone configuration, biasing is straightforward, while in phased-array implementations, the gate bias is applied globally, and the drain bias is controlled through a serial peripheral interface (SPI) to selectively switch devices on and off.

3.4. 90°. Coupler

A compact Lange coupler designed for D-band operation is implemented using a five-line coupled structure with multiple air-bridges to ensure equal potential across adjacent lines and maintain strong coupling. The coupler achieves a 90.1° phase difference between the through (S_{21}) and coupled (S_{31}) ports at 150 GHz, with a phase variation of 86° – 92° across the entire D-band. Both S_{21} and S_{31} exhibit insertion losses of $-4 \sim -4.2$ dB with less than 0.2 dB amplitude imbalance over the band, while the return loss (S_{11}) remains below -15 dB. The overall footprint of the coupler is $260 \mu\text{m}$ in length and $22.68 \mu\text{m}$ in width, making it highly suitable for integration in compact D-band front-end circuits.

4. Simulation Results of Full Circuit

The first phase-shifter architecture, which is shown in Figure 4, achieves a full 360° phase shift and operates over the 140–160 GHz frequency range. It exhibits an insertion loss

of approximately -22 dB with a loss variation of 3.8 dB. The layout occupies 0.1 mm^2 , and only one bias line is required per channel, simplifying bias control. To achieve wideband operation, the inductance values were carefully tuned so that the phase-shifting range exceeds 360° at the center frequency, effectively minimizing amplitude mismatch caused by varactor capacitance variation.

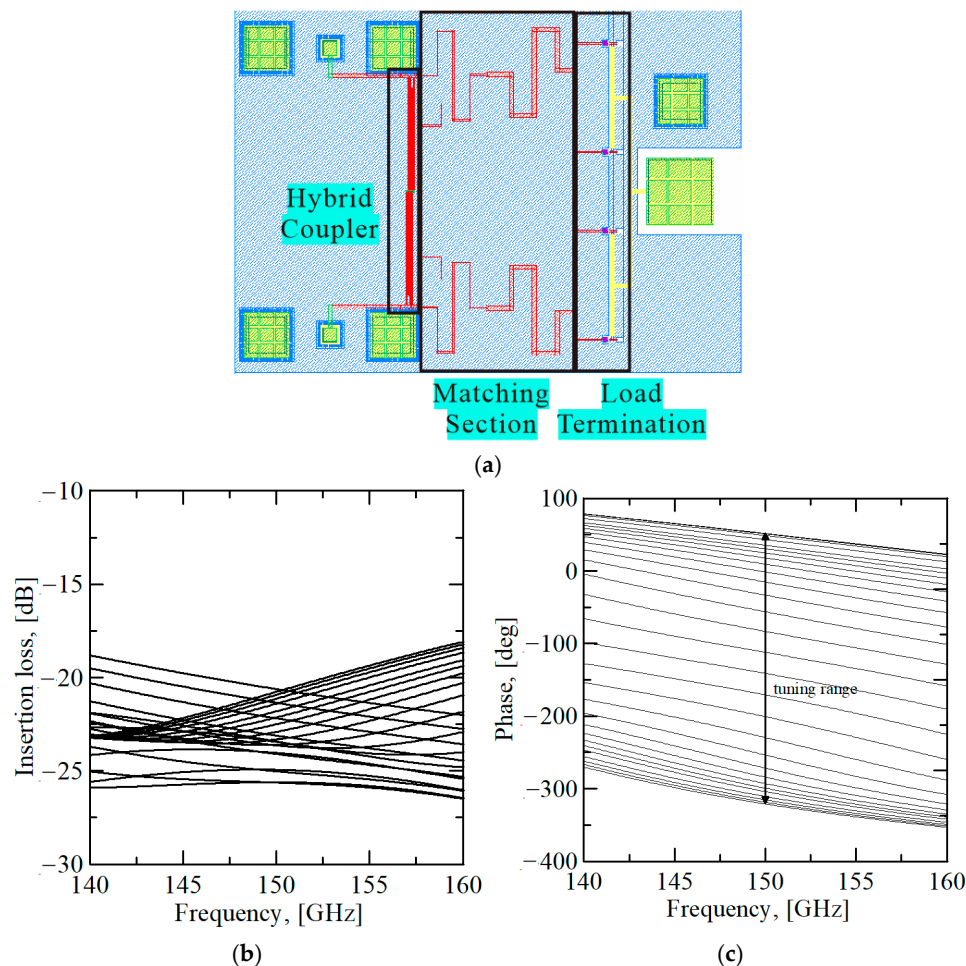


Figure 4. Layout (a) and EM-simulated insertion loss (b) and phase (c) of 360° phase shifter design.

The second phase-shifter architecture, which is shown in Figure 5, provides a 180° phase shift and operates between 145 GHz and 153 GHz with an insertion loss of approximately -20 dB and a loss variation of 4.2 dB . However, if this design is interfaced with a differential port, such as a dipole transition, the two-way divider, combiner, and phase inverter can be eliminated, resulting in a gain improvement exceeding 5 dB . This optimization would enable performance comparable to prior works while maintaining a favorable loss profile, making this architecture highly advantageous for phased-array integration. The layout area is 0.3 mm^2 , and three bias lines are required per channel.

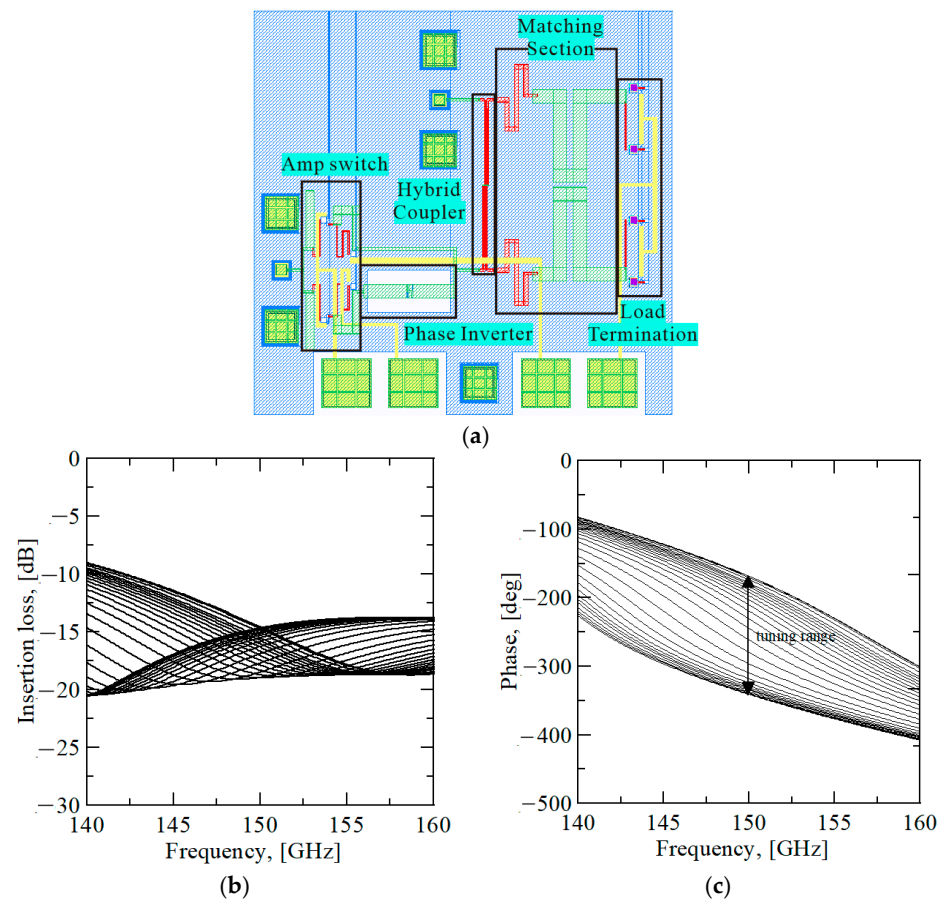


Figure 5. Layout (a) and EM-simulated insertion loss (b) and phase (c) of 180° phase shifter design when differential port is connected.

5. Conclusions

This work presents two compact D-band reflection-type phase shifter (RTPS) architectures designed to achieve wideband and power-efficient phase control for phased-array applications. The first architecture demonstrates a full 360° phase-shifting range over 140–160 GHz using a parallel LC load termination and a single bias line, achieving minimized amplitude variation while maintaining a compact layout. The second design achieves a stable 180° phase shift with improved broadband characteristics and offers opportunities for gain enhancement and reduced loss when interfaced with differential ports. The proposed designs leverage passive components, such as a Lange coupler, reflective load, and passive phase inverter, to simplify biasing and minimize chip area and power consumption. According to the FoM comparison in Table 1, the proposed designs achieve the highest figure of merit among reported D-band CMOS implementations, confirming their superior efficiency and integration capability. These results demonstrate the effectiveness of the parallel LC load termination topology for realizing scalable and energy-efficient D-band beamforming systems.

Table 1. Comparison of previously reported D-Band Reflection-Type Phase Shifters.

No.	Year	Technology	Gain [dB]	Chip Area [mm ²]	Bandwidth [GHz]	Bias Line per Channel	SPI Availability	FoM *
[9]	2022	250-nm InP HBT	−18	0.43	110–163	2	x	2.48
[10]	2022	90-nm SiGe BiCMOS	−5.5	0.57	110–145	9	o	7.01
[11]	2018	0.12- μ m SiGe	−10.2	0.41	116–128	8	o	3.53
[12]	2020	55-nm CMOS	−6	0.36	90–100	≥ 5	o	13.18

Table 1. Cont.

No.	Year	Technology	Gain [dB]	Chip Area [mm ²]	Bandwidth [GHz]	Bias Line per Channel	SPI Availability	FoM *
[13]	2025	65-nm CMOS	−12.1	0.37	136–154	6	o	4.04
This work	2025	28-nm CMOS	−22	0.22	140–160	1	o	4.09
		FD-SOI	−17	0.36	145–153	3	o	2.76

* FoM = (Gain × Bandwidth)/(Chip area × Bias line per channel).

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