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# Thermal Management of Wide-Bandgap Power Semiconductors: Strategies and Challenges in SiC and GaN Power Devices

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**Abstract**

Wide-Bandgap (WBG) semiconductors—silicon carbide (SiC) and gallium nitride (GaN)—enable high-power-density conversion, but performance is limited by where heat is generated and how it is removed. This review links device-level loss mechanisms (conduction and switching, including output-capacitance hysteresis and dynamic on-resistance) to structure-driven hot spots within the ultra-thin (tens of nanometers) two-dimensional electron gas (2DEG) channel of GaN HEMTs and to thermal boundary resistance at layer interfaces. We compare wire-bondless package concepts—double-sided cooling, embedded packaging, and interleaved planar layouts—and survey system-level cooling that shortens the conduction path and raises heat-transfer coefficients. The impact on reliability is discussed using temperature-sensitive electrical parameters (e.g., on-state VDS, threshold voltage, drain leakage, di/dt, and gate current) for real-time junction-temperature estimation and compact electro-thermal RC models for remaining-useful-life prediction. Evidence from recent literature points to interface resistance in GaN-on-SiC as a primary bottleneck, while near-junction cooling and advanced packages are effective mitigations. We argue for integrated co-design—devices, packaging, electromagnetic interference (EMI)-aware layout, and cooling—together with interface engineering and health monitoring to deliver reliable, high-density WBG systems.

**Keywords:** Wide-Bandgap (WBG); silicon carbide (SiC); gallium nitride (GaN); thermal management; power electronics packaging; reliability; co-design; thermal boundary resistance (TBR); temperature-sensitive electrical parameters (TSEPs); microchannel cooling

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## 1. Introduction

The efficient operation of power semiconductor devices in modern power conversion systems is closely linked to global energy efficiency. However, current silicon (Si)-based devices exhibit limitations at high voltage, high temperature, and high frequency, necessitating complex and costly cooling systems. To address these challenges, Wide-Bandgap (WBG) semiconductors, including silicon carbide (SiC) and gallium nitride (GaN), have emerged as materials that enable high-voltage, high-temperature, and high-speed switching owing to their Wide-Bandgap, nearly tenfold higher critical electric field, and superior thermal conductivity [1,2]. SiC offers rapid switching because of its low drift-layer resistance and the absence of minority-carrier storage. Moreover, SiC bipolar devices, particularly those with thin blocking layers, show improved characteristics relative to Si devices. GaN high electron mobility transistors (HEMTs) provide high power density and efficiency at

high frequency, enabling miniaturization and easing cooling requirements. Accordingly, WBG semiconductors are positioned to overcome key constraints of Si technologies in electric vehicles, aerospace, and renewable energy [2,3]. Despite these advantages, critical thermal bottlenecks remain. In particular, localized self-heating and the limited maturity of high-temperature packaging present significant hurdles. For example, although SiC has high thermal conductivity, it still requires advanced heat dissipation at the package level, whereas GaN faces challenges in thermal dissipation and reliability due to its lower thermal conductivity and heterojunction architecture [1,2]. Furthermore, defects introduced during SiC crystal growth and degradation in bipolar devices significantly impede reliability, while GaN can suffer performance degradation due to elevated field stress, intrinsic crystalline defects, and long-term stability issues associated with high dislocation density [1,3]. While numerous excellent reviews have addressed specific aspects of WBG thermal management—such as advanced packaging architectures or novel cooling solutions—a significant research gap remains in providing a holistic, multi-scale perspective that links device-level physics with system-level reliability. For example, challenges at the nanometer scale, including thermal boundary resistance (TBR) across AlGaN/GaN heterointerfaces only tens of nanometers thick, are often treated in isolation from macroscale packaging and cooling decisions. Moreover, reliability concerns, such as long-term degradation under mission profiles, are seldom integrated into these discussions. This review addresses these shortcomings by systematically connecting the fundamental heat-generation mechanisms in WBG devices with packaging, cooling, and reliability strategies required for robust system-level thermal design.

## 2. Thermal Generation in SiC and GaN Power Devices

### *2.1. Fundamental Thermal Properties and Loss Mechanisms*

The performance and reliability of power semiconductor devices are fundamentally influenced by intrinsic thermal properties and the loss mechanisms that occur during operation. SiC and GaN can operate under high-voltage and high-temperature conditions thanks to their Wide-Bandgaps (2.9–3.4 eV) and critical electric field strengths (2.2–4 MV $cm^{-1}$), outperforming conventional Si in these regimes [2–5]. These characteristics make them highly suitable for applications requiring high power density and high-efficiency power conversion. SiC exhibits high thermal conductivity (3.3–4.9 W $cm^{-1}$ $K^{-1}$; approximately 330–490 W $m^{-1}$ $K^{-1}$), enabling superior heat removal. GaN's thermal conductivity decreases with temperature [2,6]. In GaN-based structures, TBR at the substrate interface becomes a significant thermal bottleneck; aluminum nitride (AlN) buffer layers and interfacial defects increase TBR, and acoustic-phonon scattering exacerbates this at elevated temperatures [7,8].

#### 2.1.1. Conduction Losses

Conduction losses scale approximately with $I^2R_{DS(on)}$; $R_{DS(on)}$ itself increases with temperature (and can vary with bias). SiC mitigates conduction losses through its low drift-layer resistance, whereas GaN benefits from high electron mobility. Nevertheless, under specific operating conditions, GaN conduction losses can rise markedly, and for both device types, $R_{DS(on)}$ tends to decrease at lower temperatures [9,10].

#### 2.1.2. Switching Losses

Switching losses occur during the transient overlap of voltage and current; higher switching speeds in WBG devices can markedly reduce these losses. GaN typically exhibits lower switching losses than SiC due to lower gate and drain charge and higher carrier mobility. For example, GaN current-aperture vertical electron transistors (CAVETs) have

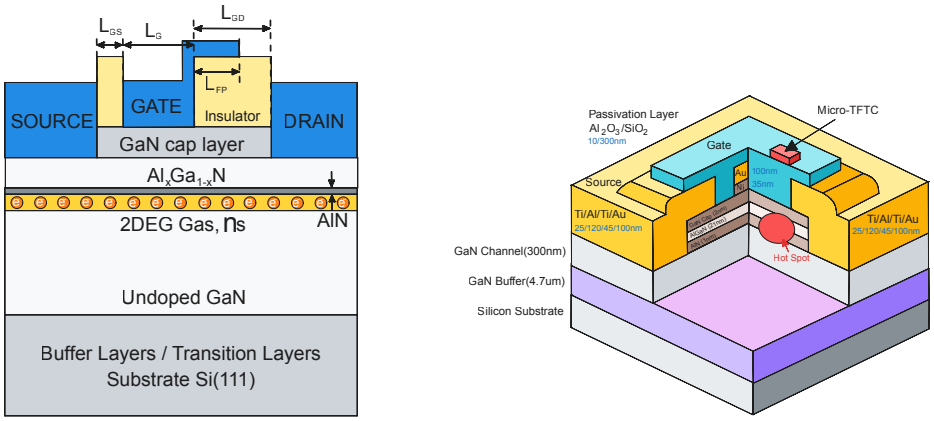
demonstrated approximately twice the switching speed and about one-third the switching loss of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) [10]. In addition, SiC devices are not affected by minority-carrier storage, facilitating rapid switching and further loss reduction as temperature decreases [1,11].

#### 2.1.3. Other Switching-Related Phenomena

Other switching-related phenomena also contribute to energy dissipation. Reverse-recovery loss is negligible for GaN HEMTs (no minority-carrier body diode), whereas in SiC MOSFETs it is lower than in Si MOSFETs but not negligible. By contrast, losses associated with output capacitance ($C_{OSS}$), gate charge, and voltage overshoot from parasitic inductance are often more significant [4,12,13]. In GaN devices, dynamic degradation—observed as an increase in $R_{DS(on)}$ during switching—may occur due to trapping effects, and its severity can escalate at higher operating frequencies. Reported measurements indicate that dynamic $R_{DS(on)}$ increases monotonically from several hundred kHz up to approximately 2 MHz under hard-switching stress, after which the effect tends to saturate as the switching period becomes shorter than the trapping/detrapping time constants. The magnitude of degradation strongly depends on test conditions: higher off-state drain bias and longer stress duration exacerbate trapping, hard-switching produces significantly larger resistance increases than soft-switching, and large drain current or low duty cycle further intensifies the effect. Accurate characterization of these losses remains challenging, since measurements must capture both high off-state voltages and millivolt-level on-state resistance within wide dynamic ranges, and conventional double-pulse test methods often underestimate steady-state degradation. These factors make loss separation and quantification in GaN and SiC devices highly non-trivial [14,15].

### *2.2. Device Structure and Localized Heating*

Effective thermal management in power semiconductor devices is fundamental to ensuring both performance and reliability. In particular, device structure directly affects localized heat intensification and hotspot formation. Devices utilizing SiC and GaN as WBG materials offer high efficiency and high-voltage capability; however, heat generation can concentrate in specific regions, limiting maximum power density and reducing lifetime [1]. Heat-generation pathways differ across device types. SiC MOSFETs comprise resistive components—including the channel, junction field-effect transistor (JFET) region, and drift layer—that act as primary heat sources. Of these, channel and JFET resistances dominate at lower voltage ratings, whereas the drift layer becomes the main contributor at higher voltages (above 3 kV) [2]. In contrast, GaN HEMTs conduct current through a two-dimensional electron gas (2DEG) formed within the AlGaN/GaN heterostructure, focusing conduction losses into an ultrathin channel and thereby intensifying localized heating [1,3,16,17]. The structural characteristics of GaN HEMTs introduce several unique thermal challenges. They are prone to hotspots in the gate-drain region, where high electric fields lead to hot-electron effects, trap generation, and the reverse piezoelectric effect, degrading performance and reliability [18–20] (Figure 1). Electroluminescence (EL) imaging confirms this, showing localized emission in field-crowding regions consistent with trap formation and current reduction [21]. Furthermore, because native GaN substrates are scarce, GaN HEMTs are typically grown on foreign substrates (Si, SiC, or sapphire). This heteroepitaxy yields high TBR at the interface, which raises channel temperature and complicates operation at high power densities [16]. Even cascode GaN devices—which stack a GaN HEMT and a Si MOSFET to reduce parasitics—introduce a complex thermal path that can elevate junction temperature and must be managed carefully [22,23].




(**a**) (**b**)

**Figure 1.** Structure of a GaN HEMT and an associated thermal hotspot. (**a**) Schematic of a GaN HEMT showing the AlGaN/GaN heterostructure and key device regions [1]. (**b**) Cross-section showing typical hotspot formation in the gate–drain region due to high electric fields [18].

Consequently, accurate temperature-field mapping and structure-aware thermal analysis are essential for devising effective cooling strategies and ensuring reliability, as localized hotspots degrade performance and can trigger failure [18,24].

## 3. Thermal Management Solutions for WBG Power Devices: Advanced Packaging and Cooling Techniques

### *3.1. Thermal Pathways and Packaging Materials*

Maximizing WBG device performance and reliability requires efficient thermal pathways and high-reliability packaging materials. Conventional wire bonding is often unsuitable for WBG devices, which switch rapidly [25–27]. For substrates, SiC (in GaN-on-SiC) offers a significant thermal advantage, exhibiting high thermal conductivity of 3.3–4.9 $W\,cm^{-1}\,K^{-1}$ (approximately 330–490 $W\,m^{-1}\,K^{-1}$). GaN-on-Diamond can further reduce channel temperature owing to the diamond substrate's thermal conductivity exceeding 700 $W\,m^{-1}\,K^{-1}$, thereby enhancing both performance and lifetime [1,2,28,29]. Because native GaN substrates remain limited, GaN is predominantly grown heteroepitaxially on Si, sapphire, or SiC, which can introduce heat-transfer bottlenecks [3,19]. Die-attach and top-side interconnection technologies are critical to thermal robustness and reliability under high-temperature operation. Traditional Sn-based solders are constrained by relatively low melting points and intermetallic compound (IMC) formation [30], motivating high-reliability alternatives [31]. IMC growth is often accelerated by microstructural defects at the solder interface (e.g., grain boundaries, oxides, interfacial roughness), which act as heterogeneous nucleation sites; in addition, unbalanced Cu/Sn interdiffusion can induce Kirkendall voiding, degrading thermo-mechanical integrity over life [30,32]. Silver-sintered joints provide excellent electrical/thermal conductivity and high-temperature stability but face electromigration (EM) and cost challenges [2,30–35]. Copper-sintered joints offer comparable performance with improved EM resistance, though oxidation control and process windows remain nontrivial [1–3,31,36–38]. As another approach, transient liquid phase (TLP) bonding achieves stable IMCs after low-temperature bonding, improving high-temperature reliability [3,30]. TBR is a significant component of the overall thermal resistance in GaN-on-SiC, where AlN nucleation and defect layers elevate interface resistance. To mitigate TBR, surface-activated bonding (SAB) has emerged as a promising interface technology, enabling high-quality interfaces and thermal boundary conductance (TBC) values approaching 230 $MW\,m^{-2}\,K^{-1}$ [1,2,39]. In summary, meeting the high-power-density demands of WBG devices requires a materials-and-interfaces-centric strategy:

select high-conductivity substrates, minimize TBR, and deploy die-attach and top-side interconnections with proven high-temperature stability. Paired with the advanced package architectures detailed in Section 3.2, this approach is instrumental in elevating WBG system effectiveness [3,30].

### *3.2. Advanced Package Architectures*

Conventional wire bonding, originally developed for Si devices, is a bottleneck that limits the attainable switching speed and power density of WBG packages. The constraints arise from three factors: substantial parasitic inductance, restricted vertical heat removal, and reduced reliability under thermomechanical stress—all of which degrade performance and lifetime [25–27,40]. To address these limitations, wire-bondless top-side interconnections have gained traction. Representative solutions include copper fins, ribbons, clips, thin films, and Cu-sintered paste interconnects, which together reduce parasitic elements and improve heat spreading [19–21]. In parallel, silver and copper microparticle sintering and transient liquid-phase bonding are recognized as reliable assembly approaches that combine excellent electrical/thermal conductivity with high-temperature stability [2,3,30] (Figure 2).

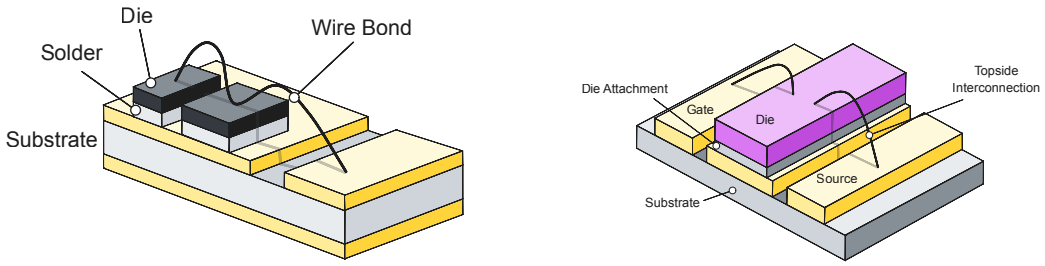



**Figure 2.** Comparison of conventional and advanced top-side interconnection technologies. (**a**) Conventional wire bonding, characterized by long, thin wires that introduce significant parasitic inductance and limit vertical heat dissipation [40]. (**b**) Advanced wire-bondless top-side interconnection (e.g., copper clips or ribbons) for reduced parasitic inductance and an improved thermal path [27].

#### 3.2.1. Double-Sided Cooling (DSC)

DSC enhances heat removal by extracting heat from both top and bottom surfaces, thereby lowering thermal resistance and equalizing temperature distribution. Copper-clip structures reduce thermal resistance by approximately 20% [27] versus single-sided layouts, while flip-chip bonding further mitigates parasitic inductance. The use of thermally conductive adhesive films (TCAFs) reduces interfacial thermal resistance. DSC has been widely implemented in SiC MOSFET high-power modules and is considered essential for extending device lifetime under high thermal loads [26,41–44].

#### 3.2.2. Embedded Packaging

Embedded packaging places power dies inside the printed circuit board (PCB), which lowers parasitic inductance/capacitance, reduces package height, and creates an efficient vertical thermal path. In SiC MOSFET modules, this approach has cut parasitic inductance by up to 87.6%, down to 1.24 nH [27]. When combined with substrate-embedded microchannels for localized convective cooling, the junction temperature can drop by approximately 50 °C, enabling more than 22% [27] higher saturation current due to improved thermal uniformity. The embedded paradigm also provides inherent electromagnetic interference (EMI) shielding and significantly improves robustness against thermal cycling and electrical overstress [29,45–49]. The typical process flow is illustrated in Figure 3.

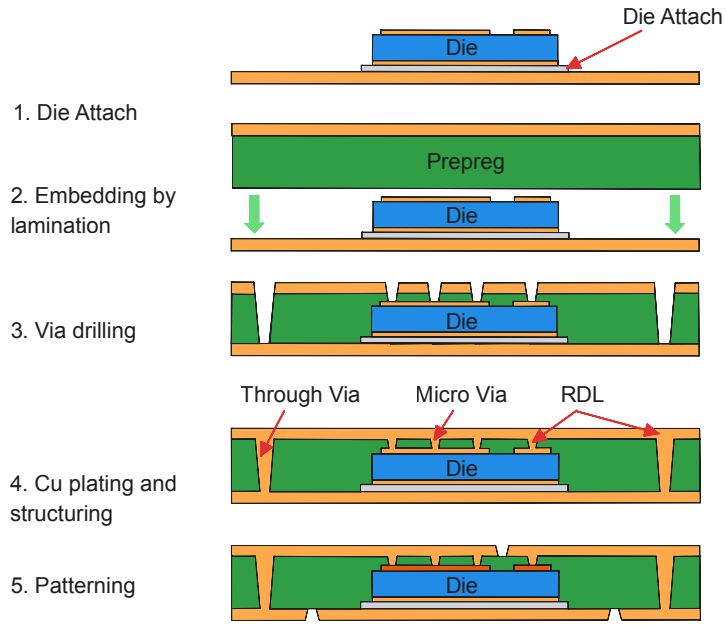



**Figure 3.** Process flow of embedded packaging technology. The sequence shows (1) die attachment, (2) lamination, (3) via drilling, (4) copper plating and structuring to form interconnections, and (5) final patterning [27].

#### 3.2.3. Interleaved Planar Packaging

Interleaved planar packaging addresses die-to-die thermal and electrical coupling in parallel-connected WBG modules. The Interleaved Switch Unit (ISU) architecture achieves a 57% [40] reduction in thermal coupling resistance via vertical (z-axis) thermal separation, improving thermal decoupling. In addition, the Current Commutator Structure (CCS) balances current distribution and reduces loop inductance to 3.8 nH [40], thereby improving transient performance and current sharing. Experiments at elevated temperature show a 20 °C [40] lower junction temperature relative to conventional planar packaging, while maintaining current imbalance within 6% [40]. Overall, interleaved planar packaging provides a robust, electromagnetically optimized, and scalable integration path for next-generation high-density WBG modules (Figure 4).

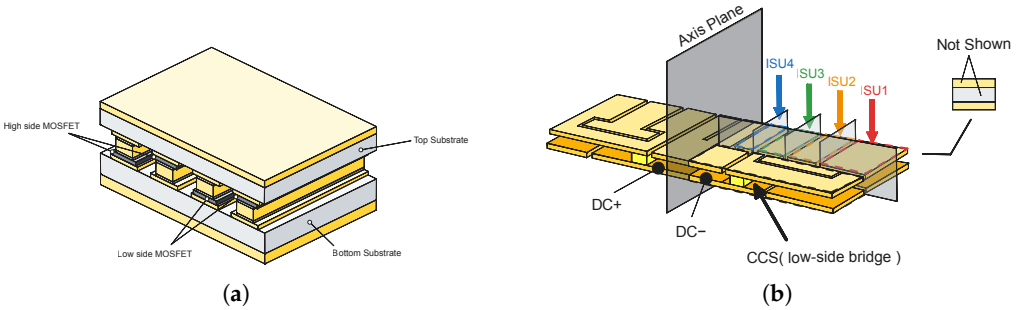



**Figure 4.** Architecture of an interleaved planar package. (**a**) Cross-sectional view showing the vertical arrangement of high-side and low-side MOSFETs. (**b**) Isometric view illustrating key components: the Interleaved Switch Unit (ISU) for thermal decoupling and the Current Commutator Structure (CCS) for current balancing [40].

### *3.3. System-Level Cooling Techniques*

The high-temperature, high-voltage, and high-frequency operating characteristics of WBG devices increase power density and heat flux, underscoring the need for advanced system-level thermal management. Among WBG materials, GaN poses greater thermal-management challenges than SiC due to its relatively low thermal conductivity [1,2,29].

Conventional approaches face inherent limits in high-density WBG systems. Air cooling, while simple and cost-effective, lacks the heat-transfer capacity to manage the intense heat flux generated by WBG devices. Although SiC-based converters can maintain thermal stability with fan-assisted heat sinks, effectiveness is limited under high-power or thermally stressed conditions [26]. Indirect liquid cooling via cold plates offers moderate improvement; however, the extended thermal path between heat sources and coolant yields a thermal resistance of 0.3–0.4 $K\,cm^2\,W^{-1}$, which is often above the approximately 0.2 $K\,cm^2\,W^{-1}$ target needed for compact, high-performance WBG applications [1,26,29]. To overcome these limitations, advanced techniques pursue two goals: shorten the thermal conduction path and maximize the heat transfer coefficient (HTC). Direct liquid cooling improves heat removal by bringing coolant into direct contact with the chip or substrate surface, thereby reducing TBR and increasing heat-transfer efficiency [29,50,51]. Jet impingement cooling uses high-speed jets from micro-nozzles to target hotspots, achieving high HTC; it is effective for thermally demanding devices such as GaN monolithic microwave integrated circuit (MMIC) power amplifiers [29,52–54]. Phase-change cooling leverages latent heat (e.g., heat pipes) for rapid heat removal. Microchannel cooling routes coolant through tens to hundreds of μm channels etched in or beneath the substrate; embedded microchannels further shorten the conduction path and have demonstrated up to a 43% [29] reduction in thermal resistance while mitigating self-heating and thermal coupling in dense power modules [55–58]. In summary, direct liquid cooling, jet impingement, phase-change, and embedded microchannel cooling are key options that extend beyond conventional solutions and enable compact, efficient, and thermally robust architectures for next-generation WBG power conversion [29,50–58].

To provide a clear comparative perspective, Table 1 consolidates the key performance improvements, practical advantages, and trade-offs of representative packaging and cooling techniques discussed in this section.

**Table 1.** Comparative and quantitative summary of advanced packaging and cooling techniques for SiC and GaN power devices, highlighting key performance improvements, advantages, trade-offs, and primary applications.

| Technology | Key Performance Improvements | Advantages | Disadvantages/Trade-Offs | Primary Applications |
|---|---|---|---|---|
| **Double-Sided Cooling** | • $R_{th}$ reduction: 20–48% (vs. single-sided) [27,42]<br>• Low $L_p$ with wire-bondless structures | • Low overall $R_{th}$<br>• Uniform temperature distribution [26,51] | • Susceptible to thermo-mechanical stress [42]<br>• Requires coordinated top/bottom thermal design | • EV/HEV traction inverters<br>• High-power modules [26,50] |
| **Embedded Packaging** | • $L_p$ reduction: up to 87.6% (<1.24 nH) [45–47]<br>• $R_{th}$ reduction: 30–48% (with DSC) [42,44] | • Very low $L_p$<br>• EMI shielding<br>• Package miniaturization [46–48] | • High thermo-mechanical stress<br>• High process complexity and cost<br>• Difficult rework [27,49] | • High-frequency DC/DC<br>• Integrated power systems [45] |
| **Interleaved Planar** | • Thermal coupling reduction: ∼57%<br>• $L_p$ as low as 3.8 nH [40] | • Balances current/temperature in parallel devices<br>• Mitigates 2D thermal coupling [40] | • High structural complexity<br>• Potential manufacturability challenges | • High-reliability, multi-chip modules [40] |
| **Jet Impingement** | • $R_{th}$ reduction: up to 64.3% (vs. indirect) [52] | • Very high HTC<br>• Effective direct hotspot cooling [52,53] | • High pumping power required (∼5×) [52]<br>• Increased system complexity<br>• Potential leakage risk | • Military and aerospace<br>• Very-high-power-density electronics [52] |

**Table 1.** *Cont.*

| Technology | Key Performance Improvements | Advantages | Disadvantages/Trade-Offs | Primary Applications |
|---|---|---|---|---|
| **Microchannel** | • $R_{th}$ reduction: up to 43.14% (vs. indirect) [29] | • Enables near-junction cooling<br>• Shortens thermal path [29] | • High fabrication complexity and cost<br>• Large pressure drop<br>• Potential channel clogging [55] | • High-frequency RF amplifiers (e.g., GaN MMIC)<br>• Dense power modules [29] |
| **Direct Liquid** | • $R_{th}$ reduction: ≈30% (vs. indirect) [51] | • Eliminates TIM layer<br>• Improved heat-transfer efficiency [50] | • CTE mismatch risk<br>• Potential leakage and corrosion risk [50] | • Automotive power modules<br>• High-performance motor drives [51] |
| **Indirect Liquid** | • Conventional baseline; moderate $R_{th}$ | • Mature, reliable, cost-effective<br>• Compatible with existing infrastructure [26] | • Limited by TIM-layer resistance<br>• Thermal grease degradation over time [51] | • General-purpose industrial PSUs<br>• Data center applications [26] |

## 4. Reliability Issues and Thermal Modeling

### *4.1. Overview of Reliability Issues and Assessment Methodologies*

While the advantages of WBG semiconductors such as SiC and GaN are well established, ensuring their long-term reliability and accurately forecasting their operational lifespan remain critical challenges [1,2,59]. Reliability concerns in SiC primarily stem from various crystallographic and point defects, whose propagation can be accelerated by thermo-mechanical stress. Extended defects such as micropipes, basal plane dislocations (BPDs), and stacking faults increase leakage current and reduce breakdown voltage [60–62], while deep-level point defects (such as the Z1/2 and EH6/7 centers) act as carrier recombination centers that shorten carrier lifetime [2]. Fundamentally, understanding the link between such structural defects and the resulting electronic and thermal properties often relies on atomistic modeling approaches like Density Functional Theory (DFT) [63]. Furthermore, degradation of bonding materials and metal electromigration at elevated temperatures undermines long-term stability [19,64]. The reliability of GaN HEMTs is affected by several degradation mechanisms rooted in their heteroepitaxial structure. Hot-carrier effects, for instance, can generate new charge trapping centers, such as interface traps at the AlGaN/GaN interface or point defects (e.g., vacancies) within the GaN buffer, leading to phenomena like current collapse and increased gate-leakage current [19]. In particular, transconductance degradation and gate lag are observed under "semi-ON" operating conditions, and the EL technique enables real-time evaluation of hot-carrier distributions [19,64]. Accelerated life testing (ALT) is critical for analyzing degradation and failure mechanisms. High-temperature gate bias (HTGB), high-temperature reverse bias (HTRB), power cycling (PC), and thermal cycling (TC) efficiently identify vulnerable failure modes within short durations and facilitate parameterization of lifetime-prediction models [64,65]. While well-established industrial standards from the Joint Electron Device Engineering Council (JEDEC)—such as JESD22 (thermal and electrical stress tests) and JESD47 (qualification procedures)—and from the Automotive Electronics Council (AEC), including AEC-Q100 and AEC-Q101 for automotive ICs and discrete devices, provide a crucial framework for reliability assessment, their direct application to WBG devices remains limited. These standards, which rely on stress tests such as HTGB, HTRB, TC, and temperature–humidity bias (THB), were originally designed for Si technologies and do not fully capture WBG-specific degradation mechanisms such as dynamic $R_{DS(on)}$ shifts or TBR-induced hotspots. Moreover, the elevated operating temperatures of SiC and GaN may activate new failure modes with high activation energies that are absent in conventional Si operation, making lifetime extrapolation from Si standards potentially misleading. Consequently, the development of WBG-specific qualification methodologies is an active area of focus for industry bodies, in-

cluding the JEDEC JC-70 committee [66]. Thermal management is directly linked to device reliability. Thermal stress accounts for approximately 60% of primary failure causes [67], and accurate estimation of junction temperature ($T_j$) is essential for reliable lifetime prediction. Analytical methods such as coupled electro-thermal analysis, lumped thermal models (LTM), and the finite element method (FEM) are used to predict $T_j$ and identify hotspots [64,68–70]. Temperature-sensitive electrical parameters (TSEPs) are widely used for real-time thermal monitoring and early fault detection. Representative TSEPs include $V_{DS(on)}$, threshold voltage ($V_{th}$), drain leakage current ($I_{dss}$), $dI/dt$, and gate current ($I_{gp}$); these parameters reflect accumulated thermal stress and form the basis of condition-based maintenance strategies [64,71]. They are also leveraged in active thermal-control implementations. Taken together, an integrated approach—combining reliability-mechanism analysis, ALT, thermal modeling, and real-time monitoring—is essential to ensure the long-term operational capability and safety of WBG devices.

### *4.2. Health Monitoring and Lifetime Prediction Techniques*

In SiC- and GaN-based power systems that demand high reliability, health-monitoring-based thermal and electrical diagnostics are essential for proactive fault identification and lifetime estimation. Conventional manual inspections are limited, especially under high switching density and elevated temperatures, motivating the development of active health monitoring technologies [64,65]. TSEPs serve as key diagnostic metrics: they indicate cumulative thermal stress and enable real-time estimation of junction temperature ($T_j$). Representative TSEPs include $V_{DS(on)}$, $V_{th}$, $I_{dss}$, Miller plateau voltage, $dI/dt$, and $I_{gp}$, which can also signal potential failure or package degradation [64,71–74]. These real-time, metric-driven prediction approaches fall into two broad categories. Physics-of-failure (PoF) models rely on the underlying mechanisms of specific failure modes—such as thermal fatigue, adhesive degradation, and oxide deterioration—and often employ cumulative damage laws (e.g., Miner's rule). Data-driven methods use empirical TSEP streams and operational histories to improve lifetime-prediction accuracy, leveraging machine learning, dynamic Bayesian networks (DBN), and dynamic reliability block diagrams (DRBD) [65,75]. Recently, for remaining useful life (RUL) estimation from time-series data, failure-correlation models have been used to track degradation and its relationship to environmental stressors such as high temperature, humidity, and mechanical vibration. Notably, multi-stress interactions are significant in WBG devices, making reliability difficult to predict with single-variable models [64]. Furthermore, recent advanced models have begun to address the non-uniform temperature distributions and localized hotspots that are particularly severe in WBG devices. Traditional lifetime models that rely on average junction temperature can lead to inaccurate RUL predictions. To overcome this, new methodologies explicitly incorporate on-chip temperature distributions. For example, Wu et al. proposed a wire-bond degradation model that accounts for the different temperature swings experienced by individual bond wires, enabling more precise RUL estimation by modeling the progressive failure of multiple wires rather than only the first one [76]. Incorporating spatial thermal gradients in this manner represents a significant step toward more realistic and physically accurate lifetime prediction. In summary, as high-speed switching and high-density designs become commonplace, passive thermal management and static design alone are insufficient. A comprehensive health-monitoring framework—combining real-time sensing, precursor detection, and lifetime prediction—is a prerequisite for broader industrial adoption of SiC and GaN devices.

### *4.3. Thermal-Aware Design for Extended Lifetime*

Building on the reliability assessment and monitoring techniques discussed above, a thermal-aware design philosophy integrates these elements to proactively ensure long-term device reliability. WBG devices experience elevated thermal stress due to high switching frequencies and power densities, which gradually degrades bonding wires, solder interfaces, and gate oxides through repeated power cycling [64,65]. Accordingly, ALT—including HTGB, HTRB, and PC—is applied to forecast and address underlying damage mechanisms, with PoF models often using Miner's rule for life prediction [64,65]. At the system level, DRBDs and DBNs capture temporal dependencies and interconnections for reliability assessment [65]. TSEPs enable real-time state monitoring. Key examples include $V_{DS(on)}$, $V_{th}$, $I_{dss}$, Miller plateau voltage, and $I_{gp}$. Notably, for SiC MOSFETs the low temperature dependence of $R_{DS(on)}$ and its higher sensitivity to gate-source voltage ($V_{gs}$) warrant care in interpretation [64]. Optimizing the thermal-resistance path is critical for reliability improvement. Dimensions of solder-mask openings, selection of high-conductivity die-attach materials, and the strategic arrangement of vias together reduce junction-to-die, die-to-sink, and junction-to-ambient thermal resistances. For example, increasing the via count from 4 to 25 reduced the peak temperature of the power amplifier by approximately 52% (from 492.956 °C to 234.836 °C) [77]. In electro-thermal simulations, FEM-derived compact RC electro-thermal network models predict $T_j$ dynamics and support RUL assessment [68,69,78]. These models, often structured as Cauer or Foster networks, derive their thermal resistance ($R_{th}$) and capacitance ($C_{th}$) parameters by fitting the network's response to transient thermal data. This data is typically generated either from detailed Finite Element Method (FEM) simulations or, as demonstrated by Xu et al., from experimental thermal impedance measurements and datasheet curves [68]. Beyond lifetime estimation, these models integrate naturally with thermal-path optimization and control-oriented dynamic thermal management. In summary, a comprehensive thermal-aware design strategy—combining PoF-based lifetime models, TSEP-based temperature estimation, thermal-path optimization, and integrated modeling—is essential for early detection of failure mechanisms and for ensuring the reliability of thermally sensitive WBG devices [79].

## 5. Technology Integration and Patent Trends

### *5.1. Co-Design and Integration Strategies*

SiC- and GaN-based WBG power semiconductors offer a Wide-Bandgap, high critical electric field, and excellent thermal conductivity, enabling high efficiency, high power density, and operation at elevated temperatures. Realizing these device-level advantages at the system level, however, requires a multidisciplinary co-design approach that jointly considers device physics, packaging, circuit topologies, gate drivers, EMI filters, and cooling—beyond optimizing isolated components [10–12,27,80,81]. High switching speed enables higher power density and smaller passives, but it also introduces voltage overshoot, increased EMI, switching losses, and thermal stress. These fast-transient behaviors couple through parasitic inductance and layout, and dynamic changes in $R_{DS(on)}$ can trigger thermal runaway. Accordingly, simultaneous optimization of electrical performance, thermal behavior, and mechanical integrity is essential [10–12,27,82]. From a reliability perspective, WBG devices exhibit failure modes distinct from Si. In SiC, BPDs and threading edge dislocations (TEDs) shorten carrier lifetime and raise leakage current [2], while gate-oxide traps and $V_{th}$ instability are additional concerns [2,64]. Elevated current density accelerates electromigration, worsening solder-layer degradation and self-heating variability [64]. GaN devices involve a complex interplay of self-heating, current collapse, and hot-carrier degradation [3,12,19,83]. Under "semi-ON" conditions, transconductance

degradation driven by hot carriers is often observed, and at higher drain-source voltage $V_{DS}$ (approximately 30–50 V), the reverse piezoelectric effect and AlGaN barrier breakdown can increase gate leakage [19]. To address these mechanisms within a unified framework, temperature-sensing and condition monitoring must be integrated into the co-design loop. TSEP-based monitoring can separate the temperatures of the internal HEMT and the Si MOSFET in cascode GaN via reverse-current analysis [23], while $dI/dt$ and $I_{gp}$ are commonly used in SiC MOSFETs [64,71]. These diagnostics improve observability but introduce cost and complexity that must be balanced at the system level [64]. Packaging and layout co-optimization further reduces the coupling between fast transients, thermal hotspots, and EMI. DSC, embedded packaging, and interleaved planar structures mitigate current imbalance across parallel dies and reduce parasitics [10,40,45,82]. Cu-based interconnections (Cu clips, Cu sintering, etc.) can cut loop inductance from 14 nH to 2.37 nH versus wire bonding, thereby lowering EMI and switching losses [25,27]. Cu sintering is effective at high temperature, though conductivity degradation and residual-stress sensitivity remain process-dependent [84]. Finally, substrate and interface engineering is essential to limit TBR while sustaining electrical performance. GaN-on-Diamond offers exceptional thermal conductivity, but a high TBR can be performance-limiting, motivating measures such as via-hole insertion [7,8,83]. In parallel, optimizing GaN layer thickness helps redistribute heat flux and relieve hotspots; three-dimensional (3D) simulations indicate that doping-layer thickness strongly affects temperature beneath the gate [7,28,29]. In sum, industrial realization of SiC and GaN demands system-level co-design that closes the loop among devices, interconnects, layout/EMI control, and cooling, with shared targets (power density, EMI compliance, $\Delta T_j$, and lifetime). Such an integrated strategy is foundational for the next phase of technological progress.

### *5.2. Patent-Based Analysis of Integration Trends in WBG Power Semiconductors*

To examine how the co-design strategies outlined in Section 5.1 translate into practice, this section analyzes patent trends in WBG power electronics and highlights representative families that catalyzed electro-thermal co-optimization.

**Methodology.** We queried WIPS ON (accessed on 4 September 2025, KST) for patent families filed in 2010–2025, focusing on Wide-Bandgap (SiC and GaN) power devices with relevance to packaging and thermal integration. To avoid pulling Si-only results, we applied the following Boolean query (English keywords; Korean synonyms were also checked in the same portal): (Listing 1)

**Listing 1.** Boolean query used for patent search in WIPS ON database.

```
(SiC OR GaN OR ‘‘Wide-Bandgap’’ OR WBG OR ‘‘power semiconductor’’)
AND (‘‘thermal management’’ OR cooling OR ‘‘heat dissipation’’ OR ‘‘heat sink’’
OR ‘‘thermal interface material’’ OR TIM OR packaging
OR ‘‘thermal resistance’’ OR ‘‘thermal conductivity’’)
```

Results were deduplicated by INPADOC family; counts were assigned to the earliest priority year; geography reflects the first-priority country; and assignee names were harmonized. Representative families were then selected using the following three objective filters: (i) *claim-level relevance*, i.e., independent claims disclose packaging/thermal integration elements (die-attach/TIM, wire-bondless interconnects, near-junction cooling, or electro-thermal co-design); (ii) *impact*, measured by age-normalized forward citations (top-quartile within the cohort); and (iii) *breadth/status*, i.e., coverage in $\geq$2 jurisdictions or one major office (US/EP/JP/CN) with at least one granted member. As a tie-breaker, assignee significance was considered when families were otherwise comparable. Illumination-only

LED families were excluded unless the claims disclose packaging/thermal constructs transferable to power-device applications.

**Representative Families.** *SiC*—US 8,329,252 B2 [85] exemplifies epitaxial/process innovations that suppress defect formation and improve substrate/epi quality, directly supporting the reliability targets in Section 4.1 and the thermal strategies in Section 3. *GaN*—US 2011/0297914 A1 [86] describes a wire-bond-free flip-chip stack that shortens the vertical heat path and reduces parasitics. Although originally framed for LEDs, this packaging architecture is platform-neutral and is cited here as an early integration precedent, consistent with Sections 2.2 and 3.2.

**Trends and Implications.** These examples reflect a broader evolution from quantitative expansion to qualitative, integration-centric innovation (Figure 5). Geographically, the United States and Japan lead in SiC, while the U.S. holds a commanding share in GaN (Figure 6). Overall, securing intellectual property (IP) on high-quality substrates, advanced interconnects, and electro-thermal co-design has become decisive for delivering reliable, high-density WBG systems at scale.

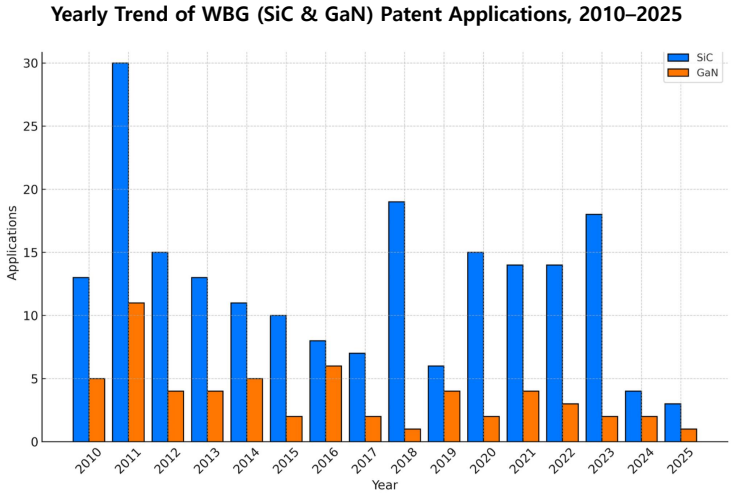



**Figure 5.** Yearly trend of WBG (SiC and GaN) patent families, 2010–2025. Counts aggregated by earliest priority year; INPADOC family deduplication; Source: WIPS ON (accessed on 4 September 2025, KST). Due to publication lags, the trend is directional.

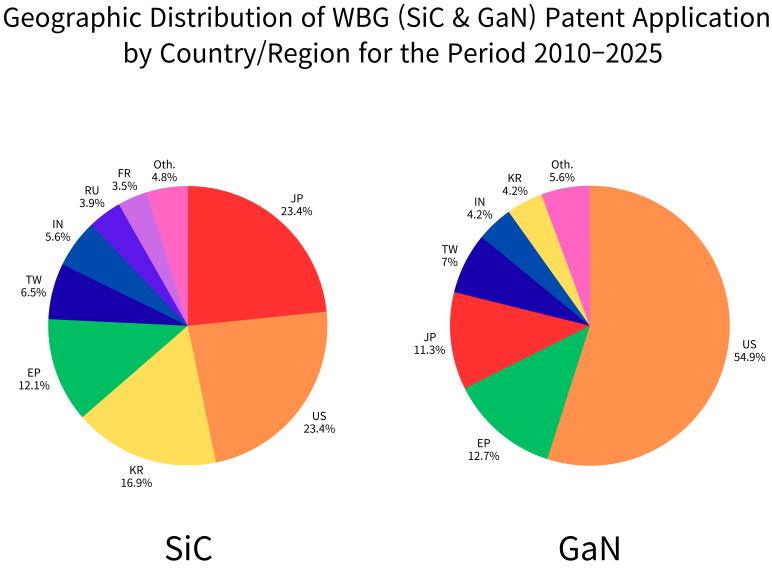



**Figure 6.** Geographic distribution of WBG (SiC and GaN) patent families by first-priority country, 2010–2025. INPADOC family deduplication; Source: WIPS ON (accessed on 4 September 2025, KST).

To complement the statistical patent analysis (Figures 5 and 6), Figure 7 provides a chronological view of major packaging and cooling innovations, highlighting how technological milestones from 2010 to 2025 align with the trends discussed in this section. As a synthesis of the literature in Sections 3 and 5.2, it consolidates major milestones without introducing new data.

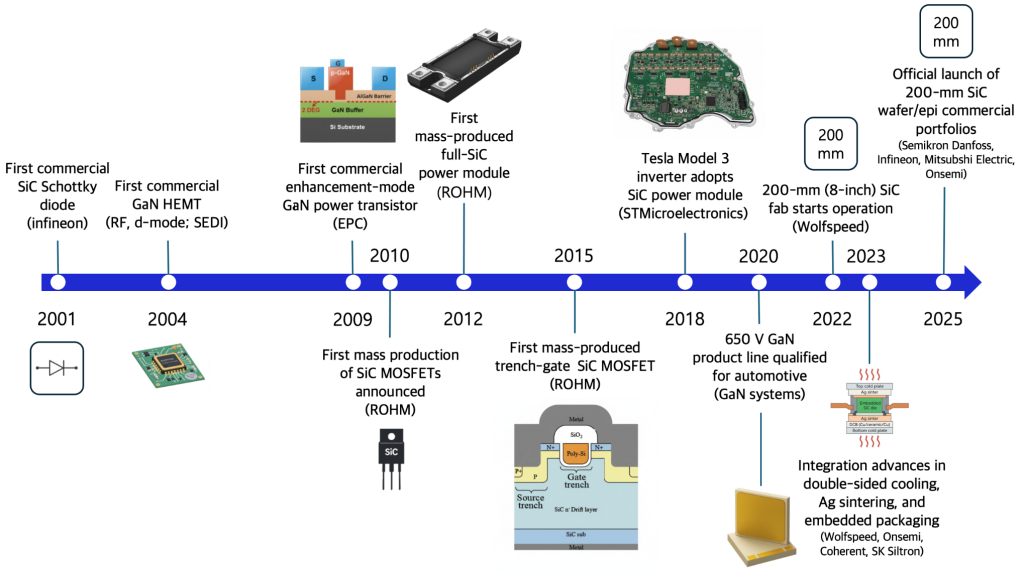



**Figure 7.** Chronological timeline of major packaging and cooling innovations (2010–2025).

## 6. Conclusions

In modern power conversion, SiC- and GaN-based WBG devices promise unprecedented power density, yet this potential is fundamentally capped by localized self-heating. This review has shown that the root of the problem lies at the multi-scale interface: from hotspots in the ultrathin 2DEG channels and TBR in GaN-on-SiC to the parasitic elements in conventional packaging. While advanced solutions such as double-sided cooling, embedded packaging, and near-junction microchannels offer effective mitigations, they must be coupled with real-time health monitoring via TSEPs and robust lifetime models. The evidence overwhelmingly demonstrates that isolated, component-level optimizations are insufficient. Therefore, an integrated co-design—spanning devices, packaging, EMI-aware layout, and cooling—is the only viable strategy to overcome these interconnected challenges and deliver reliable, high-density WBG systems.

Looking forward, this co-design principle must extend to next-generation architectures. Standardizing processes and reliability for 3D heterogeneous integration will be critical, particularly in managing new failure modes such as thermal crosstalk between stacked dies and stress-induced delamination at material interfaces. Furthermore, the development of physics-informed, AI-driven active thermal management, guided by digital-twin frameworks, will be essential to close the loop from design to real-time operational reliability, ultimately enabling reliable, high-density WBG power systems.

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## Abbreviations

The following abbreviations and symbols are used in this manuscript:

**Abbreviations**

| | |
|---|---|
| 2DEG | Two-Dimensional Electron Gas |
| 3D | Three-Dimensional |
| AEC | Automotive Electronics Council |
| AEC-Q100 | AEC Qualification Standard for Integrated Circuits |
| AEC-Q101 | AEC Qualification Standard for Discrete Semiconductors |
| ALT | Accelerated Life Testing |
| AlN | Aluminum Nitride |
| BPD | Basal Plane Dislocation |
| CAVET | Current-Aperture Vertical Electron Transistor |
| CCS | Current Commutator Structure |
| DBN | Dynamic Bayesian Network |
| DFT | Density Functional Theory |
| DRBD | Dynamic Reliability Block Diagram |
| DSC | Double-Sided Cooling |
| EL | Electroluminescence |
| EM | Electromigration |
| EMI | Electromagnetic Interference |
| FEM | Finite Element Method |
| GaN | Gallium Nitride |
| HEMT | High Electron Mobility Transistor |
| HTC | Heat Transfer Coefficient |
| HTGB | High-Temperature Gate Bias |
| HTRB | High-Temperature Reverse Bias |
| IMC | Intermetallic Compound |
| IP | Intellectual Property |
| ISU | Interleaved Switch Unit |
| JEDEC | Joint Electron Device Engineering Council |
| JESD22 | JEDEC Standard JESD22: Stress-Test Procedures |
| JESD47 | JEDEC Standard JESD47: Reliability Qualification of Integrated Circuits |
| JFET | Junction Field-Effect Transistor |
| LTM | Lumped Thermal Model |
| MMIC | Monolithic Microwave Integrated Circuit |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| PC | Power Cycling |
| PCB | Printed Circuit Board |
| PoF | Physics-of-Failure |
| RC | Resistance–Capacitance (network) |
| RUL | Remaining Useful Life |
| SAB | Surface-Activated Bonding |
| Si | Silicon |
| SiC | Silicon Carbide |

| | |
|---|---|
| TC | Thermal Cycling |
| TBC | Thermal Boundary Conductance |
| TBR | Thermal Boundary Resistance |
| TCAF | Thermally Conductive Adhesive Film |
| TDB | Time-Dependent Breakdown |
| TED | Threading Edge Dislocation |
| THB | Temperature–Humidity Bias |
| TLP | Transient Liquid Phase |
| TSEP | Temperature-Sensitive Electrical Parameter |
| WBG | Wide-Bandgap |
| **Parameters and Symbols** | |
| $C_{OSS}$ | Output Capacitance |
| $dI/dt$ | Current Slew Rate |
| $I_{dss}$ | Drain Leakage Current |
| $I_{gp}$ | Gate Current |
| $R_{DS(on)}$ | On-State Resistance |
| $T_j$ | Junction Temperature |
| $\Delta T_j$ | Junction Temperature Variation |
| $V_{DS}$ | Drain–Source Voltage |
| $V_{gs}$ | Gate–Source Voltage |
| $V_{th}$ | Threshold Voltage |
| $V_{DS(on)}$ | On-State Drain–Source Voltage |
| $R_{th}$ | Thermal Resistance (Compact Network Parameter) |
| $C_{th}$ | Thermal Capacitance (Compact Network Parameter) |
| $Z_{th}(t)$ | Transient Thermal Impedance |
| $Z_{jc}$ | Junction-to-Case Thermal Impedance |

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