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Development of High-Power DC Solid-State Power Controllers Using SiC FETs for Aircraft Electrical Systems

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Abstract

The growing demand for improved interruption performance characteristics in emerging aircraft high-voltage direct current (HVDC) electrical networks motivates the rapid development of solid-state power controllers (SSPCs). This article presents a comprehensive design procedure for a 270 V 300 A SSPC utilizing discrete SiC cascode devices. Due to the high fault current and limited power of single switches, parallel SiC FETs are essential for interrupting high fault currents in SSPCs. Consequently, the challenge of current balancing among parallel devices is addressed in this paper by adopting a passive current balancing strategy based on an irregular-shaped busbar. Furthermore, considering the voltage spikes arising from the power loop parasitic inductance and TVS characteristics during fault interruption, an RC-TVS-based transient voltage mitigation circuit is proposed to suppress these peak voltages. Moreover, thermal models for overload and short-circuit conditions were developed to optimize the thermal management system to ensure reliable operation of the SSPC. Finally, a prototype of 270 V/300 A SSPC has been built to validate the key characteristics of the proposed high power SSPC.

Keywords: HVDC SSPC; current balancing; transient surge voltage suppression; transient thermal design

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Academic Editors: Krzysztof Górecki, Paweł Górecki and Kalina Detka

Received: 9 September 2025
Revised: 19 October 2025
Accepted: 21 October 2025
Published: 23 October 2025

Citation: Zhao, X.; Xu, C.; Ma, K.; Wu, X.; Chen, X.; Li, X.; Wu, X. Development of High-Power DC Solid-State Power Controllers Using SiC FETs for Aircraft Electrical Systems. *Electronics* **2025**, *14*, 4157. https://doi.org/10.3390/electronics14214157

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1. Introduction

Driven by the requirement of improving aircraft efficiency, reducing fuel consumption, and greenhouse gas emissions, there is a growing trend to electrify the aircraft power system [1–3]. This pushes research toward the continuous development of more electric aircraft (MEA) techniques that aim to replace the conventional mechanical, pneumatic, or hydraulic system with an electrical power system [3]. Moreover, the hybrid and all-electric aircraft (HEA/AEA), which electrify the aircraft propulsion system and auxiliary power unit, can further improve the propulsive efficiency, and reduce carbon emissions and acoustic noise [3,4]. For the implementation of electrified aircraft, protection is a critical challenge to ensure safety and reliability.

Highly electrified aircraft normally utilize a power electronic converter-based HVDC power distribution system since it can reduce the cable weight and cost [5–7]. However, the HVDC system suffers from high fault current magnitude and rise rate due to the large DC-link capacitors and low fault impedance. Therefore, fast fault interruption is required to constrain the fault current and, consequently, protect the power electronic devices, which have limited surge capability, from being destroyed by overheating.

A conventional electromechanical circuit breaker (ECB), whose interruption time is around tens of milliseconds or more, cannot satisfy the protection requirement of power electronic devices in HVDC system [8]. Furthermore, the lack of zero crossing points in DC current may also accelerate the ECB contact corrosion speed. Therefore, solid state power controllers (SSPCs) have gained popularity in aircraft HVDC systems, considering the advantage of no mechanical moving contacts and arc-less current interruption capability with fast protection time.

The continuously climbing power level of the aircraft HVDC system requires the circuit breaker (CB) to have higher current interruption capability. However, the existing SSPCs only have limited capacity and can only be utilized in the aircraft secondary power distribution systems. Although companies like Data Device Corporation (DDC) [9], Sensitor [10], and HYJAS Electronics [11] have already released 270 V DC SSPC products, the maximum rated current is only 150 A, which cannot meet the requirement of the future electrified aircraft.

In the academic area, challenges like current balancing, transient voltage mitigation, and transient thermal modeling have been extensively investigated. In [12], a double edge modulation-based control strategy is proposed to decrease the $\mathrm{d}i/\mathrm{d}t$ during switching transients. However, the interruption current is only 40 A, and the proposed strategy can lead to intermittent output voltage during switching. Metal oxide varistor (MOV) combined with snubber capacitor are dedicatedly designed and utilized as a transient voltage absorption circuit in [13], and the rated/interruption current reaches 100 A/150 A under the condition of 20 μH power loop parasitic inductance. However, MOV suffers from degradation issues and is not suitable for aircraft applications. In [14], a transient voltage suppressor (TVS) array-based peak voltage clamp circuit, which can achieve faster response speed and lower clamping ratio without degradation issue, is proposed. Although the nominal current is increased to 350 A, the maximum interruption current is only 1.3 times the rated current (450 A). Furthermore, the parallel connection of TVSs may cause current imbalance due to differences in clamping characteristics.

To further increase the SSPC power capacity, parallel connection of the switching devices is inevitable considering the insufficient current rating. Active current sharing [15,16], which actively regulates the drive signals of parallel devices to mitigate the current imbalances caused by power loop parasitic parameters, has been proposed. However, since active current balancing methods commonly rely on dedicatedly designed gate drive circuits [17] and require multiple switching cycles for closed-loop current compensation [18,19], it is not suitable for SSPC applications where the power devices do not operate in continuous switching operation. It is worth noting that an active gate driver proposed in [20] utilizes a differential mode choke to achieve current sharing within a single switching cycle. However, the complexity introduced by this approach makes the driver circuit difficult to implement, particularly when paralleling more than two power devices. Consequently, passive current sharing methods are the preferred and more suitable approach for SSPC designs. These methods offer inherent current balancing without the need for a complex driver circuit, control algorithms, or multiple switching cycles, aligning well with the operational requirements of SSPCs [21]. A symmetrical circle layout is proposed with the maximum interruption current increases to 1.1 kA [22]. However, the independent heat sink required by each parallel MOSFET significantly complicates the physical and air duct design, and thus makes the method difficult to apply in practical applications. By utilizing two SiC MOSFET modules in series with liquid cooling system, the interruption current can be increased to 1.8 kA with 8 μH power loop parasitic inductance [23]. However, the high cost of the power modules and the limited availability of liquid cooling systems restrict their widespread adoption in aircraft applications. By utilizing two GaN devices in parallel, a 750 V/100 A SSPC is proposed in [24]. This work, however, does not address the current

balancing issue, and the reliance on a cryogenic cooling system further limits its practical application. The performance and key characteristics of the aforementioned SSPC designs are listed in Table 1.

Table 1. Characteristics of existing SSPCs.

Reference Design	Voltage (V)	Rated Current (A)
DDC [9]	270	150
Sensitor [10]	270	150
HYJAS [11]	270	150
Huang et al. [13]	270	100
Hayes et al. [14]	270	350
Dam et al. [24]	750	100

To summarize, current research on SSPCs primarily focuses on achieving manufacturing maturity for devices exhibiting high power density, superior protection performance, and high efficiency across diverse applications. However, the existing literature still lacks comprehensive research on high-power, low-cost, and easily integrated SSPCs. Addressing these challenges, this paper proposes a passive current balancing strategy based on an irregular-shaped power busbar and a TVS-based peak voltage mitigation strategy, alongside a comprehensive SSPC design procedure. Furthermore, the proposed SSPC requires only an air-cooling system, which simplifies the system physical structure and thus significantly extends its application range. Finally, the development of a 270 V/300 A DC SSPC prototype is presented.

The rest of the paper is organized as follows. Section 2 explains the detailed operating principle and system design considerations while Section 3 mainly discusses the switching device selection and the corresponding thermal design. Section 4 analyzes the challenges of paralleling switching devices and gives the design guidelines of the proposed irregular-shaped busbar. In Section 5, the design of the proposed RC-TVS clamping circuit is illustrated in detail. Experimental results are analyzed and discussed in Section 6. Finally, Section 7 presents the conclusion of the paper.

2. System Description and Design Considerations

The system under study, which is a generic case of a unidirectional DC SSPC system, is shown in Figure 1. The fundamental building block, which is the parallel connection of switching device and voltage clamping circuit, interfaces the power bus and the load. Note that a CAN/RS-485 communication link is required since SSPCs normally feature remote control, condition monitoring, and fault reporting functionality.

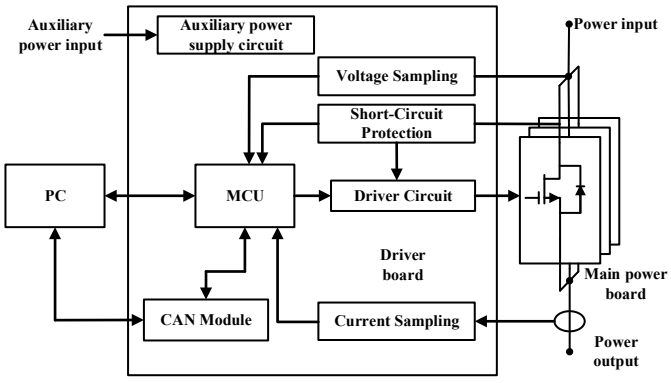


Figure 1. Structure of DC SSPC.

2.1. Specification and Configuration

The specifications of the SSPC designed in this paper are listed in Table 2. Based on the functional requirements of the primary power distribution system in electrified aircraft, a unidirectional SSPC is necessary to control power flow from the power bus to the loads. Consequently, the topology features a switching component in parallel with a TVS-based voltage clamping circuit due to its high reliability and superior voltage clamping performance, as shown in Figure 2. More detailed analysis regarding various SSPC topologies can be found in [8], and will not be further discussed in this paper. It is important to note that given the limited current rating of existing semiconductor devices, a configuration with multiple parallel devices is required for the main power switch.

Table 2. SSPC specifications.

Parameters	Value
Application	Primary power distribution
Nominal voltage	270 V
Nominal current	300 A
Protection	Overvoltage/I^2t
Short-circuit protection	1.8 kA
Total cable inductance	40 µH
Maximum operating temperature	60 °C

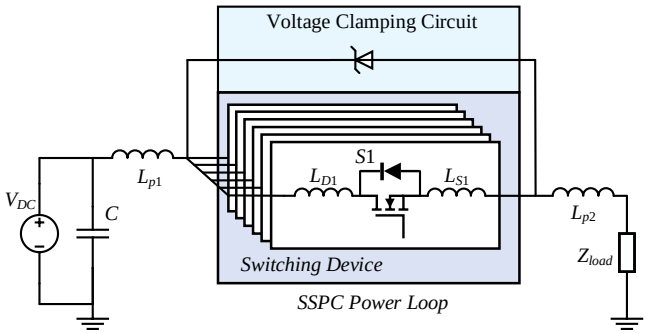


Figure 2. A generic SSPC topology.

2.2. Tripping Curve

Thermal failure is a prevalent failure mode for semiconductor devices; therefore, thermal analysis under rated conditions must be considered during the design process. This approach is generally sufficient for converters with low overcurrent capability (typically less than 1.5 times the nominal current with limited duration). However, SSPCs, which can withstand overcurrents up to 10 times the nominal current [25], require careful thermal analysis during the fault conditions to prevent the switching devices from overheating.

The nominal current of the SSPC determines the steady-state temperature of the switching devices, while the protection curve influences the heat generated during the current interruption process. Since the device temperature is the coaction of dissipated heat in the steady state and transient state, it is vital to determine the protection curve before proceeding with any detailed design.

A typical protection curve is shown in Figure 3. It typically comprises a no-trip region, an instantaneous trip region for short-circuit protection and an I^2t trip region for overload protection [25].

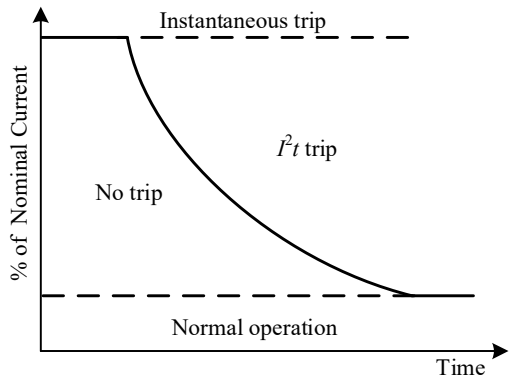


Figure 3. I^2t protection curve.

These zones should be carefully tailored to avoid undue thermal distress considering the upstream power capacity and its protection mechanism. In this paper, the I^2t protection curve is formulated according to the requirements of SAE AS4805A and IEC 60898-3 [25,26]. The protection delay with respect to the fault current is derived as (1), and the corresponding overcurrent protection delay times under different fault currents are listed in Table 3. Furthermore, the instantaneous current protection threshold is set to 6 times the rated current. Note that I^2t tripping curves and instantaneous trip current thresholds can vary across different systems due to differing electrical characteristics, with instantaneous trip currents potentially reaching up to 10 times the rated current.

$$t = \frac{8}{(I/I_p)^2 - 1} \tag{1}$$

Table 3. Overload protection time.

Overload ratio	2	3	4	5	6
Protection time (t_{OL})	2.67 s	1 s	0.53 s	0.3 s	0.23(0) s

3. Thermal Design and Parallel Device Configuration

Based on the protection curve determined in the previous section, this section details the thermal design and subsequently determines the required number of parallel power devices for the SSPC under various operating scenarios based on the thermal model. Note that the Qorvo SiC FET UF3SC065007K4S (TO-247 package) was selected as the main power device, primarily due to its high availability, scalability, low cost, and excellent low on-resistance.

The device junction temperature during both nominal and fault conditions should be less than the maximum allowable temperature to prevent thermal breakdown. The relationship between the number of parallel devices and the device junction temperature under both nominal and fault conditions is evaluated according to the system thermal model.

3.1. Junction Temperature Estimation

The power loss in an SSPC is mainly attributed to device conduction loss, which, for a single device, can be calculated as:

$$P_{dc} = \left(\frac{I_d}{N}\right)^2 R_{dson} \tag{2}$$

where I_d is the nominal current, N is the number of paralleled power devices, and R_{dson} is the device on-resistance.

The equivalent thermal model of the power device is shown in Figure 4, where T_j, T_c, T_s, and T_a denote the junction temperature, case temperature, thermal grease temperature, and ambient temperature, respectively, and R_{thjc}, R_{thcs}, and R_{thsa} represent the junction-to-case thermal resistance, thermal grease thermal resistance, and case-to-air thermal resistance, respectively. Based on this model, thermal performance under nominal, overcurrent, and short-circuit conditions can be analyzed.

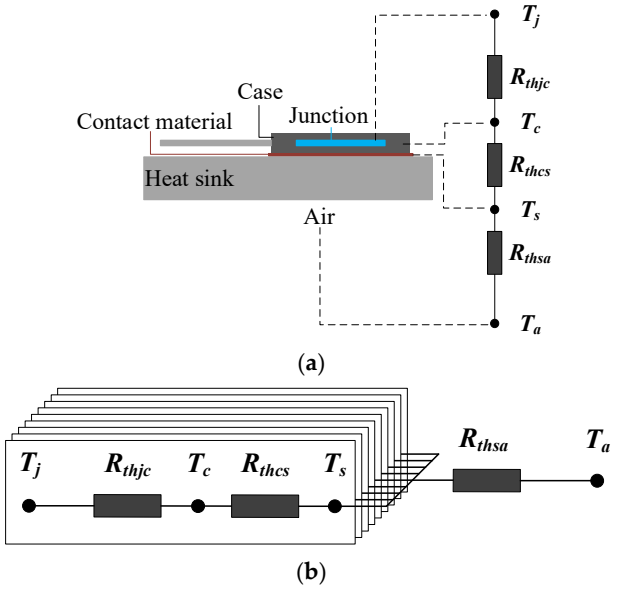


Figure 4. Equivalent thermal model of SSPC. (**a**) Individual device thermal model. (**b**) Parallel devices thermal model.

(1) Nominal operation

Under nominal operating conditions, the steady-state junction temperature of the device can be calculated as:

$$T_{j\max} \geq T_j = \frac{P_{dc}}{N} \times R_{thja} + T_a \tag{3}$$

where T_{jmax} is the maximum junction temperature of the device, P_{dc} is the device power loss, and R_{thja} is the total thermal resistance of the thermal loop.

(2) Overcurrent operation

Assuming a constant current during the fault condition, as illustrated in Figure 5, where P_{ol} represents the device power loss and t_{ol} is the duration of the overcurrent fault, the device junction temperature reaches its maximum at the end of the fault, and can then be calculated as:

$$T_j = \frac{P_{dc}}{N} \cdot R_{thja} + \left(\frac{P_{ol} - P_{dc}}{N} \right) \cdot Z_{th(tol)} + T_a \tag{4}$$

where $Zth_{(tol)}$ is the transient thermal impedance of the device corresponding to the length of fault duration t_{ol}. It should be noted that $Zth_{(tol)}$ can be obtained from the transient thermal impedance curve in the device datasheet.

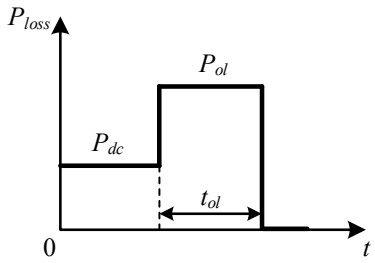


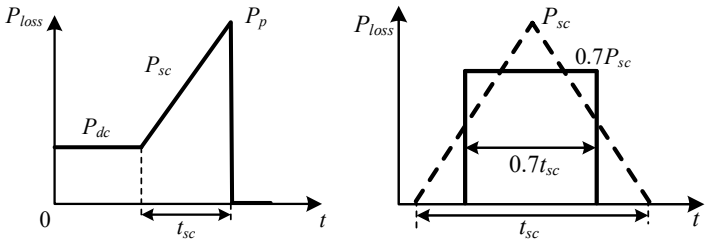
Figure 5. Overload power curve of SSPC.

(3) Short-circuit operation

The main issue in conducting short-circuit thermal analysis is the determination of the device transient thermal impedance, which varies significantly from the steady-state impedance. Assuming the device on-resistance during the fault is constant, the power dissipation waveform takes a triangular shape, as shown in Figure 6a. However, the transient thermal impedance data provided by device manufacturers is typically defined based on square-wave power pulses. Therefore, it is essential to approximate the power loss waveform under short-circuit conditions as an equivalent square wave for analytical purposes. Based on the principle of equal energy dissipation (analogous to impulse-momentum), the parameters of the equivalent square wave can be derived as:

$$t = \frac{1}{P_p}\int_0^{t_{sc}} p_d(t)dt \tag{5}$$

where $p_d(t)$ is the device power dissipation, and t_{sc} is the short circuit fault duration.



(**a**) (**b**)

Figure 6. Short-circuit power curve of the SSPC. (**a**) Actual short-circuit power curve. (**b**) Equivalent short-circuit power curve.

Based on (5), the equivalent square wave of the power dissipation waveform has an amplitude of $0.7P_{sc}$, and duration of $0.7t_{sc}$, as shown in Figure 6b. Then, the junction temperature under short-circuit state can be calculated as

$$T_j = \frac{P_{dc}}{N} \cdot R_{thja} + \left(\frac{P_{sc} - P_{dc}}{N}\right) \cdot Z_{th(tsc)} + T_a \tag{6}$$

where $Zth_{(tsc)}$ is the device transient thermal impedance corresponding to the pulse width of t_{sc}. It is worth noting that t_{sc} can be calculated by:

$$t_{sc} = \frac{LI_{sc}}{V} = 222\mu s \tag{7}$$

where L is the system total parasitic inductance, V is the nominal voltage, and I_{sc} is the maximum fault current.

To guarantee an allowable junction temperature, the device junction temperature under different operation scenarios can be obtained through (1)–(6), respectively. Subsequently, the minimum number of devices required in parallel is calculated based on these temperatures and the maximum allowable junction temperature, as shown in (8).

$$T_J = \left(\frac{I_D}{N}\right)^2 \cdot R_{DS(ON)} \cdot Z_{THJC}(t_{OL}) + T_C < T_{JMAX} \tag{8}$$

Based on the preceding calculations, the required number of parallel devices, N, was determined to be 7.67. To ensure a sufficient safety margin, the number of parallel devices was selected as 9. Then, the corresponding junction temperature and conduction losses for this configuration were calculated and are summarized in Table 4.

Table 4. Maximum device junction temperature by current.

Number of Paralleled Devices	Maximum Junction Temperature				
	Nominal	Overcurrent			Short Circuit
		3	4	5	
9	86 °C	104 °C	119 °C	139 °C	91 °C

Finally, the required thermal resistance of the heat sink (R_{thsa}) was calculated to be less than 0.31 °C/W. In this paper, an aluminum heat sink with a thermal resistance of 0.208 °C/W was designed and implemented, effectively satisfying the thermal management requirements. The specifications of the designed heat sink are detailed in Table 5. Note that the detailed heat sink design process will not be discussed here, since it is well-documented in the previous literature [27].

Table 5. Specifications of the designed heat sink.

Parameter	Value	Parameter	Value
Material	Aluminum 6063	Fin width	1.1 mm
Length	150 mm	Fin spacing	2.55 mm
Width	100 mm	Fin count	28
Height	50 mm	Flow velocity	2 m/s
Substrate thickness	5 mm	Thermal resistance	0.208 °C/W

Furthermore, thermal resistance of the heat sink can be calculated by combining (6) and (9).

$$R_{thja} = R_{thjc} + R_{thcs} + R_{thsa} \tag{9}$$

3.2. Thermal Simulation

The Foster thermal model with the designed heat sink is built in LTspice to carry out thermal simulation. The simulation is conducted with the fault current equals to $5I_d$ under 60 °C ambient temperature.

The simulation result is shown in Figure 7. As can be seen, before the fault occurs, the device power loss is 110 W and the junction temperature is 86.4 °C. When the fault occurs at t_1, the power loss of the devices abruptly increases to 2.75 kW, causing the junction temperature to gradually rise to 145.5 °C. After the fault is cleared at t_2, both the power loss and the junction temperature decrease to pre-fault levels.

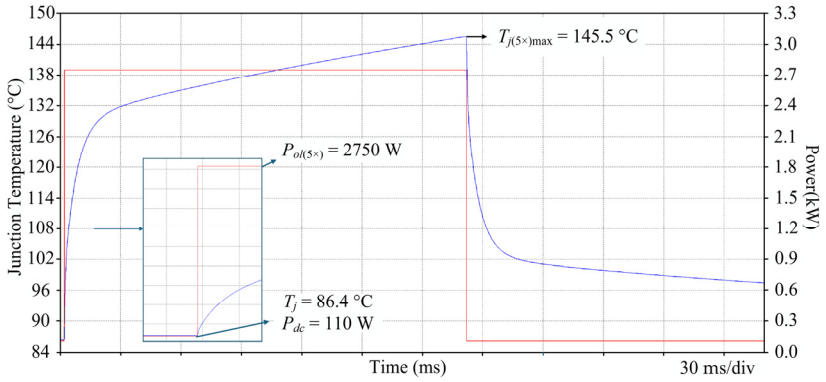


Figure 7. Thermal simulation results of 5× overload.

In addition, the device junction temperature of SSPC under different overload and short-circuit conditions is simulated according to the established thermal model, and the results are concluded in Table 6. It can be seen that the junction temperature of the device does not exceed the maximum junction temperature of 175 °C (ambient temperature 60 °C) under overload and short-circuit conditions, which proves that the designed parallel device configuration and the heat sink are appropriate.

Table 6. Simulated junction temperatures under overload and short-circuit conditions.

Conditions	2×	3×	4×	5×	6×	Short-Circuit
Temperature (°C)	97	112.4	129.7	145.5	171.4	92.3

4. Passive Current Balancing Strategy

Passive current balancing methods can be categorized into three main types: pre-screening of power devices to minimize parameter mismatch, symmetrical PCB or circuit layout to equalize parasitic effects, and the incorporation of passive components such as resistors or inductors for current equalization. Considering that inserting passive components in series with the power loop can significantly increase system losses, volume, and weight, and that the previously proposed coupled-inductor-based current balancing method may introduce higher voltage spikes across power devices, these passive strategies are not suitable to be applied to high power SSPC applications.

The parasitic parameters of the power loop significantly impact current sharing performance among parallel devices. To address this issue, this paper proposes a compensation strategy for power loop parasitic components to optimize parameter imbalance across parallel branches. Note that device preselection is a straightforward and effective method for mitigating current imbalance; however, it is not discussed here as it has been well-addressed in the existing literature.

4.1. Determination of SSPC Architecture

For the purpose of achieving uniform thermal conditions and subsequent balanced current performance among the power devices, a single heat sink was utilized for the mounting of all components, and the 9 MOSFETs were divided into three power modules, each containing three parallel power devices as shown in Figure 8.

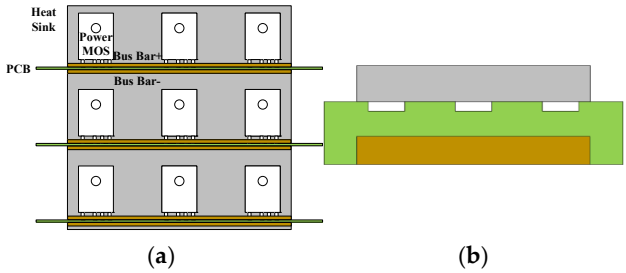


Figure 8. Structure of the power circuit. (**a**) Front view. (**b**) Top view.

4.2. Irregular-Shaped Busbar-Based Parasitic Parameter Compensation Strategy

By introducing strategic openings in the busbar, the impedance of the parallel branches is balanced. This principle of parasitic parameter compensation aims to mitigate the current imbalances caused by parasitic parameters of the parallel devices, thereby finally ensuring current balance.

Figure 9 depicts the power circuit configuration of a single module, highlighting the change introduced by the busbar window opening. As shown, the window opening increases the length of the power loop for Device 2, leading to an increase in the parasitic parameters of that parallel branch.

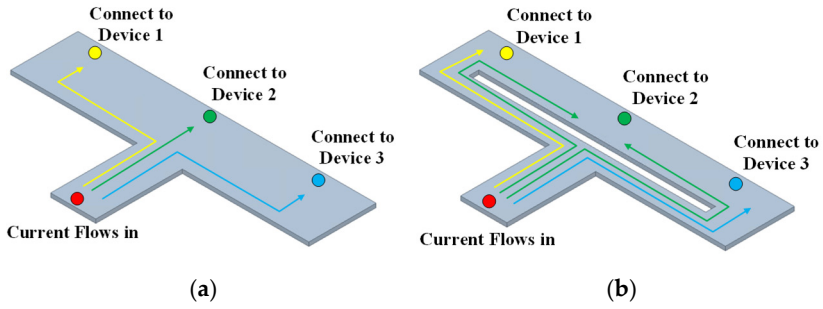


Figure 9. Power loop of a single module. (**a**) Before window opening. (**b**) After window opening.

4.3. Window Size Design of Busbar

In order to analyze the influence of window size on the parasitic parameters of parallel branches, the busbar model is established, and the parasitic parameters of different power loops are extracted by utilizing ANSYS Q3D 2024 to analyze the variations of parasitic parameters under different window sizes. The relationships between window sizes and the different parasitic parameters are presented in Figures 10–12. The inductance and resistance unbalance are calculated according to the following equation.

$$U\% = \frac{\Delta X_{\max}}{X_{avg}} \cdot 100\% \tag{10}$$

where ΔX_{max} is the maximum difference of the inductance or resistance in the different branches, and X_{avg} is the average of the inductance or resistance. Note that the window length varies from 0 mm to 80 mm, and the window width varies from 0 mm to 6 mm.

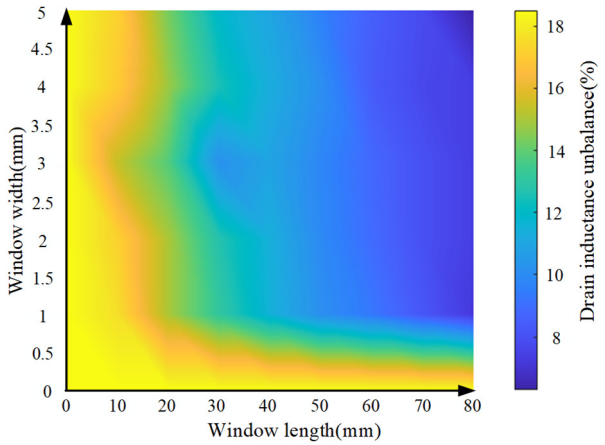


Figure 10. Relationship between U_D% and window size.

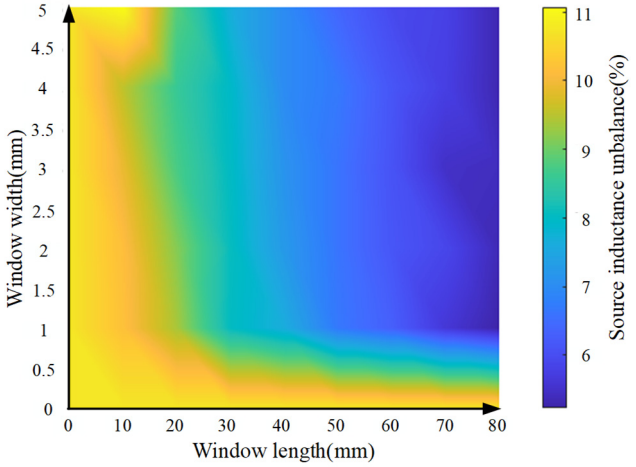


Figure 11. Relationship between U_S% and window size.

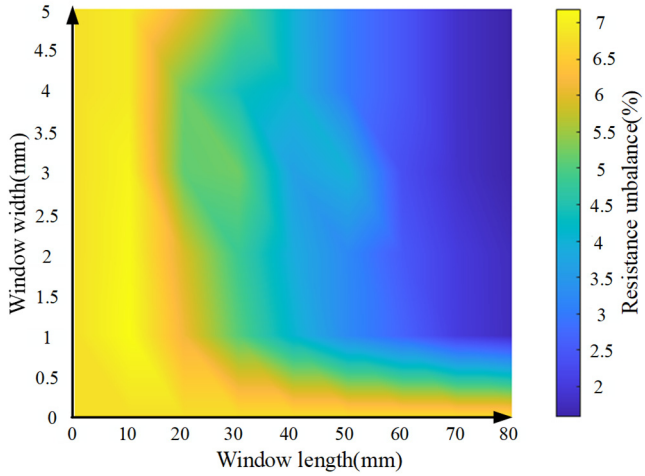


Figure 12. Relationship between U_R% and window size.

It can be seen from Figures 10–12 that with the increase of the window area, the imbalance of drain inductance, source inductance, and loop resistance decreases. Conversely, a larger window area forces the current to flow around a larger effective loop, increasing the loop self-inductance by allowing more magnetic flux to pass. Simultaneously, this larger window size reduces the effective conductive cross-sectional area and increases the current path length, thereby increasing the loop resistance. Consequently, the window size

is finally designed as 80 mm and 4 mm, respectively, to provide a compromise between current balancing performance, power loss, and transient performance characteristics. The inductance and resistance matrix of the designed busbar are shown in Tables 7 and 8.

Table 7. Parasitic inductance matrix (n*H*).

Inductance	Branch1	Branch2	Branch3	Branch4	Branch5	Branch6
Branch1	28.94	17.53	10.67	26.25	15.77	9.59
Branch2	17.53	22.78	17.44	16.56	20.27	15.75
Branch3	10.67	17.44	28.71	9.36	16.52	26.20
Branch4	26.25	16.56	9.36	28.99	17.54	10.73
Branch5	15.77	20.27	16.52	17.54	22.93	17.52
Branch6	9.59	15.75	26.20	10.73	17.52	28.98

Table 8. Parasitic resistance matrix (mΩ).

Resistance	Branch1	Branch2	Branch3	Branch4	Branch5	Branch6
Branch1	1.22	0.79	0.68	0	0	0
Branch2	0.79	1.18	0.79	0	0	0
Branch3	0.68	0.79	1.2	0	0	0
Branch4	0	0	0	1.35	0.8	0.7
Branch5	0	0	0	0.8	1.3	0.8
Branch6	0	0	0	0.7	0.8	1.34

In the inductance matrix presented in Table 7, the diagonal elements represent the self-inductance of each branch, while the off-diagonal elements represent the mutual inductance among the branches. Based on the inductance matrix and the resistance matrix, the calculated unbalance factors for drain inductance, source inductance, and total branch resistance are 7.4%, 5.3%, and 1.6%, respectively. These values indicate a low level of impedance unbalance.

4.4. Simulation Results

The extracted parasitic parameters were used in LTspice to simulate current balancing. The simulation results are shown in Figure 13.

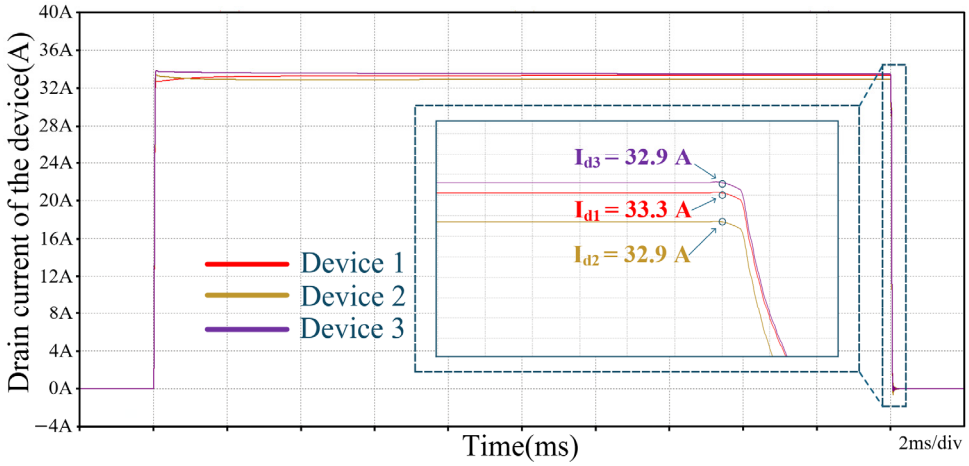


Figure 13. Current balancing performance of single module.

The current unbalance factor during both switching and steady-state operation, calculated from the simulation results, is presented in Table 9. As demonstrated by the results, the current unbalance factor remains below 5% under both operating states, provided that the devices have consistent parameters and no other supplementary current balancing techniques are employed. Note that the current unbalance factor is calculated using the following equation:

$$I_{IMB} = \frac{|I - I_{AVG}|_{\max}}{I_{AVG}} \cdot 100\% \tag{11}$$

Table 9. Current balancing simulation results.

Parameter / Device	1	2	3	Unbalance Factor
Turn-on current	32.7 A	33.4 A	33.9 A	3.6%
Turn-off current	33.3 A	32.9 A	33.4 A	1.5%
Steady-state current	33.3 A	32.9 A	33.5 A	1.8%

Furthermore, a single-parameter sensitivity analysis was conducted to evaluate parameter spread effects on current sharing in the parallel devices. Based on the device datasheet, R_{dson} ranges from 6.7 mΩ (typ) to 9 mΩ (max), threshold hold voltage Vth varies between 3.0–4.0 V, and a conservative 10% Q_g variation was assumed due to unspecified tolerance.

The analysis varied each parameter to its maximum value in one of three parallel devices while maintaining identical circuit parasitics. As shown in Figures 14–16, current unbalance factors reach 19.5% for R_{dson} variation, 0.2% for Q_g variation, and 5.3% for Vth variation. R_{dson} variation dominates steady-state performance with negligible transient impact. Lower Vth causes earlier turn-on and higher transient current amplitude but minimal steady-state effect due to current convergence. Q_g variation shows a similar trend with substantially lower impact.

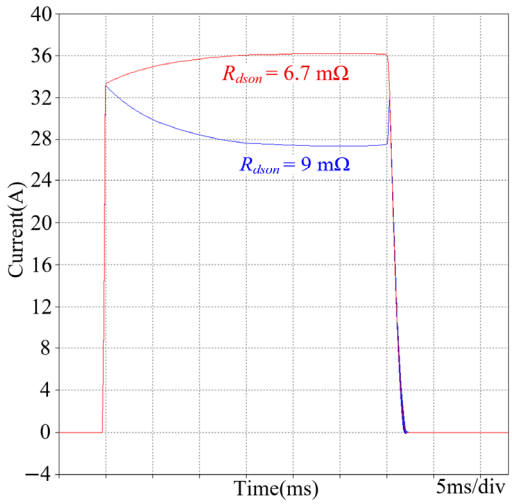


Figure 14. Impact of R_{dson} variation on current distribution.

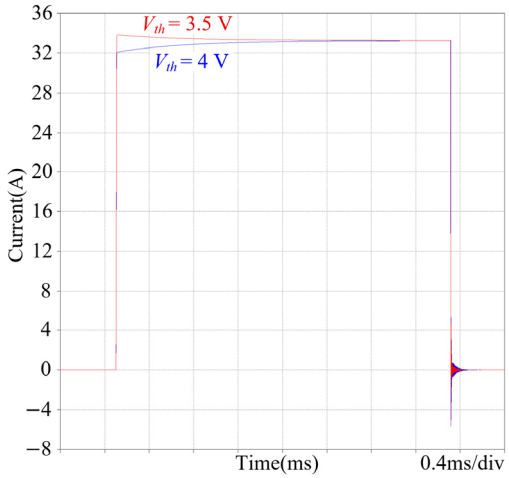


Figure 15. Impact of *Vth* variation on current distribution.

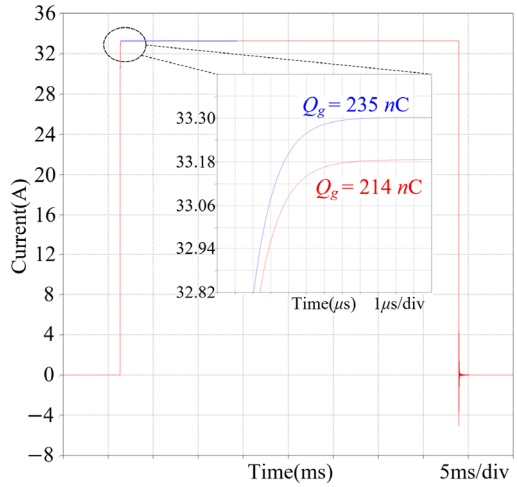


Figure 16. Impact of Q_g variation on current distribution.

5. Voltage Spike Suppression Circuit Design

During the SSPC turn-off process, the high di/dt in the main power loop induces a voltage spike across the parasitic inductance, potentially exceeding the breakdown voltage of the power device. A common method to absorb the energy stored in this parasitic inductance is to connect a MOV or TVS in parallel with the power device; TVSs are preferred in this paper due to their faster response speed and lower clamping voltage compared to MOVs, which are susceptible to aging with repeated operation. However, the parasitic inductance associated with the TVS branch can generate additional voltage spikes during SSPC turn-off, further increasing the voltage stress on the power device. To effectively mitigate these voltage spikes, an RC-TVS-based voltage spike suppression circuit is proposed.

5.1. The Cause of Voltage Spikes

The specific operation process during SSPC turn-off is detailed below, with the corresponding typical waveform shown in Figure 17.

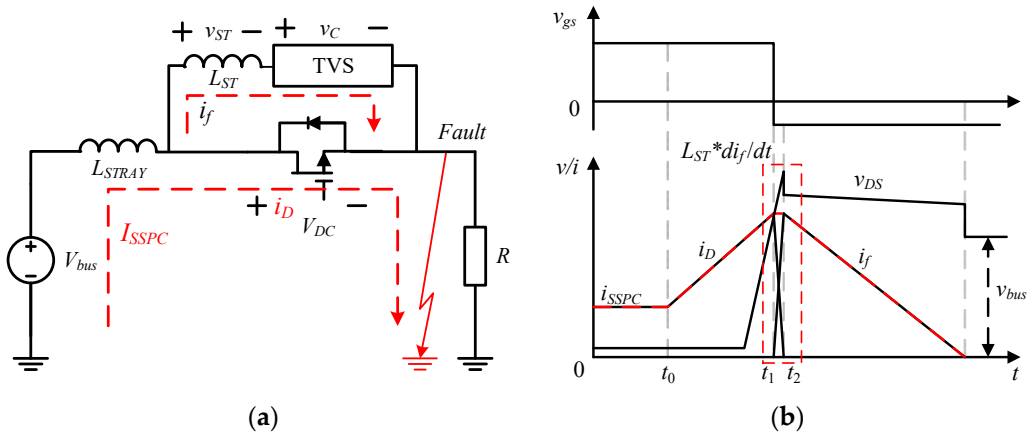


Figure 17. Turn-off voltage spike of the SSPC. (**a**) Equivalent circuit. (**b**) Waveform during SSPC turn-off.

t_0–t_1: At t_0, when a short circuit occurs, the SSPC current (I_{SSPC}) rapidly rises, and the power device drain-source voltage (v_{DS}) increases slightly.

t_1–t_2: At t_1, I_{SSPC} reaches its short-circuit protection threshold, initiating the turn-off of the power device. As the power device turns off, the current is commutated to the TVS branch, causing the power device current (i_D) to decrease and the TVS current (i_f) to increase. Consequently, the drain-source voltage (v_{DS}) rises rapidly until the TVS breaks down. Following this rapid current commutation between the main power circuit and the TVS branch, the power device current (i_D) finally drops to zero at t_2, at which point the TVS enters its reverse stand-off state.

Based on the above-mentioned analysis, during SSPC turn-off, the fault current commutates from the power device to the TVS. This rapid current change (high di_f/dt) generates an overvoltage (v_{ST}) across the parasitic inductance (L_{ST}) of the TVS branch. The relationship between v_{ST}, the TVS clamping voltage (v_C), and the voltage across the power device (v_{DS}) can be expressed as:

$$v_{ST} = L_{ST}\frac{di_f}{dt} = v_{DS} - v_C \tag{12}$$

It can be seen from (12) that the power device must withstand the sum of the voltage across the TVS branch parasitic inductance and the TVS clamping voltage during the turn-off process. Furthermore, high-power TVSs often exhibit a foldback characteristic, where the initial breakdown voltage is higher than the average clamping voltage. This foldback effect also contributes to an initial voltage overshoot at the beginning of SSPC turn-off. Based on this analysis, this paper proposes the integration of an RC snubber circuit to limit the rate of current change (di/dt) and effectively suppress the voltage spike during the initial phase of the turn-off process.

5.2. TVS Foldback Characteristics

The initial voltage spike during SSPC turn-off is composed of the clamping voltage and the voltage across the line inductance. A key consideration for high-power TVSs is their foldback characteristic [28], which significantly influences this initial spike. This characteristic, a common design in high-power TVSs with smaller die sizes to absorb high-peak pulse currents, exhibits a higher clamping voltage at the onset of breakdown. This temporary increase in clamping voltage is intentionally designed to quickly suppress overvoltage before the voltage is reduced to a lower level to limit power dissipation and avoid thermal runaway during sustained clamping. Figure 18 presents the surge response curve of a high-power TVS, illustrating its characteristic foldback behavior. This characteristic is further evident in the SSPC turn-off waveform shown in Figure 17, where

the voltage across the TVS terminals (V_{C_FB}) at the beginning of breakdown is observed to be higher than the average clamping voltage (V_{C_AVG}). This initial voltage peak is an inherent consequence of the foldback characteristic designed into high-power TVSs. As this characteristic is prevalent in high-power TVS products from leading manufacturers like Littlefuse and Bourns, mitigating the resulting voltage peak during SSPC operation when using these devices as clamping elements poses a significant challenge.

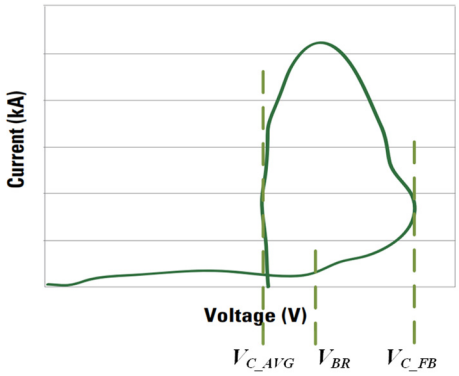


Figure 18. Surge response curve of TVS [28].

5.3. RC-TVS Parametric Design

In the proposed RC-TVS circuit, the TVS serves as the primary energy absorption component, while the RC snubber circuit, connected in parallel with the TVS, is implemented to mitigate the rate of current change ($\mathrm{d}i/\mathrm{d}t$) during the turn-off process. The buffer capacitance (C_S) can be estimated based on the buffer time (Δt_C), TVS clamping voltage (v_C), and short-circuit current (i_{SC}), as expressed by the following equation:

$$C_S \approx \frac{i_{SC}\Delta t_C}{v_C} \tag{13}$$

where Δt_C is the duration that the device drain-source voltage v_{DS} rises from 10% to 90% to its maximum. The current change rate and response speed are tested experimentally to meet the performance requirements of SSPC in this paper.

The buffer resistor serves the dual purpose of suppressing displacement current during SSPC turn-on and ensuring an overdamped RLC loop. Therefore, the buffer resistance value must satisfy the constraints shown in Equation (14).

$$R_S \geq \max\left[\frac{V_{DC}}{I_{D(PLUSE)}}, 2\sqrt{\frac{L_{STRAY}}{C_S}}\right] \tag{14}$$

When selecting the TVS diode, the key parameters to determine are the maximum reverse working voltage (V_{RWM}), the breakdown voltage (V_{BR}), and the peak clamping voltage (V_C). The breakdown voltage (V_{BR}) must be greater than the maximum bus voltage (V_{BUS}) to avoid unwanted breakdown during normal operation. Conversely, the peak clamping voltage (V_C) must be lower than the maximum breakdown voltage (V_{DS}) of the protected device to ensure its safe operation during transient events.

To provide reliable overvoltage protection for the power device, the TVS peak clamping voltage (V_C) should be chosen to be 10% lower than the power device rated voltage ($V_{DS(rate)}$). Simultaneously, to prevent significant leakage current in the TVS during normal operation, its maximum continuous reverse working voltage ($V_{M(DC)}$) should be 10%

higher than the DC bus voltage (V_{BUS}). Then, the voltage selection criteria for the TVS are summarized in (15).

$$V_C \leq 0.9 \cdot V_{DS(rate)}, V_{M(DC)} \geq 1.1 \cdot V_{BUS} \tag{15}$$

Moreover, to calculate the power dissipation in the TVS during a fault, the duration of the current pulse must be determined. This pulse width can be derived from the current waveform experienced by the TVS during the protection process in an ideal scenario. Considering that the TVS current typically exhibits an exponential decay, whereas the initial fault current can be modeled as a sawtooth, an appropriate conversion is required to find the equivalent pulse width under the exponential waveform for accurate power rating calculation. Equation (16) provides the formula for the converted pulse width.

$$t_{PE} = \frac{L_{STRAY} I_{SC}}{2.8(V_C - V_{BUS})} \tag{16}$$

where L_{STRAY} is parasitic inductance, and t_{PE} is the equivalent pulse duration. The selection of an appropriate TVS requires considering its peak pulse current (I_{PP}) and peak pulse power (P_{PP}) capabilities, both of which are related to the current pulse width determined by equation (16). For reliable protection during a short circuit, the TVS must be able to handle the SSPC peak short-circuit current (I_{SC}) and peak short-circuit power (P_{SC}), as indicated by the conditions in (17) and (18). Note that I_{PP} and P_{PP} of the TVS for a given pulse width can be found on the peak pulse power derating curve in its datasheet.

$$I_{PP} > I_{SC} \tag{17}$$

$$P_{PP} > P_{SC} = V_C I_{SC} \tag{18}$$

Based on the preceding analysis, the TVS selection procedure can be summarized as follows: First, determine the voltage ratings of the TVS. The breakdown voltage should be greater than the system nominal voltage (270 V), and the peak clamping voltage should be less than the maximum rated drain-source voltage of the protected device (650 V). Secondly, assuming a TVS clamping voltage of 450 V, the current pulse widths are calculated using Equation (16) as t_{P1} = 142.9 μs and t_{P2} = 47.6 μs. Based on these pulse widths, the TVS must be capable of withstanding a peak pulse current of 1800 A (corresponding to t_{P1} = 142.9 μs) and a peak pulse power of 270 kW (corresponding to t_{P2} = 47.6 μs). These conditions ensure the selected TVS provides effective overvoltage protection for the SSPC.

In this paper, the KC380 TVS diode from DOWOSEMI is selected. Its specifications include a maximum reverse working voltage of 380 V, a minimum breakdown voltage of 401 V, and a peak clamping voltage of 520 V under an 8/20 μs pulse. The peak pulse current rating is 10 kA for an 8/20 μs pulse, which is derated to 7.5 kA under the same 8/20 μs pulse at an ambient temperature of 60 °C.

6. Experimental Verification

To validate the effectiveness of the proposed passive current sharing strategy and the RC-TVS voltage spike suppression strategy, a 270 V/300 A SSPC prototype was built in this paper, as shown in Figure 19. The prototype consists of a control circuit and a power circuit. The control circuit incorporates an MCU minimum system, a driver circuit, a short-circuit protection circuit, a sampling circuit, an auxiliary power supply circuit, and a CAN communication circuit. The power circuit features 9 power devices, the designed irregular-shaped busbar, and the RC-TVS overvoltage mitigation circuit.

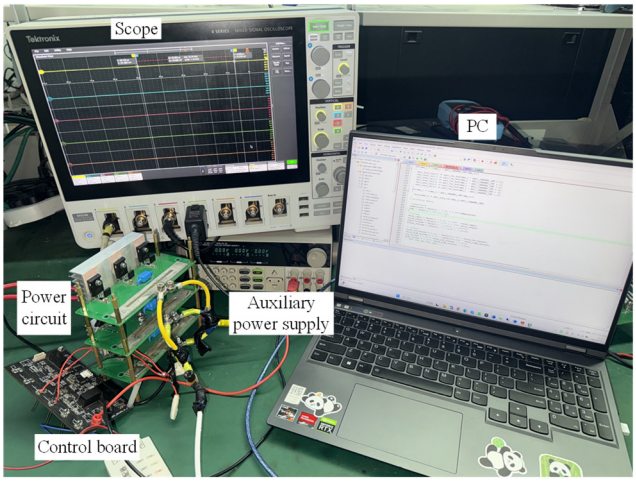


Figure 19. Experimental setup.

The implemented design utilizes the Qorvo UF3SC065007K4S SiC FET featuring a Kelvin source pin, driven by an Infineon IED3124MU12FXUMA gate driver IC (200 kV/µs common-mode transient immunity). With a peak output current of 14 A, the driver supplies approximately 1 A per channel under the configured turn-on gate resistance of 18.5 Ω. This single-driver configuration effectively controls all nine parallel MOSFETs while minimizing inter-device switching delays, thereby improving current sharing performance. For protection, a shunt resistor [29] enables overcurrent and short-circuit detection with a measured response latency of around 500 ns.

6.1. SSPC Switching Test

The switching transient performance of the SSPC was investigated under conditions of 270 V DC bus voltage and a resistive load. The measured voltage and current waveforms during turn-on and turn-off are presented in Figures 20 and 21, respectively. A noticeable voltage overshoot is observed during turn-off, where the peak voltage reaches 297.5 V. Note that the black trace represents the turn-on and turn-off signals received via communication.

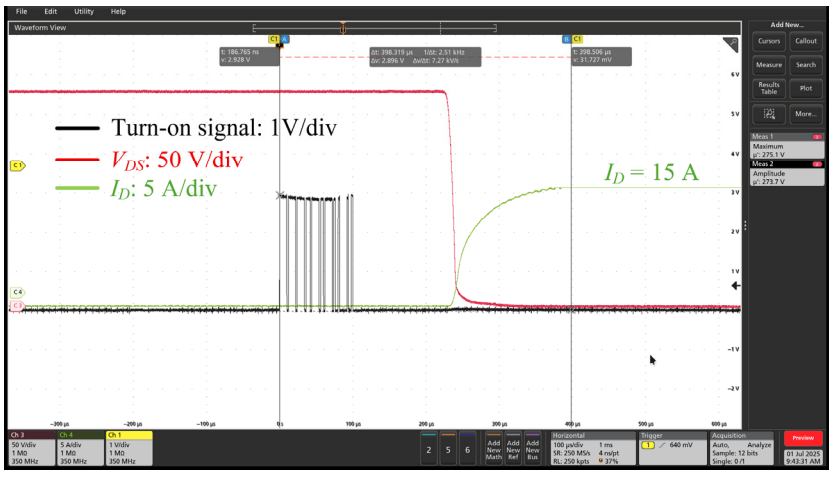


Figure 20. SSPC turn-on voltage and current waveform.

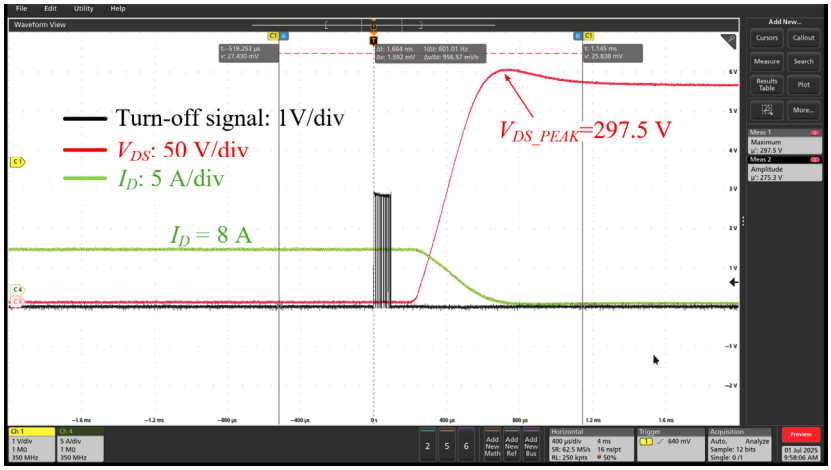


Figure 21. SSPC turn-off voltage and current waveform.

6.2. Current Balancing Experiment

Figure 22 shows the current waveforms of the nine parallel power devices operating under a 300 A load. Analysis of these waveforms, following Equation (11), reveals a steady-state current balancing unbalance factor of 4.2%. The dynamic current balancing unbalance factor is 2.2% during turn-on and 7% during turn-off, respectively. These results indicate that the current sharing among the parallel devices is satisfactory. Note that the current unbalance factor during turn-on, steady-state, and turn-off is measured at points A, B, and C, respectively.

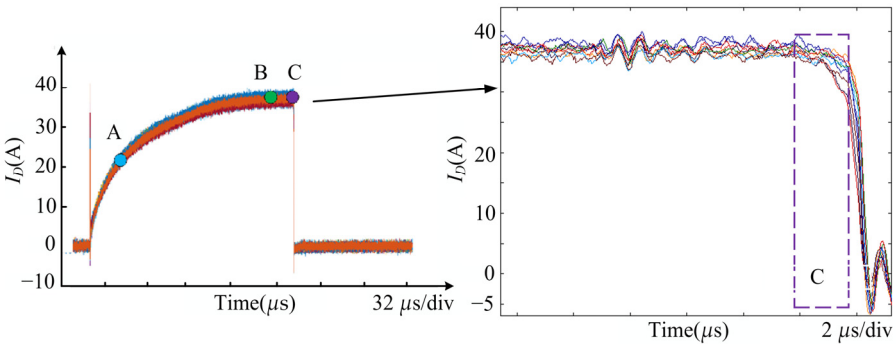


Figure 22. Current balancing performance of the SSPC.

6.3. Overvoltage Suppression Effect of RC-TVS

Figure 23 illustrates the experimental waveform obtained under a fault current of 1.6 kA and a parasitic inductance of 40 µH. The waveform shows that the peak voltage across the power device reached 475 V, while the clamping voltage provided by the RC-TVS circuit was 295 V. These results demonstrate the effectiveness of the proposed RC-TVS circuit in suppressing overvoltage during the SSPC turn-off process.

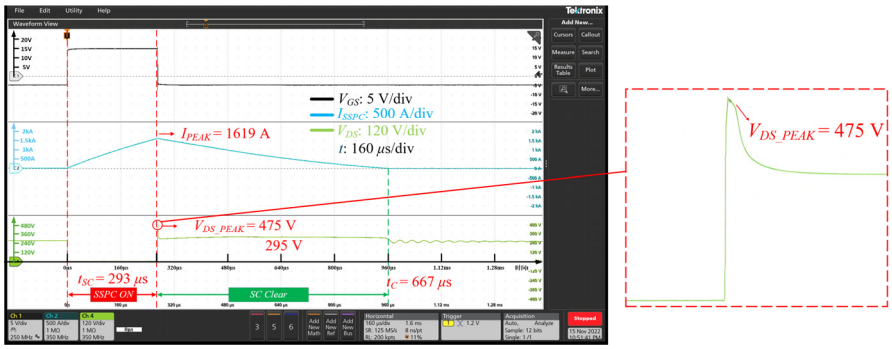


Figure 23. Turn-off voltage spike of the SSPC.

6.4. Short-Circuit Experiment

Figure 24 illustrates the turn-off waveform of the SSPC under a short-circuit fault, where the peak short-circuit current reached 1.82 kA. During the short-circuit turn-off process, the drain-source voltage peaked at 483 V, and the total turn-off duration was 700 µs. The results indicate that the proposed SSPC design strategies can successfully balance the current among the 9 branches and effectively mitigate the voltage spike during short-circuit faults.

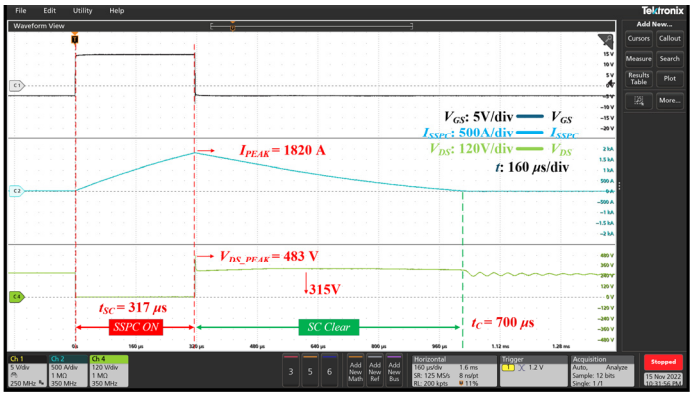


Figure 24. Turn-off voltage spike of the SSPC during short-circuit fault.

6.5. Thermal Experiment

Thermal performance of a single power module was evaluated under the load current of 100 A. Figure 25 shows the temperature distribution of the module after 30 min of stable operation at an ambient temperature of 23 °C. The maximum measured case temperature of the power device was 65.9 °C, which is in close agreement with the estimated junction temperature of 68 °C, exhibiting a difference of approximately 2.1 °C.

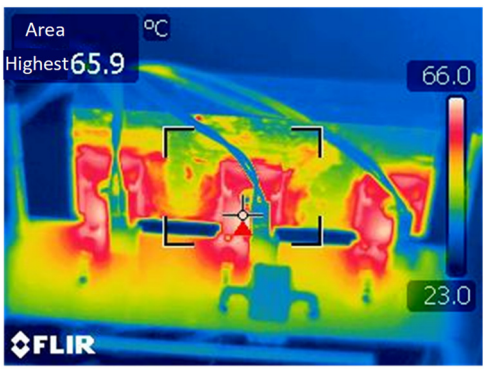


Figure 25. SSPC thermal images during steady-state operation.

6.6. Applicability and Limitations

The current design establishes a foundational framework for SSPC applications, and its analysis has not been formally verified for compliance with applicable certification standards. To address the specific influences on component selection and system robustness, the following points should be considered for aircraft integration.

Firstly, concerning high-altitude operation and partial discharge, the busbar spacing (e.g., 4 mm used in the prototype) is a preemptive design based on the understanding that creepage and clearance requirements significantly increase with altitude. The final specification must be determined by the maximum altitude of the specific aircraft and relevant environmental standards. Regarding EMC robustness, the TVS is not designed to withstand direct, several-kilovolt ESD or lightning surges. A system-level design, such as installing the SSPC within a well-grounded metallic enclosure, is mandatory to shunt such high-energy transients. Furthermore, for communication robustness in a harsh aircraft electromagnetic environment, the prototype wiring should be enhanced to a 120 Ω shielded twisted pair for the CAN bus, complemented by differential isolation.

These design measures enhance the SSPC compatibility with the stringent requirements of airborne applications.

7. Conclusions

This paper presents the development of a high-power DC SSPC that uses discrete power devices tailored for aircraft electrical systems. The study focused on key challenges, including parallel current balancing, voltage spike suppression, and transient thermal design, which were examined in detail. To address these challenges, this paper proposes a parasitic parameter compensation strategy based on an irregular-shaped busbar. The method analyzed the impact of slot dimensions in the busbar on current sharing performance, and conducted a theoretical analysis of the optimal design method for busbars. Then, an RC-TVS type overvoltage mitigation circuit is proposed along with its parameters design strategy to absorb the energy stored in the loop inductances. Furthermore, thermal stress induced by high magnitude fault current is analyzed. This approach analyzes equivalent power dissipation and thermal impedance characteristics during transient conditions, enabling optimized paralleling of power devices while ensuring safe operating temperatures. Finally, the effectiveness of these proposed strategies was experimentally verified using a 270 V/300 A SSPC prototype with a short-circuit current rating of 1.8 kA. The proposed design ensures that the steady-state and dynamic current unbalance factor among the 9 parallel power devices remains within 7%.

Author Contributions: Conceptualization, X.Z.; methodology, X.Z. and C.X.; software, C.X. and X.L.; formal analysis, X.Z. and C.X.; Validation, C.X. and K.M.; investigation, X.W. (Xuanlyu Wu); resources, X.W. (Xuanlyu Wu) and X.W. (Xiaohua Wu); data curation, X.C.; writing—original draft preparation, C.X.; writing—review and editing, X.Z. and K.M.; visualization, X.C.; supervision, X.Z.; project administration, X.L.; funding acquisition, X.W. (Xiaohua Wu). All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

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