

Article

Wideband ASK-OOK Data Recovery Circuit for Data Transmission in Over-Coupled Mode of SWPDT System

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Abstract: This paper presents an efficient wideband data recovery circuit (DRC) for forward data transfer in the over-coupled mode of dynamic SWPDT systems. In the over-coupled mode, where the operating frequency varies, conventional DRCs often become ineffective due to their limited operating frequency range. To address this issue, we propose a wideband DRC using amplitude shift keying (ASK) with on-off keying (OOK) modulation. The proposed circuit also eliminates the need for diodes and averaging circuits, which are typically required in traditional designs. The proposed circuit achieves data recovery by passing the OOK-modulated signal through a proposed Voltage-to-Time Converter (VTC), followed by a comparator and inverter. Implemented in 180 nm CMOS technology, the circuit occupies an area of 2440 μm^2 and a power consumption of 52.08 μW . The circuit can operate across a wide range of carrier frequencies. It was tested and validated with OOK-modulated signals at 5 MHz, 50 MHz, and 150 MHz, confirming its versatility and robustness. The prototype circuit enables wireless data transmission in critically coupled, weakly coupled, and over-coupled modes of WPT systems, achieving a 2 Mb/s data rate without requiring receiver repositioning.

Keywords: wideband; data recovery circuit (DRC); on-off keying (OOK); wireless power transfer



Academic Editor: Paulius Sakalas

Received: 8 November 2024

Revised: 23 December 2024

Accepted: 14 January 2025

Published: 17 January 2025

Citation: Ullah, N.; Barakat, A.; Kanaya, H.; Pokharel, R.K. Wideband ASK-OOK Data Recovery Circuit for Data Transmission in Over-Coupled Mode of SWPDT System. *Electronics* **2025**, *14*, 355. <https://doi.org/10.3390/electronics14020355>

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1. Introduction

Recently, simultaneous wireless power and data transfer (SWPDT) has gained attention due to its ability to minimize system size by using the same inductive coils for both functions [1–4]. These inductive coupling systems operate in three modes: weakly coupled, critically coupled, and over-coupled [5]. A key challenge arises in the over-coupled mode, where frequency splitting occurs as the Receiver (Rx) moves closer to the Transmitter (Tx), generating two frequencies (f_{os1}, f_{os2}), as shown in Figure 1 [6]. This results in a significant drop in wireless power transfer efficiency and disrupts data recovery, which is typically designed for a single frequency, leading to data transfer malfunctions. The operating frequency ω_{OP} can be calculated as (1).

$$\omega_{OP} = \begin{cases} \omega_R & k < y \\ \omega_R \left(1 \pm \frac{1}{2} \sqrt{(k^2 - y^2)} \right) & k > y \end{cases} \quad (1)$$

where ω_R is the resonance frequency with no load, k is the coupling coefficient of inductive system, and y is the loss constant. When the coupling coefficient (k) is lower than the critical

coefficient value, the system operates within the weak coupling region. However, if k surpasses this critical threshold, the system transitions into an over-coupling region. In the over-coupled region, the frequency deviates by approximately $\pm 20\%$. To improve power efficiency, a dynamic response in WPT systems has recently been achieved using non-linearity parity–time (PT) symmetry circuits, offering improved performance regardless of the variation in transfer distance between the Tx and Rx [6].

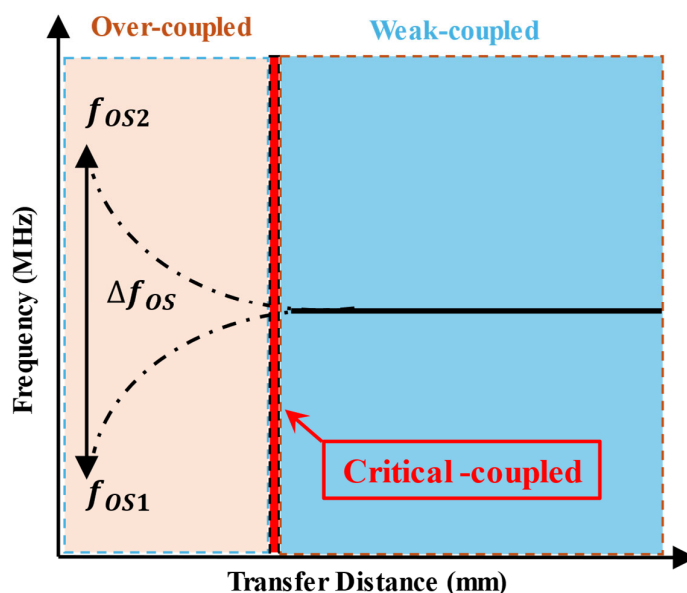


Figure 1. Operating frequency response with respect to transfer distance.

For biomedical implants, various modulation schemes have been reported [6–10] such as ASK [6,10], Frequency Shift Keying (FSK) [11], and Phase Shift Keying (PSK) [12]. Among them, ASK modulation is commonly used due to its simplicity and low power consumption requirements. Within ASK modulation, OOK is frequently employed to modulate the data by switching the carrier signal on and off. Figure 2a illustrates a schematic of an inductively coupled SWPDT system with ASK-OOK modulation. At the transmitter end, the amplitude of the carrier signal is modulated to encode data, as depicted in Figure 2b, where the presence and absence of the carrier signal correspond to bit values of 1 and 0, respectively. A demodulator circuit is used for data recovery at the receiver end, as shown in Figure 2c.

Traditionally, data from a modulated ASK-OOK signal can be recovered using an envelope detector (ED)-based demodulator circuit. It comprised diode, an averaging circuit, and a voltage comparator. However, the diode-based ED system is limited to a fixed carrier frequency and suffers from high power consumption due to energy loss during diode conduction [13]. Additionally, traditional ASK designs require large capacitors, which occupy a large chip area [14]. To reduce chip size, capacitor-less, and all-MOS-based ASK architectures have been developed [15,16] to address the need for efficient data recovery in communication systems. Despite these advancements, such designs exhibit lower data rates [10] and higher power consumption [15,16]. To overcome these drawbacks, MOS-based active switch shaper architectures were introduced [17], offering a smaller chip area but achieving a lower data rate of 0.5 Mb/s. In response to the growing demand for higher data rates, carrier width modulation (CWM) techniques were developed to support multiple carrier frequencies [12]. However, these designs still suffer from large chip areas and complex circuitry at the demodulator side to recover the data. Since the data recovery methods proposed so far [14–17] operate at a single frequency, they are unable to recover data when the Rx moves closer to the Tx, as shown in Figure 1. These limitations highlight

the need for a data recovery method that can efficiently function across a wide range of frequencies.

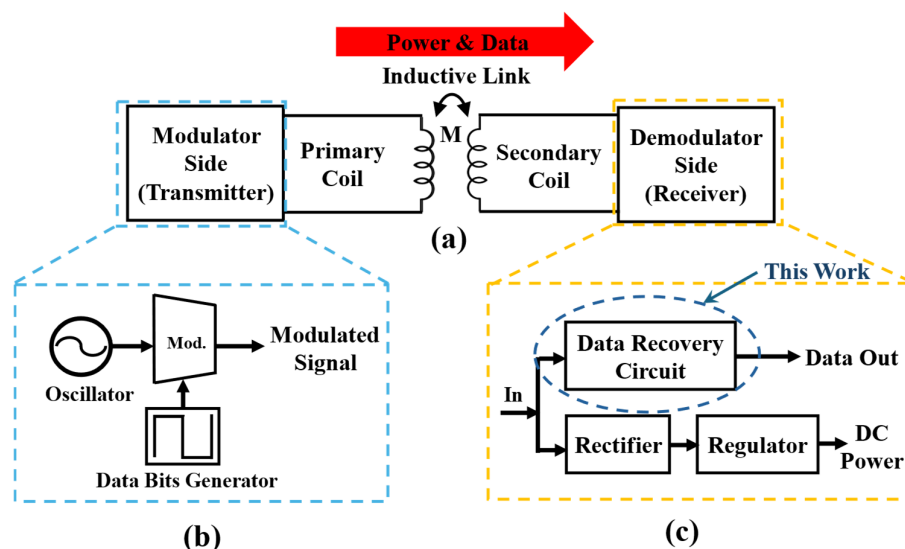


Figure 2. Typical block diagram wireless power and data transfer over inductive coupled link utilizing ASK-OOK modulation. (a) Inductive coupled link; (b) transmitter end for modulation; (c) receiver end for data and power recovery.

To overcome the limitations of fixed carrier-frequency-based methods, we propose a wideband ASK-OOK data recovery circuit (DRC) that can efficiently recover data regardless of carrier frequency changes. This circuit employs a Voltage-to-Time Converter (VTC), a comparator, and an inverter to achieve efficient data recovery across a wide range of frequencies. The designed chip was implemented in 180 nm Complementary Metal Oxide Semiconductor (CMOS) technology and tested.

The remaining sections of this paper are as follows: Section 2 discusses the proposed data recovery circuit design. Section 3 covers the fabrication process, where the circuit is implemented using 180 nm CMOS technology, along with the measurement setup used for performance evaluation. Section 4 presents the experimental results, validating the system's performance through various metrics. Finally, Section 5 concludes this paper, summarizing the findings.

2. Proposed Data Recovery Design

Figure 3 illustrates the architecture of the proposed DRC, which addresses the issue of limited operating frequency range observed in conventional designs. The recovery process begins by feeding the modulated OOK signal into a Voltage-to-Time Converter (VTC). The VTC converts the modulated ASK-OOK signal into a sawtooth waveform with two distinct levels determined by the *toff* of the incoming ASK-OOK signal. This waveform is then processed by a comparator circuit, which transforms it into a square wave. Finally, an inverter circuit flips the polarity of the square wave, producing the recovered data signal. This step ensures reliable decoding of the transmitted data by subsequent receiver stages.

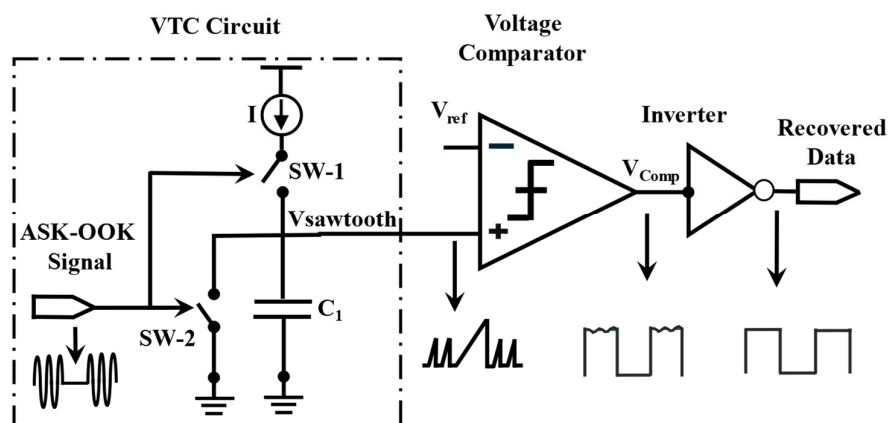


Figure 3. Proposed architecture of the implemented data recovery circuit.

2.1. Conversion of ASK-OOK to Sawtooth Signal

The first stage of the designed circuit is the VTC shown in Figure 4. The VTC plays a critical role in the proposed data recovery process by converting the modulated input OOK signal into a time-based signal. This converter circuit transforms the OOK signal into a sawtooth waveform. It employs a complementary pair of switch-based integrators, replacing ED and averaging circuits.

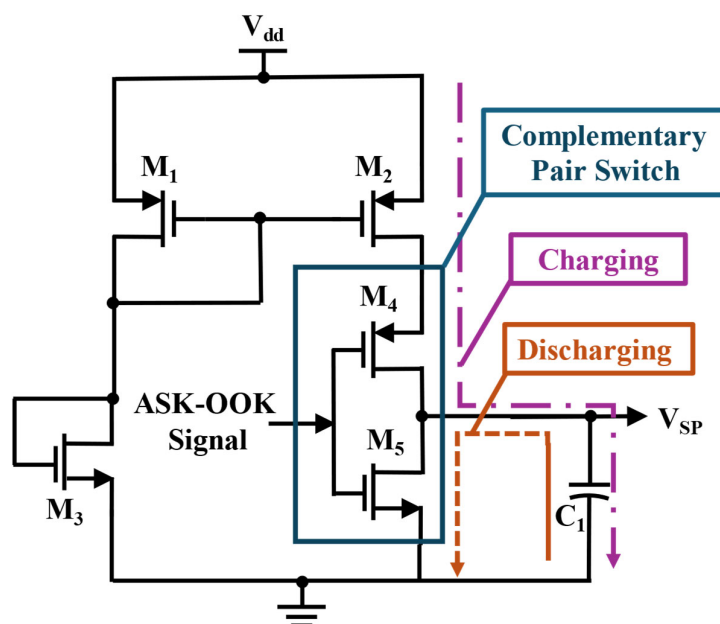


Figure 4. Schematic of the proposed Voltage-to-Time Converter circuit.

A complementary pair of NMOS (M5) and PMOS (M4) transistors is employed to charge and discharge the capacitor under specific biasing conditions. When the input voltage amplitude falls below the threshold voltage at the gate of NMOS transistor M5, PMOS transistor M4 conducts while M5 remains inactive. Consequently, current flows through M4, charging the capacitor (C1) at the output. Charging continues until the input voltage surpasses the gate threshold of M5, causing M4 to turn off and M5 to turn on, initiating capacitor discharge. During the positive cycle of the carrier signal, the capacitor

discharges, and during the negative cycle, it charges. This alternating process results in the generation of an analog sawtooth peak signal V_{SP} . The capacitor voltage can be written as

$$V_{SP} = \begin{cases} V_i (1 - e^{-t/\tau_c}) \\ V_i e^{-t/\tau_d} \end{cases} \quad (2)$$

where V_i is the capacitor initial voltage, τ_c and τ_d are the time constants for charging and discharging, and they can be expressed as follows [7]:

$$\tau_c = (R_{ON2} + R_{ON4})C_1 \quad (3)$$

$$\tau_d = (R_{ON5})C_1 \quad (4)$$

The dimensions of the transistors and capacitor, shown in Table 1, are meticulously chosen to ensure sufficient current handling, a slow charging time constant for the capacitor, and rapid discharge times. This optimization guarantees efficient circuit operation across a range of signal conditions.

Table 1. Optimized dimensions in μm of the proposed VTC circuit.

Components	M1	M2	M3	M4	M5	C1 (665fF)
Width (μm)	0.5	1.0	0.3	3	3	25
Length (μm)	0.2	0.22	0.2	0.18	0.18	25

Additionally, the proposed ASK-OOK modulator circuit exhibits noise immunity, particularly during the off cycle (T_{off}) of the signal, where power supply noise becomes more significant relative to the signal strength. As shown in Figure 5, the noise level remains below the threshold voltage (V_{thn}) of the NMOS-5 transistor, ensuring that the VTC circuit's performance remains unaffected. This design enhances resilience to transient disturbances, offering robust noise tolerance and reliable operation even in low-amplitude signal conditions.

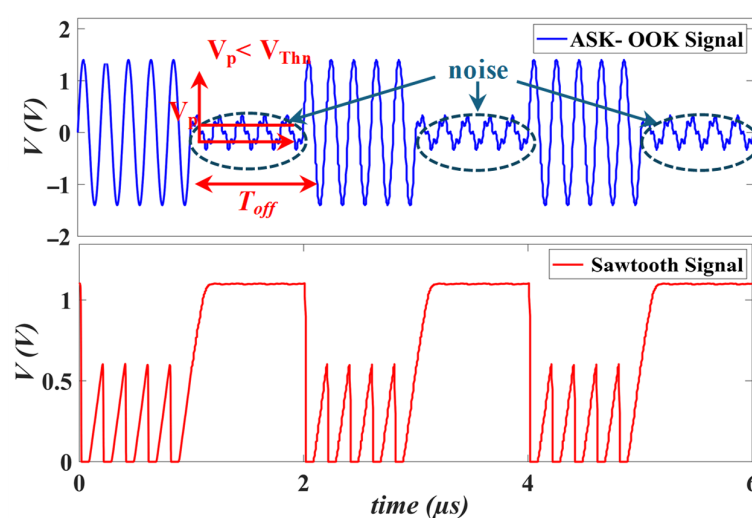


Figure 5. Time domain simulation result of the VTC circuit.

2.2. Conversion of Sawtooth Peak Signal to Square Wave

In the second stage, the sawtooth signal is converted into a digital bit stream using a comparator with an inversion output circuit, depicted in Figure 6. This process involves

comparing the sawtooth peak signal with an external voltage reference level (V_{ref}). When the sawtooth signal (In) at the comparator input exceeds the reference voltage, the comparator outputs a high voltage (V_{comp}). Conversely, when the signal drops below the reference, the output switches to a low voltage.

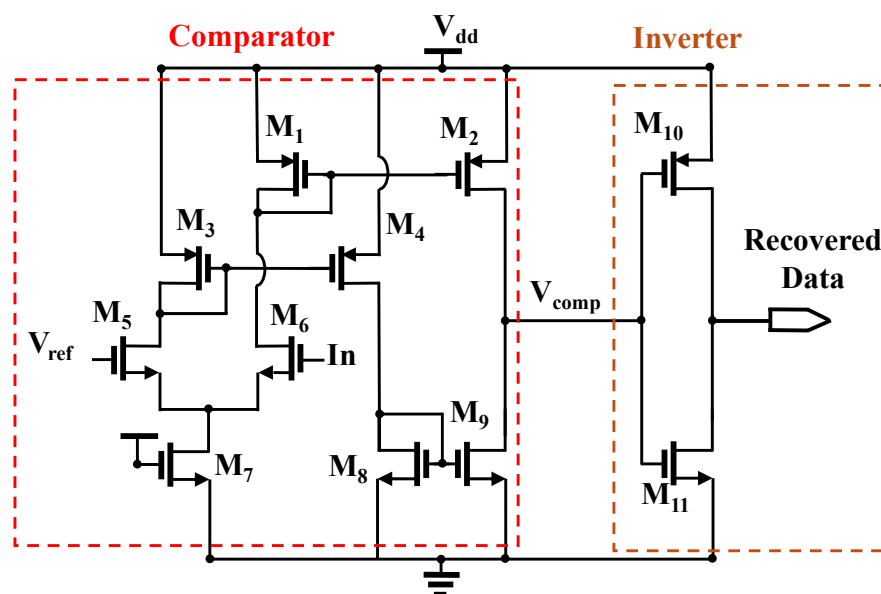


Figure 6. Schematic of comparator circuit for sawtooth peak signal to square wave.

The circuit is divided into three stages. The differential input stage processes the input signal (In) and the reference voltage (V_{ref}), where M_5 receives V_{ref} , and M_6 handles the input signal, generating a small differential signal. The tail current source, formed by M_7 , provides a constant current through the differential pair. The intermediate stage amplifies the small voltage difference generated in the first stage. Transistors M_3 and M_4 constitute a current mirror load, converting the differential current into a corresponding voltage signal. In the push–pull output stage, when $In > V_{ref}$, transistor M_2 turns on, pulling V_{comp} high, while for $In < V_{ref}$, M_2 turns off, enabling M_4 to pull V_{comp} low through M_9 . Finally, the inverter stage flips the polarity of V_{comp} , producing the recovered data signal.

The off time (T_{off}) of the signal varies with the data rate, leading to a proportional change in the output of the VTC circuit.

A push–pull comparator was used to detect the input signal and suppress minor VTC peaks, thereby generating a square waveform. A comprehensive parametric simulation was conducted to elucidate the delay in the comparator output relative to reference voltages. Upon analysis, we observed that higher V_{ref} levels can affect the different reference voltages, highlighting corresponding operational delays with increasing reference voltage, as shown in Figure 7. Therefore, to achieve optimal performance, we maintained $V_{ref} = 0.6V$ for the comparator. An external reference voltage source was utilized to provide the reference voltage.

The inversion output stage, formed by transistors M_{10} and M_{11} , plays a crucial role in processing the output of the comparator. This stage inverts and sharpens the signal, effectively converting the comparator’s analog output into a digital data signal, referred to as ‘Data Out.’ Figure 8 provides a detailed illustration of the signal processing flow within the system. It starts with the ASK-OOK modulated input signal delivered to the VTC, followed by the generated sawtooth waveform from the VTC. Subsequently, the comparator output waveform is shown, which reflects the intermediate signal prior to final

processing. The figure concludes with the recovered 'Data Out' signal, demonstrating the overall data recovery mechanism employed by the circuit.

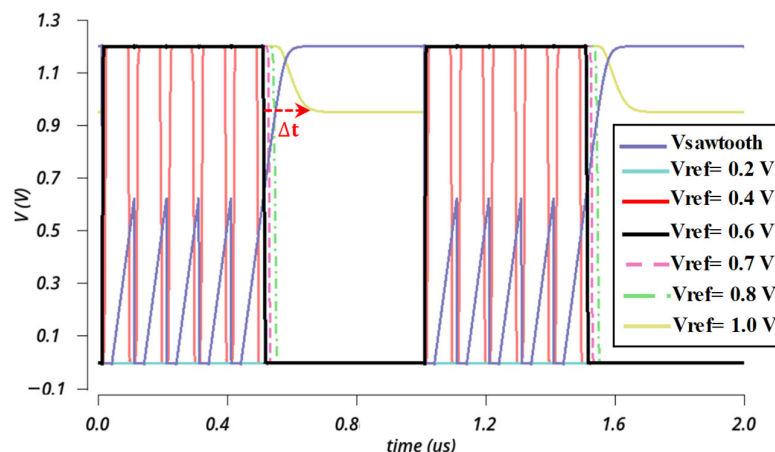


Figure 7. Output waveform of the comparator for different reference voltage.

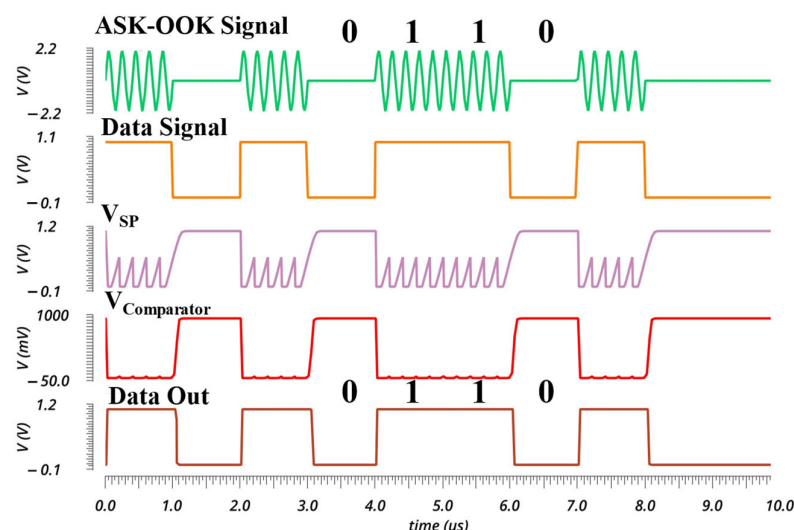


Figure 8. Time domain simulation results (in Cadence) of proposed DRC illustrating waveforms at each stage of the proposed ASK-OOK DRC for a 10 MHz carrier signal with a data rate of 2 Mb/s.

Furthermore, the proposed wideband DRC was thoroughly evaluated under a range of operating conditions, including variations in modulation indices, and environmental factors such as temperature fluctuations and process corners. This comprehensive analysis is essential for applications in wireless data transfer, particularly where data stability and recovery accuracy must be maintained across diverse conditions. As shown in Figure 9, a shmoo plot depicts the performance of the DRC, highlighting pass and fail conditions in data recovery across different test parameters. This plot effectively captures the circuit's resilience and robustness, showing its responses across various process variations, temperature extremes, and data rate ranges, providing a detailed assessment of its suitability for demanding wireless data transfer applications. The pass/fail criteria are defined by the reliability of data recovery displayed at the output of circuit, as analyzed using Cadence Virtuoso. The design shows failure at a 20% Modulation Index (MI) across all corner conditions due to minimum difference between the high voltage level and low voltage signal. The circuit fails in the SS corner at 30% MI, primarily due to significant output delay.

Temp.(°C) Mode. Index (%)	TT (−80 to 80)	FF (−80 to 80)	FS (−80 to 80)	SF (−80 to 80)	SS (−80 to 80)
MI= 100%					
MI=75%		Pass			
MI=50%					
MI=30%					
MI=20%					Fail

Figure 9. Shmoo plot illustrating different modulation indices versus various temperatures under distinct process corners, highlighting the performance characteristics of the data recovery circuit.

3. Fabrication and Measurement Setup

3.1. Fabrication

The data recovery circuit was fabricated using 180 nm CMOS technology. The layout was designed in the Cadence Virtuoso environment. The resulting prototype incorporates measurement pads for precise testing and evaluation, as shown in Figure 10, which illustrates the fabricated CMOS chip layout. Two EYEPASS PROBES (AC version) were used for on-wafer probing. This circuit prototype has an active area of $2440 \mu\text{m}^2$. It operates at 1.4 V DC, drawing $37.2 \mu\text{A}$ of current and leading to a power dissipation of $52.08 \mu\text{W}$. This dissipation is higher than the value reported in [14], primarily due to the circuit's broader carrier frequency range requirements.

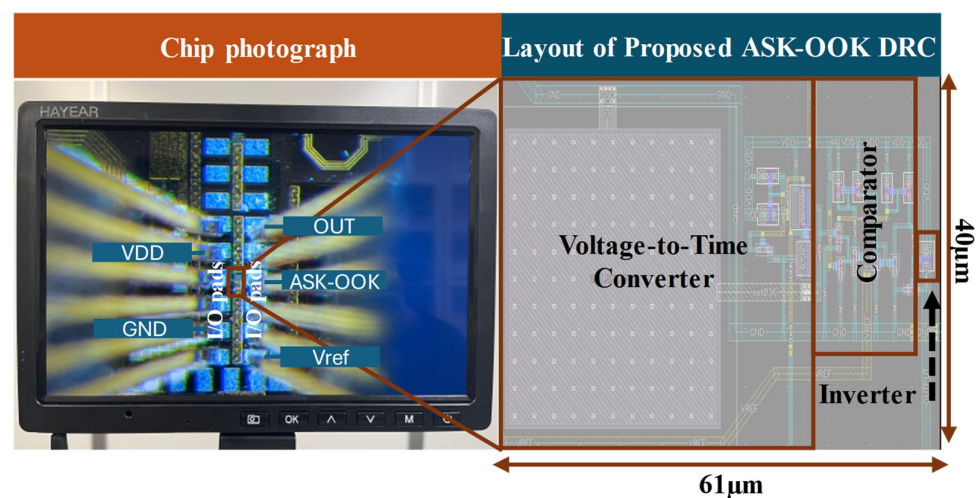


Figure 10. Fabricated chip micrograph (left) and layout (right) of the proposed ASK-OOK data recovery circuit with layout.

3.2. Measurement Setup

The measurement setup consisted of an NF multifunction generator (Model WF1968), which generated the OOK-modulated signal at a data rate of 2 Mb/s. It also included a RIGOL mixed-signal digital oscilloscope (Model MSO5354) with an active probe to measure the recovered data waveform, as shown in Figure 11. A Cascade probe station with two LGLLGL EYEPASS probes was used for on-wafer probing, allowing precise contact with the circuit under test. The DC power supply (Agilent B2962A) provided both the required power and a reference voltage (V_{ref}) of 0.6 V.

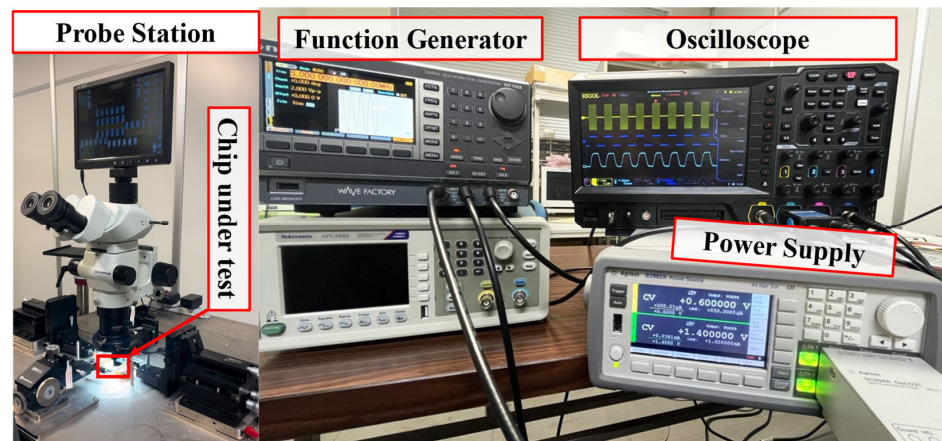


Figure 11. Experimental setup for proposed ASK-OOK data recovery circuit.

4. Experiment Results

This section presents the experimental results obtained from the testing and validation of the proposed system, highlighting key performance metrics, and demonstrating its effectiveness in data recovery across a range of modulated signals.

The OOK-modulated signal was generated using a multifunction generator with a data rate of 2 Mb/s. Figure 12a presents the results of the data recovery process for a 5 MHz carrier frequency. The top waveform (yellow) shows the 5 MHz modulated ASK/OOK signal, where amplitude variations encode the binary data. The middle waveform (blue) represents the original data signal, providing a reference for the intended binary sequence with high and low levels for binary '1' and '0', respectively. The bottom waveform (cyan) illustrates the recovered data, showing the output of the data recovery circuit, which accurately demodulates the signal and reconstructs the original data sequence. This confirms the circuit's capability to retrieve data at 2 Mb/s using a 5 MHz carrier frequency.

Figure 12b shows the data recovery results for a 50 MHz carrier frequency, with a data rate of 2 Mb/s. Similar to Figure 12a, the top waveform (yellow) displays the 50 MHz ASK/OOK-modulated signal. The middle waveform (blue) is the original data signal, while the bottom waveform (cyan) shows the recovered data. The circuit effectively demodulates the 50 MHz modulated signal, accurately reconstructing the binary data sequence and validating its performance under this increased carrier frequency.

Figure 12c illustrates the performance of the data recovery circuit for a 150 MHz carrier frequency with the same data rate of 2 Mb/s. The top waveform (yellow) represents the 150 MHz OOK-modulated signal, while the middle waveform (blue) shows the original data signal. The bottom waveform (cyan) is the recovered data, indicating successful data recovery even at this high carrier frequency. These results validate the circuit's wideband capability for robust data recovery across varying carrier frequencies, ensuring reliable performance for applications with high data rates and different operating conditions.

Table 2 presents a comparison of the experimental results for the proposed data recovery circuit with state-of-the-art methods. The proposed design demonstrates operation over a wide frequency range of 5 MHz to 150 MHz. Compared to the results reported in [18–21], our approach achieves a significantly more compact size of $2440 \mu\text{m}^2$, making it a highly efficient solution for wideband data recovery. Additionally, the circuit demonstrates low energy consumption per bit, with an energy dissipation of 26.08 pJ/bit during data transmission while supporting high data rates of up to 2 Mbps. To evaluate the performance of our design, we utilize various figures of merit (FoMs) that consider critical parameters such as data rate, power consumption, area, and the fabrication process. The FoM from [17] includes critical parameters such as data rate, power consumption, area, and the fabrication

process, which are essential for assessing the efficiency of the design. These metrics allow for a comprehensive analysis and comparison with existing technologies in terms of overall performance and feasibility. The $[FoM]^1$ in [13] includes data rate, power consumption, area, and fabrication process, as expressed in (5):

$$[FOM]^1 = \frac{\text{Data rate} \times (\text{Process})^2}{\text{Carrier Frequency} \times \text{Power} \times \text{Area}} \quad (5)$$



Figure 12. Measured waveforms at a 2 Mb/s data rate, displaying the ASK-OOK modulated and data signals, and recovered data for modulated signals at (a) 5 MHz, (b) 50 MHz, and (c) 150 MHz.

Table 2. Comparison table of previous works with our proposed method.

References	TBCAS [19]	TBCAS [20]	JSSC [21]	TBCAS [22]	Our Work
Year	2024	2024	2024	2022	2024
Modulation Type	ASK	ASK	LSK	LSK	OOK
CMOS Technology (μm)	0.25	0.18	0.065	0.18	0.18
Carrier Frequency (MHz)	13.56	6.78 and 13.56	13.56	13.56	5–150
Data Rate (Mbps)	0.5	0.678	0.42	1	2
Power (μW)	94.88	46	-	280	52.08
Active Area ($10^3\mu\text{m}^2$)	23	820	48.40	514.00	2.44
Wideband Carrier (MHz)	No	No	No	No	Yes
E/b (pJ/bit)	189	67	N. A	280	26.08
$[\text{FoM}]^1 \times 10^{-2}$	0.72	8.59	N.A.	0.002	10.20
$[\text{FoM}]^2 \times 10^{-2}$	0.72	17.18	N.A.	0.002	305.96

To ensure a fair and comprehensive comparison, we have introduced an additional figure of merit, denoted as $[\text{FoM}]^2$, to better capture the performance characteristics of the proposed design relative to other state-of-the-art methods. The expression for $[\text{FoM}]^2$ is given in (6).

$$[\text{FoM}]^2 = \frac{\text{Data rate} \times (\text{Process})^2 \times \frac{f_{\max}}{f_{\min}}}{\text{Carrier Frequency} \times \text{Power} \times \text{Area}} \quad (6)$$

which also includes the carrier frequency ratio $= \frac{f_{\max}}{f_{\min}}$, in which the $f_{\max}$ and $f_{\min}$ are the maximum carrier frequency and minimum carrier frequency. In our experiment, the maximum and minimum frequencies were 150 MHz and 5 MHz, respectively. The key parameters were data rate, process technology, maximum and minimum frequency ratios, carrier frequency, power consumption, and chip area. By considering these factors, $[\text{FoM}]^2$ provides a broader evaluation, accounting for both the efficiency and scalability of the design in various operational conditions. This allows for a more accurate comparison of the overall performance and feasibility across different technologies.

To the best of our knowledge, the proposed circuit outperforms previously reported methods in terms of key figures of merit (FoMs), demonstrating enhanced efficiency and effectiveness. Additionally, the method shows notable versatility, operating across a wide range of carrier frequencies and supporting data rates up to 2 Mb/s, ensuring consistent high performance under varying conditions. Overall, the results validate the proposed approach and highlight its promising potential for data transfer in biomedical implants, utilizing a single inductive link for communication.

5. Conclusions

A novel wideband ASK-OOK data recovery circuit has been proposed for data transmission in the over-coupled mode of wireless data and power transfer systems. The design integrates a VTC, comparator, and inverter, facilitating robust data recovery across a range of coupling modes. The prototype chip, fabricated in 180 nm CMOS technology, achieves a data rate of 2 Mb/s with a power consumption of 52.08 μW . Furthermore, with a compact area of 2440 μm^2 , the design is optimized for space-constrained applications. It demonstrates significant potential for efficient and reliable wireless data transmission in dynamic SWPDT systems, not only in weakly coupled and critically coupled modes but also in

strongly coupled mode, making it suitable for health monitoring system in biomedical applications.

Author Contributions: Conceptualization, N.U., A.B., H.K. and R.K.P.; methodology, N.U.; software, N.U., A.B. and H.K.; validation, N.U., A.B. and H.K.; formal analysis, A.B.; investigation, A.B. and H.K.; resources, R.K.P.; data curation, N.U.; writing—original draft preparation N.U.; writing—review and editing, A.B., H.K. and R.K.P.; visualization, N.U.; funding acquisition, A.B. and R.K.P.; supervision, A.B. and H.K.; and R.K.P. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by MIC/SCOPE, Grant Number: JP215010003, and in part by the JSPS KAKENHI, Grant Numbers: 21K04178 and 22K14260. This work is also supported by the VLSI Design and Education Center (VDEC), The University of Tokyo in collaboration with Cadence Corporation, the Mentor Graphics Corporation, and Keysight Technologies Japan, Ltd.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

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