

Review

Research Trends and Challenges of Integrated Constant On-Time (COT) Buck Converters

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Abstract

Constant on-time (COT) buck converters offer fast transient responses and a simple architecture but face challenges like switching frequency variation, instability with low-equivalent series resistance (ESR) capacitors, and DC output voltage offset. This paper reviews advanced COT control techniques developed to overcome these limitations. We examine methods for frequency stabilization (e.g., adaptive on-time, phase-locked loop), stability with low-ESR capacitors (e.g., passive and active ripple injection, virtual inductor current), and improved DC regulation (e.g., offset cancellation). This review also covers techniques for optimizing transient response and multiphase architectures for high-current applications.

Keywords: power management IC (PMIC); constant on-time (COT) control; buck converter; DC-DC converter; ripple injection; transient response; frequency stabilization

1. Introduction

In the past two decades, advancements in mobile devices have spurred on the development of power management ICs (PMICs). Now, with the rise of artificial intelligence (AI) and electric vehicles (EVs), PMICs are poised for a new era of growth. Modern power management systems for high-performance computing, such as AI servers, are tasked with delivering power efficiently and with a fast transient response from a location very close to the processor. A converter that supplies power from a location very close to the processor is called a point-of-load (POL) converter. The concept of these POL converters is being used not only for AI processors but also for modern memory modules and converters for automotive systems, both of which have a surging demand for fast transient responses and high efficiency. For example, modern DDR5 memory modules are required to have steep load transient characteristics of 10 A/ μ s and a high efficiency above 85% (92.5% peak efficiency) over a wide load range (100 mA~10 A) [1]. In addition to a fast transient response and high efficiency, a common challenge across these applications is also the need for high step-down conversion ratios, which is defined as a conversion ratio of 10:1 or more (e.g., 12 V to 1 V), which require an extremely small on-duty cycle. This very short on-time makes the system highly susceptible to noise, causing significant issues with stability and regulation accuracy.

In conventional PMICs, the pulse-width modulation (PWM) controller has typically been used as a linear control approach. PWM controllers can be broadly categorized into voltage mode control (VMC) and current mode control (CMC), which operate at a fixed frequency and regulate the output voltage and current by adjusting the pulse width.



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However, they often require complex compensation networks to enhance stability, which may fail to meet the fast transient characteristics required for POL converters. Additionally, their fixed-frequency operation can lead to reduced efficiency under light load conditions. To overcome these drawbacks, a nonlinear control technique known as hysteretic mode control (HMC) can be used [2]. Traditionally, HMC uses a bang–bang control method that sets high- and low-voltage boundaries to keep the output voltage within that range. HMC does not require a complex compensator for control and offers the advantage of a very fast transient speed due to its variable frequency. Furthermore, in light-load situations, it has the advantage of automatically slowing switching operations, which can increase light-load efficiency [3]. Therefore, it is advantageous to introduce HMC to satisfy a fast transient response and high efficiency across a wide load range. However, traditional HMC techniques have some disadvantages, including a wide variable frequency range that leads to EMI issues and an inability to reduce output ripple. Although current mode hysteretic control (CMHC) was introduced to overcome this [3–9], EMI problems can still arise if clock synchronization or a phase-locked loop (PLL) is not used, as the frequency can still fluctuate significantly. Moreover, in high step-down situations, the regulation performance can be degraded by the effects of jitter caused by the comparator and logic components. This irregular switching caused by jitter can exacerbate EMI problems and increase the likelihood of switching loss. In this context, constant on-time (COT) control offers a robust solution. By fixing the on-time, COT control makes the on-duty cycle less vulnerable to noise compared with traditional VMC, CMC and conventional HMC particularly in short duty-cycle condition. As a form of HMC, COT control is a pulse frequency modulation (PFM) control method that enables high-speed operation during transient events, making it an excellent candidate for POL converters that require a fast response [10,11]. The conventional COT controller is architecturally simple, requiring only a comparator and an on-time generator. Its compensation-free structure allows for operation beyond the bandwidth limitations of compensation networks. Additionally, its inherent pulse-skipping characteristic at light loads ensures high efficiency over a wide load range [12,13]. Although the COT controller has long been a subject of research in discrete applications, it is now widely applied in the power management integrated circuit (PMIC) field to meet the wide load range (e.g., 100 mA–10 A), high step-down (e.g., 12 V to 1 V), and fast transient (e.g., 10 A/ μ s) characteristics demanded by AI servers, memory modules, and automotive applications.

However, conventional COT control has several inherent limitations. The use of low-ESR capacitors, which are desirable for reducing overall system ripple, can cause instability and sub-harmonic oscillations in COT controllers [14]. Another issue is the DC output voltage offset, which degrades regulation accuracy. This occurs because the conventional COT controller compares the divided feedback voltage directly with a reference voltage, causing the feedback voltage's valley point to coincide with the reference voltage. To overcome these challenges while retaining the advantages of COT control, various ripple injection and offset cancellation techniques have been developed [10,14–22]. Moreover, the switching frequency can fluctuate significantly with changes in input voltage, output voltage, and load current, which complicates the design of electromagnetic interference (EMI) filters. To address this frequency deviation, an adaptive on-time (AOT) controller has been proposed, which dynamically adjusts the on-time based on the input voltage, output voltage, and load current to achieve a relatively constant switching frequency [12,13,16,23–28].

This paper is structured as follows. Section 2 examines the operation of a conventional constant on-time (COT) controller and compares it with conventional voltage mode control (VMC), current mode control (CMC), and hysteretic mode control (HMC) controllers, while also detailing the problems that can arise with conventional COT control. Section 3

presents research that has addressed the instability issues caused by low ESR and the DC offset issue [8,10,11,14–22,29–33]. Section 4 introduces methods developed to resolve the frequency deviation of COT controllers [11,13,16,23–28]. Section 5 discusses recent research challenges related to COT controllers, specifically the optimization of transient speed [11,16,18,23,34–36] and the development of COT methods for multiphase topologies [1,3,34,37–48].

2. Conventional Constant On-Time Control

2.1. A Comparative Analysis of COT and PWM Control

The constant on-time (COT) buck converter operates based on an event-driven switching decision, directly sensing the output voltage and comparing it to a reference voltage (V_{REF}). This enables it to react instantly to load changes, delivering a fast dynamic performance that overcomes the bandwidth limitations of traditional pulse width modulation (PWM) controllers. The conventional operation principle of COT control and CMC in a buck converter are expressed in Figure 1.

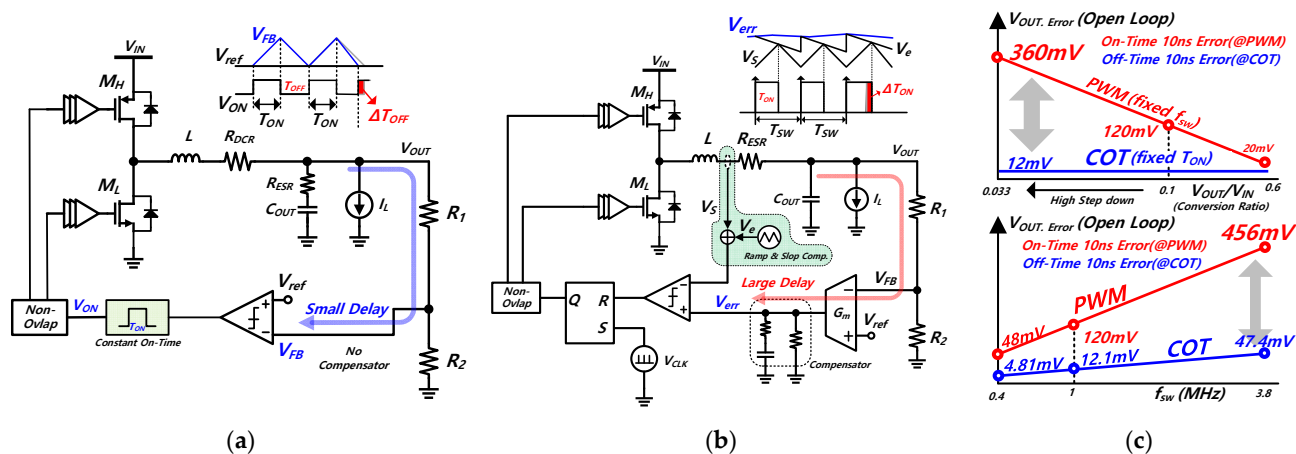


Figure 1. (a) Conventional COT control buck converter architecture. (b) Conventional CMC buck converter architecture. (c) Output voltage error comparison between PWM and COT control.

As shown in Figure 1a, the conventional constant on-time (COT) control loop senses the feedback voltage (V_{FB}), which is a divided version of the output voltage (V_{OUT}). When V_{FB} drops below V_{REF} , a fixed on-time pulse (T_{ON}) is generated, turning on the high-side switch M_H . During this T_{ON} period, the inductor current increases and charges the output capacitor, causing the output voltage to increase. At the end of the T_{ON} period, the high-side switch turns off, and the off-time (T_{OFF}) begins with the low-side switch M_L turning on. The T_{OFF} period continues until V_{FB} decreases and again meets the threshold voltage (V_{REF}), at which point a new switching cycle repeats. In this operation, the output voltage ripple effectively serves as the “ramp signal” for switching decisions. Because the output voltage itself is the basis for changing the switch state, it differs from traditional pulse width modulation (PWM) controllers that wait for a fixed clock cycle. PWM controllers are broadly classified into voltage mode control (VMC) and current mode control (CMC). PWM control typically regulates the output voltage (V_{OUT}) by amplifying the difference between the output voltage and a reference voltage (V_{REF}) into an error voltage (V_{ERR}) through an error amplifier and a compensator as shown in Figure 1b. This error voltage is then compared with a ramp signal to generate a pulse-width modulated (PWM) signal with a linear duty cycle. In voltage mode control (VMC), an artificial ramp signal is used for this comparison. In contrast, current mode control (CMC) utilizes the sensed inductor current as the ramp signal.

Conventional voltage mode control (VMC) utilizes a single control loop and a compensation network to regulate the output voltage. This method generates a PWM signal using a ramp signal with a fixed frequency and an error amplifier. However, using a compensator with a large time constant for stability can limit the control loop's bandwidth, leading to a slow transient response. Conventional CMC adds a current sensor and a slope compensator to the conventional VMC structure as shown in Figure 1b. This inner current loop effectively reduces the power stage's double pole to a single pole. This allows for a faster response compared with VMC. However, conventional CMC still uses large time constant compensators and requires slope compensation to prevent sub-harmonic oscillation at duty cycles exceeding 50%, which may limit its transient response. In comparison, the COT control method, a type of hysteretic mode control (HMC), is a clock-free, event-driven technique. This characteristic allows it to bypass the compensator delays inherent in both VMC and CMC, resulting in a very fast response [11]. Furthermore, its event-driven nature automatically performs pulse-skipping during light-load operation, enabling high-efficiency operation across a wide load range [12].

Furthermore, as illustrated in Figure 1c, constant on-time (COT) control offers an advantage over PWM control in high step-down applications where the on-duty cycle is inherently small. The effectiveness of COT control in such cases can be understood through a simple calculation. Let us consider a buck converter using PWM control that operates at a switching frequency of 1 MHz to achieve a 1.2 V output from a 12 V input. In this high step-down scenario, the on-duty time is approximately less than 100 ns. If an on-duty error of 10 ns occurs due to jitter or other external disturbances, the output voltage would change to 1.08 V, representing a significant error. In contrast, COT control operates by fixing the on-time and modulating the off-time. Assuming a COT-controlled buck converter also operates at an average frequency of 1 MHz, a similar 10 ns error occurring in the off-time (because of constant on-time control) would only change the on duty from 0.1 to 0.101. Consequently, the output voltage would shift from 1.2 V to 1.212 V, resulting in a much smaller error of only 12 mV. Therefore, COT control can be seen as having a significant advantage over PWM control as a control method for modern point-of-load (POL) converters that require high step-down ratios, such as 48 V to 1 V or 12 V to 1 V. Similarly, the effect of an error in the duty cycle on the output voltage when the switching frequency (f_{SW}) is fixed and the conversion ratio is changed is shown on the upper side of Figure 1c. Here, $V_{OUT.error}$ is defined as the difference between the desired V_{OUT} and the V_{OUT} varied by the error. Furthermore, the lower part of Figure 1c illustrates the effect on the output voltage when the conversion ratio is fixed at 0.1 and f_{SW} is changed. In conclusion, it was confirmed that the error becomes larger when a PWM controller is used in a high step-down case with a small duty ratio (360 mV @ $V_{OUT}/V_{IN} = 0.33$). Moreover, when the conversion ratio is fixed at 0.1, it can be easily confirmed that the output voltage error of the PWM controller increases more significantly as f_{SW} increases (456 mV @ $f_{SW} = 3.8$ MHz). In other words, although the feedback mechanism can mitigate the error, PWM control exhibits a greater sensitivity to the same level of jitter compared with COT control.

Despite its advantages such as robustness in high step-down applications and fast dynamic response, conventional constant on-time (COT) control has several drawbacks compared with pulse width modulation (PWM) control, which will be discussed below.

2.2. Low ESR Unstability and Frequency Deviation Issues of Conventional Constant On-Time (COT) Control

As illustrated in Figure 2, conventional COT buck converters face several inherent limitations. Firstly, because the control loop uses a single comparator to compare the feedback voltage (V_{FB}) with the reference voltage (V_{REF}) without an error amplifier or a

ramp signal, a DC offset of $\Delta V_{FB}/2$ is introduced. This offset voltage between the average output voltage and the desired setpoint degrades regulation accuracy.

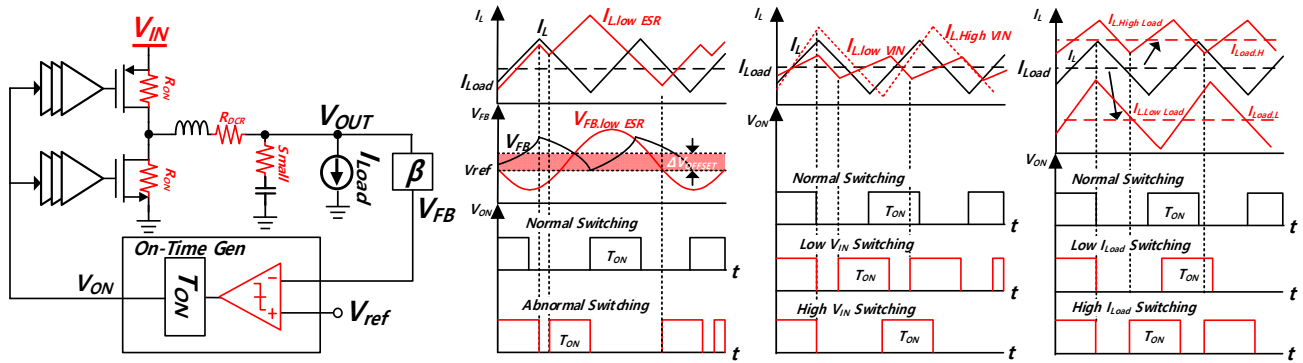


Figure 2. Limitations of conventional constant on-time control.

Additionally, since constant on-time (COT) control is fundamentally a ripple-based control method, if the ripple magnitude is too small, the comparator may not be able to accurately compare the feedback voltage with the threshold voltage. The output voltage ripple must be large in COT control to operate accurately, so it is impossible for a conventional COT controller that makes a decision with just one comparator to reduce the output voltage ripple. Also, a significant stability issue arises from the phase delay between the inductor current and the voltage across the output capacitor in COT controllers. This is particularly problematic when using low-ESR ceramic capacitors, where a phase delay of approximately 90° can cause the COT buck converter to suffer from sub-harmonic oscillation because of the comparator's wrong decision. To maintain stability, conventional COT control requires a specific ESR value that satisfies the condition in Equation (1) [10].

$$R_{ESR} \cdot C_{OUT} > T_{ON}/2 \quad (1)$$

$$f_{SW_ideal} = V_O/V_{IN} \cdot 1/T_{ON} \quad (2)$$

$$f_{SW_real} = \frac{V_{OUT} + I_L \cdot (R_{ONL} + R_{DCR})}{V_{IN} - I_L \cdot (R_{ONH} - R_{ONL})} \cdot \frac{1}{T_{ON}} \quad (3)$$

Another major drawback of conventional COT control is its significant frequency variation. In an ideal buck converter using COT control, the on-time (T_{ON}) is fixed, so the switching frequency (f_{SW}) is determined by Equation (1). Even in this ideal scenario, f_{SW} is highly dependent on the input voltage (V_{IN}) and output voltage (V_{OUT}). When considering more realistic scenarios that include the on-resistance of the switches and the DC resistance (DCR) of the inductor, the switching frequency is also strongly affected by the load current (e.g., $I_{Load,H}$ or $I_{Load,L}$), as shown in Equation (3). This can lead to unpredictable frequency fluctuations, creating a wide EMI spectrum that complicates filter design and compliance with industrial EMI regulations [14,23,25,28,49]. For example, consider a COT converter with an output voltage of 1.2 V and a fixed on-time (T_{ON}) of 150 ns. If the input voltage varies from 5 V to 48 V, the ideal switching frequency f_{sw_ideal} (2) changes significantly from 1.6 MHz to 167 kHz. Since modern point-of-load (POL) converters are required to cover a wide load range from several tens of milli-amperes to several amperes, it is also necessary to examine the switching frequency variation caused by load changes. Assuming series resistance of the inductor R_{DCR} , and that the on-resistance of the high-side switch (R_{ONH}) and the on-resistance of the low-side switch (R_{ONL}) are each 20 mΩ, let us consider the case where the load current varies from 100 mA to 5 A. In this case, with $V_{OUT} = 1.2$ V, $V_{IN} = 12$ V, and $T_{ON} = 150$ ns, the real switching frequency f_{sw_real} (3) can

further vary from 669 kHz to 778 kHz due to load fluctuations. Such drastic switching frequency variation, caused by multiple parameters, may complicate the design of the converter's EMI filter.

The unstable issue caused by low-ESR capacitors can be solved by adding a zero, which replaces the zero generated by the ESR, through ripple injection. The DC offset issue in the feedback voltage (V_{FB}) can be resolved by extracting and removing the DC offset. These methods will be explained in Section 3. Frequency variation can be suppressed by adjusting the on-time based on the input, output, and load currents, or by using a PLL (phase-locked loop). This will be explained in Section 4.

3. Ripple Injection and DC Offset Cancellation Techniques

3.1. Ripple Injection Techniques

Low-ESR ceramic capacitors are favoured for their small size and ability to achieve low output ripple, but they can pose a serious stability problem for COT control. Unlike conventional PWM control, COT inherently lacks an error amplifier and compensator. Consequently, in the absence of an ESR-induced zero, the LC resonant double pole can render the system unstable. More specifically, this issue, caused by a phase shift in the output capacitor, leads to sub-harmonic oscillation and unstable switching. To address this problem, it is essential to inject a ripple signal that is in phase with the inductor current into the feedback path. This allows for low output ripple while providing a phase lag-free ripple to the feedback signal (V_{FB}). As shown in Figure 3, ripple injection methods can be categorized into passive ripple compensation [10,15–18,20,22,30–32], active ripple compensation [14,19], and current estimation ripple compensation [8,21]. Passive ripple compensation uses an RC network to generate the ripple signal. Type 1 passive compensation directly uses the ESR of the output capacitor, while Type 2 adds a feed-forward capacitor (C_{FF}) to amplify high-frequency ripple by directly passing it to the feedback voltage (V_{FB}) to compensate for the phase shift [30]. Type 3 compensation, suitable for cases where the output ripple is less than 20–40 mV [10], involves connecting an RC network in parallel with the inductor to sense its current ripple and add it to the feedback signal [10,30–32]. Type 1 compensation is the simplest, but for stable operation, the ripple size due to the resistance must be greater than the capacitive ripple. Therefore, in a low step-down case at the same frequency, that is, when V_{IN} is low, the inductor current ripple is low, and the ripple due to ESR becomes small, which causes a decrease in stability. Instead of Type 1, Type 2 compensation can be used to enable the use of a capacitor with a low ESR. This has the advantage of significantly reducing the output voltage ripple and, in addition, can improve the transient response by coupling the output voltage ripple to the feedback node (V_{FB}). However, Type 2 can also have a stability problem when V_{IN} decreases. Additionally, since the zero that is generated is related to the value of the feedback network's resistor, there is a disadvantage in that stability changes according to the variation in the resistive dividing network. The Type 3 method, as shown in Figure 3a, solves the instability by injecting an inductor current ripple signal with a 90-degree leading phase to the output voltage's phase into the feedback node (V_{FB}). It is possible to use a low ESR, and it is easier to maintain stability compared with Type 2 because the location of the zero is not affected by the resistive dividing network. However, the design of the feedback network is more complex than the previous Type 1 and 2 methods, and for applications with a wide V_{IN} range, the size of the injected ripple becomes small when V_{IN} is small, so there is a stability dependence on the V_{IN} level, just like with the Type 1 and 2 compensation methods. Furthermore, if the size of the coupling capacitor C_{FF} is increased in Type 3 to increase the size of the injected ripple, the transient response performance may be degraded [31]. As types of passive methods, virtual inductor current

(VIC) or emulation inductor current (EIC) injection techniques exist [15,17,22,29]. These are also a form of passive ripple compensation that filters the switching node voltage with an RC network to inject a leading-phase signal into the feedback node. This approach requires an additional block to perform DC extraction to inject only the ripple component. Voltage ripple compensation (VRC) also uses VIC and an integrator to generate a virtual voltage ripple (VVOR) that is then superimposed in reverse with the actual ripple to cancel the phase delay [22]. These ripple injection methods using an RC network and a DC extractor, like the existing Type 2 and 3 methods that only use a passive RC, have the advantage of allowing the use of a low-ESR capacitor. Furthermore, they have the advantage of using fewer passive components compared with Type 3. However, the simple VIC technique has the disadvantage of a slow transient response speed because the gain of inductor current AC ripple should be bigger than the output voltage ripple. To address this transient response limitation, ref. [22] introduced the VVOR technique, which enhances the transient response by adding the output AC ripple to the inductor AC ripple component. Active ripple compensation (ARC) methods directly sense the current of the power transistors to extract AC information and enhance the feedback ripple. ARC techniques have the advantage of sensing ripple with a smaller footprint compared with passive methods [14,19]. ARC techniques have the advantage of reducing silicon area because it does not use a large RC network for sensing. However, the complexity of the current sensor and its correction circuit can increase the difficulty of the design. The current estimation ripple compensation methods are a technique that extracts the inductor current ripple from the output voltage and injects it into the feedback node [21,50]. The Quadratic Differential and Integration (QDI) technique uses a second-order differentiation and integration of the output voltage ripple to derive a precise current sensing signal that is independent of ESR [50]. To implement ripple injection, digital control can be used, but it requires a high-speed external clock and an ADC [35]. These ripple estimation techniques, like active sensing techniques, have the advantage of reducing silicon area because they do not use passive devices. However, they may rely on the precision of internal passive components to increase control performance, and a complex computing unit must be added. Although various techniques for ripple injection have been studied, commercial products usually use Type 1, 2, or 3 passive compensation techniques for stability [51–54].

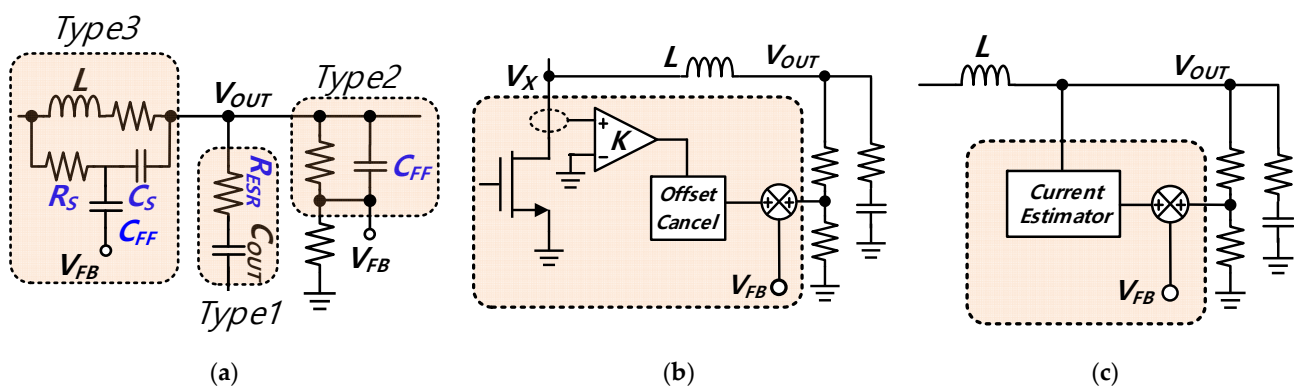


Figure 3. Passive ripple injection techniques. (a) Passive ripple compensation. (b) Active ripple compensation. (c) Current estimation compensation.

3.2. Offset Cancellation Techniques

Along with ripple injection techniques, many studies are also focused on effectively eliminating the inherent DC offset of conventional COT control [15–22]. Most research applies offset cancellation techniques in conjunction with ripple injection. As presented in Figure 4a, the conventional COT controller generates on-time (T_{ON}) by directly comparing

the voltage at the feedback node with the reference voltage (V_{REF}) voltage. The feedback voltage (V_{FB}) (assuming Type 1 compensation) takes on a triangular waveform, and after the off-time, a new on-time begins the moment the valley point of the triangular wave meets V_{REF} . As such, because the conventional COT controller operates by sensing the valley point, a DC offset of $1/2$ of V_{OUT} 's ripple is inevitable. As shown in Figure 4b, offset calibration methods in COT control extract the DC component from the feedback signal and either subtract it or add it to the reference voltage to eliminate the inherent offset of the COT circuit [14,15,17,20]. Since most of them use similar techniques, the operating principles and pros and cons of several papers are presented below.

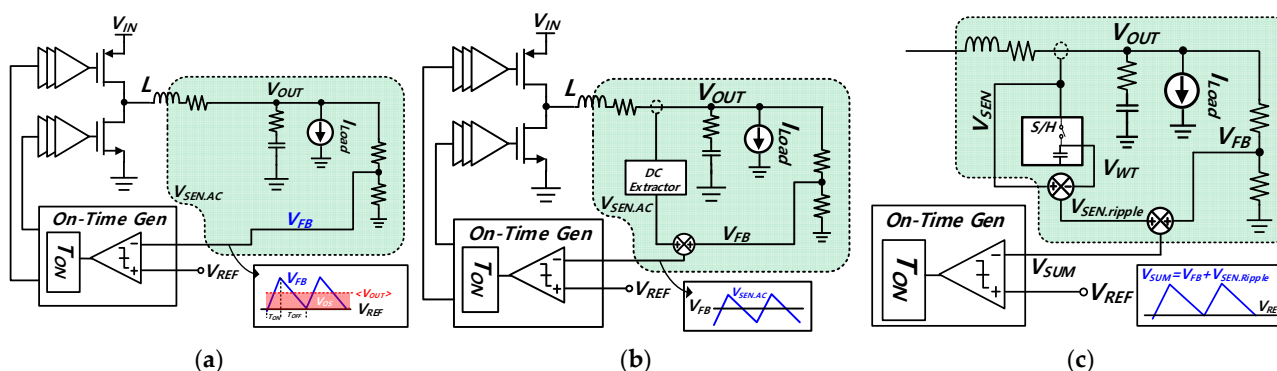


Figure 4. (a) Offset in the conventional COT control. (b) Basic concept of offset cancellation technique in COT control. (c) Pseudowave tracking (PWT) technique [18].

One method used alongside the virtual inductor current (VIC) technique involves low-pass filtering the output voltage to obtain its DC value and then feeding the difference between this value and the reference to a new reference voltage to cancel the offset [15]. However, as mentioned earlier, the VIC method has the disadvantage of a slow transient response. The pseudowave tracking (PWT) technique, which solved the transient response drawback, is presented in Figure 4c [18]. The PWT method points out that in conventional designs, the summing node voltage (V_{SUM}) is composed of V_{SEN} and V_{FB} , and V_{SEN} can have its DC level shifted by load changes, which degrades load regulation. It also notes that even when a DC extraction block is used to add only the AC current voltage to the feedback, an offset of $1/2 V_{SEN}$ can still occur. PWT introduces a new voltage, V_{WT} , which senses current information relative to DC 0 V instead of V_{REF} . This allows for an ideal V_{FB} with a 0 V offset. In addition, unlike the existing VIC method, the PWT method improves the transient response by rapidly extending the duty cycle up to 100% when the controller detects the minimum off-time twice during a transient situation. Although there has been much progress, it could not solve the stability issue caused by the decrease in ripple size injected in low conversion ratio situations where the input voltage is low. However, it can be easily solved by controlling the inductor current sensing resistor value along with input voltage variation. A digital implementation of offset cancellation has also been proposed [21], where the output voltage is sensed using an ADC, the inductor current is estimated, and valley detection is used to perform offset cancellation, all in a digital domain. However, a digital implementation may require a high-speed external clock to sense instantaneous changes in the output.

4. Frequency Stabilization Techniques

As can be seen from Equations (1) and (2), the rapid frequency fluctuation of COT controllers is influenced not only by changes in the input voltage (V_{IN}) and output voltage (V_{OUT}) but also by changes in the load. This frequency variation makes it difficult to

design EMI filters for the system and can potentially cause noise on high-speed data paths, leading to signal distortion. Therefore, a technique for stabilizing the frequency despite changes in V_{IN} and V_{OUT} is needed. However, since COT control is a PFM (Pulse frequency modulation) technique that maintains the output voltage by fixing the on-time and varying the switching frequency, fixing both the on-time and the switching frequency would cause a regulation error. Thus, frequency stabilization techniques have evolved to allow some variation in on-time to stabilize frequency fluctuations while maintaining output voltage regulation. This approach is called adaptive on-time (AOT) control. It can be broadly divided into AOT techniques that do not use a phase-locked loop (PLL) [12,16,25–27,55] and AOT techniques that use a PLL [13,23,24,56]. We will first explain the basic operating principles of AOT.

4.1. Principle of Adaptive On-Time Control

The adaptive on-time (AOT) technique dynamically adjusts the on-time to maintain a pseudo-constant switching frequency in Continuous Conduction Mode (CCM). By rearranging Equation (2), the on-time (T_{ON}) can be calculated as in Equation (4).

$$T_{ON} = \frac{V_O}{V_{IN}} \cdot \frac{1}{f_{SW,ideal}} \quad (4)$$

Therefore, if the on-time is set to be proportional to $K \cdot V_{OUT} / V_{IN}$ (where K is a constant), the switching frequency will ideally be constant, suppressing fluctuations caused by changes in V_{IN} and V_{OUT} .

Figure 5a shows a conventional adaptive on-time (AOT) generator circuit [23]. During the on-time, a current proportional to the input voltage ($K_1 \cdot V_{IN}$) is injected into the C_{TON} capacitor to form a ramp signal. When this ramp signal reaches a threshold value proportional to the output voltage ($K_2 \cdot V_{OUT}$), the high-side switch is turned off. This operation results in a T_{ON} that follows Equation (5).

$$T_{ON} = \frac{K_1 \cdot V_O \cdot C_{TON}}{K_2 \cdot V_{IN}} = K \cdot C_{TON} \cdot \frac{V_O}{V_{IN}} \quad (5)$$

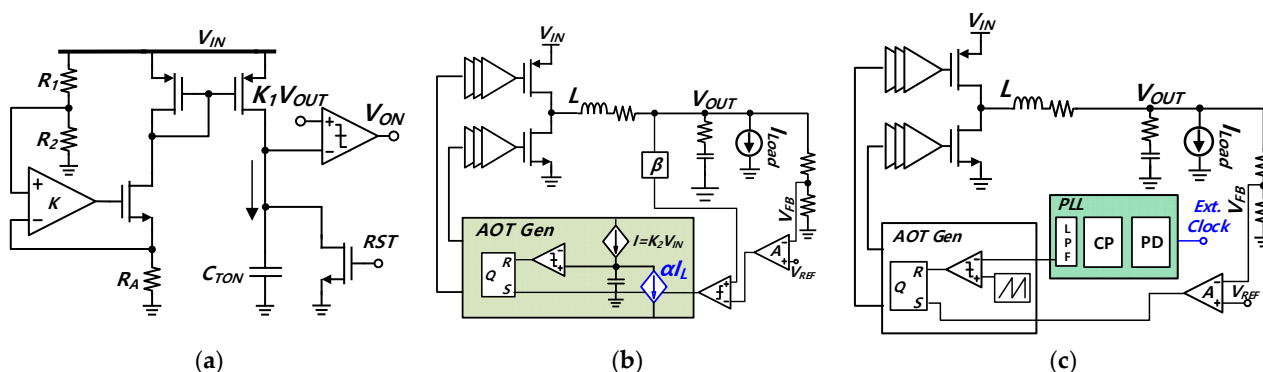


Figure 5. (a) Conventional AOT generator. (b) Load-dependent AOT techniques [3]. (c) PLL-based AOT [23].

By combining Equations (4) and (5), a fixed switching frequency can be obtained as shown in Equation (6).

$$f_{SW,ideal} = \frac{1}{K \cdot C_{TON}} \quad (6)$$

However, this value does not account for realistic factors like the resistance of the power switch, the inductor's DCR, and parasitic resistances in the circuit. Therefore, the

parasitic resistances are considered in advanced adaptive on-time (AOT) systems. AOT also adds an error amplifier to eliminate the output offset, thereby achieving a stable switching frequency and an output voltage without a DC offset [16].

4.2. Adaptive On-Time Techniques

Non-PLL AOT techniques [16,25–28] are primarily based on mathematical stabilization methods. For instance, ref. [16] addresses the influence of load current on the switching frequency, as mentioned in Equation (7), by adding a Load Current Correction (LCC) block inside the on-time generator.

$$f_{SW} = \frac{1}{K \cdot C_{TON}} \cdot \frac{V_O \cdot I_{Load} \cdot (R_{DCR} + R_{ON})}{V_O} \quad (7)$$

As shown in Figure 5b, the LCC technique uses a sensed inductor current to generate a new current proportional to the load current. This new current is used to adjust the slope of the ramp signal inside the on-time generator, allowing the generated on-time to increase in proportion to the load current. This compensates for frequency fluctuations caused by load changes [16,26,27].

The Predicting Correction Technique (PCT) [25] differs from LCC by adjusting the $K_1 \cdot V_{OUT}$ term of the on-time generator's ramp signal, rather than the ramp's slope, to control the on-time. To implement PCT, a power stage Equivalent Output Voltage Synthesizer (EOVS) is included, which emulates the power stage to create an equivalent output voltage proportional to the duty cycle. When the load current increases, the duty cycle rises due to losses from parasitic resistances (R_{ON} , R_{DCR}), causing the equivalent output voltage ($V_{OUT.eq}$) generated by the EOVS to increase. Conversely, when the load current decreases, $V_{OUT.eq}$ decreases. This method provides a load-compensated on-time, which can suppress switching frequency variation to as little as 0.32%. However, this complex circuitry can increase power consumption, and the bandwidth limitations of the T_{ON} adjustment circuit can cause overshoot and undershoot during transient events. Another approach in [28] is similar to LCC in that it uses a current sensor to sense the load current and suppress frequency fluctuations. However, it differs by adjusting the reference voltage (V_{REF}) in proportion to the sensed load current.

The most widely used methods for fixing the switching frequency are phase-locked loop (PLL) and frequency-locked loop (FLL). In COT and AOT control, PLL/FLL techniques are used to lock the frequency to a fixed external clock or internal clock generator [11,23,24,35] as shown in Figure 5c. However, if the PLL/FLL gain is too high, the frequency can be forcefully locked to the external clock, causing regulation errors in COT control. Therefore, when applying a PLL to COT, the loop gain must be designed to be low, and AOT must be used to allow for duty cycle variation [36]. This approach can achieve a minimum frequency variation of 0.05% with load current changes and provides good transient performance by allowing the circuit to operate at high speeds only during dynamic events. Ref. [24] proposes a fixed off-time controller, similar to COT, for low step-down situations (not just low on-duty cycles). It uses a PLL on the off-time generator to reduce frequency variation and adds a frequency dithering technique to mitigate EMI issues. Compared with non-PLL methods, PLL techniques offer the advantage of more precise frequency locking. However, forcefully locking the switching frequency of a PFM-based COT controller with a PLL can limit its transient performance and lead to additional power consumption.

5. Research Challenges of Constant On-Time (COT) Control in Integrated Circuits

The ripple injection, offset cancellation, and frequency stabilization techniques mentioned in Sections 3 and 4 have a high degree of maturity as control methods. However, technologies and techniques to further improve and optimize the transient performance using COT control, as well as the control of multiphase buck converters using COT techniques, are still areas for academic development due to their high difficulty.

5.1. Load Transient Enhancement and Optimization Techniques

Buck converters using COT control exhibit an excellent dynamic performance due to their event-driven switching characteristics. For example, during a load step-up (heavy load to light load) event, the COT controller generates a series of on-time pulses to rapidly increase the inductor current. Conversely, during a load step-down (light load to heavy load) event, it extends the off-time to quickly decrease the inductor current. While COT control fundamentally has a fast transient response, its fixed on-time can prevent it from immediately supplying or cutting off the necessary energy during abrupt load changes. This can lead to a slow recovery time (T_R) beyond the ideal scenario and a large drop in the output voltage (V_{OUT}), as presented in the right side of Figure 6. The transient response of a buck converter is limited by the inductor's size and can be improved by extending the on-time during transient conditions.

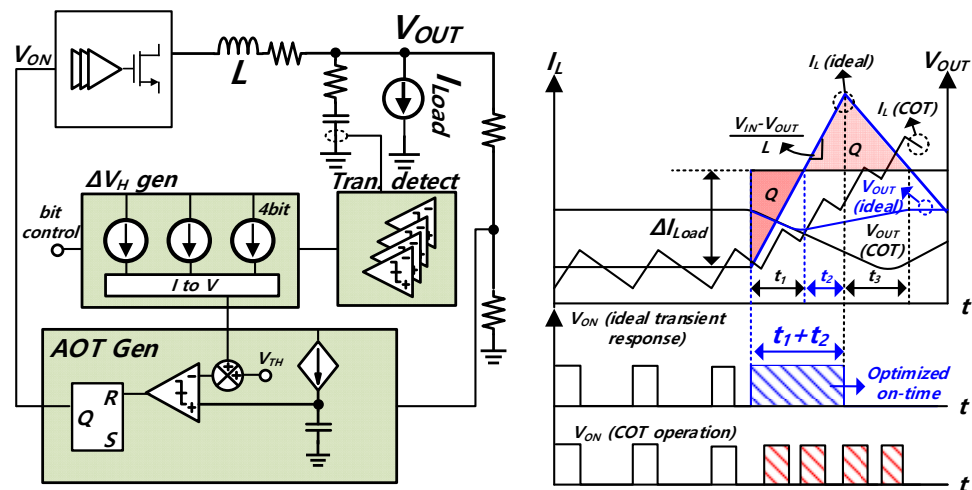


Figure 6. Block diagram of analogue time-optimized control (OTC) [57] and transient response limitation of conventional constant on-time control under light to heavy load step.

The pseudowave tracking (PWT) technique [18] uses a sample-and-hold voltage (V_{WT}) from the valley point and compares it with a ripple sensing value to achieve a precise, offset-free output voltage. However, the sample-and-hold delay can limit the transient response. To overcome this, ref. [18] forces the V_{WT} value to follow a real-time waveform-tracking voltage during transitions, which instantly increases the on-time. With a transient sensing block, this method achieved a recovery time (T_R) of 4 μ s and an undershoot voltage of 75 mV for a load change from 0.3 A to 1.7 A. Similarly, other studies [11,16,23] have adopted methods that instantly increase the on-time during a transition by changing the ramp value or the boundary of the on-time generator.

$$t_1 = \frac{L}{V_{IN} - V_O} \cdot \Delta I_{LOAD} \quad (8)$$

$$t_2 = \left(\sqrt{\frac{V_O}{V_{IN}}} \right) \cdot t_1 = \left(\frac{L_O}{V_{IN} - V_O} \right) \cdot \left(\sqrt{\frac{V_O}{V_{IN}}} \right) \cdot \Delta I_{LOAD} \quad (9)$$

Beyond the transient enhancement technique, the transient optimization technique has been studied [38,39,50,57,58]. Mathematical calculations for load transient situations were conducted in [38,50] with the aim of achieving the ideal settling time. The theoretical length of extended on-time is given in (8) + (9), as illustrated on the right side of Figure 6 under a light to heavy load step (and vice versa operation for a heavy to light load step). The challenges of the transient optimization technique are how to create the optimized on-time during a transient situation and how to sense the transient response. Although this paper was not performed at the IC level and the method for sensing transient situations is somewhat idealistic, it provides a background for accurate analysis. Against this background, the transient optimization technique in PWM-based control was introduced in [39,50]. The author proposes a method to achieve an ideal response by adding an additional square root calculation of optimization time to the on-duty through capacitive charging and discharging. Additionally, a capacitive current sensor (CCS) was introduced for immediate transient situation sensing, which significantly reduces the delay caused by transient sensor operation. However, a method to change the accuracy of the capacitive current sensor according to the load step may be additionally needed. This method can be applied to constant on-time (COT)-based control.

As shown in Figure 6, the ideal recovery time is achieved by allowing a calculated amount of inductor current overshoot, which provides the necessary residual charge while accounting for the slewing limited by the inductor [57]. Compared with conventional COT, the adaptive on-time (AOT) technique provides the flexibility to adaptively adjust the on-time during transient periods, offering an improved transient response. An analogue time-optimized on-time control (OTC) method was proposed to optimize the transient response by extending the on-duty cycle during a transient event [57]. The OTC circuit consists of a threshold detector, a ΔV_H generator composed of a current DAC, and an on-time generator. During a transient event, the threshold detector senses the change in the capacitor current and activates the ΔV_H generator. The current DAC's components are then adjusted to control the reference voltage of the on-time generator's internal comparator, thereby extending the length of the on-time pulse (T_{ON}) as a function of the square root of the conversion ratio. This method fine-tunes the I_{DAC} value based on a calculated figure to achieve an optimized transient response. For example, it has been shown to achieve a low undershoot of 20 mV and a fast recovery time of 3 μ s during an 840 mA (heavy to light) load step. However, variations in the current source due to process, voltage, and temperature (PVT) changes or fluctuations in the supply voltage (V_{DD}) can occur, which may reduce the accuracy of this method. Studies also suggest using digital control techniques to enhance transient response [34–36]. Specifically, a digital transient-optimized control (DTC) method to optimize transient performance was introduced in [36]. While digital controllers require a high-speed external clock and ADCs, which increases complexity, their transient response can be slow due to sampling speed and ADC delay. To overcome this, DTC adds an analogue transient detection circuit that operates without an ADC. It also uses a pre-calculated look-up table (LUT) to reduce the recovery time from 9 μ s to 3 μ s. However, this approach requires memory for the LUT and may have limited flexibility for various operating conditions.

Existing constant on-time (COT) control, while exhibiting a sufficiently fast dynamic performance, fails to achieve an ideal transient performance due to repetitive switching during transient events. Instead of multiple switching during dynamic situations, extending the on-time to its ideal duration during a transient event can not only prevent output voltage droop but also significantly reduce the settling time. However, this approach

faces two key limitations: the requirement to implement a complex square root function and the necessity for an ideal response time from the transient sensing circuit, which is practically unattainable. Consequently, based on established theoretical equations, there is a need to develop a simple square root extended on-time function that accurately accounts for the transient sensing delay. Simultaneously, research into methods to improve the precision of this function is also essential. Furthermore, this method can be broadened to multiphase converters.

5.2. Multiphase Techniques

COT controllers, due to their fast transient response and noise-immune on-time, are used as controllers for point-of-load (POL) converters that supply power to high-performance processors. Modern high-performance processors are low-voltage and have a high-current consumption load, which is typically supplied by multiphase buck converters. In multiphase converters, issues related to phase-shedding, current balancing, or phase synchronization commonly arise. The phase-shedding technique improves the overall converter efficiency by adaptively adjusting the number of active channels according to the load current. Current balancing refers to the technique of equalizing the current flowing through each channel, which is commonly achieved using PLL/DLL methods. Of these, current balancing (or phase synchronization) across phases represents a more critical challenge [1,33,34,37,39–48] in a multiphase buck converter with COT control, since COT inherently lacks a reference clock. The factors that induce current imbalance include duty cycle mismatch and the inconsistency of various parasitic components in the power path. For example, a mismatch in R_{ON} resistance, an inductor DCR, a PCB trace and on-chip wiring resistance, and package parasitic components can all cause current imbalance. Among these, duty cycle mismatch between channels is a major contributor to current imbalance. In particular, the duty cycle mismatch between channels causes a 20 times larger mismatch in the inductor current. That is, a slight duty cycle mismatch of just 1% can cause a 20% inductor current imbalance [39]. Inductor current imbalance concentrates excessive current on a specific phase, which significantly increases the conduction loss of that phase, thereby reducing the system's efficiency. In addition, this overcurrent concentration phenomenon causes local hot spots in the corresponding phase, shortening the lifespan of the device and reducing the reliability of the system. In hysteretic control multiphase converters, PLL/DLL techniques and pulse distribution methods are employed to address the current imbalance problem (shown in Figure 7).

A current balancing in a multiphase converter can be achieved by sensing the error current using a current sensor, but in this case, it is greatly affected by the precision of the current sensor. Usually, to solve the current mismatch of each channel, a phase-locked loop (PLL) or delay-locked loop (DLL) technique is used [41–43]. For example, a four-phase multiphase hysteretic converter was proposed in [41]. The authors in [41] proposed precise control that reduces jitter to 6.33 ps using the DLL technique, but it requires a complex controller for the DLL, which increases the circuit complexity, and the quiescent current increases due to the additional bias circuit needed to drive the charge pump. A method which synchronizes the on-time by configuring a PLL for each channel using an external fixed clock was proposed in [42]. However, since a PLL block is added to each channel, the area increases and the quiescent current may increase, and there is the limitation that an external clock is used. A master–slave structure in a four-phase hysteretic buck converter was proposed in [43]. Through the proposed master–slave architecture with the DLL technique, a precise current sharing error of $\pm 3.6\%$ was achieved. However, the DLL used in this paper synchronizes with an external clock reference, which can limit the overall loop speed. In multiphase control, using PLL or DLL techniques allows for precise control,

but there is a limitation that the complexity of the control circuit increases, which can increase the power consumption used by the controller, and the transient performance can be limited by the speed of the locking loop. Furthermore, the biggest advantages of constant on-time (COT)/adaptive on-time (AOT) control circuits are a low complexity and a fast transient response. While PLL/DLL methods allow for precise control, they can diminish the advantages of COT/AOT control if they do not overcome the issues of circuit complexity and the speed limitations of the locking loop. Therefore, in multiphase converters with hysteretic control like COT/AOT, a method of correcting mismatch based on the pulse distribution (PD) method has been proposed [1,33,34,37,40,45–48]. The PD method uses a counter to distribute the same length of on-time to multi-channels.

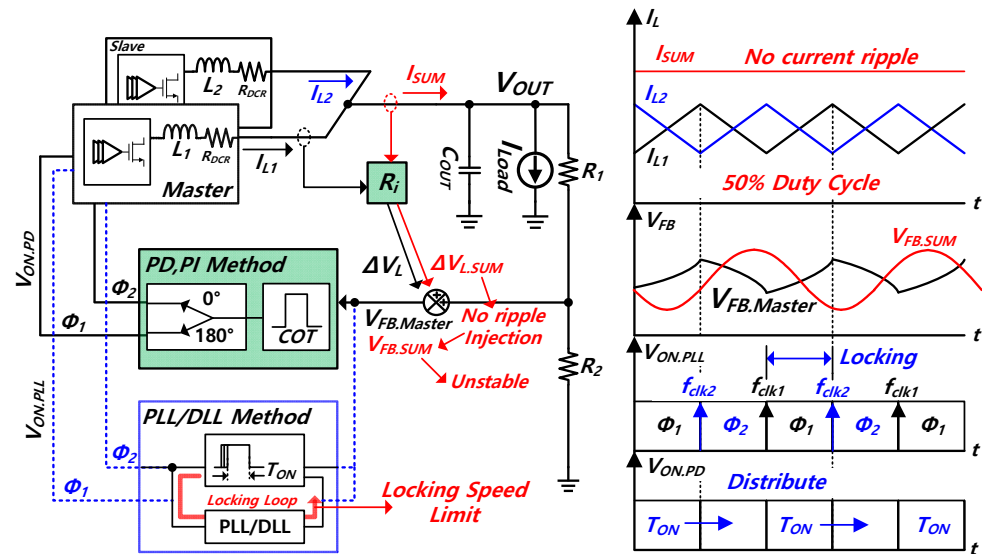


Figure 7. Issues of multiphase buck converter with COT control.

A COT or AOT technique senses the inductor current ripple and compensates the overall system. When applied to a multiphase converter employing the PD method, however, a problem can arise in which the ripple injection becomes zero in a low-ripple duty cycle region. For example, in a dual-phase buck converter, as presented in Figure 7, the current ripple ideally becomes zero at a 50% duty cycle point. In this case, assuming each channel is configured with a Type 3 compensation method, the magnitude of the sum of injected ripple (V_{FB_SUM}) becomes zero, which can make the entire control circuit unstable (Figure 7) and be greatly affected by jitter. An adaptive quasi-constant on-time current mode (AQCOTCM) method was proposed in [44] to improve transient performance. An architecture that extends the AQCOTCM to being multiphase was also presented in [44]. However, the proposed architecture employs a PD method that generates the on-time (T_{ON}) by injecting a summed current ripple and subsequently distributing it. This approach can lead to instability in duty cycle regions where the current ripple is small. A similar issue is reported in [34]. A current-mode digital AOT controller was presented in [34] with a single comparator for voltage matching between sub-converters. The digitally generated ripple of each phase is injected into the single comparator sequentially. After each comparison, an injection code (INJ_CODE) is increased by $\Delta V_{INJ,PH}$, which is determined by the phase shift time and injection gain. The injected voltage sequentially estimates each inductor current, and when the injection target arrives at a predetermined phase shift time, the phases are automatically synchronized. However, the inductor current digital emulation technique in this paper does not provide a solution for the duty region where the ripple becomes small, and there is the limitation that an external high-speed clock is required. A

two-phase AOT control method was adopted in [1] to achieve a fast transient response of 10 A/ μ s for a DDR5 DIMM. This paper maintains a constant switching frequency using the AOT method. Although the author does not address current balancing, it uses a phase detector to utilize two synchronized main ramp signals and two replicas for the dual-phase operation. However, there is no proposed solution for ripple reduction issue during dual-phase operation in [1]. Current balancing was achieved by sensing the inductor current of each phase and averaging them in [3]. This average value is set as the current reference for setting the on-time of each phase. Because the ripple generated in each channel is sensed, the effect of a low ripple problem can be prevented. However, as the number of channels increases, the required sensing blocks also increase, resulting in a larger area. To address this issue, a phase interpolator (PI) technique without PLL was proposed in [37]. The PI determines the on-time of the second phase converter using the T_{ON} timing of phase 1. In addition, it employs a threshold derived from the input voltage (V_{IN}) through an R-string DAC. This allows phase 2 to be synchronized with and shift according to phase 1, which can significantly improve dynamic performance. This paper, similar to [45], adopts a master–slave structure. As illustrated in Figure 7, ripple is injected only through the master channel (V_{FB_Master}), while the slave channels employ a phase interpolator using a replica ramp. This enables proper ripple injection and prevents stability issues even in duty cycles with low output ripple. In addition, the chip area can be reduced by minimizing the number of current sensing blocks. However, when V_{IN} is small, there is a limitation that the accuracy of the replica ramp may be limited by the precision of the R-string DAC used for phase interpolation.

In summary, a formalized control technique has not been established in multiphase COT/AOT control methods. PLL/DLL techniques can be employed to achieve a high accuracy, while PD techniques can be utilized to reduce complexity and enable fast control. Configuring the inter-channel control in a leader and follower manner not only prevents the instability in the low-ripple duty cycle region but also significantly reduces the control complexity. In the future, by continuing to leverage PD for the advantages of hysteretic control, both precision and control speed are expected to be further improved through the adoption of low-complexity, high-speed locking techniques.

6. Conclusions

This paper comprehensively reviews the advancements in constant on-time (COT) buck converters. Table 1 is a performance comparison table on constant on-time (COT) buck converter studies. COT control is utilized as a power management integrated circuit for high-speed processors due to its simple structure and fast response speed. However, it faces challenges such as instability caused by low ripple, DC output voltage offset issues, and EMI problems due to switching frequency variations. Various studies have been conducted to address these issues. Diverse ripple injection methods have been studied to resolve instability problems arising from low-output voltage ripple, along with techniques to extract DC from the injected ripple to eliminate offset. Digital control is sometimes employed for inductor current sensing for ripple injection, but it typically requires a high-speed external clock. EMI problems are being addressed through frequency stabilization methods, notably adaptive on-time (AOT) methods, and sometimes by incorporating PLL/FLL.

Table 1. Performance summary of integrated constant on-time control buck converters.

	Unit	[5]	[8]	[12]	[13]	[14]	[16]	[18]	[19]	[20]
Tech.	μm	0.18	0.35	0.18	0.13	0.5	0.35	0.028	0.13	0.18
V_{IN}	V	1.8	3.3	2.1–5.5	4–19	4.5–30	3.3–4.2	2.6–3.63	7–15	5–12
V_{OUT}	V	0.9–1.2	2	1.8	0.25–2.5	1	1.2	1.05	5–7	1.05–3.3
L	μH	0.24	4.7	2.2	0.15	2.2	4.7	1	2.2	1.5
C_{OUT}	μF	16	4.7	10	470	88	8.9	4.7	N/A	22
f_{SW}	MHz	3	0.8	N/A	0.8	0.4	0.75	2.5	2	0.7
I_{Load}	A	3	0.5	0.3	40	1.2–4	0.745	0.3–1.7	0–2	1–5
Peak Eff.	%	95.58	93	90.04	92	95	86.6	94	95.56	92
Settling time	μs	2	10	N/A	40	28	3.6	4	3	15.4
$V_{US/OS}$	mV	80	50	50	28/18	24	75	90/75	72/85	30/58
$\Delta f_{SW}/f_{SW}$	%	N/A	N/A	N/A	±0.16	N/A	N/A	N/A	N/A	N/A
Area	mm ²	1.41	2.89	1.1	N/A	N/A	1.9	N/A	3	3.01
Multiphase	-	2Φ, PD	X	X	X	X	X	X	X	X
	Unit	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[34]	
Tech.	μm	0.18	0.13	0.35	0.13	0.028	0.18	0.35	0.028	
V_{IN}	V	12	19	3–3.7	1.8	3.3	2.7–3.6	40	4.2	
V_{OUT}	V	1	5.1	1.2–1.8	0.5–1.7	1.05	1–1.2	5	0.6–1.0	
L	μH	2.2	1.5	4.7	0.47	1	N/A	0.47	0.015	
C_{OUT}	μF	66	22 × 4	10	22	4.7	N/A	22	3.2	
f_{SW}	MHz	0.5	0.57	1	<1	2.5	1	10	75	
I_{Load}	A	0–5	0–8	0.7	0.5	0.3–1.7	1.1	0–2	1.2	
Peak Eff.	%	N/A	94	90	97.6	89	88.2	90.5	89	
Settling time	μs	10	40	0.96	0.4	10	10	0.48	0.08	
$V^*_{US/OS}$	mV	80/100	120/180	N/A	66/92	95/400	76	9/12	80	
$\Delta f_{SW}/f_{SW}$	%	N/A	N/A	N/A	N/A	0.32	5.2	N/A	N/A	
Area	mm ²	1.2	N/A	1.971	1.955	2.4	1.1	5.75	0.39	
Multiphase	-	X	X	X	X	X	X	X	4Φ, PD	
	Unit	[36]	[57]	[56]	[41]	[43]	[47]	[48]	[50]	
Tech.	μm	N/A	0.18	0.065	0.5	0.18	0.13	0.18	0.13	
V_{IN}	V	2.7–4.2	3.3	2.7–4.5	4.8	2–3.3	1.35–1.65	3.3	4.25–15	
V_{OUT}	V	1.2	0.6–1.2	0.6–1.3	3.3	0.8–1.6	0.75–1	0.7–3.0	0.8–1.43	
L	μH	4.7	1	0.47	0.11–0.22	0.33	0.005	0.22	0.68	
C_{OUT}	μF	4.7	4.7	10	0.008–0.19	10	0.22	0.62	47 × 3	
f_{SW}	MHz	1	1.5	2.5	~30	3~9.5	100	30	0.5–1.25	
I_{Load}	A	0.1–0.5	1.25	1.6	1	6	8	2.5	10	
Peak Eff.	%	81.6	90.2	86	83	93	88	88.1	92.5	
Settling time	μs	2.5	3	13.7	N/A	6	0.15	0.0225	60	
$V^*_{US/OS}$	mV	50/68	10/20	113/91	0.4/0.35	X	0.25/0.25	0.06/0.14	40	
$\Delta f_{SW}/f_{SW}$	%	2.8	N/A	0.13	N/A	±1.5	N/A	N/A	N/A	
Area	mm ²	N/A	1.423	13.3	3.3	12.5	N/A	1.93	6.5	
Multiphase	-	X	X	X	4Φ, DLL	4Φ, DLL	4Φ, PD	4Φ, DLL	2Φ, PD	

$V^*_{US/OS}$: undershoot voltage, overshoot voltage.

While constant on-time (COT) controllers are well known for their fast dynamic response, their inherent switching action during transient events prevents them from achieving an ideal performance without modification. To achieve an enhanced transient performance, many studies instantly increase the on-time during dynamic situations. A fast transient event detection circuit and a square root function have been developed to achieve an ideal transient response, based on theoretical equations. However, in practice, it

is necessary to develop a circuit that reduces complexity. Furthermore, a circuit that reflects the delay of the transient detection circuit also needs to be developed.

In virtue of their fast dynamic performance, COT buck converters are being utilized as PMICs for processors and memory that require large currents on the order of 10 A. In such cases, converters are configured in a multiphase arrangement to supply a high current, necessitating current balancing to eliminate local hot spots generated by duty cycle errors. To achieve precise current balancing, utilizing a phase-locked loop (PLL) or a delay-locked loop (DLL) can be effective. However, these methods suffer from significant drawbacks, including a limited circuit response speed due to the loop's locking time and a substantial increase in circuit complexity. Due to these limitations, conventional hysteretic converters often employ a pulse distribution (PD) method, though it is known to have issues with precision. Furthermore, a specific challenge in applying constant on-time (COT) control to a multiphase buck converter is the inherent instability that occurs at duty cycles where both the inductor current and output voltage ripple are at their minimum. To address these issues, a leader–follower architecture has been proposed. This structure offers a compelling solution by significantly reducing the number of required controllers and current sensors. By sensing the current of only the leader channel, this architecture is capable of mitigating the instability that arises at low-ripple duty cycle points. Consequently, there is a need to develop a new control technique that can leverage the benefits of the leader–follower architecture while simultaneously enhancing the precision of the conventional pulse distribution (PD) method.

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