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High-Efficiency Partial-Power Converter with Dual-Loop PI-Sliding Mode Control for PV Systems

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Abstract

This paper presents a novel partial-power DC-DC converter architecture specifically designed for Photovoltaic (PV) energy systems. Unlike traditional full-power converters, the proposed topology processes only a fraction of the total power, resulting in improved overall efficiency, reduced component stress, and lower system cost. The converter is integrated into a PV-based energy system and regulated by a dual-loop control strategy consisting of a Proportional-Integral (PI) voltage controller and an inner Sliding-Mode Controller (SMC) for current regulation. This control scheme ensures robust tracking performance under dynamic variations in irradiance, load, and reference voltage. The paper provides a comprehensive mathematical model and control formulation, emphasizing the robustness and fast transient response offered by SMC. Simulation results obtained in *MATLAB-Simulink*, along with real-time implementation on the *OPAL-RT hardware-in-the-loop* (*HIL*) platform, confirm the effectiveness of the proposed design. The system achieves stable voltage regulation with low ripple and accurate current tracking. Compared to conventional boost configurations, the proposed converter demonstrates superior performance, particularly under moderate voltage conversion conditions. The system achieves high efficiency levels, validated through both analytical estimation and *real-time hardware-in-the-loop* (*HIL*) implementation. Its high efficiency, scalability, and real-time control feasibility make it a promising solution for next-generation PV systems, battery interfacing, and DC-microgrid applications.

Keywords: partial-power converter; photovoltaic power system; dual *PI-sliding mode control*; *maximum power point tracking* (*MPPT*); output voltage ripple; *hardware-in-the-loop* (HIL)

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1. Introduction

The increasing deployment of residential and distributed Photovoltaic (PV) systems has intensified the need for high-efficiency and cost-effective power conversion architectures. These systems operate under variable environmental and load conditions, which introduce nonlinearities into the electrical behavior of PV modules and necessitate real-time adaptation of the operating point to track the maximum power point [1,2]. This critical function is typically handled at the DC-DC conversion stage, where both energy transfer and regulation tasks converge.

DC-DC converters represent a fundamental component in PV energy systems, as they interface directly with the source and execute Maximum Power Point Tracking (MPPT) algorithms. A variety of topologies have been investigated for this purpose, including

boost, buck-boost, interleaved, and coupled-inductor configurations, each offering distinct advantages in terms of voltage gain, component stress, and conversion efficiency. In addition to tsopology, the control strategy employed plays a decisive role in ensuring system robustness and dynamic response. In recent years, Sliding Mode Control (SMC) techniques have gained prominence due to their robustness to parameter uncertainties and external disturbances, offering fast convergence and accurate current tracking in power converters [3,4].

Beyond traditional full-power designs, recent research has explored the use of Partial-Power Processing (PPP) architectures, in which only a fraction of the total load power is processed by the converter. These topologies, such as the Input-Parallel Output-Series (IPOS) configuration analyzed in this paper, enable significant reductions in converter size, thermal stress, and power losses, thereby increasing global system efficiency. PPP converters are especially promising for PV systems, where the voltage and current profiles allow for effective partial processing without compromising control performance. This work presents a novel non-isolated buck-boost-based PPP architecture with dual-loop PI–SMC control, designed to enhance efficiency and stability under variable operating conditions and validated through both simulation and Hardware-in-the-Loop (HIL) implementation.

In recent years, *Sliding Mode Control* (*SMC*) has emerged as a powerful alternative to classical control techniques—such as *PI* or *PID*—for DC-DC power converters due to its robustness against model uncertainties, parameter variations, and external disturbances [5]. Unlike linear controllers, which often struggle under nonlinear or time-varying dynamics, SMC ensures finite-time convergence and high disturbance rejection, making it particularly suited for photovoltaic systems operating under rapidly changing environmental conditions. Various advanced SMC strategies have been explored to improve system performance: non-singular terminal SMC with extended state observers for uncertainty compensation and chattering reduction [6]; adaptive SMC schemes tuned via metaheuristic optimization for enhanced dynamic response [7]; and hyperbolic tangent sliding functions to smooth control actions and reduce switching noise [8]. Other works focus on digital implementations using FPGA for real-time control [9] or discrete-time formulations with disturbance estimators to tackle mismatched uncertainties [10]. The integration of SMC in converters with input filters and constant power loads has also shown effectiveness in stabilizing oscillatory behaviors [11]. Despite its advantages, SMC can introduce chattering phenomena and requires careful design of the sliding surface and switching logic. Nevertheless, the wide range of enhancements proposed in the literature reflects its strong potential for robust control in high-performance and real-time PV energy systems.

In this context, the present work addresses several of the gaps identified in the prior literature. Specifically, it introduces a partial-power DC-DC converter [12] with a *PI–SMC* control scheme, emphasizing both the control performance [13] and the power processing efficiency under dynamically variable conditions [14]. Unlike prior studies, the proposed system includes an integrated evaluation of current and voltage regulation, power transfer efficiency, and converter stability, all validated through real-time hardware simulation. This holistic approach contributes a novel and practical perspective on the design and assessment of robust *MPPT* controllers for PV systems.

The Partial-Power Converter (PPC) paradigm has gained attention as an effective strategy to increase energy efficiency and reduce stress on power components in applications such as PV systems [15,16], electric vehicle chargers [17,18], active power-buffer in fuel-cell [19], and high-density data centers [20]. The reviewed literature reveals a broad spectrum of topologies—ranging from non-isolated *Cuk*-based stages [21] to isolated full-bridge and resonant designs—each tailored to specific constraints of power density, scalability, and modularity. Main innovations include reconfigurable architectures, flux

cancellation techniques [22], hybrid control strategies, and topology adaptation [23,24] to reduce the processed power ratio [17] and improve thermal performance. Many works report efficiencies exceeding 98%, with some surpassing 99.5% [18,25], and significant reductions in power stage ratings [20]. Additionally, several studies [26,27] validate their proposals through experimental or real-time simulation platforms [28]. These contributions reinforce the versatility of PPC architectures and motivate their integration in next-generation renewable energy systems and high-performance conversion platforms [17,29].

In light of the reviewed developments, this work presents a novel PV-oriented converter architecture based on a non-isolated buck-boost topology with Partial-Power Processing (PPP). The converter is regulated by a dual-loop control scheme combining a Proportional–Integral (*PI*) voltage regulator with an inner *Sliding-Mode Controller* (*SMC*) for current tracking (*Dual PI–Sliding Mode Control*). This configuration enables accurate regulation while minimizing the processed power, thus reducing component stress and improving overall energy efficiency. The system is validated through both *MATLAB-Simulink* simulation and *real-time Hardware-in-the-Loop* (*HIL*) implementation using the *OPAL-RT* platform. The results confirm the architecture's suitability for scalable, robust, and cost-efficient deployment in modern distributed PV systems and DC microgrids.

Tables 1 and 2 summarize recent developments in DC-DC converter architectures and control strategies applied to photovoltaic systems, respectively. These comparative references help position the proposed converter topology and dual-loop control scheme within the context of existing works.

Table 1. Summary of recent sliding mode control strategies for DC-DC converters.

Author (Year)	Control Strategy	Application Converter	Main Contribution
[6] Chang et al. (2023)	Non-Singular Terminal SMC + ESO	Buck-Boost	Improved robustness and chattering mitigation
[7] Zambrano et al. (2024)	Adaptive SMC + Metaheuristic Optimization	Buck-Boost	Parameter tuning via custom metaheuristics
[8] Linares-Flores et al. (2020)	Adaptive SMC with Tanh Sliding Surface	Buck-Boost	Reduced switching noise and smoother control
[9] Huerta-Moro et al. (2024)	FPGA-Based SMC + PID	Buck	Real-time digital implementation on FPGA
[10] Wang et al. (2020)	Discrete-Time Fast Terminal SMC	Buck	Robustness under mismatched disturbances
[11] Tatar et al. (2023)	SMC in Buck with LC Input Filter	Buck with CPL	Stabilization under input filter dynamics
[5] Li et al. (2024)	SMC with Improved Exponential Reaching Law + Droop Control	Bidirectional DC-DC Converter	Reduced chattering, enhanced dynamic performance, and improved power allocation accuracy

Partial-power converter architectures have emerged as a promising solution for high-efficiency power management in renewable energy systems. Their defining feature—the ability to process only a fraction of the total power—enables reduced conduction losses, improved thermal performance, and lower component stress compared to full-power topologies. These advantages make them particularly attractive for a wide range of applications, including Photovoltaic (PV) installations, battery energy storage systems, Maximum Power Point Tracking (MPPT), and DC microgrids, see Figure 1.

Table 2. Comparative summary of recent converter architectures based on Partial-Power Processing (PPP).

Author (Year)	Converter Topology	Efficiency	Main Innovation	Application Focus	Isolated
[15] Iyer et al. (2021)	Phase-Shifted Full-Bridge (PSFB)	Up to 1.6% improvement at 50% load	Independent EV charging with 27% converter rating	EV Extremely Fast Charging	Yes
[25] Liu et al. (2022)	Bidirectional Step-Up/Down with Transformer	Peak > 99.5%	Unified control & stress reduction via transformer decoupling	Solid Oxide Electrolysis Systems	Yes
[16] Muller et al. (2022)	Reconfigurable Full-Bridge	Validated by simulation	Reconfigurable topology for flexible PV optimization	PV Module Power Optimizer	Yes
[30] Zientarski et al. (2018)	Series-Connected FB/Push–Pull	Reduced 46.9% nonactive power	Design method based on step-up/down voltage regulation	PV String-Level MPPT	Yes
[17] Anzola et al. (2024)	Dual Active Bridge (DAB)	Above 99%, lower than SiC losses	Si-based PPC competes with SiC in efficiency	Onboard EV Charger (OBC)	Yes
[20] Wu et al. (2024)	2-Phase Buck-Boost with IPOS/ISOP	Over 98% with hybrid control	Topology selection strategy + hybrid ZVS control	Data Centers/ High-Density DC Systems	No
[31] Artal-Sevil et al. (2022)	Non-Isolated Cuk	High efficiency, validated via Simulink	Comparative non-isolated PPC architectures	EV Auxiliary and Industrial Systems	No
[22] Mira et al. (2019)	Isolated Full-Bridge Boost (FCC)	98.2% (80% power rating reduction)	Low-cost, wide-range FCC for energy storage	Electrochemical Energy Storage	Yes

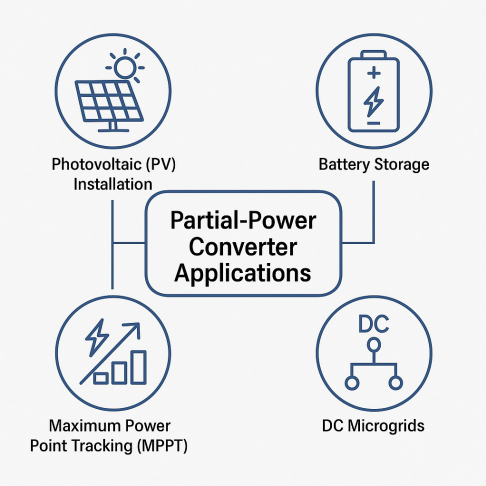


Figure 1. Application areas of partial-power converters in renewable energy systems.

In PV arrays, partial-power converters facilitate efficient MPPT implementation by allowing for direct energy transfer through a passive path while regulating only the required portion of the power, thereby enhancing energy harvesting. In storage interfaces, their bidirectional operation improves round-trip efficiency while preserving component lifespan. Furthermore, when deployed in modular or series-stacked system architectures, they offer inherent scalability and contribute to distributed thermal management. Nevertheless, their performance can be affected by variations in the input–output voltage ratio, especially under wide dynamic conditions. This necessitates the use of robust and well-coordinated control strategies to ensure stability, accurate power regulation, and proper interaction with the passive power flow. Despite these considerations, partial-power converters present a highly effective and scalable alternative for modern, cost-sensitive renewable energy applications where moderate voltage conversion is acceptable.

To address the aforementioned ideas and propose an efficient alternative for PV power processing, this paper presents the design, control, and validation of a partial-power converter regulated through a dual-loop *PI–Sliding Mode Control* strategy. This document is organized as follows. Section 1 provides a contextual introduction, including the motivation, state-of-the-art review, and identification of current limitations in MPPT and converter topologies. Section 2 presents the theoretical foundation and dynamic behavior of the proposed partial-power converter, highlighting its operating modes and characterizing the system's power ratio and voltage gain in relation to the duty cycle. Section 3 describes the full configuration of the PV-converter system, including component modeling, power flow equations, and relevant operating constraints under realistic irradiance and load profiles.

Section 4 develops the control architecture, detailing the design of a PI controller for voltage regulation and a Sliding-Mode Controller (SMC) for inductor current tracking. The section also discusses the advantages and practical considerations of implementing SMC in power converters. Section 5 presents simulation results under dynamic conditions, along with a real-time implementation using the *OPAL-RT* platform to evaluate the system's performance in hardware-oriented scenarios. Comparative results validate the accuracy and robustness of the proposed approach. Finally, Section 6 summarizes the main contributions of the work and outlines potential directions for future developments in partial-power control systems for PV applications.

2. Dynamic Behavior and Operation Modes of Partial-Power Converter

As a novelty, the architecture under study is a bidirectional, non-isolated partial-power DC-DC converter derived from the classical buck-boost topology. This converter is integrated into a series configuration with the load, allowing only a fraction of the total power to be processed by the converter itself. Such an arrangement significantly enhances overall system efficiency, reduces converter size, and lowers thermal stress on power components. This partial-power processing architecture is being studied for higher power renewable energy applications [12,17]. Unlike general treatments of buck-boost converters, this section introduces a partial-power architecture with modified gain and impedance behavior. The theoretical analysis focuses on steady-state and power flow modeling in to Input-Parallel Output-Series (IPOS) configurations.

Figure 2 illustrates the fundamental difference between conventional full-power converter architectures and the proposed partial-power configuration. In a full-power system, the entire energy flow from the DC source to the load is processed through the converter stage, which must handle 100% of the power, leading to increased conduction losses, larger component sizing, and higher thermal stress. In contrast, the partial-power architecture connects the DC-DC converter in series with the load—either at its input or output terminal—such that only a fraction of the total power is actively processed by the converter. This structure, typically referred to as an Input-Parallel Output-Series (IPOS) configuration, enables a significant portion of the power to bypass the active stage, flowing passively from the source to the load. As a result, the converter operates with reduced power handling requirements, which translates into higher overall system efficiency, improved thermal performance, and potential reductions in cost and size of the power processing unit.

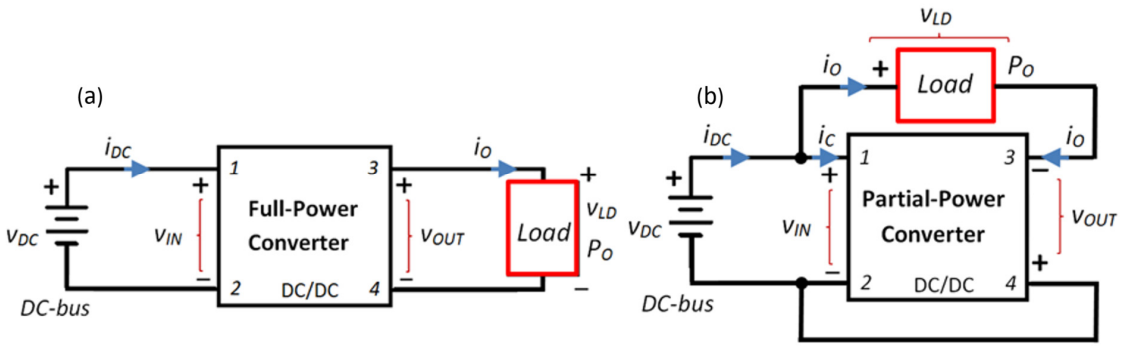


Figure 2. Block diagram of (**a**) full-power and (**b**) partial-power converter architectures.

In the full-power topology, the converter processes all the power flow supplied to the load from the DC-bus ($+v_{DC}$). Thus, the converter output voltage (v_O) is equal to the load voltage (v_{LD} ($v_O = v_{LD}$)). Whereas, in the partial-power topology, the load is connected in series between the DC-bus and the input or output of the DC converter, see Figure 2.

In the proposed Partial-Power Processing (PPP) topology, the converter is arranged in a series configuration with the load, following an Input-Parallel Output-Series (IPOS) topology [15], which minimizes the converter's processed power, enabling higher efficiencies, especially in high-power applications such as photovoltaic systems or electric mobility [19]. This structural arrangement leads to a split in the total power delivered to the load: a portion flows directly from the DC source through the passive path, while the remainder is regulated by the DC-DC converter. The voltage relationship at the load node can be written as follows:

$$v_{LD} = v_{DC} - (-v_O) = v_{DC} + M_f v_{DC} = v_{DC}\left(1 + M_f\right) \tag{1}$$

$$G_{vPPC} = \frac{v_{LD}}{v_{IN}} = \frac{v_{DC}\left(1 + M_f\right)}{v_{DC}} = \left(1 + M_f\right) \tag{2}$$

where v_{LD} is the load voltage (DC-bus), $v_{IN} = v_{DC}$ is the input voltage from the source (e.g., photovoltaic panel v_{pv}), v_O is the output voltage of the converter (v_C), and Mf is the gain of the buck-boost converter as a function of the duty cycle (D). This relationship guarantees that the load voltage (v_{LD}) is always greater than the source voltage, aligning with the requirements of step-up operations commonly seen in renewable energy systems (v_{DC}) [21]. Consequently, the converter gain (Mf) and the system gain (M) can be defined as follows:

$$M_f = \frac{v_C}{v_{IN}};\ M = \frac{v_{DC}\left(1 + M_f\right)}{v_{DC}} = \left(1 + M_f\right) \tag{3}$$

This expression highlights the additive voltage behavior inherent to the IPOS configuration and sets the basis for modeling the converter's role in partial-power handling. The processed power ratio, a key metric for evaluating efficiency, is defined as follows:

$$k_{pr} = \frac{P_{conv}}{P_{load}} = \frac{v_O}{v_{DC} + v_O} = \frac{M_f}{\left(1 + M_f\right)} \tag{4}$$

This parameter directly quantifies the fraction of power managed by the converter. It decreases as the converter output (v_{C2}) (and thus Mf) becomes smaller relative to the total load voltage (v_{LD}), confirming that efficiency improves when most of the power is transferred passively. This analytical framework defines the operational principle of the converter and supports the subsequent modeling of steady-state and dynamic performance.

Unlike traditional boost converters, which often suffer from severe efficiency drops due to high duty cycles, current ripple, and component stress, the partial-power converter can achieve similar or better output performance while handling significantly less power internally [31]. This results in reduced thermal losses, increased reliability, and lower costs. Figure 3 depicts the power flow distribution in the partial-power setup, clearly indicating that only a controlled portion of power passes through the converter stage [21]. The introduction of new partial-power processing topologies allows us to develop smaller and cheaper DC-DC converters, while power losses are reduced. In this paper, some advantages of the partial-power architecture on renewable energy applications have been verified.

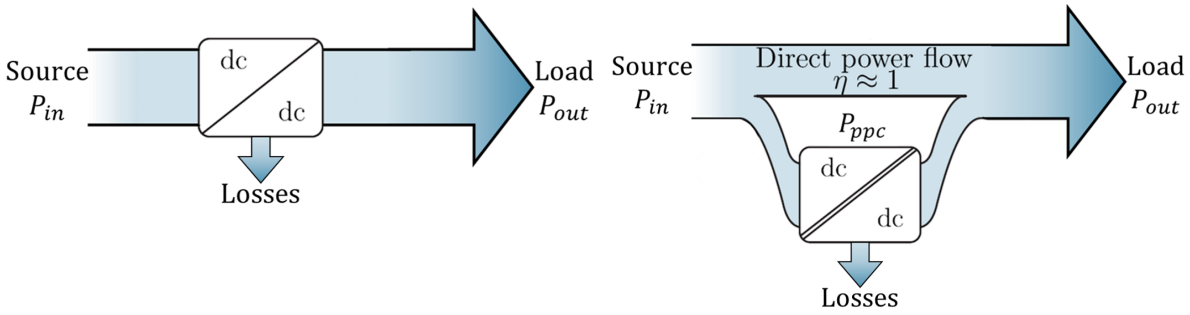


Figure 3. Concept of power flow in a partial-power converter. The main advantage of this partial-power architecture is that, now, the DC-DC converter only processes a fraction of the power supplied to the load.

Table 3 summarizes the main differences between traditional full-power converter architectures and the proposed partial-power approach. As shown, the partial-power solution introduces significant advantages in terms of efficiency, size, cost, and reliability, making it particularly attractive for renewable energy applications such as photovoltaic and storage-based systems.

Table 3. Comparative table: full-power vs. partial-power converter architectures.

Feature	Full-Power Converter	Partial-Power Converter
Power Processed by Converter	100% of the load power	Only a fraction of the total load power
Efficiency	Generally lower due to higher conduction and switching losses	Higher efficiency due to reduced processed power
Size of Magnetic Components	Larger inductors and capacitors required	Smaller magnetics possible due to reduced energy transfer
Thermal Management	Higher heat generation; requires more robust cooling systems	Lower thermal stress; smaller or passive cooling often feasible
Control Complexity	Conventional control methods	Requires modified or additional control logic (IPOS/ISOP)
Voltage Gain Range	Typically wider, but constrained by duty cycle and losses	Limited by series configuration, but improved step-up ratio
Application Cost	Higher due to power-hardened components	Lower cost for the same output performance
Reliability	Lower due to higher stress on components	Increased reliability through derated operation
Component Stress	High voltage and current stress on switches	Reduced electrical stress thanks to partial-power handling
Suitability for Renewable Energy	Moderate: needs adaptation for efficiency	Highly suitable: tailored for PV and storage systems

To quantitatively assess the benefits of the partial-power processing approach, the *processed active power ratio* (k_{PR}) is introduced. This parameter represents the proportion of power actively processed by the converter relative to the total power supplied by the source, and is defined as follows:

$$k_{PR} = \frac{P_{Conv}}{P_{DC}} = \frac{v_O \times i_O}{v_{DC} \times i_{DC}} \tag{5}$$

For the converter to operate effectively in the partial-power mode, the condition $k_{PR} < 1$ must be satisfied. This implies that only a fraction of the total power is handled by the converter, while the remaining power is directly delivered to the load through the passive path. In this way, the partial architecture will be more feasible, compared to the conventional option, when the reference parameter k_{PR} is lower.

By applying Kirchhoff's voltage law to the series-connected architecture, the relationship between k_{PR} and the static voltage gain (G_{vPPC}) is derived as follows:

$$k_{PR} = \eta_{system}\left(1 - \frac{1}{G_{vPPC}}\right) \tag{6}$$

where η_{system} is the overall system efficiency. Assuming an ideal converter ($\eta_{converter} \approx 1$, it is possible due to the high efficiency of DC-DC converters), this equation shows that when the voltage gain approaches unity (i.e., input and output voltages are similar), the power processed by the converter is minimized.

Figure 4 presents the characteristic curves of the power processing ratio (k_{PR}) as a function of the static voltage gain for both step-up (*IPOS*) and step-down (*ISOP*) partial-power topologies. These curves demonstrate that partial-power converters offer their greatest performance advantages in scenarios where the voltage difference between the input and the load is relatively small. Under such conditions, the converter processes only a minimal fraction of the total power, resulting in enhanced system efficiency and reduced stress on active components.

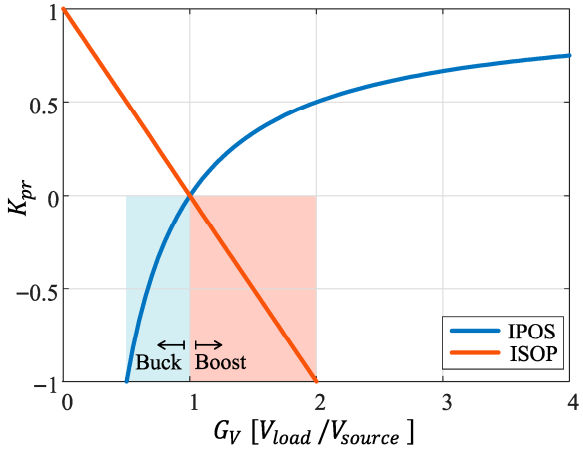


Figure 4. Characteristic k_{PR} curves for step-up (*IPOS*) and step-down (*ISOP*) architectures.

In order to simplify the steady-state analysis of the proposed architecture, some assumptions are made, such as ideal inductors and switching devices without delay in the switching process (see Figure 5). Thus, for the T_{SW} switching time, the switch is ON for $D \times T_{SW}$ time while OFF for $(1 - D) \times T_{SW}$ time. Therefore, depending on the state of the switch, two modes of operation in the continuous conduction mode (*CCM*) can be identified. The following is considered as an initial assumption:

$$\langle v_L(t) \rangle = 0;\ \langle i_C(t) \rangle = 0 \tag{7}$$

In this way,

Mode 1: ON-state [0 ≤ t ≤ D(t)T_{SW}].

At the initial time $t = 0$, when switch S_1 turns on, diode D_{S2} turns off. As a consequence, the diodes D_1 and D_2 are in conduction, while D_3 remains in cut, and the inductor currents (i_{L1} and i_{L2}) increase from their respective initial values. In this case, the voltage and current equations are as follows:

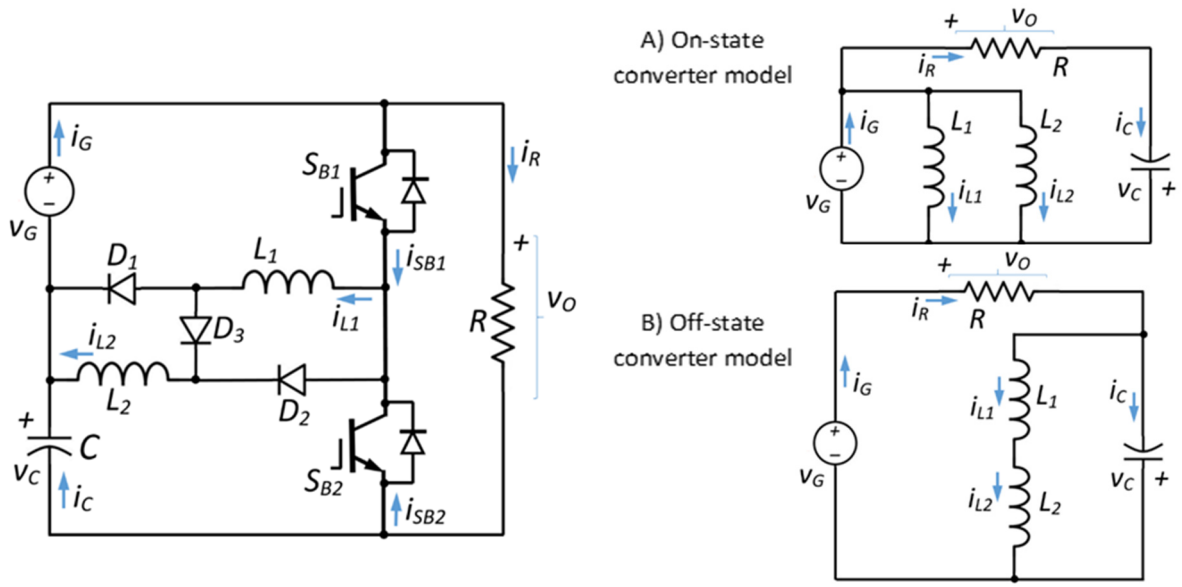


Figure 5. Equivalent model of the partial-power converter in the on-state (A) and off-state (B) modes in the continuous conduction mode (*CCM*). Diodes D_{S1} and D_{S2} represent the body diodes of switches S_{B1} and S_{B2}, respectively.

$$v_L(t) = L\frac{di_L}{dt} = v_G \tag{8}$$

$$i_C(t) = C\frac{dv_C}{dt} \tag{9}$$

$$i_R = \frac{v_O}{R} = \frac{v_G - (-v_C)}{R} = i_C(t) \tag{10}$$

Mode 2: OFF-state [D(t)TSW $\leq t \leq$ *TSW].*

When switch S_1 turns off ($t = D \times T_{SW}$), D_{S2} becomes forward-biased. Diodes D_1 and D_2 are now off, while D_3 conducts. The voltage and current dynamics in this interval are as follows:

$$2v_L(t) = 2L\frac{di_L}{dt} = -v_C \tag{11}$$

$$i_C(t) = C\frac{dv_C}{dt} \tag{12}$$

$$i_R = i_L + i_C;\ i_C(t) = i_R - i_L = \frac{v_G + v_C}{R} - i_L \tag{13}$$

For steady-state operation, the average inductor voltage (v_L) over a switching period must be zero. Therefore, analyzing the *volts–second balance* for the inductors (L) during a T_{SW} switching period, we obtain the following:

$$\langle v_L(t)\rangle = 0 \rightarrow v_G D + \left(-\frac{v_C}{2}\right)(1 - D) = 0 \tag{14}$$

Solving for v_C (capacitor voltage) and substituting the following:

$$v_C = v_o - v_G \tag{15}$$

$$v_G(1 + D) = v_O(1 - D) \tag{16}$$

The input voltage (v_G) is assumed to be constant over a switching period, thus solving for the steady-state output voltage v_O as follows:

$$\frac{v_O}{v_G} = M = \frac{(1+D)}{(1-D)} \tag{17}$$

This expression highlights the step-up characteristic of the buck-boost-based partial-power converter. The instantaneous duty cycle $D(t)$ can be expressed as a function of v_G and v_O, as follows:

$$D(t) = \frac{(M-1)}{(M+1)} = \frac{(v_O - v_G)}{(v_O + v_G)} \tag{18}$$

In addition, the average capacitor current (v_C) should be zero at the steady state. In this way, analyzing the current–second balance for the capacitor (C), during a T_{SW} switching period, we obtain the following:

$$\langle i_C(t) \rangle = 0 \rightarrow i_R D + (i_R - i_L)(1-D) = 0 \tag{19}$$

$$i_R = i_L(1-D) \tag{20}$$

The input current (i_G) supplied by the DC source (v_G) can be written as follows:

$$i_G = (2i_L + i_R)D + i_R(1-D) = 0 \tag{21}$$

Substituting the previous results, the following is obtained:

$$i_G = i_L(1-D) \tag{22}$$

$$i_R = i_G \frac{(1-D)}{(1+D)} \tag{23}$$

These equations show how the converter dynamically distributes power between the passive path and the active converter stage. The reduction in converter-handled current leads to substantial decreases in conduction losses.

Figure 6 presents the simulation waveforms of the proposed converter using *MATLAB-Simulink R2024b*. It includes the current and voltage profiles of all key components, such as the inductor currents (i_{L1} and i_{L2}), diode currents (i_{D1}, i_{D2}, and i_{D3}), source current (i_G), capacitor current (i_C), or simply the load current (i_R). In the analyzed scenario, an input voltage of v_G = +400 V, a duty cycle of D = 11.11%, and output voltage of v_O = +500 V have been considered. The load resistance (R) is set accordingly to achieve steady-state operation.

The plots confirm that the converter operates in the intended partial-power mode, with a reduced current stress on the switching devices and predictable voltage conversion behavior. These simulations validate both the dynamic model and the theoretical relationships derived above.

The relationship between the duty cycle (D), converter gain ($Mf = v_{C2}/v_{pv}$), and total system gain ($M = v_O/v_{pv}$) can be analytically derived from the operating principles of the series-connected partial-power architecture. Considering the converter output voltage (v_{C2}) in terms of D, the gain of the converter is defined as follows:

$$M_f = \frac{v_{C2}}{v_{pv}} = \frac{2D}{(1-D)} \tag{24}$$

Given that the system output voltage is the sum of the PV input and the converter output voltages ($v_O = v_{pv} + v_{C2}$), the system gain becomes the following:

$$M = \frac{v_O}{v_{pv}} = \frac{v_{pv} + v_{C2}}{v_{pv}} = 1 + M_f = \frac{(1+D)}{(1-D)} \tag{25}$$

In partial-power converter architectures, particularly in Input-Parallel Output-Series (IPOS) configurations, the input impedance seen from the source plays a key role in defining system stability, dynamic performance, and energy transfer capability. A proper impedance profile ensures that the source operates under favorable loading conditions, avoiding excessive current stress or inefficient operating points. For the proposed topology, the following two impedance perspectives must be distinguished: the equivalent input impedance of the overall system and the intrinsic input impedance of the converter stage.

The normalized input impedance of the system (R_G), referred to as the load resistance (R_L), can be expressed as follows:

$$R_G = R_L\left(\frac{1-D}{1+D}\right)^2 \rightarrow \left(\frac{R_G}{R_L}\right)_{system} = \left(\frac{1-D}{1+D}\right)^2 \tag{26}$$

This expression accounts for the power flow partially bypassing the converter and highlights the decrease in effective impedance as the duty cycle increases. On the other hand, the input impedance referred only to the converter stage is given by the following:

$$R_G = R_L\left(\frac{1-D}{2D}\right)^2 \rightarrow \left(\frac{R_G}{R_L}\right)_{converter} = \left(\frac{1-D}{2D}\right)^2 \tag{27}$$

which reveals a more rapid decrease in impedance for an increasing D. These relationships are fundamental for assessing the interaction between the source and the converter and must be considered when selecting operating ranges or designing upstream PV or energy-harvesting subsystems. In particular, excessive impedance mismatches at high duty cycles may deteriorate voltage regulation and dynamic response, especially under variable irradiance or load transients.

Figure 7 presents a comprehensive analysis of the converter's behavior by plotting both the voltage gain and input impedance ratio as functions of the duty cycle (D). The system voltage gain (M) and the converter voltage gain (Mf) increase nonlinearly with D, maintaining a constant offset between them ($M = Mf + 1$).

This relationship is inherent to Input-Parallel Output-Series (IPOS) topologies, where the output voltage results from the additive contribution of a passive and an actively regulated power path. The figure also includes the normalized input impedance ratio (R_G/R_L) for both the system and the converter stage, showing a smooth or steep decline, respectively, as D increases. These profiles illustrate how duty-cycle modulation affects source loading and converter stress.

The detailed analysis of the dynamic behavior and operational principles of the partial-power converter confirms its suitability for high-efficiency renewable energy applications. The following section addresses the experimental validation and performance assessment under real-world operating conditions. Future developments may focus on enhancing dynamic performance through advanced control strategies, adaptive duty-cycle modulation, and seamless integration with intelligent MPPT algorithms to further optimize energy conversion under variable operating conditions.

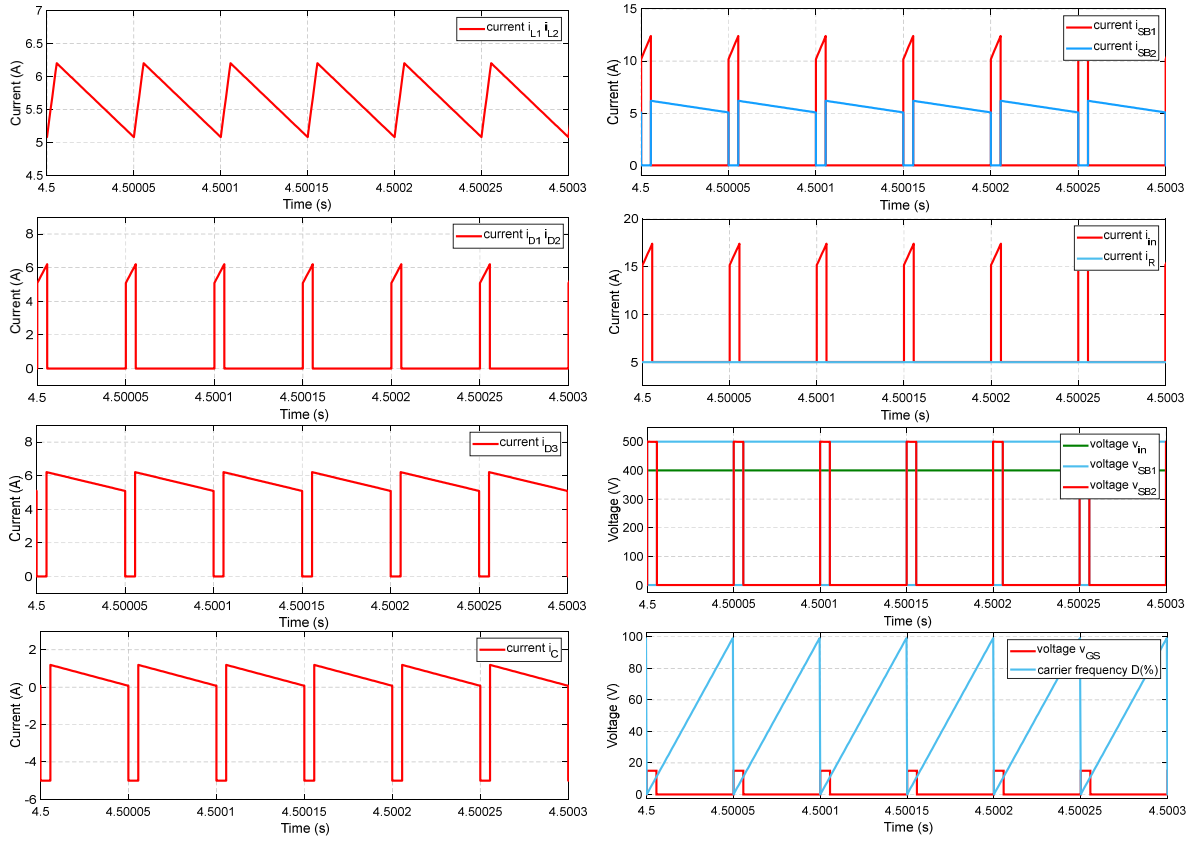


Figure 6. Simulation results of the partial-power converter architecture discussed above. The model was simulated using the *MATLAB-Simulink* software.

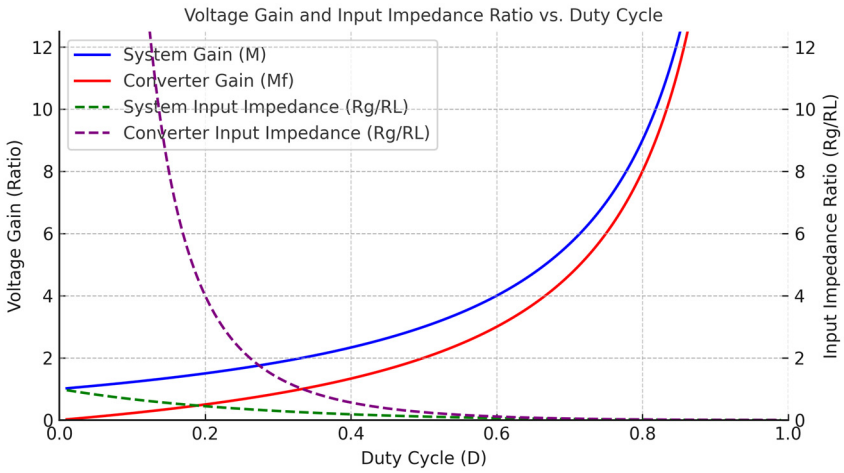


Figure 7. Voltage gain (*M*; *Mf*) and input impedance ratio (R_G/R_L) as functions of the duty cycle for the proposed partial-power converter.

3. System Description

The overall configuration of the PV partial-power converter system is depicted in Figure 8, based on the topology presented in [4]. The system integrates a photovoltaic (PV) array composed of four modules, connected to a two-stage single-phase inverter. The first stage consists of an improved DC-DC buck-boost converter, which is responsible for executing maximum power point tracking (*MPPT*). The second stage is an inverter that converts the regulated DC voltage into AC, which is subsequently applied to the load through an *LC* output filter.

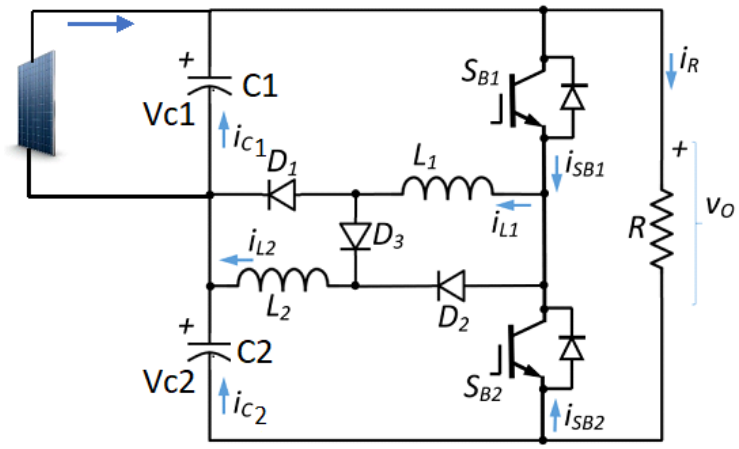


Figure 8. Schematic diagram of the proposed partial-power converter architecture. Current directions and switching elements are indicated for analysis of the dynamic behavior.

Figure 8 illustrates a schematic diagram of the system, highlighting key components: C_1 and C_2 are the intermediate capacitors that provide voltage stabilization and energy buffering; L_1 and L_2 are inductors used in the converter; the resistive load (R) is used to simulate the current injection into the DC-bus, effectively emulating a real power system interconnection. The signal u (1, 0) represents the discrete-time control input of the step-up stage, while S_1 and S_2 are the active switching devices. This operating principle is further detailed through differential Equations (29)–(31), which describe the dynamic evolution of the inductor and capacitor voltages under PWM modulation. These relationships serve as the basis for the subsequent control design.

The dynamic behavior of the system is described by the following set of differential equations:

$$\frac{dv_{c_1}}{dt} = \frac{1}{C_1}\left[i_{pv} - ui_L - \frac{v_{c_1} + v_{c_2}}{R}\right] \tag{28}$$

$$\frac{di_L}{dt} = \frac{2^u}{L}[uv_{c_1} - (1-u)v_{c_2}] \tag{29}$$

$$\frac{dv_{c_2}}{dt} = \frac{1}{C_2}\left[-\left(v_{C_1} + v_{c_2}\right)/R + (1-u)i_L\right] \tag{30}$$

where i_{PV} denotes the current generated by the PV array, i_L denotes the current flowing through the equivalent inductor, as defined in the simplified model shown in Figure 4, and v_C is the voltage across capacitor (C_1), which also defines the operating point of the PV system. Likewise, v_{C2} is the voltage across capacitor C_2, determining the DC-link voltage delivered to the inverter ($v_O = v_{C1} + v_{C2}$). The signal u is a binary control variable (either 0 or 1) that governs the switching state of the buck-boost converter.

The electrical behavior of the PV-array is described by the single-diode model (Figure 9), whose characteristic equation is given by the following:

$$i_{pv} = i_{sc}\left(1 - e^{\left(\left(v_{pv} - v_{oc} + R_s i_{pv}\right)/V_t\right)}\right) \tag{31}$$

Here, i_{pv} is the photovoltaic output current; i_{SC} is the short-circuit current; v_{PV} is the array output voltage, which is regulated by the voltage on C_1; v_{OC} is the open-circuit voltage; R_S is the series resistance; and v_T is the thermal voltage of the PV cell. This nonlinear equation reflects the dependency of the PV output on both the environmental and electrical operating conditions. The single-diode PV model adopted here offers a reasonable trade-off between accuracy and computational efficiency for control development and

simulation purposes. Although more complex models exist (e.g., double-diode or dynamic thermal–electrical coupling), they are often unnecessary for control-level design.

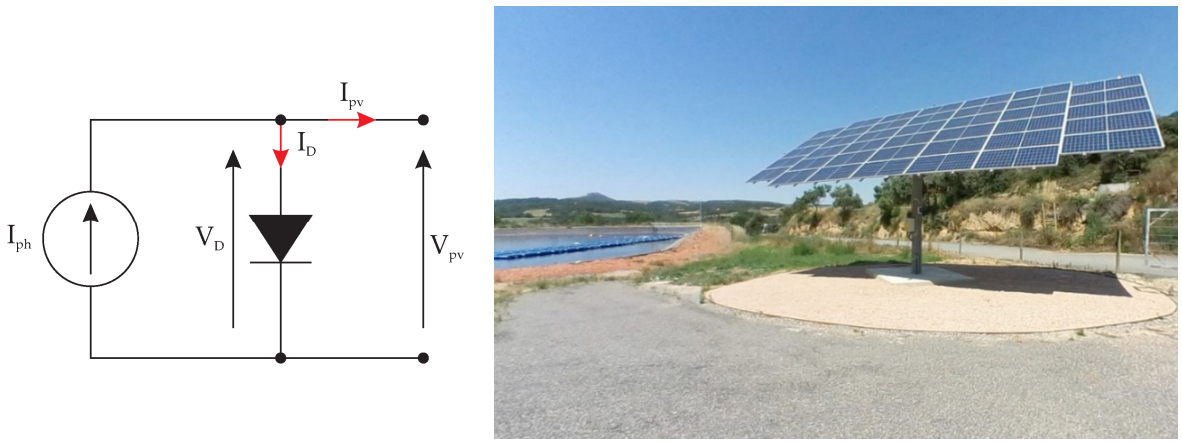


Figure 9. Ideal solar PV model. Photovoltaic panels located on a solar-tracker and floating photovoltaic modules. Stand-alone solar photovoltaic water pumping system for vineyard irrigation.

The sizing and dynamic behavior of the DC-link capacitor (C_2) play crucial roles in maintaining voltage stability at the intermediate bus, especially under rapid load variations or switching transients. Adequate capacitor selection is essential not only to limit voltage ripple but also to ensure proper decoupling between the boost and inverter stages. An undersized DC-link may lead to degraded output quality or instability in the AC voltage waveform generated by the inverter.

The complete system was implemented and simulated using *MATLAB-Simulink*, allowing for time-domain analysis of the converter behavior, energy transfer, and control response. To evaluate the effectiveness of the partial-power architecture in conjunction with the PV source, dedicated control algorithms were developed. These are described in detail in the following section.

Furthermore, the proposed system architecture is inherently modular, allowing it to be extended to larger-scale PV arrays or integrated into distributed energy systems. Multiple converter units can be interconnected in series or parallel configurations, supporting increased power levels and enhancing redundancy. This modular approach aligns well with the scalability requirements of modern DC microgrids and smart-grid infrastructures.

3.1. Power Flow and Efficiency Analysis in Partial-Power Mode

In the studied *IPOS*-based architecture, the PV array is connected in series with the output of the DC-DC converter. As a result, the total bus voltage is the sum of the PV output voltage and the converter output voltage, expressed as follows:

$$v_{bus} = v_{pv} + v_{C2} \tag{32}$$

Under this topology, the converter does not need to process the entire power demand. Instead, the passive series path allows for part of the power to reach the load directly, which reduces the burden on the converter's switching and magnetic components. Assuming ideal conditions, the voltage at the output of the converter (v_{C2}) can be expressed as a function of the PV voltage and the duty cycle (D).

$$v_{C2} = v_{pv}\frac{2\mathrm{D}}{(1-D)} \tag{33}$$

Substituting this into the expression, the instantaneous power processed by the converter is the following:

$$P_{conv} = v_{C2} \cdot i_{C2} = v_{pv} \frac{2\mathrm{D}}{(1-D)} i_{load} \tag{34}$$

The instantaneous power generated by the photovoltaic array is given by the following:

$$P_{PV} = v_{pv} \cdot i_{pv} \tag{35}$$

While, the total power delivered to the load, assuming resistive emulation of the DC-bus current, can be written as follows:

$$P_{load} = v_{bus} \cdot i_{load} = (v_{pv} + v_{C2}) \cdot i_{load} = v_{pv} \left(1 + \frac{2\mathrm{D}}{(1-D)}\right) i_{load} \tag{36}$$

The resulting power balance across the system can be expressed as follows:

$$P_{PV} + P_{conv} = P_{load} + P_{loss} \tag{37}$$

Thus, the processed power ratio is the following:

$$k_{PR} = \frac{P_{Conv}}{P_{load}} = \frac{v_{C2}}{v_{pv} + v_{C2}} = \frac{2D}{(1+D)} \tag{38}$$

This expression highlights the dependency of k_{PR} on the voltage gain and, indirectly, on the duty cycle (D). At low duty cycles, v_{C2} is small, and most of the power flows passively, maximizing the efficiency. Figure 11 illustrates how k_{PR} evolves as a function of D, confirming that partial-power operation is most effective under low-to-moderate gain conditions.

To evaluate the energy performance, the system-wide efficiency (η_{system}) is expressed as follows:

$$\eta_{system} = \frac{P_{load}}{\frac{P_{conv}}{\eta_{conv}} + P_{direct}} \tag{39}$$

where η_{conv} is the converter's intrinsic efficiency, and P_{direct} is the direct power flow (total power that is not processed by the converter), that is, the power that flows directly from the source (PV) to the load. Analytical and simulated results (Figures 12 and 13) demonstrate that the overall efficiency increases as k_{PR} decreases, outperforming full-power architectures, especially in scenarios with low conversion demands. This methodological framework establishes a rigorous basis for analyzing and designing partial-power converters, linking topology, control, and energy flow characteristics. It also justifies the architecture's suitability for photovoltaic systems, where efficiency and thermal optimization are critical.

$$P_{load} = P_{conv} + P_{direct} \tag{40}$$

$$P_{load} = (v_{pv} + v_{C2}) \cdot i_{load};\ P_{conv} = v_{C2} \cdot i_{load};\ P_{direct} = v_{pv} \cdot i_{load} \tag{41}$$

This equation highlights the core principle of partial-power processing: the converter handles only a fraction of the total power, with the remainder directly transferred through the passive path. This configuration enables improved efficiency, lower thermal stress, and optimized component usage.

Figure 10 illustrates the evolution of the power delivered to the load (P_{load}) as a function of the duty cycle (D) for the following three representative values of load current: 1 A, 2.5 A, and 5 A. The results, obtained under ideal operating conditions and assuming a constant photovoltaic input voltage of +400 V, reveal the nonlinear dependence of the output power on the duty-cycle modulation. As analytically described in Equation (39),

P_{load} increases sharply as D approaches unity—a trend that becomes more pronounced at higher load currents due to the combined rise in converter output voltage and total system power. The plotted curves emphasize the high sensitivity of the delivered power to small changes in the duty cycle, particularly in the upper operating range, highlighting the critical need for precise and stable duty-cycle control in partial-power converter architectures to ensure accurate power regulation and avoid overshoot or instability.

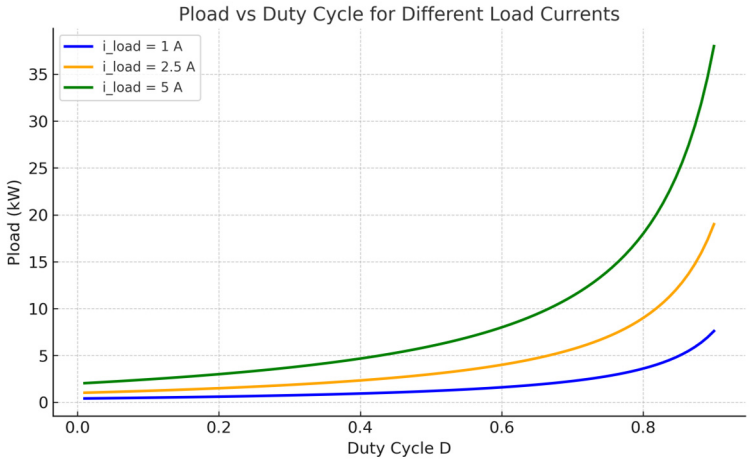


Figure 10. Power delivered to the load (P_{load}) as a function of the duty cycle (D) for different values of load current.

Figure 11 illustrates the relationship between the power processing ratio k_{PR} and the converter duty cycle (D). In this architecture, k_{PR} depends solely on D and remains independent of the load current, as both P_{conv} and P_{load} are linearly dependent on it. The graph highlights that, at low duty cycles, the converter processes only a small fraction of the total power, reducing conduction and switching losses. As D increases, k_{PR} approaches unity, indicating that the converter begins to handle a greater share of the total power. This trend underscores the importance of optimizing the duty cycle to maintain high efficiency while minimizing converter stress.

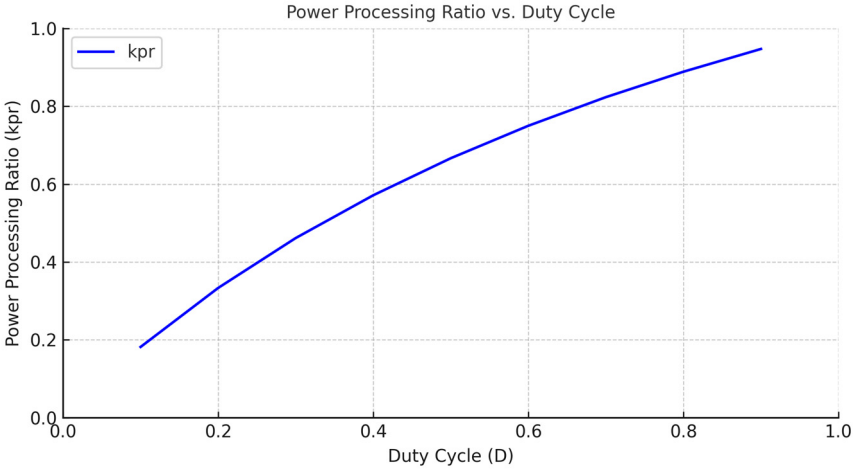


Figure 11. Variation in the power ratio ($k_{PR} = P_{conv}/P_{load}$) as a function of the duty cycle (D) in an *IPOS* partial-power converter configuration. The curve shows that the fraction of power processed by the converter decreases significantly at lower values of D, confirming its partial-processing nature.

It is worth noting that the system exhibits increasing sensitivity to control variations as the duty cycle (D) approaches unity. In this region, even small perturbations in D can produce significant changes in both the converter output voltage and the power

processed. This behavior necessitates precise control resolution and stability in the duty-cycle modulation to maintain the desired performance and avoid overshoot or instability in dynamic operation.

3.2. Efficiency Analysis: Partial Power vs. Full Power

In partial-power converter architectures, the total power processed by the converter varies with the operating duty cycle (D). This behavior directly influences the overall system efficiency. As the duty cycle decreases, the voltage gain of the converter reduces, resulting in less power processed by the active conversion stage and more power flowing directly through the passive path. This section analyzes the relationship between system efficiency and duty cycle and compares it to the performance of a conventional full-power converter.

The estimated system efficiency for the partial-power converter can be expressed as follows:

$$\eta_{system} = 1 - k_{pr}(1 - \eta_{conv}) \tag{42}$$

$$k_{PR} = \frac{Mf}{1 + Mf} = \frac{2D}{(1 + D)} \tag{43}$$

where η_{conv} is the efficiency of the converter, and M is the system voltage gain defined as v_{bus}/v_{pv}. As M increases with a higher D, the denominator decreases, and η_{system} becomes more sensitive to the internal efficiency. Conversely, at lower values of D, M approaches 1, and η_{system} tends toward unity, maximizing the overall performance.

In contrast, a full-power converter processes the entire load power regardless of D, so the overall system efficiency equals the internal converter efficiency, as follows:

$$\eta_{full} = \eta_{conv} \;\rightarrow\; k_{pr} = 1 \tag{44}$$

This distinction underscores one of the principal advantages of partial-power converter architectures: by actively processing only a fraction of the total system power, they can achieve superior global efficiency compared to conventional full-power configurations. When appropriately designed and controlled, the reduced processing burden leads to lower conduction and switching losses within the active stage. Figure 12 presents a comparative analysis of system efficiency as a function of the duty cycle (D), assuming an internal converter efficiency (η_{conv}) of approx. 98.25%. The results clearly show that the partial-power configuration outperforms the full-power counterpart, particularly in the low-to-moderate duty-cycle range, where the converter handles a smaller portion of the total energy flow. This operational regime maximizes the benefit of partial-power processing by allowing for more energy to be transferred through the passive path, thus minimizing losses and enhancing overall performance.

In this study, a more realistic efficiency model for the converter has been adopted, incorporating the degradation observed under light-load conditions. Specifically, a slight efficiency penalty is introduced at low power levels due to the relative impact of fixed losses—including core, switching, and control circuitry losses—which become dominant when the processed power decreases. This phenomenon, commonly observed in converter architectures operating at low duty cycles, leads to a gradual reduction in efficiency as the duty cycle moves toward the lower end of the operational range. Accordingly, the converter efficiency can be approximated by the following expression:

$$\eta_{real}(D) = \eta_{nominal} - \Delta\eta(D) \tag{45}$$

where $\eta_{nominal}$ denotes the peak or nominal efficiency under full-load operation (typically around 98.25%), and $\Delta\eta(D)$ represents a nonlinear decreasing function that quantifies the efficiency loss associated with reduced power processing. This model provides a more accurate representation of the converter's performance over a wide operating range and is essential for correctly estimating the global system efficiency in partial-power architectures.

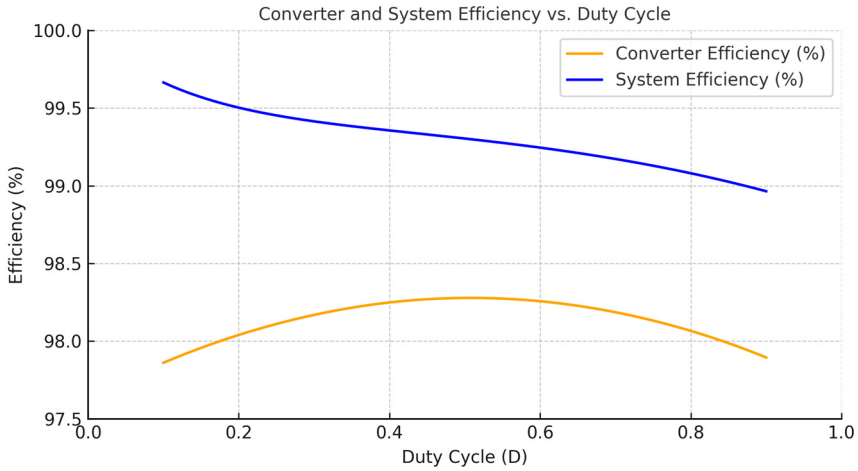


Figure 12. Estimated system efficiency as a function of the duty cycle (D), comparing a partial-power converter architecture with a conventional full-power converter.

Figure 13 illustrates a contour map of the global system efficiency (η_{system}) as a function of the duty cycle (D) and the internal efficiency of the partial-power converter (η_{conv}). The map reveals the interaction between the control modulation and converter performance, highlighting how system-level efficiency improves when the processed power fraction is minimized, i.e., at lower values of duty cycle (D). This is because, under these conditions, the active converter handles only a small portion of the total load power, while the majority is transferred directly via the passive path, thereby avoiding conversion losses.

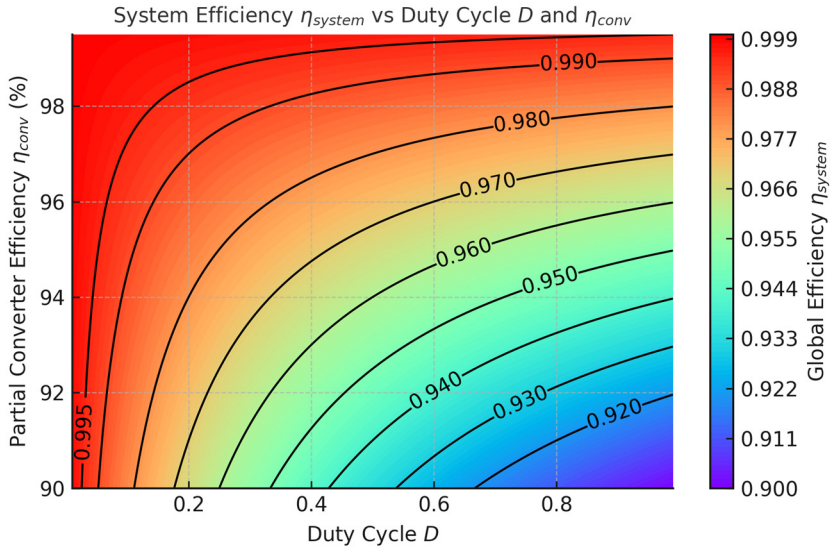


Figure 13. Global system efficiency (η_{system}) as a function of the duty cycle (D) and the partial converter efficiency (η_{conv}). The diagram highlights the influence of both variables on the overall performance, with contour lines indicating efficiency thresholds between 92% and 99.5%.

At high values of η_{conv} (above 97%) and low-to-moderate values of D (below 0.4), the global efficiency reaches or exceeds 99%, which is significantly higher than what would be achievable with full-power processing using the same conversion stage. Conversely,

when $D \rightarrow 1$, the system becomes increasingly dependent on the converter, and η_{system} asymptotically approaches η_{conv}, as the passive contribution diminishes. The iso-efficiency contours (from 92% to 99.5%) provide insight into optimal design regions for partial-power architectures, and serve as a useful tool for evaluating the trade-offs between converter quality and control requirements in high-efficiency renewable energy systems.

The results presented in this section emphasize the critical role of the converter architecture in optimizing system-wide energy performance. The iso-efficiency contours guide the selection of duty cycle and converter efficiency pairs to meet specific performance targets. To fully exploit the advantages of partial-power processing, it is essential to implement robust and efficient control algorithms, which are addressed in the following section.

4. Control Algorithms

This section describes the two control strategies implemented in the partial-power converter system. The first is a nonlinear *Sliding Mode Control* (*SMC*) [13] designed for current loop regulation, providing robustness against disturbances and model uncertainties. The second control strategy consists of a conventional *Proportional-Integral* (*PI*) regulator implemented in the outer voltage loop, tasked with ensuring accurate tracking of the reference voltage and generating the corresponding inductor current reference required by the inner control loop.

4.1. Theoretical Foundations of Sliding Mode Control

Sliding Mode Control (SMC) is a robust, nonlinear control technique well suited for power electronics due to its fast response and insensitivity to bounded disturbances and model inaccuracies. The system state is forced to evolve along a pre-defined sliding surface, $s(t) = 0$, leading to invariant system dynamics. This approach guarantees global stability within the sliding domain, and robustness is inherently achieved without requiring precise knowledge of all system parameters.

SMC is particularly advantageous in current-mode control of converters, where fast switching and high dynamics are needed to reject fast load transients and input fluctuations. To provide a clearer perspective on the suitability of sliding mode control in power converter applications, Table 4 summarizes its main advantages and practical limitations. This comparative overview highlights the method's key strengths, such as robustness and fast dynamic response, while also addressing implementation challenges, including the well-known chattering effect and sensitivity to switching constraints in digital systems.

Table 4. Sliding mode control (SMC)—advantages and limitations.

Aspect	Advantages/Strengths	Limitations
Robustness	High robustness to parameter variations and load disturbances	
Dynamic Response	Fast transient response and high bandwidth	
Implementation Complexity	Simple control law with binary output	May require additional logic for switching management
Chattering Effect		Presence of high-frequency oscillations near the sliding surface
Switching Frequency Dependency		Requires smoothing strategies (e.g., hysteresis and boundary layer)
Model Sensitivity	Insensitive to parameter uncertainties in sliding mode	
Digital Implementation		Requires careful tuning to preserve sliding conditions under sampling

This dual-loop control structure provides a flexible and efficient approach for regulating power flow in partial-power converter architectures, combining the robustness of SMC for current tracking with the simplicity of a PI controller for voltage regulation.

4.2. Current Loop Control with Sliding Mode Control and PI Control

To regulate the inductor current (i_L), a sliding surface is defined as follows:

$$s(t) = i_L - i_{L_{ref}} \tag{46}$$

where i_{Lref} is the current reference, derived from the outer voltage loop, as follows:

$$i_{L_{ref}} = \frac{V_{ref}}{(1-d)R} \tag{47}$$

where d represents the duty cycle, and R is the equivalent resistive load. The control action is implemented through a discontinuous sliding-mode law, as follows:

$$u(t) = \frac{1}{2} - \frac{1}{2} sign(s(t)) \tag{48}$$

This binary control signal ensures that the system trajectory is driven toward the sliding surface and maintained there, enabling fast and robust current tracking under parameter variations or external perturbations.

To track the voltage reference (v_{ref}), a standard PI controller is adopted in the outer loop, generating the current reference, as follows:

$$u(t) = k_p\left(v_{ref} - v_c\right) + k_i \int \left(v_{ref} - v_c\right) dt \tag{49}$$

where k_p and k_i are the proportional and integral gains, and $v_c(t)$ is the measured output voltage across the DC-link capacitor. The PI structure ensures zero steady-state error under constant references and is well suited for voltage regulation in the outer loop, complementing the fast response of the inner SMC loop.

The dual-loop control strategy implemented in the proposed system combines an outer Proportional–Integral (PI) voltage regulator with an inner Sliding Mode Current Controller (SMCC), resulting in a robust and high-performance control framework for partial-power converter architectures (see Figure 14). The PI controller operates on the voltage error to generate the current reference (i^*), which is then tracked by the SMCC to regulate the inductor current (i_L). The SMCC outputs a discontinuous switching signal (u), which governs the converter's operation and ensures accurate tracking of both voltage and current under dynamic conditions.

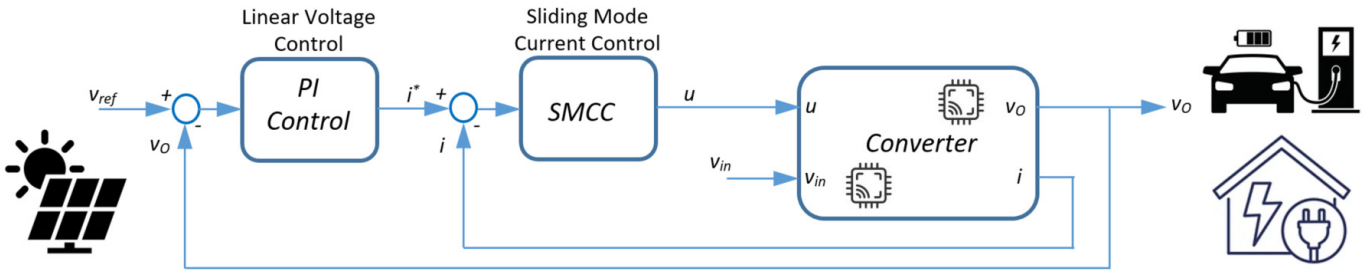


Figure 14. Dual-loop control diagram with PI voltage and sliding-mode current regulation. The outer *PI voltage controller* generates the current reference (i^*), which is regulated by the inner *Sliding Mode Current Controller* (SMCC).

This coordinated control mechanism enables stable energy flow management and strong disturbance rejection, even in the presence of rapid variations in input voltage or load. The control topology also facilitates precise regulation while minimizing sensitivity to parameter variations, making it well-suited for renewable energy applications. Furthermore, the modularity of this scheme allows for future extensions, such as the integration of adaptive-, predictive-, or MPPT-based intelligent control strategies. The effectiveness of the implemented dual-loop system is evaluated in the following section through detailed simulation results under representative operating scenarios.

5. Results

The proposed PV partial-power converter system has been modeled and simulated using *MATLAB-Simulink*. The values of the main electrical and control parameters are summarized in Table 5 (refer to Nomenclature section for details).

Table 5. Electrical and control parameters used in the simulation of the partial-power converter system.

PV Module Parameter	Value	Converter Parameter	Value
Rated Power, P_{pv}	320 W	Inductance, L_1 and L_2	0.50 mH
Short-Circuit Current, i_{sc}	9.26 A	Output Capacitors, C_1 and C_2	500 µF
Open-Circuit Voltage, v_{OC}	45.3 V	PI Gain—Proportional, kp	0.0003
Series Modules per String, Ns	4	PI Gain—Integral, ki	0.0385
Parallel Strings, Np	2	Switching Period, Ts	10 µs

The maximum power handled by the partial-power converter (P_{ppmax}) is directly determined by the total photovoltaic generation capacity connected to its input stage. This total input power can be expressed as follows:

$$P_{ppmax} = N_s \cdot N_p \cdot P_{pv} \tag{50}$$

where *Ns* represents the number of PV modules connected in series per string, *Np* denotes the number of parallel strings, and *Ppv* is the rated power of each individual panel. This formulation provides a direct estimation of the upper power limit that the converter must be capable of processing under full irradiance and optimal operating conditions, and its serves as a key design criterion for sizing the active components and the thermal management system of the converter stage.

All simulations were carried out using *MATLAB-Simulink* with a fixed-step solver and a sampling time of 5 µs, ensuring accurate representation of switching dynamics. Standard test conditions were assumed for the PV array, as follows: irradiance of 1000 W/m^2 and ambient temperature of 25 °C. The electrical parameters of the modules and passive components were selected based on commercially available hardware, allowing for straightforward extrapolation to real-world implementation scenarios. These settings establish a realistic framework for evaluating the dynamic performance and energy efficiency of the proposed system under typical operating conditions.

5.1. Simulation Analysis

Figure 15 illustrates the temporal evolution of the test conditions applied to the photovoltaic system under real-time validation. The upper plot shows the step changes in the following three critical parameters: solar irradiance E (in W/m^2), load resistance R (in ohms), and reference voltage v_{ref} (in volts). These variations are introduced to emulate realistic operating scenarios, including transient solar conditions and load disturbances, which pose a challenge for voltage regulation and dynamic stability. The system is initially subjected to high irradiance (1100 W/m^2) and a moderate load, followed by a sudden

drop in solar input to 600 W/m^2. Later, both the load and the voltage reference are varied independently to evaluate the controller's response under multiple perturbations. The dynamic nature of these changes directly affects the power available from the PV generator and the current demanded by the load, making it a representative testbench for converter performance assessment.

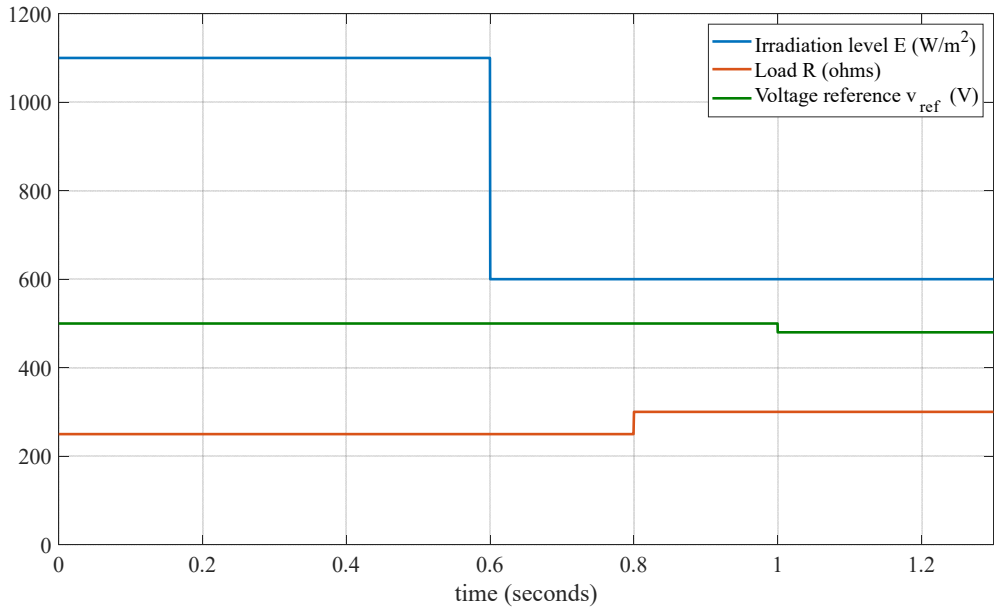


Figure 15. Time evolution of the test conditions used for system validation. The plot shows the profiles of solar irradiance E (W/m^2), load resistance R (Ω), and reference voltage v_{ref} (V) applied during the simulation and real-time testing phases.

Despite these variations, the system maintains regulated output behavior, as shown in Figure 16, thanks to the robustness of the proposed partial-power topology and its dual-loop PI–SMC control scheme. The output voltage (v_O) (DC-bus) closely follows the reference (v_{ref}) with minimal steady-state error and low ripple, while the duty cycle (D) adapts smoothly to the imposed transitions. This confirms the converter's ability to handle time-varying conditions while preserving output stability and efficiency.

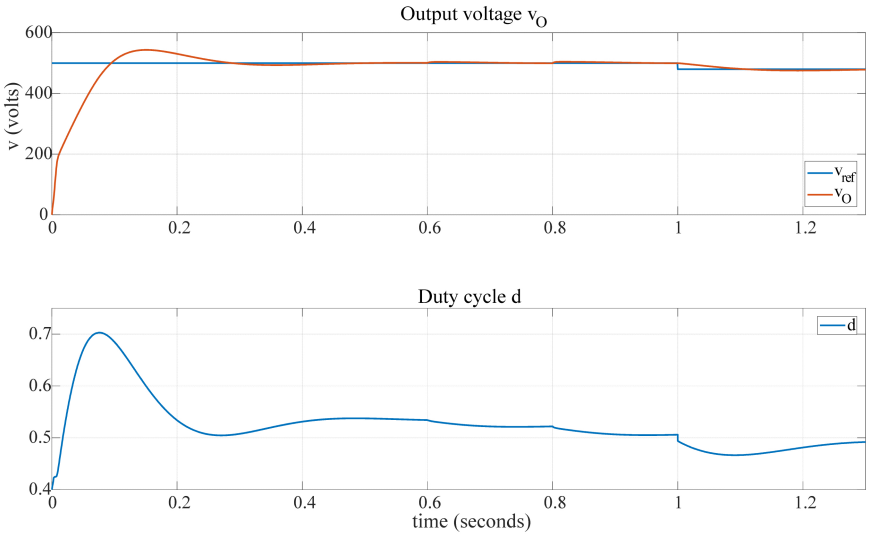


Figure 16. Output voltage response (DC-bus) and control signal D under varying irradiance, load, and reference voltage conditions. The system tracks the reference (v_{ref}) with high stability and dynamic adaptation of the duty cycle.

Figure 17 illustrates the internal dynamics of the current control loop governed by the Sliding-Mode Controller (*SMC*). The waveform of the inductor current (i_L) shows fast convergence toward its reference value (i_{Lref}), with minimal steady-state error and strong disturbance rejection. The sliding surface signal ($s(t) = i_L - i_{Lref}$) demonstrates that the system rapidly reaches and maintains sliding mode operation, confirming the existence of a sliding regime. The control action ($u(t)$) exhibits characteristic high-frequency switching, inherent to the discontinuous nature of the *SMC* law. This confirms that the controller enforces the intended dynamics by switching the control state in response to deviations from the sliding surface, ensuring robust and stable current regulation.

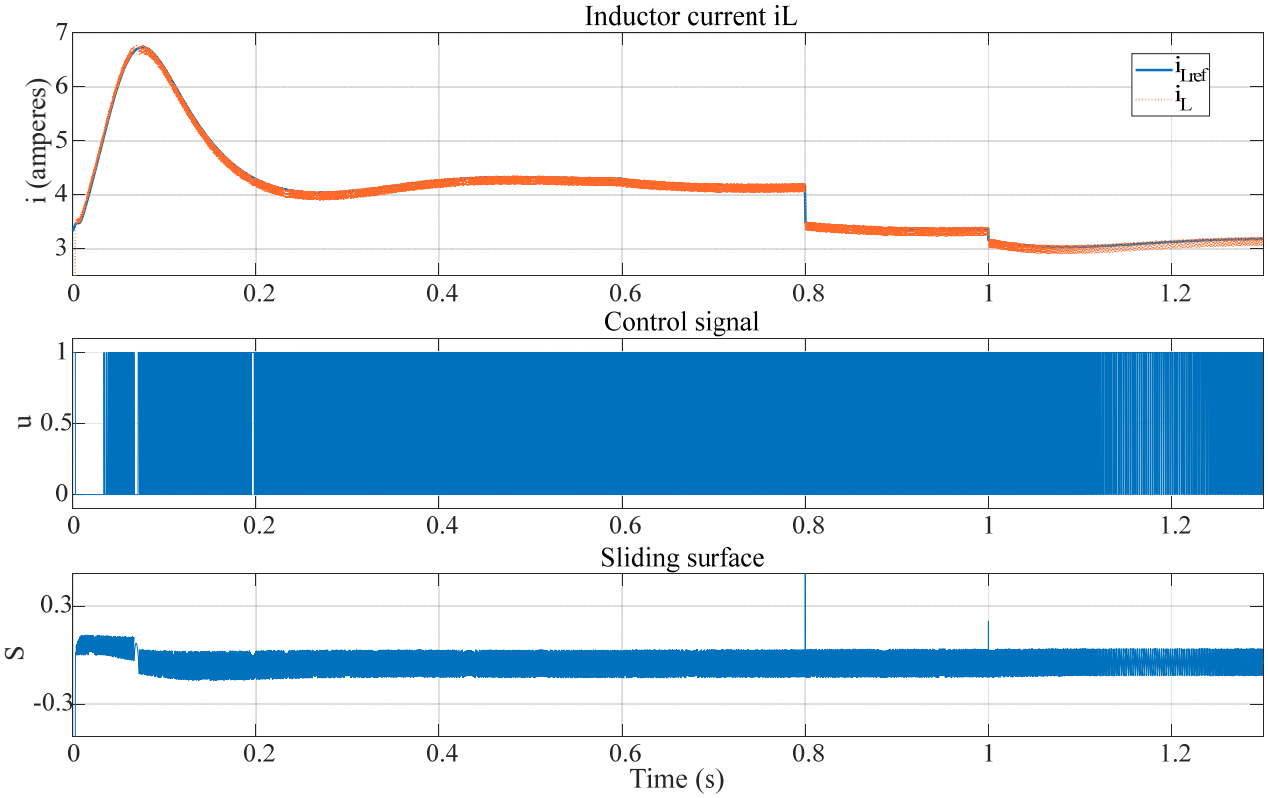


Figure 17. Inductor-current tracking performance and sliding-mode-control behavior. The top plot shows accurate tracking of the reference current (i_{Lref}) by the inductor current (i_L). The middle plot displays the binary switching signal (u), and the bottom plot shows the sliding surface (S), which remains bounded and stable throughout the dynamic sequence.

Figure 18 provides a detailed view of the switching behavior associated with the sliding mode control implementation. The control signal alternates between two discrete states ($u = 0$ and $u = 1$), forcing the system's trajectory to remain within the vicinity of the sliding surface. This high-frequency switching is a direct consequence of the discontinuous control law, which aims to counteract disturbances and model uncertainties by reacting instantaneously to sign changes in the error. Although this behavior ensures robustness and precision, it also reveals the presence of chattering—a known limitation of ideal SMC—which may require mitigation techniques such as hysteresis bands or boundary layer approximations in practical implementations.

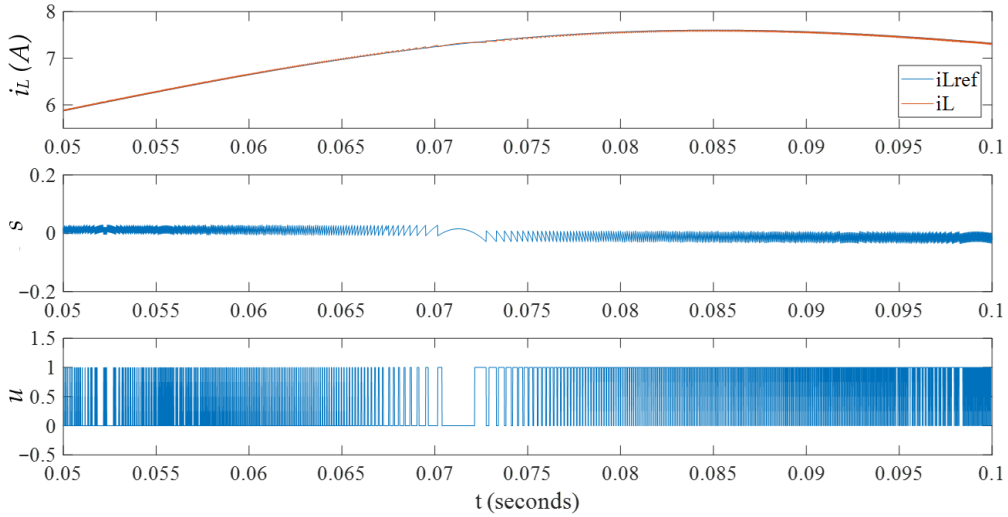


Figure 18. Detailed view of the sliding-mode current control dynamics. The top subplot shows inductor current (i_L) closely following its reference (i_{Lref}). The middle plot illustrates the evolution of the sliding surface (s), highlighting high-frequency switching activity. The bottom plot displays the corresponding discontinuous control signal (u), characteristic of sliding mode regulation.

The simulation results confirm that the combined *PI–SMC* control structure achieves fast, stable, and robust regulation of both current and voltage, even under dynamic operating conditions. To further validate its performance under real-time constraints, the system was subsequently implemented in a hardware-in-the-loop environment using *OPAL-RT*.

5.2. Real-Time Simulation with OPAL-RT

The proposed system model has been implemented within a real-time simulation environment using the *OPAL-RT* platform. This *Hardware-in-the-Loop* (*HIL*) configuration enables the evaluation of the converter's dynamic behavior and control performance under realistic operating conditions, leveraging *FPGA*-based execution. The use of *HIL* has been widely adopted in power electronics research and is considered a robust validation methodology when direct prototyping is impractical due to voltage, power, or cost constraints.

Figure 19 shows the real-time simulation platform based on *OPAL-RT* technology, used for *hardware-in-the-loop* (*HIL*) validation of the proposed partial-power converter system. The *OPAL-RT HIL* environment enables high-fidelity emulation of power electronic systems with sub-microsecond time resolution, allowing for the execution of real-time models that interact dynamically with physical controllers. This setup provides a safe, reproducible, and flexible framework to assess control strategies and converter behavior under realistic operating conditions without the risks or limitations associated with full-scale laboratory hardware testing. The *HIL* methodology plays a crucial role in bridging the gap between numerical simulation and experimental prototyping, supporting accelerated development and robust validation of advanced control schemes.

Figure 20 presents the high-level block diagram of the simulation model implemented in the *OPAL-RT* environment, detailing the signal acquisition, communication, and visualization structure used for real-time execution. The model includes multiple *OpComm* and *OpComm Acq* modules responsible for bidirectional data exchange between the physical controller and the digital real-time model. Each key system variable—such as input/output voltages, inductor currents, duty cycle, and control references—is monitored and logged through interface blocks, enabling comprehensive analysis of the system response under dynamic operating conditions. This modular and synchronized configuration ensures real-time observability and interaction with the converter model, as well as supports hardware-in-the-loop experimentation with high fidelity and temporal resolution.



Figure 19. OPAL-RT HIL (*hardware-in-the-loop*) real-time analysis device.

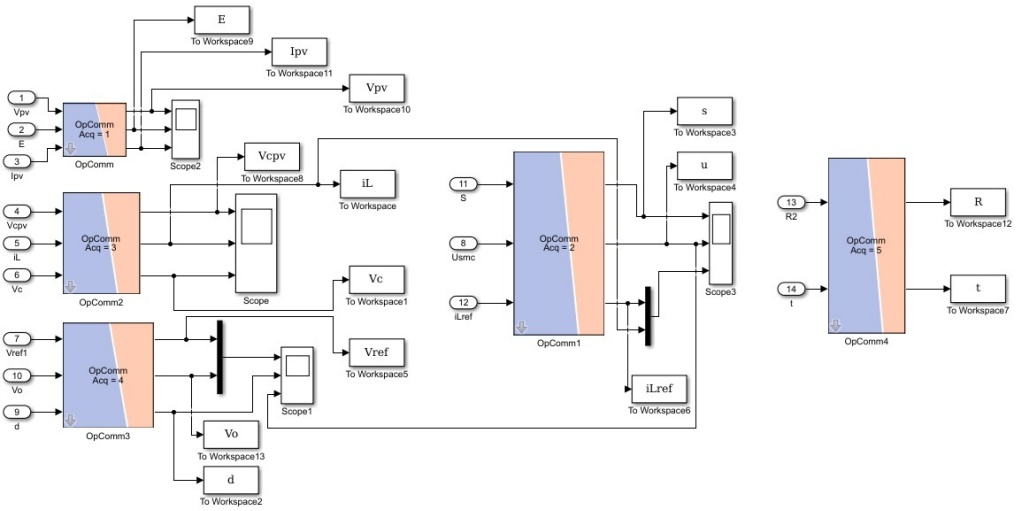


Figure 20. Real-time implementation of the converter model on the *OPAL-RT* platform (*Hardware-in-the-Loop—HIL*).

Figure 21 compares the output voltage dynamics obtained from the *MATLAB-Simulink* simulation and the real-time execution on the *OPAL-RT* platform. The results show excellent agreement between both environments, with the voltage signal exhibiting smooth transient response and accurate tracking of the reference in both cases. Minor differences in the rise time or steady-state ripple may be attributed to numerical discretization and the real-time scheduling constraints of the hardware-in-the-loop system.

Figure 22 presents the evolution (detail) of the inductor current as simulated in *MATLAB-Simulink* and replicated in *OPAL-RT*. The current follows the expected trajectory in both cases, confirming that the sliding mode current controller maintains stable operation and correct switching behavior when deployed on *FPGA*-based hardware. The high similarity between both responses validates the effectiveness of the proposed control algorithm and its feasibility for embedded real-time applications. The observed response time in both the simulated and HIL results suggests an effective bandwidth exceeding 3 kHz, consistent with typical design expectations for fast current-mode regulation in power converters.

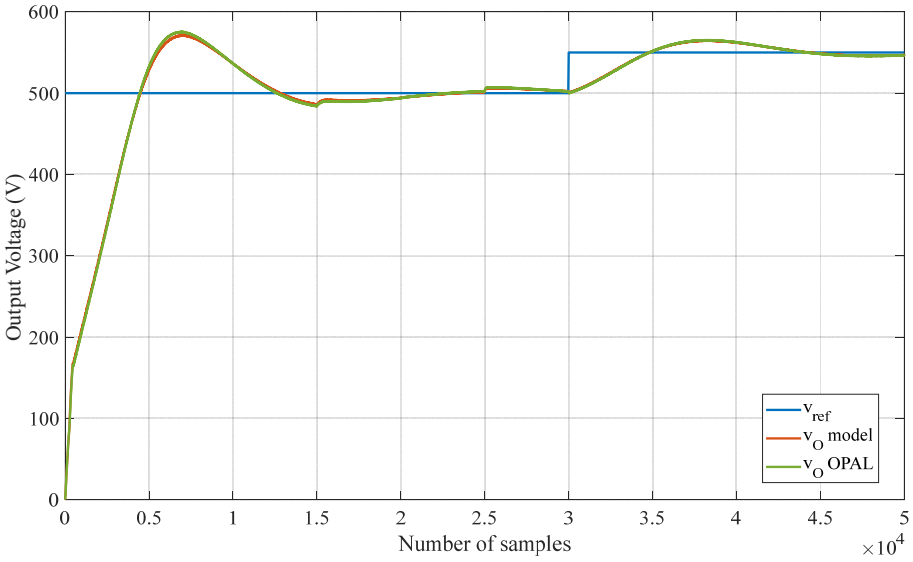


Figure 21. Output voltage (v_O) tracking performance under simulation and *OPAL-RT* (*HIL*) real-time validation. The output follows the reference (v_{ref}) with high accuracy during dynamic transitions, confirming the effectiveness of the proposed control strategy.

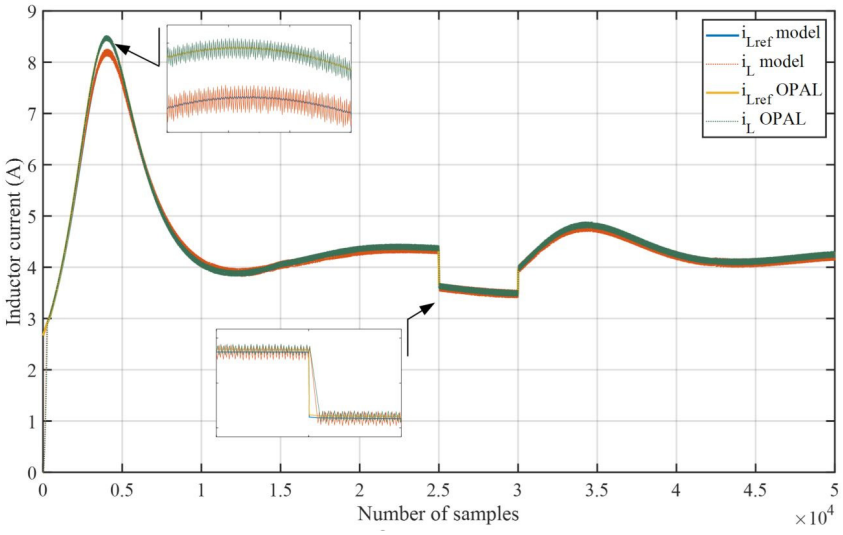


Figure 22. Inductor current tracking performance comparing *MATLAB-Simulink* model and real-time *OPAL-RT* results. The current reference (i_{Lref}) and actual current (i_L) exhibit excellent agreement across dynamic transients. The embedded zoom highlights the steady-state ripple and synchronization between the hardware and model outputs.

After compiling the system for *FPGA* execution, the model was simulated with a fixed step size of 20 µs using a *Runge-Kutta* solver. Figures 21 and 22 compare the dynamic response of the *MATLAB-Simulink* model and the *OPAL-RT* hardware implementation for the output voltage and inductor current, respectively. The results confirm excellent agreement between both platforms, with accurate tracking of the reference signals in both cases. Given the converter's voltage and power rating, full-scale hardware testing poses significant practical challenges. These include safety risks, the need for isolation and protection hardware, and access to high-voltage laboratory infrastructure. In this context, real-time *HIL* simulation offers a technically robust and economically viable alternative. It enables closed-loop validation under realistic dynamic conditions, ensuring that both control algorithms and system behavior are accurately characterized without the limitations of physical prototyping at early development stages.

Beyond validating the steady-state and dynamic performance of the control system, the real-time *HIL* experiments also confirm the robustness of the converter's response to parameter variations and external disturbances. The ability to inject controlled transients, emulate load fluctuations, and modify environmental conditions (e.g., irradiance profiles) in a fully deterministic and repeatable manner is a key advantage of the *HIL* framework. Furthermore, the results obtained from the *OPAL-RT* platform closely match the expected theoretical behavior predicted by the analytical model, thereby reinforcing the consistency between the system-level design, control strategy, and hardware implementation. This level of correlation substantiates the applicability of the proposed architecture to practical photovoltaic systems with high reliability and minimal design uncertainty.

Finally, Figure 23 shows the sliding surface obtained in the real-time implementation, verifying the correct operation of the sliding mode control in the *FPGA*-based environment.

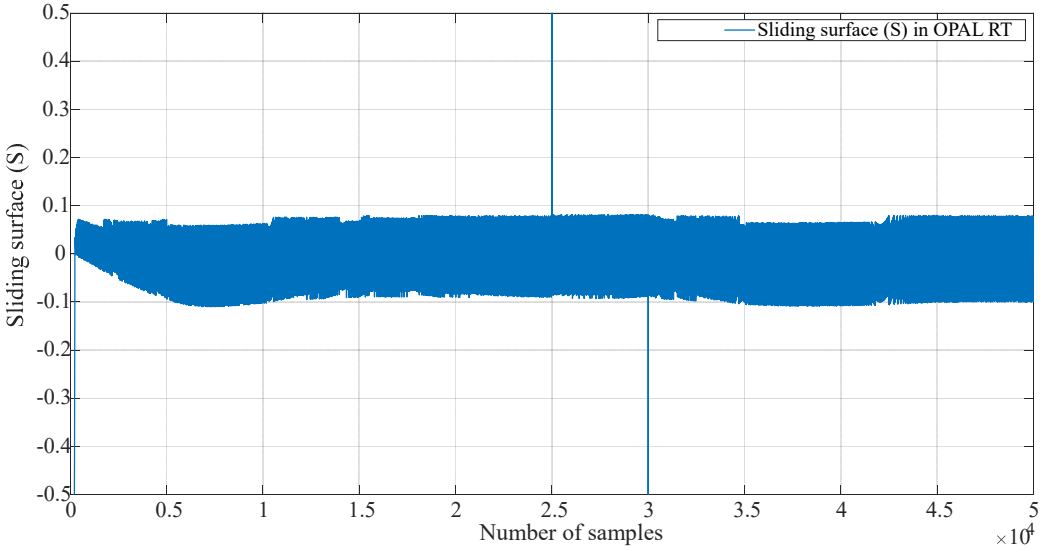


Figure 23. Sliding surface signal (S) obtained during *OPAL-RT* real-time validation. The sliding variable remains bounded and centered around zero throughout the operation, confirming correct behavior of the current-mode sliding control under dynamic conditions.

The simulation and real-time results demonstrate the accuracy, robustness, and hardware feasibility of the proposed control architecture, confirming its suitability for partial-power converter applications in dynamic environments. The following section summarizes the main findings and outlines the conclusions of this study.

5.3. Comparative Analysis with Recent Works

To evaluate the relevance and competitiveness of the proposed partial-power converter system, a comparative analysis is conducted against recent contributions in converter architectures based on partial-power processing (PPP). The goal is to assess the proposed design in terms of efficiency, control robustness, implementation feasibility, and suitability for PV systems.

Table 6 provides a structured overview of relevant works published in the last few years, highlighting key parameters, such as converter topology, energy efficiency, estimated processed power ratio (k_{PR}), conversion characteristics, isolation, application domain, and primary innovations. The concept of Partial-Power Processing (PPP) has gained substantial attention due to its potential to increase global system efficiency by reducing the portion of energy processed through active converter stages. Unlike full-power converters, which handle the entire power flow, PPP architectures operate by interconnecting the load in series or parallel with the energy source, thus allowing part of the power to bypass the

converter via a passive path. This design strategy enables notable reductions in conduction losses, magnetic component sizing, and thermal stress, which are especially beneficial in high-efficiency, space-constrained, or cost-sensitive applications.

Table 6. Comparative table of recent partial-power converter architectures.

Author (Year)	Topology	Efficiency (%)	k_{PR} (Estimated)	Conversion Type	Isolated	Application Domain	Innovation/Focus
Iyer et al. (2021) [15]	Phase-Shifted Full-Bridge (PSFB)	Up to 98.4	0.27	step-down	Yes	EV Extreme Fast Charging	Reduced converter rating
Liu et al. (2022) [25]	Bidirectional Step-Up/Down with Transformer	>99.5	0.22	step-up/down	Yes	SOEC Systems	Transformer decoupling, high peak efficiency
Wu et al. (2024) [20]	2-Phase Buck-Boost (IPOS/ISOP)	>98.0	0.35	step-up/down	No	Data Centers	Topology selection + hybrid ZVS
Anzola et al. (2024) [17]	Dual Active Bridge (DAB)	≈99.0	0.25–0.4	Bidirectional step-up/down	Yes	On-Board EV Charger	Si-based PPP competitive with SiC
Artal-Sevil et al. (2022) [21]	Non-Isolated Ćuk (PPP)	>98.5	0.3–0.5	step-up/down	No	EV Auxiliary/Industrial	Comparative non-isolated PPP study
This Work	Non-Isolated Buck-Boost (IPOS)	97.5 (HIL)	0.18–0.4	step-up	No	PV Systems/Microgrids	PI–SMC control, HIL validation, low stress

As shown in Table 6, a wide range of converter topologies have been explored within the PPP framework, including both isolated (e.g., PSFB, DAB, and bidirectional transformer-based stages) and non-isolated implementations (e.g., buck-boost and Ćuk). Reported efficiencies often exceed 98%, with some systems achieving up to 99.5% under optimized conditions. However, such figures must be interpreted considering the corresponding power processing ratio (k_{PR}), which typically ranges from 0.2 to 0.5 in most cases. This parameter directly indicates the fraction of total power processed by the converter, with lower values implying improved energy utilization through the direct path.

Another relevant factor is the type of voltage conversion performed by the architecture. Most isolated designs support bidirectional or step-up/down conversion, providing flexibility for applications such as electric vehicle charging, electrolysis systems, or battery interfacing. Non-isolated topologies, while generally simpler, are typically constrained to unidirectional operation, but still offer sufficient performance for photovoltaic (PV) or industrial auxiliary applications.

In comparison to the reviewed architectures, the proposed system distinguishes itself by combining several advantageous features, as follows:

- It uses a non-isolated buck-boost IPOS configuration, which simplifies the design while maintaining step-up capability for PV integration;
- It achieves an estimated system efficiency of 98.25%, validated through both simulation and real-time Hardware-in-the-Loop (HIL) implementation on the OPAL-RT platform;
- The converter operates with a processed power ratio $k_{PR} \approx 0.18$–0.4, depending on duty cycle and load, thereby minimizing active-stage stress;
- A dual-loop control strategy combining Proportional–Integral (PI) voltage regulation and Sliding Mode Current Control (SMC) is implemented, offering robust performance under dynamic conditions and enhancing MPPT compatibility;
- Given that $k_{PR} \approx 0.2$–0.4, the power stage components can be sized to handle only 20–40% of the total power, resulting in a proportional reduction in magnetic volume and switch rating.

In summary, while many works in the literature demonstrate high efficiency or advanced topological features, few combine those aspects with real-time validation and a scalable, low-complexity control approach. The proposed converter, therefore, contributes

a practical and experimentally supported alternative for distributed PV systems and DC microgrids, bridging the gap between theoretical efficiency and real-world applicability.

In contrast to intelligent or adaptive control schemes requiring extensive computation or parameter tuning, the PI–SMC implementation offers a low-complexity yet high-performance alternative compatible with real-time embedded systems.

Despite the demonstrated advantages of the proposed architecture, several design limitations must be acknowledged. First, the control system exhibits increased sensitivity as the duty cycle approaches unity, where small perturbations in modulation may lead to large variations in output voltage and power transfer, thus requiring high-resolution control and robust stability margins. Second, the inherent structure of the IPOS configuration imposes constraints on the achievable voltage gain, particularly in applications requiring wide dynamic range or deep step-up conversion. Finally, while Sliding Mode Control (SMC) provides excellent robustness, it may introduce high-frequency chattering in the control signal, which can lead to increased switching losses or Electromagnetic Interference (EMI). This issue can be mitigated through the incorporation of boundary layer approximations or hysteresis modulation strategies. These trade-offs should be carefully considered in practical implementations and guide future refinements in both topology and control design.

6. Discussion and Conclusions

The increasing penetration of photovoltaic (PV) systems into the global energy mix necessitates the development of more efficient power conditioning systems. This paper introduces a novel partial-power converter architecture designed for renewable energy applications, particularly photovoltaic systems, where the aim is to improve energy conversion efficiency while reducing component stress and system size.

A dual-loop control strategy combining a *PI* voltage controller and a *Sliding Mode Current Controller* (*SMC*) has been proposed to achieve optimal performance under dynamic conditions. Through *MATLAB-Simulink* simulations and real-time implementation using the *OPAL-RT* platform, the results confirm the effectiveness of the proposed system. Some advantages of the partial-power converter include the following:

- Improved Efficiency: the converter processes only a fraction of the total power, which reduces conduction and switching losses, thus increasing overall system efficiency compared to traditional full-power converters;
- Reduced Thermal Stress: by minimizing the power processed by the converter, the thermal load on power components is significantly lower, enhancing system reliability and lifespan;
- Compactness and Cost Reduction: the reduced component ratings allow for smaller inductors and capacitors, lowering system cost—particularly valuable in cost-sensitive PV and storage applications.

Nevertheless, some limitations must be addressed. The control becomes increasingly sensitive as the duty cycle approaches unity, and the inherent structure of PPP architectures imposes constraints on the achievable voltage gain range. These aspects require careful consideration during design and implementation to ensure reliable system operation.

In conclusion, the partial-power converter architecture, combined with advanced control strategies, offers a promising and efficient alternative to conventional full-power converters for renewable energy applications. Future research will focus on improving dynamic performance through adaptive or intelligent control methods, exploring the integration with *MPPT* algorithms, and evaluating performance in modular and multilevel configurations to further increase versatility and application scope.

The results presented confirm the potential of partial-power converter architectures as a scalable and high-efficiency solution for distributed photovoltaic systems. In addition to the demonstrated performance under nominal operating conditions, future investigations should address the long-term reliability and durability of such systems, particularly when deployed in complex and dynamically reconfigurable microgrid environments. Moreover, the modular nature of the proposed architecture opens promising avenues for adaptive reconfiguration and fault-tolerant operation, which are essential features in next-generation smart energy networks. The integration of machine learning techniques for real-time control adaptation, predictive maintenance, or MPPT optimization under highly variable conditions constitutes a logical and impactful extension of this research line.

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Nomenclature

v_{pv}	Voltage of the photovoltaic array
i_{pv}	Current of the photovoltaic array
C_1	Capacitor 1 for PV system, μF
L_1, L_2	Inductor of the partial-power converter, μH
u	Sliding mode control signal of the boost stage (1,0)
D	Diode
C_2	Capacitor 2 of the boost stage, μF
R	Load resistance, Ω
v_{OC}	Open-circuit voltage, V
i_{SC}	Short-circuit current, A
R_s	Series resistance, Ω
v_t	Thermal stress, V
$s(t)$	Sliding surface
δ	Positive number (>0)
k_p	Proportional gain
k_i	Integral gain
Ppv	Rated power by PV module
Ns	Series modules per string
N_p	Parallel strings, Np

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