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A High-Efficiency GaN-on-Si Power Amplifier Using a Rapid Dual-Objective Optimization Method for 5G FR2 Applications

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Abstract

A broadband, efficient monolithic microwave integrated circuit power amplifier (MMIC PA) in OMMIC's 0.1 μm GaN-on-Si technology for 5G millimeter-wave communication is presented. This study concentrates on the output matching design, which has an important influence on the PA's performance. A compact one-order synthesized transformer network (STN) is adopted to match the 50 Ω load to the extracted large-signal output model of the transistor. A dual-objective strategy is developed for parameter optimization, incorporating the impedance transformation trajectory inside the predefined optimal impedance domain (OID) that satisfies the required specifications, with approximation to selected optimal load impedances. By introducing a custom adjustment factor β into the error function, coupled with an automated iterative tuning process based on S-parameter simulations, desired broadband matching results can be rapidly achieved. The proposed two-stage PA occupies a small chip area of only 1.23 mm² and demonstrates good frequency consistency over the 24–31 GHz band. Continuous-wave characterization shows a flat small-signal gain of 19.7 ± 0.5 dB; both the output power (P_{out}) and the power-added efficiency (PAE) at the 4 dB compression point remain smooth, ranging from 32.3 to 32.7 dBm and 35.5% to 37.8%, respectively. The peak PAE reaches up to nearly 40% at the center frequency.

Keywords: 5G millimeter-wave; broadband power amplifier; GaN HEMT; high efficiency; optimal impedance domain; synthesized transformer network



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1. Introduction

5G has been extensively deployed worldwide and serves as fundamental infrastructure for digital transformation. It has now evolved into 5G-Advanced (5G-A), corresponding to Release 18 of the 3GPP technical specifications. Beyond ongoing network performance upgrades, Release 18 emphasizes further integration of the 5G ecosystem with non-terrestrial networks, aiming to achieve ubiquitous global cellular connectivity [1]. With growing adoption of the broadband internet services provided by commercial low-Earth-orbit (LEO) satellite constellations like Starlink and OneWeb, the convergence of satellite and terrestrial 5G networks is emerging as a significant trend that will play a crucial role in future space–air–ground integrated networks [2].

As a cornerstone of 5G-A and high-throughput satellite communication (SATCOM), millimeter-wave (mmWave) technology shows great promise for cutting-edge fields, owing to its distinctive features of a wide contiguous bandwidth, low latency, flexible deployment, and high-precision sensing. The 5G New Radio mmWave spectrum, known as Frequency Range 2 (FR2), extends from 24.25 GHz up to 71 GHz, covering the K to V bands. Despite its

many benefits, mmWave technology faces high-frequency-related problems, including severe path, penetration, and blockage losses [3]. Moreover, modern wireless systems impose stringent requirements on size, weight, power, and cost (SWaP-C), creating considerable challenges for designing mmWave front-end modules [4,5], particularly the power amplifier (PA), which directly affects signal quality, coverage, and energy consumption. Therefore, to address the ever-growing demand for data, support multiple communication standards, and ensure a high-quality user experience, the development of efficient mmWave PAs with a small footprint and a watt-level output power (P_{out}) over a wide bandwidth has become a key research focus.

The performance bottleneck for PAs is essentially dictated by the device technology. As a leading third-generation wide-bandgap semiconductor, gallium nitride (GaN) offers outstanding properties, including a high breakdown electric field, high saturation velocity, and good thermal conductivity. These inherent advantages enable GaN high-electron-mobility transistors (HEMTs) to achieve a better frequency response, operate at higher bias voltages, and sustain greater power densities [6]. Compared to silicon-based processes such as CMOS and SOI, which typically require transistor stacking to increase the voltage swing under the same current conditions [7,8], or gallium arsenide (GaAs) counterparts, which rely on bulky and lossy power-combining networks to attain comparable P_{out} [9,10], the adoption of GaN devices simplifies the circuit design and eases thermal management. These features make GaN PAs ideal for mmWave communication systems that demand compact, lightweight, and high-efficiency solutions [6,11–16].

In addition to device-level considerations, the pursuit of both broadband operation and high efficiency in PAs necessitates careful circuit design. Nevertheless, these two goals are often mutually restrictive. Ensuring broadband impedance matching and a flat frequency response may result in reduced efficiency over part of or even the entire operating band, whereas optimizing the matching network (MN) for peak efficiency at specific frequencies inevitably sacrifices bandwidth. Numerous studies have illustrated this inherent contradiction. For instance, distributed amplifiers utilize artificial transmission lines to absorb the parasitic capacitance of transistors, enabling a multi-octave bandwidth but at the expense of low gain, poor power-added efficiency (PAE), and large chip area [17]. Balanced amplifiers leverage a pair of quadrature couplers to cancel the reflections caused by mismatches at the circuit's input and output, thereby achieving an excellent broadband voltage standing wave ratio and stability, but they also incur a higher insertion loss, which degrades the PAE [5]. Others, comprising switch-mode PAs (Class E, F, F^{-1} , etc.) that rely on harmonic control or waveform shaping to minimize the overlap between the output voltage and current [18,19], as well as Doherty PAs that use a load modulation technique, have also been extensively researched [20]. Overall, taking all of the necessary trade-offs into account, the most cost-effective solution lies in the design and optimization of the MN. One category relates to a CAD-dependent numerical optimization methodology, with the simplified real-frequency technique (SRFT) as a notable example. The SRFT enables the construction of a broadband MN by optimizing the transducer power gain function based on acquired load data, without predefining any topology [21]. However, a robust and computationally expensive optimization algorithm ought to be employed in order to obtain the globally optimal solution. Another category belongs to mathematically synthesized networks derived from broadband matching theory [22–24]. While these approaches are straightforward to implement, they are constrained by the equivalent circuit model of the load, generate MNs with fixed or patterned topologies, and require the bandwidth, impedance transformation ratio (ITR), and ripple of the frequency response to be balanced during the design procedure [18,19,25].

This paper presents a 0.1 μm GaN-on-Si MMIC PA designed through a combination of analytical network synthesis and numerical optimization methods. Special attention is given to the output matching network (OMN), which employs a synthesized transformer network to absorb the transistor's output capacitance (C_{out}). A simple method is offered for selecting the optimal load impedance (Z_{opt}) that enables a favorable compromise between P_{out} and PAE. Furthermore, a dual-objective optimization strategy guided by impedance rather than performance metrics is developed, along with an error function incorporating a tunable factor β to manage matching quality across different frequencies. The proposed parameter optimization procedure operates efficiently, as it avoids the need for time-consuming harmonic balance (HB) simulations. The implemented two-stage PA exhibits consistent small- and large-signal characteristics across the 24–31 GHz band. The electromagnetic (EM) simulation outcomes are summarized and benchmarked against those from recent work.

2. A Rapid Output Matching Optimization Method with Dual-Objective Orientation

As the final stage of RF power transmission in a PA, the OMN plays a decisive role. The large-signal behavior of a transistor is sensitive to the load impedance, making precise OMN design essential to achieving the expected matching conditions. At mmWave frequencies, Z_{opt} shows pronounced frequency dependence due to the device's enhanced parasitic effects, primarily the nonlinear drain-source capacitance (C_{ds}), and is denoted as $Z_{\text{opt}}(f_i)$ at the frequency f_i . Additionally, the OMN transforms the standard 50 Ω load into the impedance $Z_{\text{omn}}(f_i)$, whose rotational trajectory on the Smith chart opposes that of $Z_{\text{opt}}(f_i)$. These two issues hinder the design of a broadband OMN, making point-by-point matching unfeasible, especially under complexity limitations. Thus, industry practice is to choose an appropriate OMN topology and fine-tune its component values to closely approach $Z_{\text{opt}}(f_i)$ with reasonable compromises in matching accuracy. This section details a rapid and automated parameter optimization method for the OMN, free of artificial intelligence algorithms.

2.1. Selection of the Optimal Load Impedance

The intended operating bandwidth (BW_o) is 24–30 GHz. To account for possible performance deviations due to process variations and inaccuracies in device modeling, the design bandwidth (BW_d) is defined by adding a 2 GHz margin to both the lower and upper boundaries of BW_o , thus providing sufficient frequency redundancy.

To guarantee the linear output capability of the PA, load-pull simulations were conducted on a stabilized $46 \times 8 \mu\text{m}$ power cell at the 1 dB compression point at six frequencies f_i ($i = 1$ to 6) spaced 2 GHz apart in the BW_d of 22–32 GHz. The obtained $Z_{\text{opt}}(f_i)$ for the maximum $P_{1\text{dB}}$ and PAE are denoted as $U_1(f_i)$ and $U_2(f_i)$, respectively, both of which are expressed in the complex impedance form, as given by Equations (1) and (2). Varying degrees of deviation between $U_1(f_i)$ and $U_2(f_i)$ exist at different frequencies. Selecting a target matching impedance $Z_{\text{opt},s}(f_i)$ closer to $U_1(f_i)$ favors a higher $P_{1\text{dB}}$ but moves further away from $U_2(f_i)$, resulting in a reduced PAE. Consequently, $Z_{\text{opt},s}(f_i)$ is generally chosen at an intermediate position between $U_1(f_i)$ and $U_2(f_i)$ to strike a balance between $P_{1\text{dB}}$ and PAE. To determine $Z_{\text{opt},s}(f_i)$, weighting coefficients m and n are assigned to the impedance points $U_1(f_i)$ and $U_2(f_i)$, respectively, with $m + n = 1$, as described by Equation (3). Since PAE exhibits greater fluctuations in response to mismatch than $P_{1\text{dB}}$, m and n are set to 1/3 and 2/3, respectively. The calculated values are listed in Table 1 and plotted in Figure 1a.

$$U_1(f_i) = R_1(f_i) + jX_1(f_i) \quad (1)$$

$$U_2(f_i) = R_2(f_i) + jX_2(f_i) \quad (2)$$

$$Z_{\text{opt},s}(f_i) = mU_1(f_i) + nU_2(f_i) = mR_1(f_i) + nR_2(f_i) + j[mX_1(f_i) + nX_2(f_i)] \quad (3)$$

Table 1. The optimal load impedances obtained via load-pull simulations and calculations.

f_i (GHz)	$U_1(f_i)$ (Ω)	$U_2(f_i)$ (Ω)	$Z_{\text{opt},s}(f_i)$ (Ω)
22	15.6 + j12.3	15.4 + j16.8	15.5 + j15.3
24	14.1 + j13.1	13.9 + j16.4	14.0 + j15.3
26	14.3 + j11.2	12.9 + j15.5	13.4 + j14.1
28	12.8 + j10.4	11.5 + j14.2	11.9 + j12.9
30	12.7 + j9.8	10.9 + j12.5	11.5 + j11.6
32	12.2 + j8.6	9.3 + j11.2	10.3 + j10.3

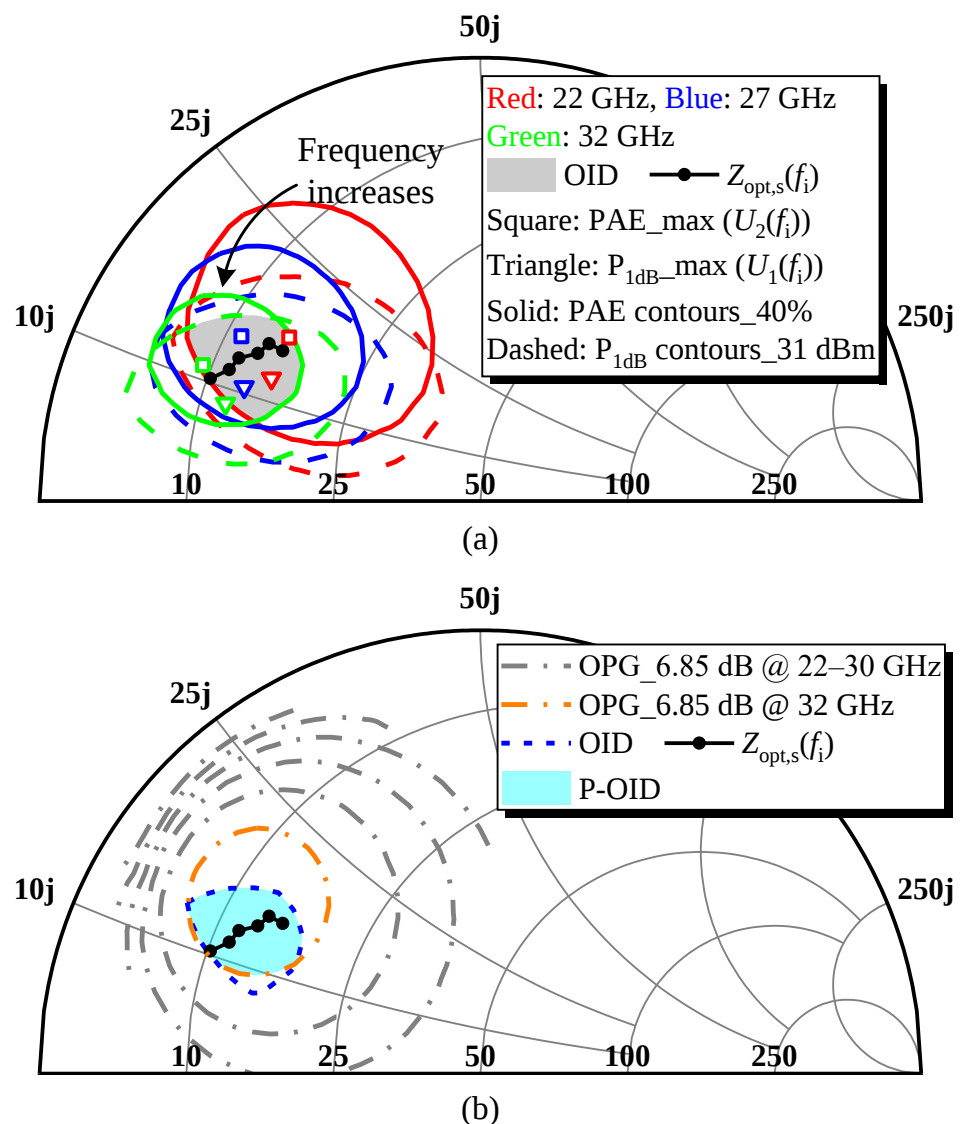


Figure 1. (a) Load-pull simulation results at the 1 dB compression point and the determination of OID; (b) OPG contours of 6.85 dB within the BW_d and the determination of P-OID.

2.2. Determination of the Optimal Impedance Domain

Subsequently, the optimal impedance domain (OID) is defined as the intersection region of the $P_{1\text{dB}}$ contour of 31 dBm and the PAE contour of 40%, as highlighted by the gray shading in Figure 1a. With an increasing frequency, the $P_{1\text{dB}}$ and PAE contours gradually shrink, and both rotate counterclockwise toward the real axis of the Smith chart,

reflecting the trajectory of $Z_{\text{opt}}(f_i)$. This trend indicates that the transistor's performance deteriorates at higher frequencies. Approximately two-thirds of the OID boundary is delineated by the contours at 32 GHz. The operating power gain (OPG) is also a key metric that should not be overlooked, as achieving the target gain with fewer amplification stages can greatly improve the overall PAE. As depicted in Figure 1b, a value of 6.85 dB is chosen for the OPG because the corresponding narrowest contour at 32 GHz and the OID together create a new overlap area that still contains every $Z_{\text{opt},s}(f_i)$, without significantly reducing the original OID, which is termed the preferred OID (P-OID). As long as all $Z_{\text{omn}}(f_i)$ across BW_d fall inside the P-OID, the transistor's large-signal output capability is assured, eliminating lengthy HB simulations. The OMN parameter optimization can then be focused on minimizing the offset between each $Z_{\text{omn}}(f_i)$ and $Z_{\text{opt},s}(f_i)$.

When the transistor enters the gain compression region, its transconductance g_m and C_{ds} exhibit strong nonlinearity. Therefore, based on the derived P-OID, two-tone load-pull simulations can be further performed to obtain the third-order intermodulation distortion (IMD3) contours, leading to a stricter definition of the OID and thus providing more comprehensive guidance for optimizing the parameters of the OMN. IMD3 is a major concern in linearity requirements because it lies near the operating frequencies and causes spectral regrowth. Assume that the two-tone excitation $v_{\text{in}}(t)$ is expressed as

$$v_{\text{in}}(t) = A \cos(\omega_1 t) + B \cos(\omega_2 t) \quad (4)$$

where A and B represent the amplitudes of two fundamental components. Neglecting memory effects and higher-order nonlinearities, the drain current equations for IMD3 frequencies are

$$I_d = I_{d0} + \sum_{k=1}^n g_{mk} V_{gs}^k \quad (5)$$

$$i_{(2\omega_1 - \omega_2)} = \frac{3}{4} g_{m3} A^2 B \cos[(2\omega_1 - \omega_2)t] \quad (6)$$

$$i_{(2\omega_2 - \omega_1)} = \frac{3}{4} g_{m3} A B^2 \cos[(2\omega_2 - \omega_1)t] \quad (7)$$

where I_d and I_{d0} represent the total drain current and the DC drain current, respectively, while V_{gs} denotes the RF voltage applied across the gate-source terminals. The parameter k indicates the nonlinear order, and g_{mk} is the k -th order transconductance. For every frequency component present at the device ports, g_{mk} values are associated with the load impedance, as they are defined by the combinations of the drain and gate voltages with the current during an RF swing [26]. Since g_{m3} is determined by the IMD3 products shown in Equations (6) and (7), the IMD3 value is also related to the load impedance [27]. Figure 2 depicts the IMD3 load-pull contours for a two-tone sinusoidal signal with a power level around the 1 dB compression point, a center frequency of f_i , and a 100 MHz tone spacing. As can be observed, the contours enclose a relatively wide impedance domain that extends into the lower half of the Smith chart and shifts toward the short-circuit point as the frequency increases. The IMD3 contour of -22 dBc at 32 GHz passes through $Z_{\text{opt},s}(f_i)$ with the maximum imaginary part, overlapping with the previously identified P-OID to form a strict OID (S-OID) constrained by four performance metrics.

Importantly, although the OID is progressively reduced by an increasing number of constraints, it is purposely maintained to encompass all $Z_{\text{opt},s}(f_i)$ to ensure the consistency and compatibility of the optimization objectives.

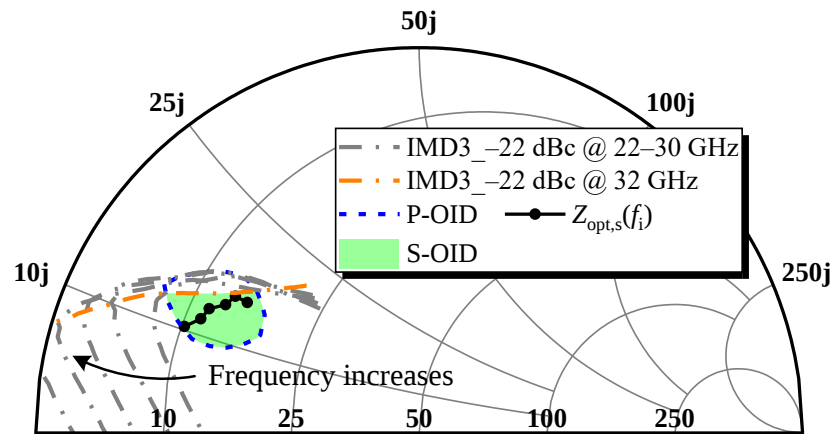


Figure 2. IMD3 load-pull contours and the determination of S-OID.

2.3. Verification of the Impedance Point Within the OID

The OID is essentially a closed polygon formed by connecting a series of discrete impedance points successively. To quickly determine whether the complex impedance $Z_{\text{omn}}(f_i)$ resides inside the predefined OID, the ray-casting algorithm is utilized, as it is well suited to both convex and concave polygons and offers high computational efficiency. It works by emitting a ray from the point of interest and counting the intersections with the polygon boundaries, applying the parity rule to distinguish between interior and exterior positions. Consider the OID as a non-self-intersecting closed polygon with V vertices on the real (X)–imaginary (Y) plane, with the vertex coordinates $\{(x_1, y_1), (x_2, y_2), \dots, (x_V, y_V)\}$, where $x_1 = x_V$ and $y_1 = y_V$ to ensure closure. The point under investigation, $Z_{\text{omn}}(f_i)$, has the coordinates $(x_{\text{omn}}, y_{\text{omn}})$. To facilitate computation, the ray is emitted horizontally towards the positive X-axis. The specific identification steps are as follows:

Step 1: Traverse all edges of the polygon

Each edge of the polygon is traversed in sequence to check for intersection with the horizontal ray. In particular, edges whose endpoints have the same imaginary value (horizontal edges) are disregarded to prevent miscounting caused by coinciding with the ray.

Step 2: Check whether the range of the edge's imaginary part covers y_{omn}

An edge is considered for intersection only when y_{omn} of the test point lies within the range of the edge's imaginary part; that is, $\min(y_a, y_{a+1}) \leq y_{\text{omn}} \leq \max(y_a, y_{a+1})$. If the condition is not fulfilled, skip this edge.

Step 3: Compute the X-coordinate where the horizontal ray intersects with the edge

The parametric equation for the edge can be expressed as Equation (8). Substituting the ray formula $y = y_{\text{omn}}$ yields the parameter t , as shown in Equation (9). If $t \in (0, 1)$, the intersection exists on the edge, with the X-coordinate given by $x_{\text{cr}} = x_a + t(x_{a+1} - x_a)$. Only when $x_{\text{cr}} \geq x_{\text{omn}}$ is this intersection counted, confirming it is situated to the right of the test point.

$$\begin{cases} x = x_a + t(x_{a+1} - x_a) \\ y = y_a + t(y_{a+1} - y_a) \end{cases} \quad (8)$$

$$t = \frac{y_{\text{omn}} - y_a}{y_{a+1} - y_a} \quad (9)$$

Step 4: Count the total number of intersections

After iterating through all polygon edges, the sum of valid intersections is computed, and its parity is examined. An odd total indicates that $Z_{\text{omn}}(f_i)$ is located inside the OID; otherwise, it is outside the domain.

In cases where $Z_{\text{omn}}(f_i)$ lies exactly on an edge or a vertex of the polygon, the determination mechanism classifies it as being inside the OID. Notably, if the ray passes through a polygon vertex, the intersection is counted for only one of the adjacent edges to avoid duplication.

2.4. Error Function Formulation

As the S-OID results from compressing the upper space of the P-OID further, which itself is derived by removing a portion of the lower region from the OID, the set of $Z_{\text{omn}}(f_i)$ over the BW_d may not entirely fall inside the smaller S-OID or simultaneously approach the respective $Z_{\text{opt},s}(f_i)$ under a given OMN topology. To optimize the OMN parameters for these two objectives while considering practical constraints, an error function Err is proposed, which comprises an out-of-domain penalty term and a weighted matching error term, defined in three parts:

(1) The out-of-domain penalty

The BW_d is known to consist of the BW_o and a redundant bandwidth of 4 GHz in total. As a hard constraint, all $Z_{\text{omn}}(f_i)$ within the BW_o must be inside the S-OID; otherwise, the total error (E_{tol}) is instantly assigned an upper bound of 1 ($0 \leq E_{\text{tol}} \leq 1$). In contrast, for redundant bands, deviations in $Z_{\text{omn}}(f_i)$ from the S-OID are allowed, but each outlying impedance point incurs a penalty K to E_{tol} . The sum of these penalties cannot exceed 10% of E_{tol} (i.e., 0.1). If there are Q impedance points under consideration in redundant bands, and P of them fall outside the S-OID, then $K = 0.1/Q$, yielding a total out-of-domain penalty of KP .

(2) The matching error

The objective is to minimize the distance between $Z_{\text{omn}}(f_i)$ and $Z_{\text{opt},s}(f_i)$, as a smaller distance indicates better impedance matching. The matching error is therefore modeled as the Euclidean distance $d(f_i)$ in the complex plane, calculated according to Equation (10), and is normalized by the maximum value among all $d(f_i)$. The weighted sum of normalized matching errors is given a coefficient of 0.9 in E_{tol} , maintaining E_{tol} within the $[0, 1]$ interval.

$$d(f_i) = |Z_{\text{omn}}(f_i) - Z_{\text{opt},s}(f_i)| \quad (10)$$

(3) Weight allocation

Because the large-signal characteristics of transistors deteriorate as the frequency increases, the matching accuracy at higher frequencies is given greater priority by increasing the matching error weight W_i with respect to f_i . In this context, a frequency-dependent weighting scheme is introduced. By evaluating $P_{1\text{dB}}$, PAE, and OPG at six equally spaced frequencies over BW_d under the condition that the load of the final-stage transistor is set to $Z_{\text{opt},s}(f_i)$, it is found that the PAE is most sensitive to frequency. Let $\eta(f_i)$ represent the PAE at f_i , with the maximum among these values denoted as η_{max} . The definition of W_i is provided in Equation (11), where the adjustment factor β controls the extent of the weight difference between low and high frequencies. Empirically, a recommended range for β is $[0.1, 0.3]$. The normalized form of the weights, w_i , is obtained according to Equation (12). In conjunction with the HB simulation outcomes at the 1 dB compression point, the values of w_i for $\beta = 0.1$ are listed in Table 2.

$$W_i = e^{\beta[\eta_{\text{max}} - \eta(f_i)]} \quad (11)$$

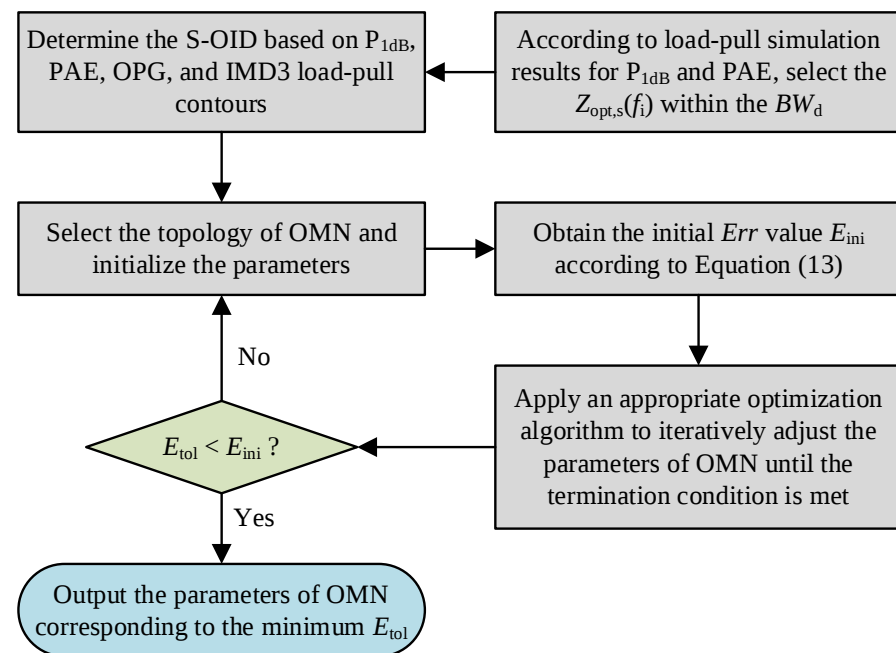
$$w_i = \frac{W_i}{\sum_{i=1}^N W_i} \quad (12)$$

Table 2. Weight allocation for matching error based on PAE differences.

f_i (GHz)	$Z_{\text{opt},s}(f_i)$ (Ω)	PAE (%)	w_i
22	$15.5 + j15.3$	54.02	0.115
24	$14.0 + j15.3$	52.58	0.133
26	$13.4 + j14.1$	51.34	0.151
28	$11.9 + j12.9$	50.03	0.172
30	$11.5 + j11.6$	48.73	0.196
32	$10.3 + j10.3$	46.97	0.234

In conclusion, the complete formulation of Err is given in Equation (13). Lastly, a suitable optimization algorithm, such as particle swarm optimization (PSO), differential evolution, or simulated annealing, is employed to iteratively tune the component values of the OMN so as to minimize E_{tol} . If E_{tol} remains at its initial value E_{ini} or consistently equals 1 during the optimization, this implies that the current OMN topology is inadequate and requires modification or increased complexity. If E_{tol} improves and the optimization meets the termination criteria, such as convergence, a predefined number of iterations, or a time limit, the OMN parameters yielding the minimum E_{tol} are recorded as the final output. The overall optimization procedure is illustrated in Figure 3.

$$Err = \begin{cases} 1, & \exists f_i \in BW_o : Z_{\text{omn}}(f_i) \notin \text{S-OID} \\ 0.1 \times \frac{P}{Q} + 0.9 \times \sum_{i=1}^6 w_i \frac{d(f_i)}{\max[d(f_i)]}, & \forall f_i \in BW_o : Z_{\text{omn}}(f_i) \in \text{S-OID} \end{cases} \quad (13)$$

**Figure 3.** A flowchart of the parameter optimization method for the OMN.

3. Broadband PA Implementation

According to the design specifications, process characteristics, and simulation evaluation, a cascaded two-stage common-source amplifier architecture is adopted, with a device periphery ratio of 1:2 to guarantee a sufficient driving capability. All transistors operate in class AB mode, biased at the recommended gate and drain voltages of -1 V and 12 V, respectively, to achieve a compromise between efficiency and linearity while preserving

high-frequency gain. In addition, an appropriate parallel RC network is connected in series at the gate of each transistor, which not only enhances the in-band stability and suppresses parasitic oscillations but also compensates for the gain roll-off to help extend the bandwidth of the PA and facilitates input impedance adjustments for improved matching with the preceding stage, thereby lowering the reflection coefficient. Based on load-pull simulations, C_{out} of the transistors in the power stage and the driver stage is extracted as 0.27 pF and 0.13 pF, respectively, with the corresponding optimal intrinsic load (R_{opt}) determined to be 26 Ω and 75 Ω [16]. Using the Bode–Fano criterion, the theoretical bandwidth limit can thus be derived. This section will mainly discuss the design of broadband MNs.

3.1. The Synthesized Transformer Output Matching Network

A large-signal output model of the transistor can be approximated using a parallel $R_{opt}C_{out}$ network, where C_{out} is the main contributor to the frequency-dependent nature of $Z_{opt}(f_i)$ and is the key limitation on the bandwidth. To mitigate this, a synthesized transformer matching technique is applied to absorbing C_{out} into the OMN [28,29]. This method not only eliminates the need for extra compensation components but also leverages C_{out} as a beneficial element, resulting in a simpler MN, a lower insertion loss, and improved broadband matching.

The synthesized transformer network (STN) originates from a magnetic coupling resonance model, illustrated in Figure 4a, where both LC resonators resonate at the same angular frequency ω_0 . The transformer, with an ITR of T and mutual inductance M , can be equivalently represented as the T-type inductor network described in Figure 4b, where M is determined by the coupling coefficient k . By setting the terminal resistances of the STN to R_{opt} and R_L and assigning C_2 to C_{out} , the following relationships are obtained:

$$T = \frac{R_L}{R_{opt}} = \frac{L_1}{L_2} = \frac{C_{out}}{C_1} \quad (14)$$

$$M = k\sqrt{L_1L_2} \quad (15)$$

$$\omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_{out}} \quad (16)$$

$$\begin{cases} L_1 - M > 0 \\ L_2 - M > 0 \end{cases} \quad (17)$$

Taking the red dashed plane outlined in Figure 4b as the reference boundary, the admittances seen from both sides of the plane are made conjugate, as expressed in Equation (18), where $Y_L = 1/R_L$. This condition enables the maximum power transfer. By substituting Equations (14)–(16) into Equation (18) and performing algebraic manipulation, the lower and upper resonance frequencies (f_L and f_H) of the STN can be derived, as given by Equations (19) and (20), where $Q_d = 1/(\omega_0 R_{opt} C_{out})$.

$$Y_A = \left(\frac{1}{R_{opt}} \right) = Y_A^* = Y_B = j\omega C_{out} + \frac{1 - \omega^2 L_1 C_1 + j\omega L_1 Y_L}{j\omega L_2 - \omega^2(j\omega C_1 + Y_L)(L_1 L_2 - M^2)} \quad (18)$$

$$f_L = \frac{\omega_0}{2\pi} \sqrt{\frac{-Q_d^2 + Q_d^2 k^2 + 2 - \sqrt{[Q_d^2(1 - k^2) - 2]^2 - 4(1 - k^2)}}{2(1 - k^2)}} \quad (19)$$

$$f_H = \frac{\omega_0}{2\pi} \sqrt{\frac{-Q_d^2 + Q_d^2 k^2 + 2 + \sqrt{[Q_d^2(1 - k^2) - 2]^2 - 4(1 - k^2)}}{2(1 - k^2)}} \quad (20)$$

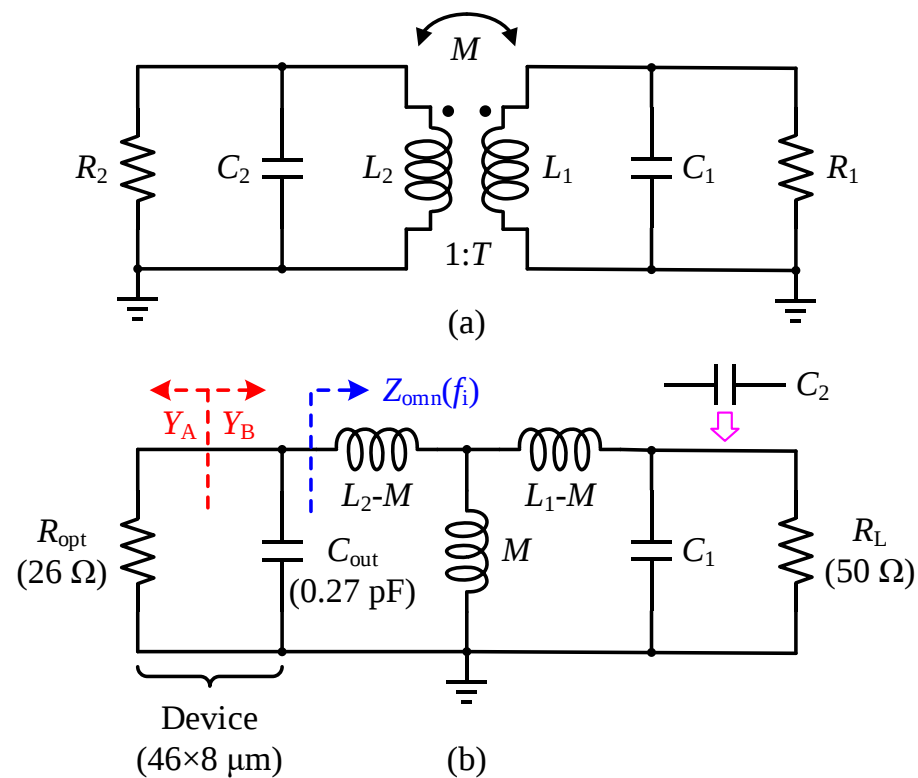


Figure 4. STN: (a) magnetic coupling resonance model; (b) equivalent T-network.

Assigning f_L and f_H to the lower and upper edge frequencies of the BW_d ($f_{min} = 22$ GHz, $f_{max} = 32$ GHz) and using the known design parameters (R_L , R_{opt} , and C_{out}), together with the relevant derived equations, the remaining component values in the STN can be solved. The results comply with the physical implementation condition described in Equation (17). Subsequently, f_L and f_H are simultaneously moved toward the center frequency f_c (27 GHz) in small steps of 0.05 GHz, with the STN parameters updated in tandem. The iteration proceeds until the S_{11} of the STN at f_{min} , f_c , and f_{max} becomes equal. The STN parameters before and after the adjustment of the resonance frequencies are summarized in Table 3. The comparison curves in Figure 5 reveal that the STN provides the optimal S_{11} response at f_L and f_H , and a larger separation between the two resonance frequencies results in a more pronounced upward curvature in the central part of the curve, with its peak appearing at f_c . Therefore, to minimize the reflected energy, the resonance frequencies are adjusted closer together so that S_{11} stays below -27 dB throughout the BW_d .

Table 3. The parameters of the STN.

	R_{opt}	C_{out}	L_2-M	M	L_1-M	C_1	R_L
Initial	26 Ω	0.27 pF	0.9 pH	190.47 pH	177.56 pH	0.14 pF	50 Ω
Adjusted	26 Ω	0.27 pF	6.19 pH	176.35 pH	174.69 pH	0.14 pF	50 Ω

To complete the OMN topology, a DC-blocking capacitor C_2 with an initial value of 2 pF was added to the adjusted STN, as depicted in Figure 4b, with the inductor M serving as the drain bias line. In the end, optimization of the OMN's parameters was carried out by applying the aforementioned rapid dual-objective optimization method combined with the PSO algorithm, leading to a notable reduction in the final E_{tol} to 0.3, compared to the E_{ini} of 0.73. Figure 6 shows the trajectory of $Z_{omn}(f_i)$, where only at 22 GHz does the transformed impedance fall outside the S-OID, while at mid and high frequencies,

$Z_{\text{omn}}(f_i)$ closely matches the respective $Z_{\text{opt},s}(f_i)$. Although the deviation between $Z_{\text{omn}}(f_i)$ and $Z_{\text{opt},s}(f_i)$ is somewhat greater at lower frequencies, $Z_{\text{omn}}(f_i)$ remains within the P-OID. Such a deliberate matching strategy ensures compliance with large-signal performance requirements over the BW_d and a flat frequency response.

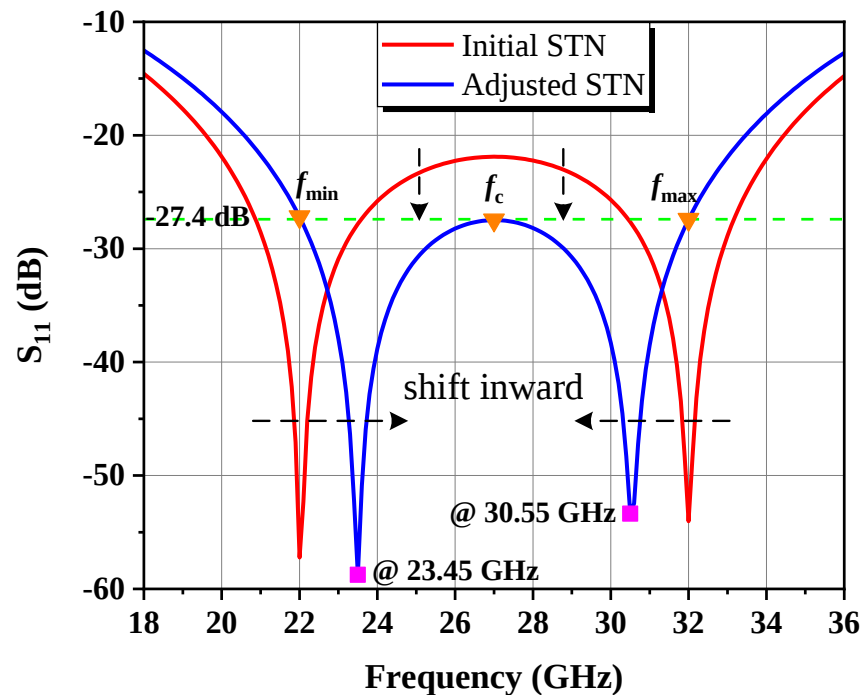


Figure 5. Reflection coefficients of the initial and adjusted STN.

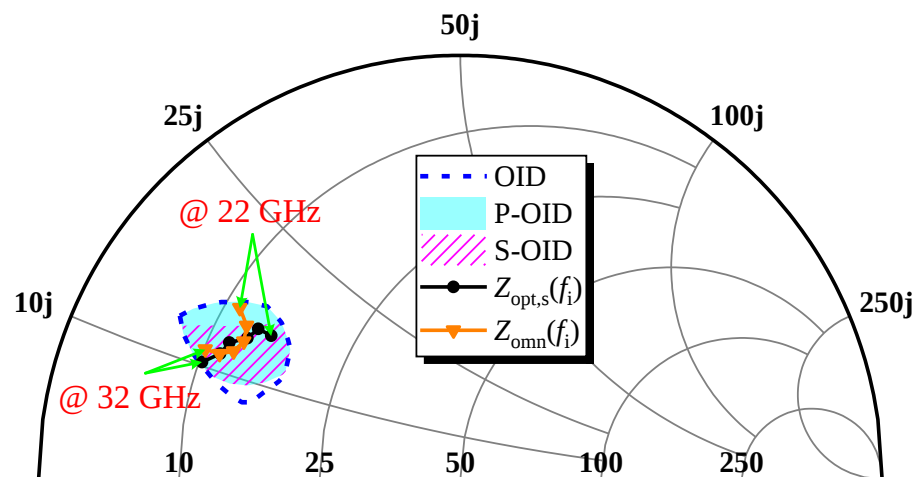


Figure 6. The transformation features of the optimized OMN from 22 to 32 GHz.

3.2. Interstage and Input Matching Network Design

After replacing the OMN and the gate-side parallel RC stabilization network with their respective EM models, a $46 \times 8 \mu\text{m}$ cell was added to perform source-pull simulations for the maximum PAE. The distribution of the resulting optimal source impedance can be characterized as a series RLC circuit, which serves as one end of the interstage matching network (ISMN), while the other end corresponds to the large-signal output equivalent circuit of a $46 \times 4 \mu\text{m}$ cell, which is represented by the parallel $R_{\text{opt}}C_{\text{out}}$ network. Although the STN can be extended to higher-order configurations to introduce more resonance frequencies for broadband matching, its inherent topological characteristics render it unsuitable for an asymmetric ISMN. To determine the topology and component values of

the broadband ISMN, a parametric matching technique based on generalized parallel and series LC units is adopted, wherein the reactance of each series or parallel inductor L or capacitor C is correlated with the phase angle of its reflection coefficient, thereby mapping all possible values of L and C onto a finite and continuous open interval of radians $(-\pi, \pi)$ [10]. Such a mapping facilitates the use of CAD tools to swiftly search for the optimal parameter combinations and overcome convergence difficulties, with the optimization objectives set analogously to those in the OMN case. As for the input matching network (IMN), its primary target is to achieve conjugate matching between the transistor's input impedance and the $50\ \Omega$ source to minimize the input reflection. Equally, it should also be capable of assisting in optimizing the gain flatness of the cascaded PA. Since the real part of the small-signal input impedance, as seen from the input side of the stabilized driver-stage transistor, shows little variation, while the imaginary part can be modeled as a series LC circuit, the design of the IMN is accomplished using an analytical approach based on a Chebyshev prototype network and the closed-form solutions supplied in [23].

A schematic of the final PA and its corresponding layout, which passed the design rule check, are shown in Figures 7 and 8, respectively. To minimize the chip area, narrow microstrip lines with widths of $15\ \mu\text{m}$ for the OMN and $10\ \mu\text{m}$ for the other sections were employed. Additionally, the same type of bias supply is provided to both stages through a common square pad, with inductors incorporated to suppress potential signal crosstalk. On-chip bypass capacitors were placed near the power supply pads to mitigate unwanted signal interference and improve the circuit's stability. To reduce mutual coupling, the spacing between parallel microstrip lines was maintained at a minimum of three times the line width. Furthermore, all bends in the matching microstrip lines were implemented with 45-degree angles to decrease signal reflections. Specifically, double-layer metal was applied to the OMN and the drain bias lines of both stages to enhance the current-carrying capability and reduce the power dissipation and thermal issues caused by ohmic losses. The overall circuit dimensions are $1.4 \times 0.88\ \text{mm}^2$.

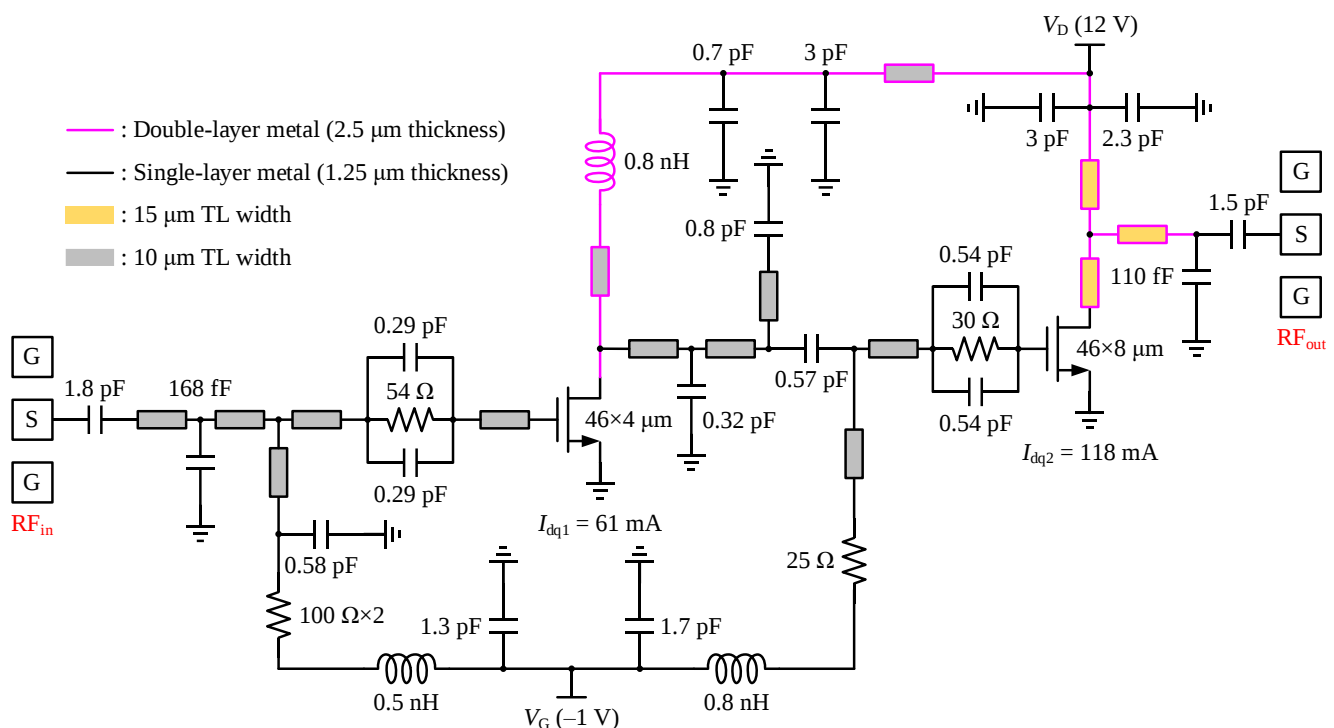


Figure 7. A schematic diagram of the two-stage PA.

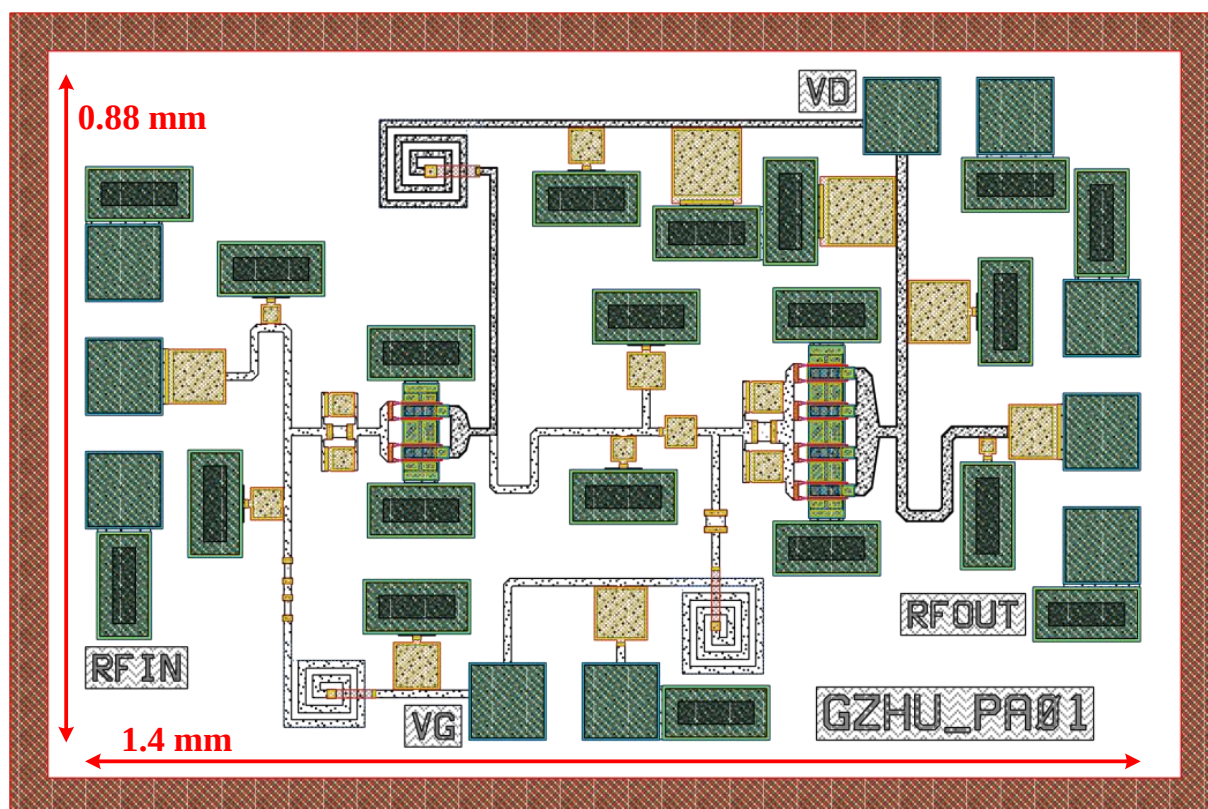


Figure 8. The complete layout of the GaN MMIC PA.

4. Simulation Results

The passive components of the layout, excluding the dicing streets, were simulated using ADS Momentum (a 2.5D planar EM simulator) with a mesh density of 50 cells per wavelength over the DC–100 GHz frequency range. The generated EM model was then integrated with active device library models for circuit–field co-simulation. After rigorous stability verification, the developed PA’s performance was assessed in continuous-wave (CW) mode.

4.1. Small-Signal Characterization

As plotted in Figure 9, S_{21} varies smoothly from 19.2 to 20.2 dB across 24–31 GHz at room temperature, with a maximum at 25.3 GHz and rapid out-of-band attenuation. Within the same band, S_{11} and S_{22} are below -10 dB and -16.7 dB, respectively, each displaying two distinct notches, demonstrating broadband input and output matching characteristics. The fact that the S_{22} curve exhibits a much deeper notch at 31.4 GHz than that at 25.4 GHz is a direct result of the OMN design strategy, which emphasizes improved high-frequency matching while intentionally introducing some mismatch at lower frequencies to flatten the in-band response. Moreover, S_{21} declines by no more than 1.2 dB as the temperature rises, with negligible in-band ripple, indicating that the PA maintains a stable small-signal gain across varying temperatures. Although S_{22} is slightly more susceptible to temperature changes compared to S_{11} , both remain within acceptable tolerance levels.

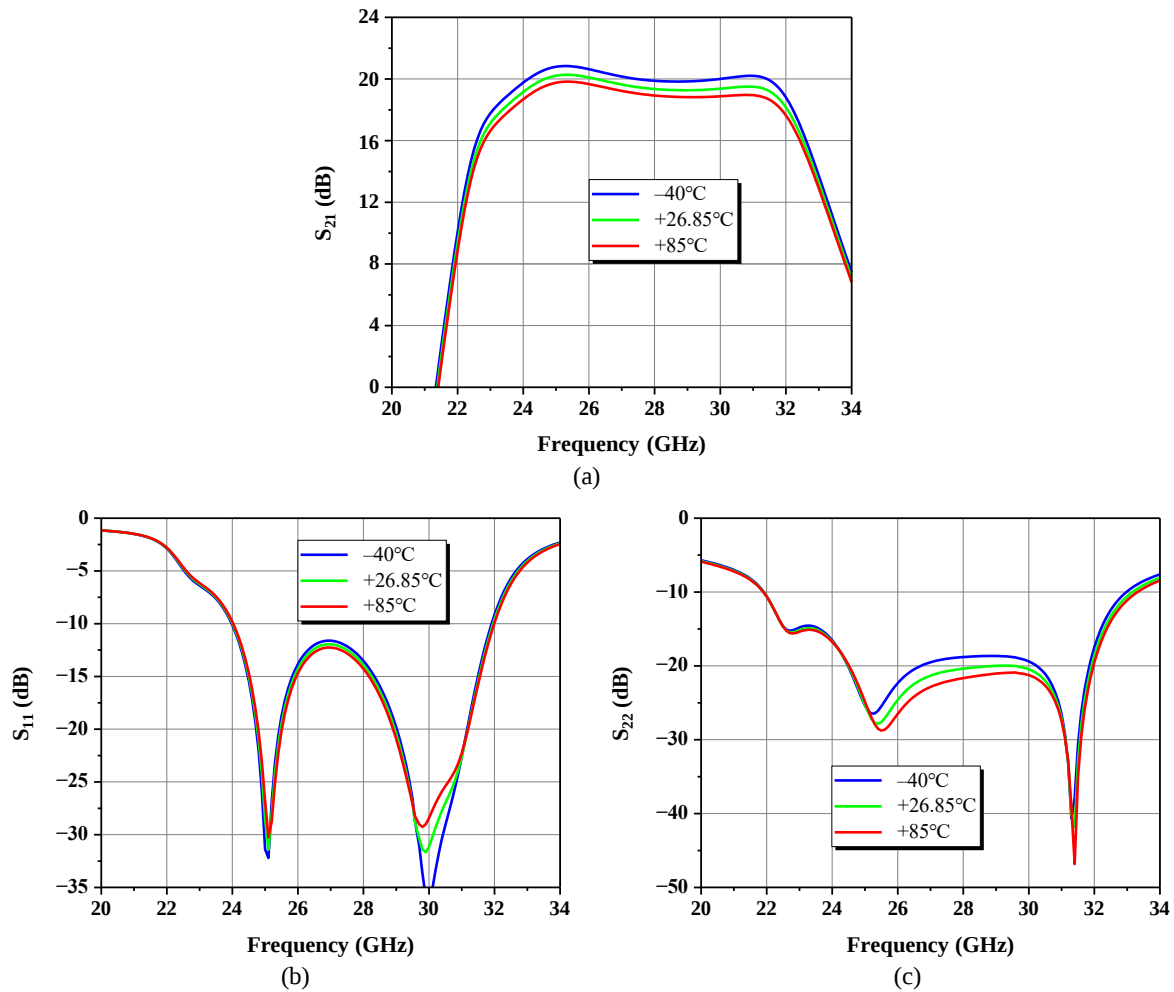


Figure 9. The simulated (a) S_{21} , (b) S_{11} , and (c) S_{22} at different temperatures.

4.2. Large-Signal Characterization

Figure 10a demonstrates that P_{1dB} lies between 30.5 dBm and 31.8 dBm, peaking at 27 GHz, with the corresponding PAE ranging from 31.3% to 37.6% over the 24–31 GHz band. Both of them follow the trend of higher values near the band center and lower values at the band edges. By contrast, P_{4dB} exceeds 32.3 dBm, with a maximum in-band fluctuation of only 0.4 dB, and the associated PAE increases to a range of 35.5–37.8%. Figure 10b presents the power sweep characteristics of the PA, showing that the best performance is achieved at the center frequency, where the peak PAE approaches 40% at an input power (P_{in}) of 15 dBm, corresponding to P_{2dB} . The responses at low and high frequencies are similar, with the PA reaching a saturation state and the maximum PAE as P_{in} nears the 4 dB compression point.

Under the preset bias conditions, the quiescent current of the two-stage PA is 179 mA, as described in Figure 11a. The total DC consumption rises markedly as P_{out} increases beyond 25 dBm, especially in the saturation region, where it peaks at nearly 450 mA. Similar current profiles are obtained at the three representative frequencies, indicating consistent power consumption over the band of interest. Figure 11b displays the IMD3 performance of the PA under two-tone power sweep simulations at 24 GHz, 27.5 GHz, and 31 GHz. The best overall linearity occurs at the center frequency, where the single-tone P_{out} at an IMD3 of -25 dBc is about 25.6 dBm.

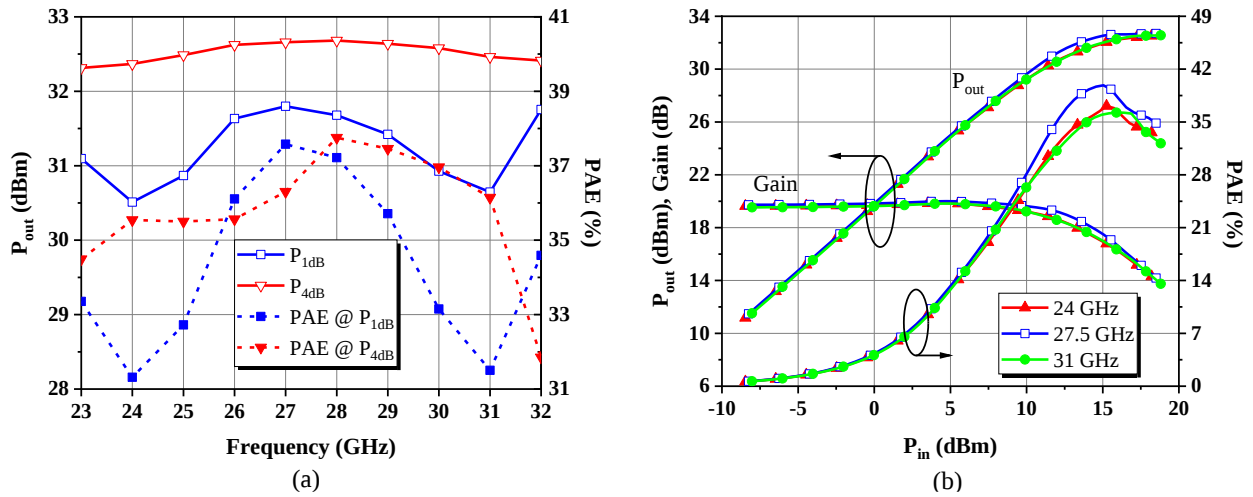


Figure 10. The simulated (a) P_{out} and PAE at 1 dB and 4 dB compression points; (b) P_{out} , PAE, and gain behaviors with respect to P_{in} .

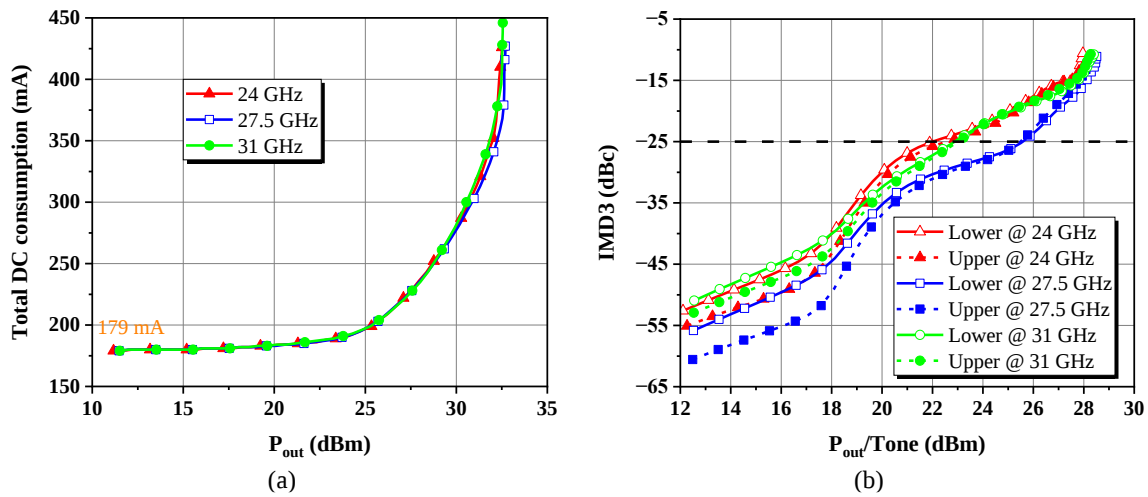


Figure 11. The simulated (a) total DC consumption versus P_{out} ; (b) two-tone power sweep with a 100 MHz frequency spacing.

Table 4 summarizes the performance of this work and compares it with recently reported GaAs and GaN PAs operating in similar frequency bands. To enable a comprehensive and relatively robust and fair assessment, a figure of merit (FoM) is introduced, which incorporates all of the parameters listed in the table and considers both high performance and consistency. The FoM is defined as follows:

$$FoM = \frac{FBW(\%) \times \overline{P_{out}}(W) \times \overline{PAE}(\%)}{Area(mm^2) \times V_{DD}(V) \times \prod_i \left(1 + \frac{\Delta x_i}{\bar{x}_i}\right)} \quad (21)$$

where FBW is the fractional bandwidth, V_{DD} denotes the supply voltage, and Δx_i and $\bar{x}_i$ refer to the in-band fluctuation and the mean of each metric (P_{out} , PAE, and gain), respectively. Note that the gain must be converted from its logarithmic ratio into a linear value before being used in calculations. In contrast to conventional FoM formulas, the cumulative multiplication term added to the denominator serves for evaluating the overall flatness of both large- and small-signal responses, while the use of the average rather than the maximum values for P_{out} and PAE in the numerator underscores the importance of a balanced broadband performance. The inclusion of the V_{DD} product term in the denomi-

nator improves the comparability among varying technologies and supply voltages. As evidenced in Table 4, the proposed mmWave PA demonstrates a superior FoM, achieving the smallest chip size and excellent frequency consistency under similar conditions, reflecting its advanced comprehensive performance.

Table 4. Performance summary and comparisons with contemporary works.

Ref.	[9]	[11]	[12]	[13]	[14]	[15]	This Work
Process	0.15 μm GaAs	0.15 μm GaN/SiC	0.15 μm GaN/SiC	0.1 μm GaN/Si	0.1 μm GaN/Si	0.1 μm GaN/Si	0.1 μm GaN/Si
BW. (GHz)	24–32	24.5–29	23–29.5	24–29	24–30	24–31	24–31
FBW (%)	28.6	16.8	24.8	18.9	22.2	25.5	25.5
Supply (V)	5	28	20	12	12	12	12
Gain (dB)	16.5 ± 0.5	11.5 ± 2.2	32.5 ± 2.5	20 ± 1.3	19.3 ± 1	25.5 ± 1.5	19.7 ± 0.5
P_{out} (dBm)	29 ± 0.6	29.8 ± 0.4	34.1 ± 0.8	30.7 ± 0.7	30.6 ± 0.5	34.3 ± 0.3	32.5 ± 0.2
PAE (%)	27–33 ^b	28.3–42.8 ^c	24.7–39.1 ^c	27.6–38.9 ^b	30.9–39.8 ^a	35.8–37.4 ^b	35.5–37.8 ^a
Size (mm^2)	2.4×1.1	2.1×1.3	3.4×1.9	2.2×1.3	1.65×0.78	3.25×1	1.4×0.88
FoM	41.8	4.4	10.8	15.8	45.7	61.3	104.3

^a PAE @ specific gain compression point. ^b PAE @ specific input drive. ^c peak PAE.

5. Conclusions

A mmWave PA features multiple critical performance metrics that are often mutually constrained, necessitating the OMN's design to achieve a balance among them, which is typically accomplished through effective parameter optimization. The conventional strategies usually optimize several large-signal targets directly, which demands resource-intensive HB simulations to assess the response for each OMN parameter set. Additionally, meticulous selection of the target thresholds is essential; otherwise, stringent requirements, excessive objectives, and complicated OMN topologies can easily lead to optimization stagnation or failure, thus hindering design progress. In contrast, the proposed rapid optimization method incorporates only two objectives: all $Z_{\text{omn}}(f_i)$ must fall inside the OID, and the deviation between $Z_{\text{omn}}(f_i)$ and $Z_{\text{opt},s}(f_i)$ should be minimized. The required large-signal specifications are first mapped to a set of desired impedances, i.e., the OID. Upon satisfying the basic output criteria, adjustments are deliberately made to the matching conditions with the corresponding $Z_{\text{opt},s}(f_i)$ at various frequencies, which facilitates the achievement of broadband and uniform output characteristics.

To conclude, the proposed dual-objective optimization strategy utilizes rapid S-parameter simulations to obtain the impedance transformation trajectory, thereby predicting the transistor's large-signal behavior. Although this method cannot provide precise performance evaluations or the specific deviation from the target, the considerable savings in the simulation time greatly benefit optimization tasks involving numerous iterations. Equally, acquiring detailed trial-and-error performance data is not necessary for the overall optimization effectiveness. Thanks to its high optimization efficiency and fully automated iterative process, the proposed method allows for a convenient assessment of the matching capabilities across various OMN topologies, significantly boosting both the design efficiency and success rate. For different terminal impedance model circuits, OMN, ISMN, and IMN, respectively, employ the synthesized transformer matching technique, the parametric matching technique, and a bandpass-filter-based matching structure to accomplish broadband impedance transformation with limited component usage.

The implemented two-stage PA occupies a compact footprint of 1.23 mm^2 and delivers a small-signal gain averaging 19.7 dB with less than 1 dB fluctuations over the 24–31 GHz band, exhibiting excellent broadband matching characteristics. Moreover, it demonstrates good temperature stability and features a flat $P_{4\text{dB}}$ of at least 32.3 dBm, along with a high

associated PAE, reaching a peak PAE close to 40%. The adoption of a silicon substrate process endows the GaN PA with significant cost effectiveness, making it well suited to mass production and compatible with mainstream CMOS fabrication technologies, thereby facilitating multifunctional and heterogeneous integration. As a result, the proposed MMIC PA not only meets the stringent SWaP-C requirements of millimeter-wave applications such as 5G-A wireless communications and SATCOM but is also ideal for highly integrated T/R-module front ends.

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Abbreviations

The following abbreviations are used in manuscript:

3GPP	Third-generation partnership project
5G	Fifth-generation mobile communication network
5G-A	5G-Advanced
ADS	Advanced design system
CAD	Computer-aided design
CMOS	Complementary metal oxide semiconductor
CW	Continuous-wave
EM	Electromagnetic
FBW	Fractional bandwidth
FoM	Figure of merit
FR	Frequency range
GaAs	Gallium arsenide
GaN	Gallium nitride
GaN-on-Si	Gallium nitride-on-silicon
HB	Harmonic balance
HEMT	High-electron-mobility transistor
IMD3	Third-order intermodulation distortion
IMN	Input matching network
ISMN	Interstage matching network
ITR	Impedance transformation ratio
MMIC	Monolithic microwave integrated circuit
mmWave	Millimeter-wave
MN	Matching network
OID	Optimal impedance domain
OMN	Output matching network
OPG	Operating power gain
PA	Power amplifier

PAE	Power-added efficiency
P-OID	Preferred optimal impedance domain
PSO	Particle swarm optimization
SATCOM	Satellite communication
SOI	Silicon-on-insulator
S-OID	Strict optimal impedance domain
SRFT	Simplified real-frequency technique
STN	Synthesized transformer network
SWaP-C	Size, weight, power, and cost

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